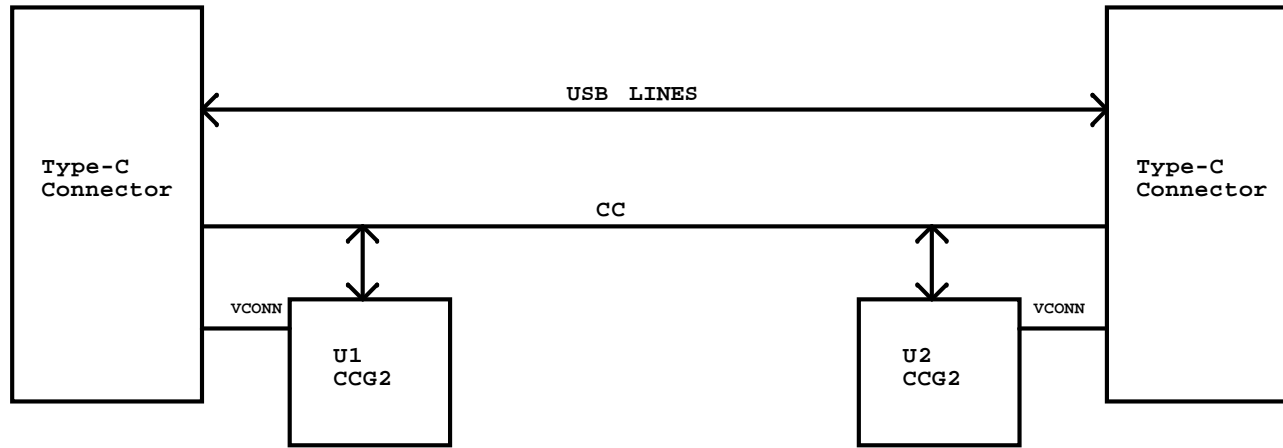
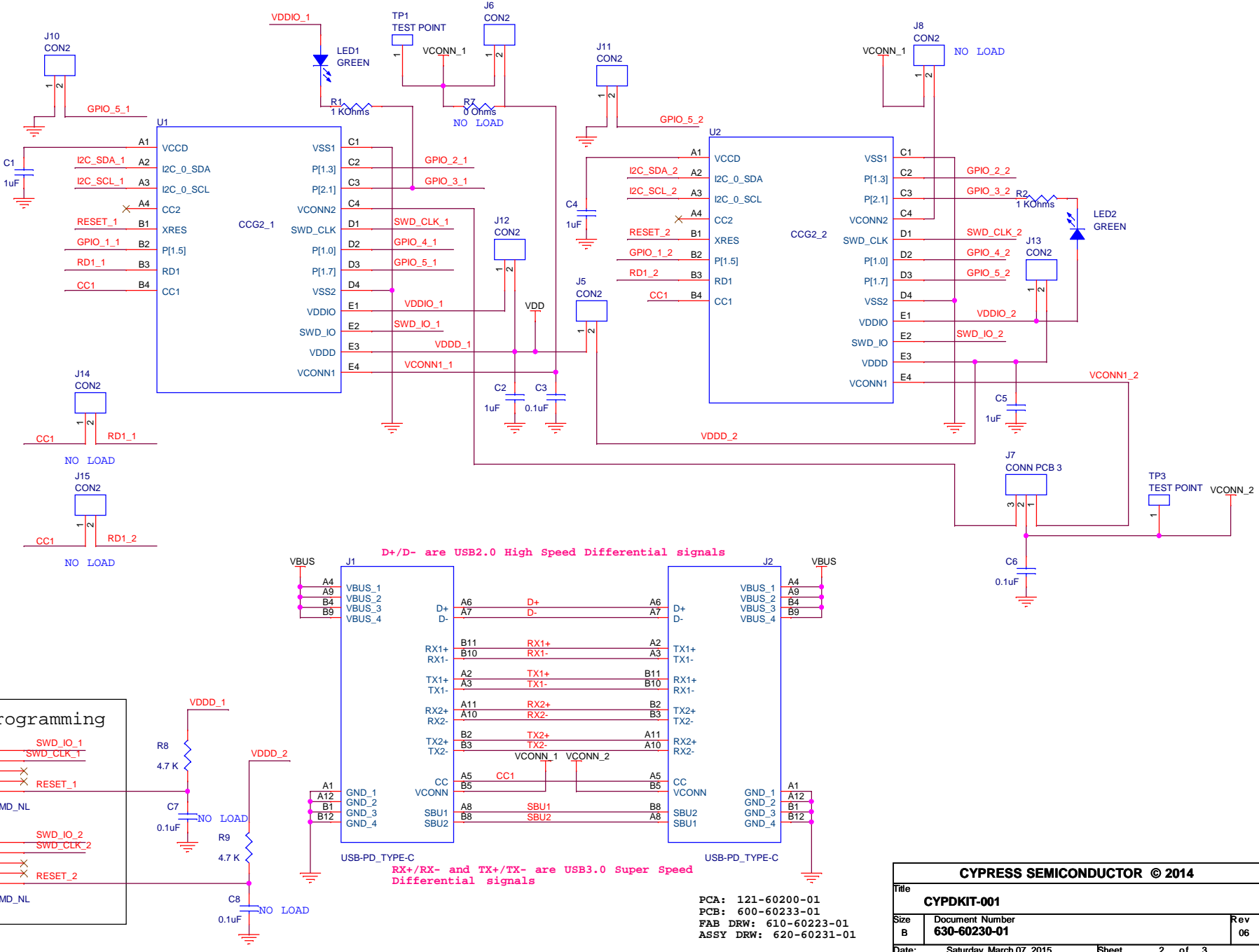
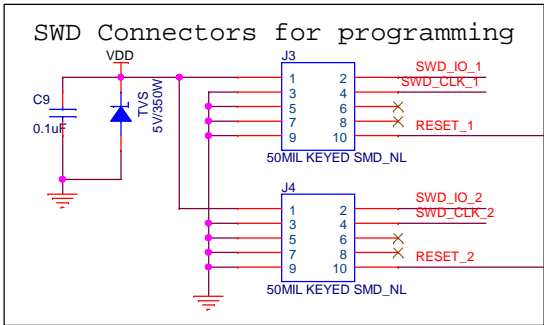
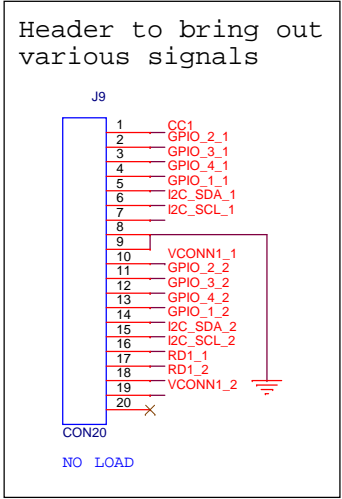
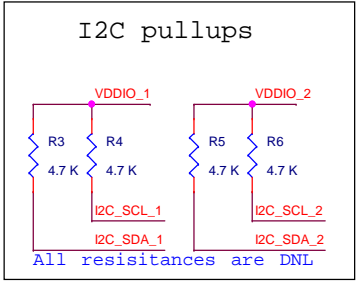


BLOCK DIAGRAM



PCA: 121-60200-01  
PCB: 600-60233-01  
FAB DRW: 610-60223-01  
ASSY DRW: 620-60231-01

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<b>CYPDKIT-001</b>		
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D+/D- are USB2.0 High Speed Differential signals

RX+/RX- and TX+/TX- are USB3.0 Super Speed Differential signals

PCA: 121-60200-01  
 PCB: 600-60233-01  
 FAB DRW: 610-60223-01  
 ASSY DRW: 620-60231-01

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Title: <b>CYPDKIT-001</b>		
Size: B	Document Number: <b>630-60230-01</b>	Rev: 06
Date: Saturday, March 07, 2015	Sheet: 2	of 3

<b>Revision</b>	<b>Description of the change</b>
<b>02</b>	Updating for the sanity no changes in the schematic
<b>03</b>	Changing the revision number to match with Layout
<b>04</b>	Changing the revision number to match with Layout
<b>05</b>	Added a pull-up on the XRES line of each chip
<b>06</b>	Added Jumper J8 Increases R1 and R2 from 150 Ohms to 1K Ohms

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Title <b>CYPDKIT-001</b>		
Size A	Document Number <b>630-60230-01</b>	Rev 06
Date: Saturday, March 07, 2015		Sheet 3 of 3