KSZ8873MML/RRL_LQFP Demo Board Revision 1.0

REVISION HISTORY

DATE:	DESCRIPTION	REVISION
04/30/2009	Initial release	1.0

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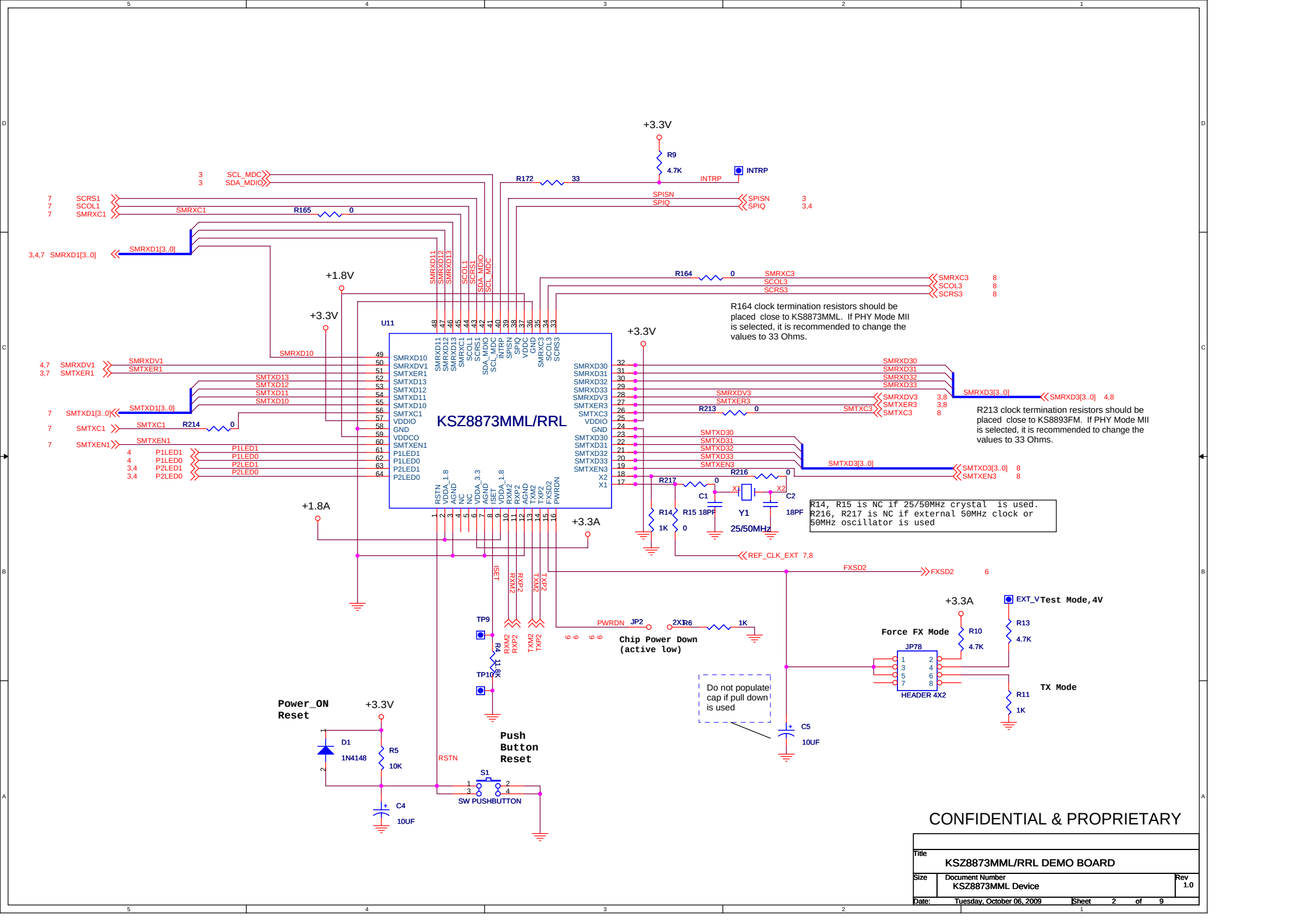
+3.3V
R9
4.7K
INTRP
R172
33
SCL_MDC
SDA_MDIO
SPISN
SPIQ
SCRS1
SCOL1
SMRXC1
R165
0
SMRXD1[3..0]
+1.8V
+3.3V
U11
KSZ8873MML/RRL
R164
0
SMRXC3
SCOL3
SCRS3
R164 clock termination resistors should be placed close to KS8873MML. If PHY Mode MII is selected, it is recommended to change the values to 33 Ohms.
SMRXD30
SMRXD31
SMRXD32
SMRXD33
SMRXDV3
SMTXER3
SMTXC3
R213
0
SMRXD3[3..0]
R213 clock termination resistors should be placed close to KS8893FM. If PHY Mode MII is selected, it is recommended to change the values to 33 Ohms.
SMRXDV1
SMTXER1
SMTXD13
SMTXD12
SMTXD11
SMTXD10
SMTXD1[3..0]
SMTXC1
R214
0
SMTXEN1
P1LED1
P1LED0
P2LED1
P2LED0
SMTXD30
SMTXD31
SMTXD32
SMTXD33
SMTXEN3
SMTXD3[3..0]
R216
0
R217
0
C1
18PF
C2
18PF
X1
X2
Y1
25/50MHz
R14
1K
R15
0
R14, R15 is NC if 25/50MHz crystal is used.
R216, R217 is NC if external 50MHz clock or 50MHz oscillator is used
+1.8A
+3.3A
REF_CLK_EXT
FXSD2
ISET
RXM2
RXP2
TXM2
TXP2
TP9
TP10
R4
11.8K
PWRDN
JP2
R6
1K
Chip Power Down (active low)
Do not populate cap if pull down is used
C5
10UF
Force FX Mode
JP78
HEADER 4X2
R10
4.7K
R13
4.7K
R11
1K
EXT_V
Test Mode,4V
TX Mode
Power_ON Reset
D1
1N4148
R5
10K
C4
10UF
RSTN
S1
SW PUSHBUTTON
Push Button Reset
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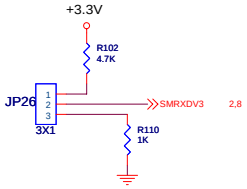
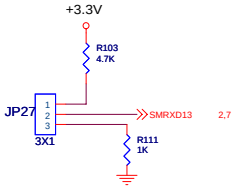
[P2LED1, P2LED0]	Serial Bus Configuration
[0,0]	I2C (master mode) EEPROM
[0,1]	I2C Slave mode
[1,0]	SPI Slave mode
[1,1]	SMI Mode

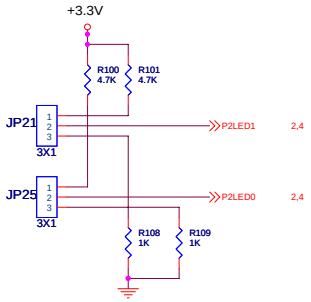
Bus Selection	Jumper Setting
SMI / MIIM (SW) I2C Master / I2C Slave / SPI Slave	close JP34 and JP35. open JP79
MIIM (PHY only)	open JP34 and JP35. close JP79

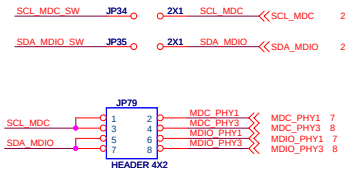
SMRXDV3	Switch MII Configuration(P3)
1	PHY mode MII
0	MAC mode MII

SMRXD13	Switch MII Configuration(P1)
1	PHY mode MII
0	MAC mode MII





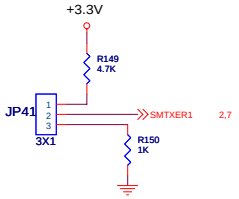


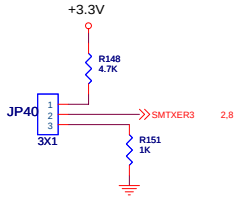


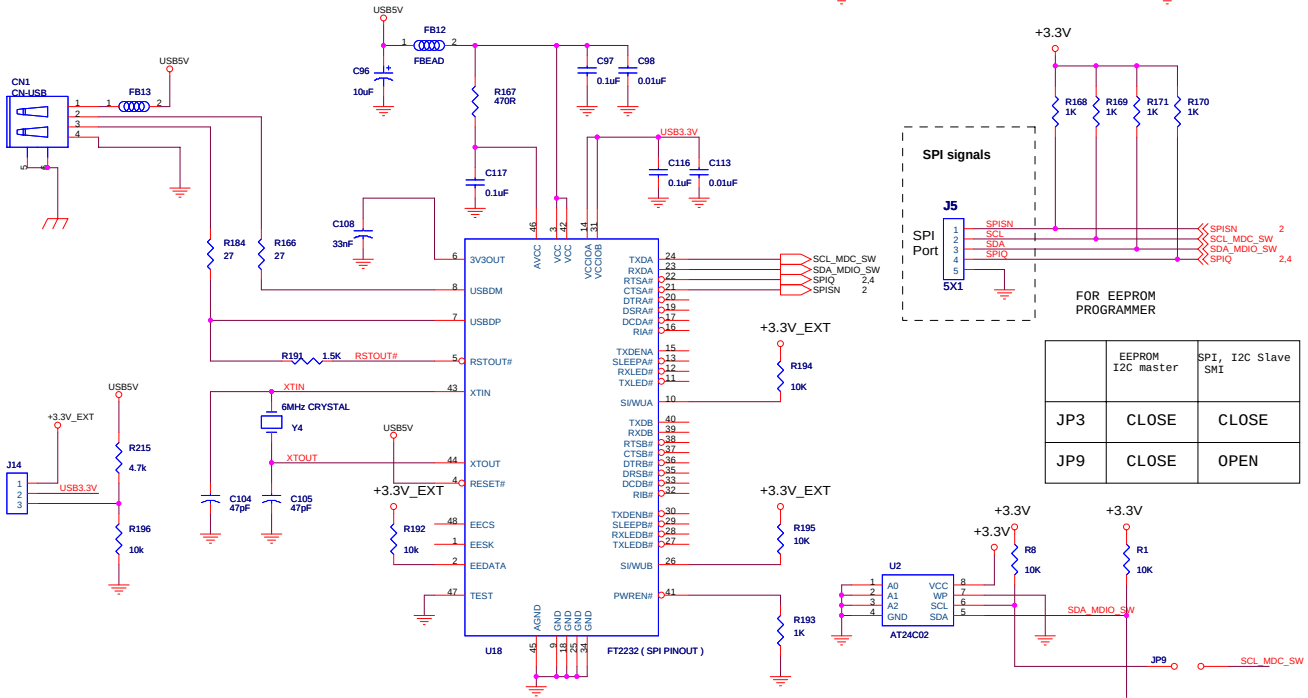
1-2 and 5-6 for port 1
3-4 and 7-8 for port 3

SMTXER1	Port 1 SWITCH MII Configuration
1	MII no link in PHY mode
0	Tie to GND in RMII mode

SMTXER3	Port 3 SWITCH MII Configuration
1	MII no link in PHY mode
0	Tie to GND in RMII mode







	EEPROM I2C master	SPI, I2C Slave SMI
JP3	CLOSE	CLOSE
JP9	CLOSE	OPEN

1-2 Close for default

1-2	USB 3.3V from LDO
2-3	USB 3.3V from USB port. Don't suggest to use.

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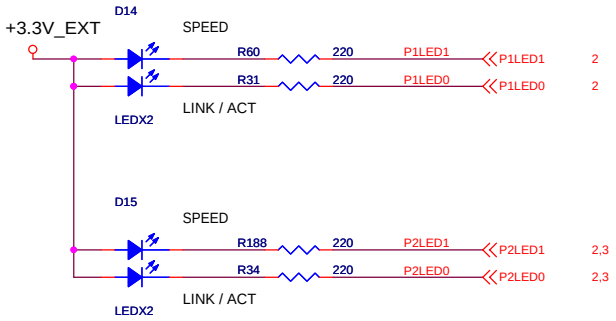
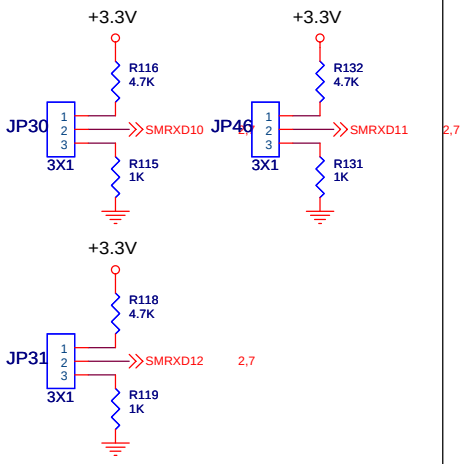
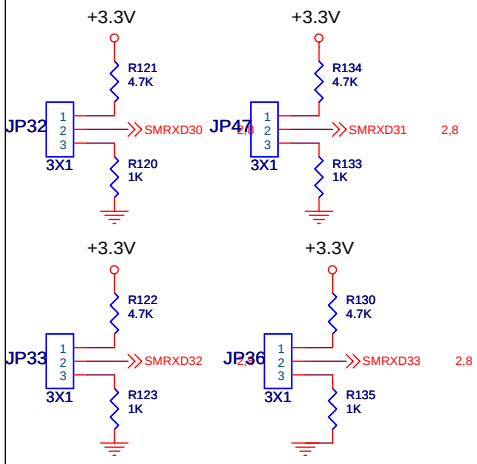


PORT 1



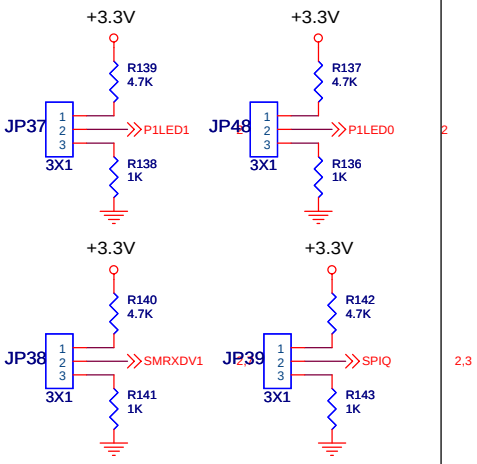
JP30	Force Flow Control High = ENABLE Low = DISABLE
JP46	Force Full/Half High = Full Duplex Low = Half Duplex
JP31	Force Speed High = 100BaseTX Low = 10BaseT

PORT 2



JP32	Force Flow Control High = ENABLE Low = DISABLE
JP47	Force Full/Half High = Full Duplex Low = Half Duplex
JP33	Force Speed High = 100BaseTX Low = 10BaseT
JP36	Auto-negotiation High = ENABLE Low = DISABLE

PORT 3



JP37	Force Flow Control High = ENABLE Low = DISABLE
JP48	Force Full/Half High = Half Duplex Low = Full Duplex
JP38	Force Speed High = 10BaseT Low = 100BaseTX
JP39	XCLK Frequency High = 25MHz Low = 50MHz

MICREL
KENDIN OPERATIONS

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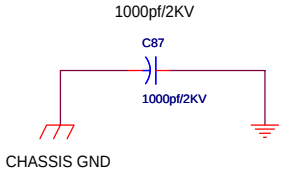
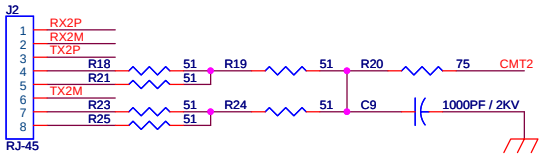
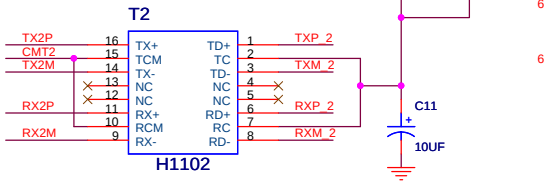
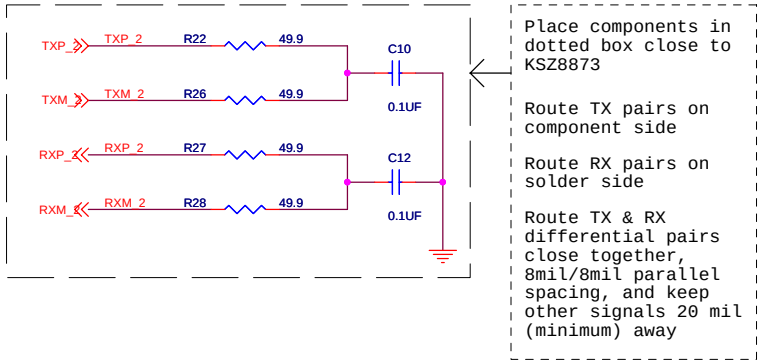


Compatible Isolation Transformers

Pulse H1102
Transpower HB726
Bel Fuse S558-5999-U7
YCL PT163020
DELTA LF8505







Place components in dotted box close to KSZ8873

Route TX pairs on component side

Route RX pairs on solder side

Route TX & RX differential pairs close together, 8mil/8mil parallel spacing, and keep other signals 20 mil (minimum) away

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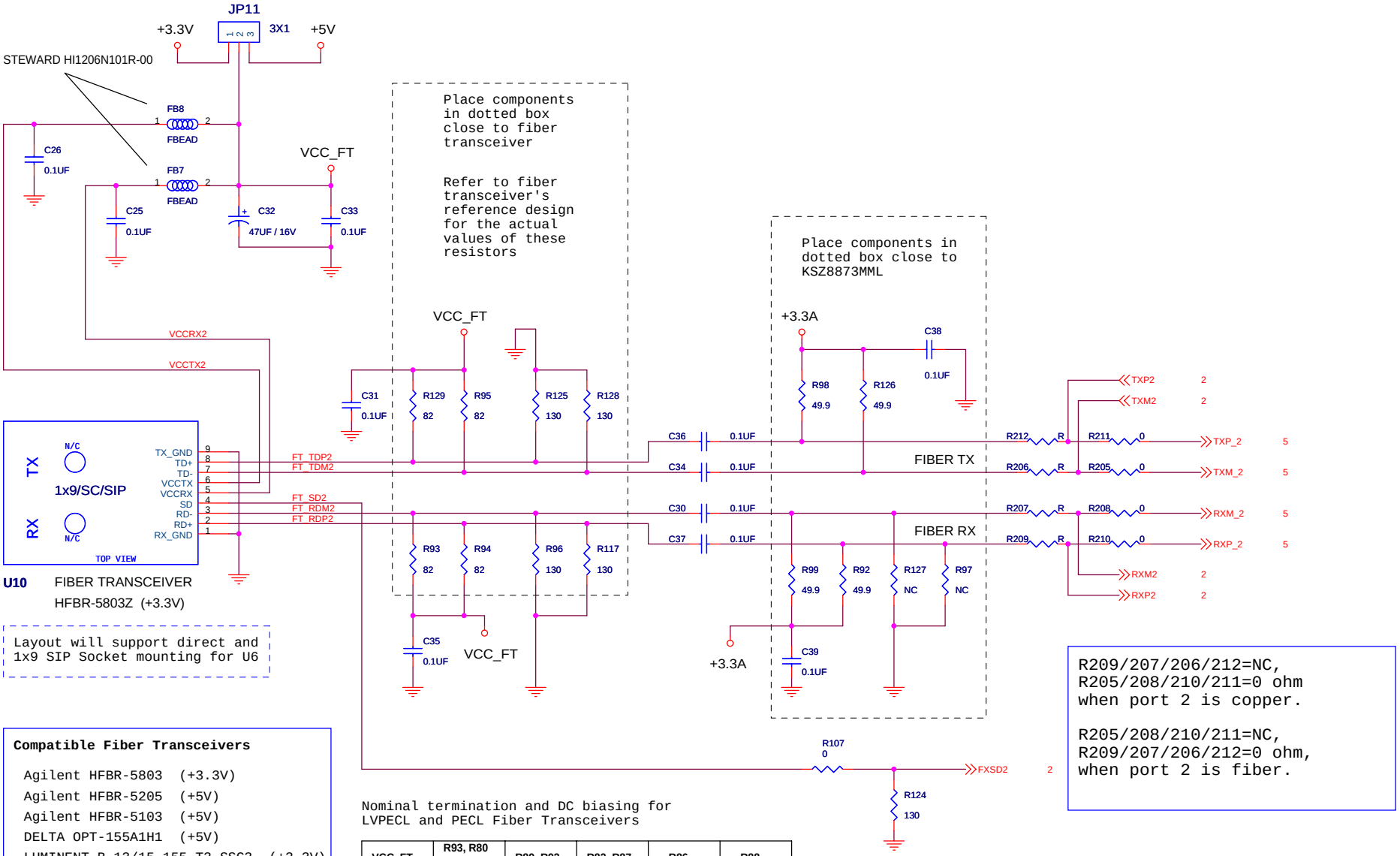

Compatible Fiber Transceivers

Agilent HFBR-5803 (+3.3V)
Agilent HFBR-5205 (+5V)
Agilent HFBR-5103 (+5V)
DELTA OPT-155A1H1 (+5V)
LUMINENT B-13/15-155-T3-SSC3 (+3.3V)
LUMINENT B-13/15-155-T-SSC3 (+5V)

Nominal termination and DC biasing for LVPECL and PECL Fiber Transceivers

VCC_FT	R93, R80 R79, R81	R89, R92	R82, R87	R86	R88
+3.3V	82 Ohms	130 Ohms	130 Ohms	O Ohm	130 Ohms
+5V	68 Ohms	191 Ohms	270 Ohms	4.75K 1%	5.62K 1%

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RMII option

KS8873MML provides RMII signals with respect to both PHY and MAC sides.

For this board, the KS8873MML provides RMII signals with respect to MAC side only. The RMII signal connections between KS8873MML and external PHY are shown in the table to the right.

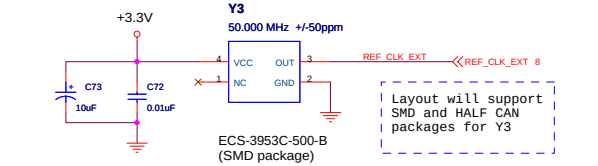
To enable RMII option,

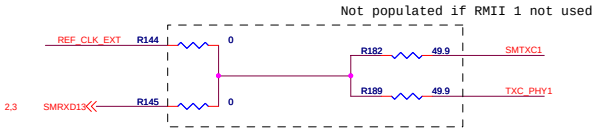
1. Populate 50 MHz OSC circuit. This system clock is an input to both PHY and MAC sides. Alternatively, if the 50 MHz clock is provided from the PHY side, this 50 MHz OSC circuit should not be populated .

2. Remove R58 and R82 to break TX_CLK and RX_CLK connections between PHY and MAC. Remove R57 and R106.

3. Connect RMII PHY (e.g. Micrel KS8721B) to MAC Mode MII port.

External PHY RMII (with respect to PHY)		KSZ8873MML RMII (with respect to MAC)		
Signal	**Type**	**Signal**	**Pin #**	**Type**
REF_CLK	Input	SMTXC1	56	Input
CRS_DV	Output	SMTXEN1	60	Input
RXD[1]	Output	SMTXD11	54	Input
RXD[0]	Output	SMTXD10	55	Input
TX_EN	Input	SMRXDV1	50	Output
TXD[1]	Input	SMRXD11	48	Output
TXD[0]	Input	SMRXD10	49	Output
RX_ER	Output	SMTXER1	51	Input



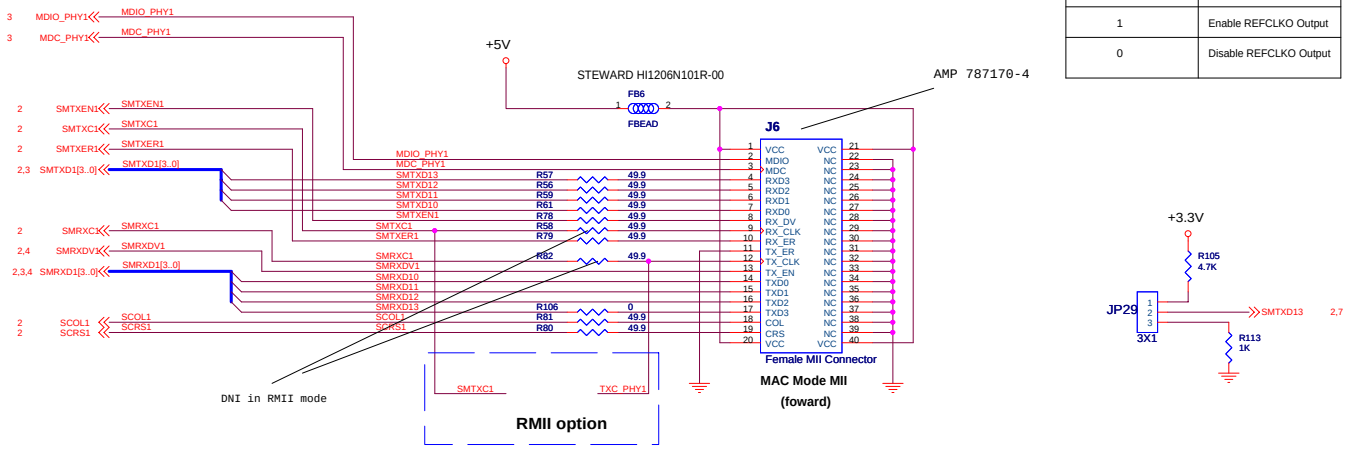


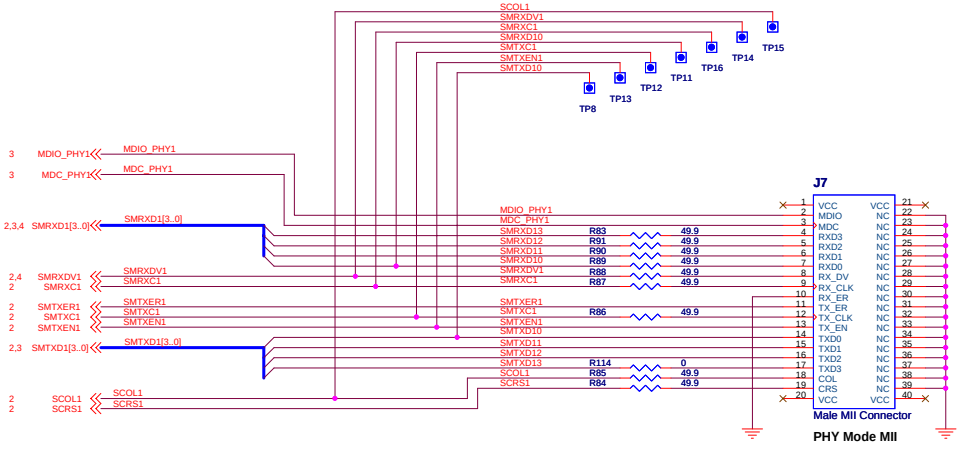
R145 NC, External Clock

R144 and R182 NC, Internal Clock for Port 1 RMII

NOTE:
MII BUS FROM DEVICE TO CONNECTOR MUCT
MATCH EQUAL LENGTH WITHIN +/- 100ML

SMTXD13	Reference Clock selection Port 1 RMII
1	Enable REFCLKO Output
0	Disable REFCLKO Output





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RMII option

KS8873MML provides RMII signals with respect to both PHY and MAC sides.

For this board, the KS8873MML provides RMII signals with respect to MAC side only. The RMII signal connections between KS8873MML and external PHY are shown in the table to the right.

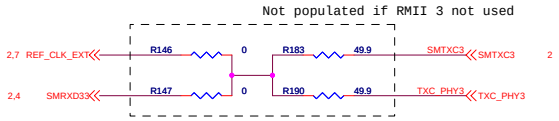
To enable RMII option,

1. Populate 50 MHz OSC circuit. This system clock is an input to both PHY and MAC sides. Alternatively, if the 50 MHz clock is provided from the PHY side, this 50 MHz OSC circuit should not be populated .

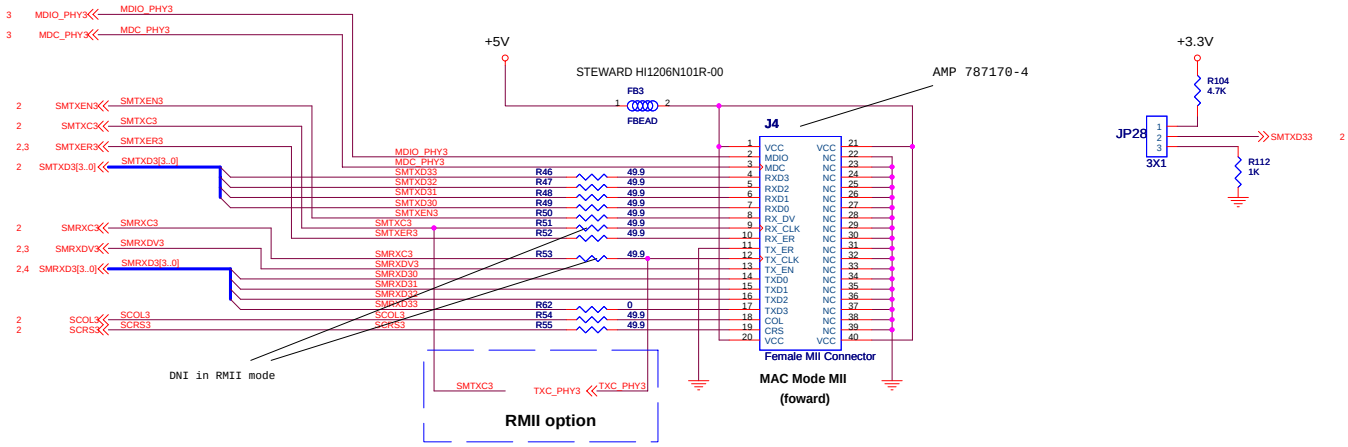
2. Remove R51 and R53 to break TX_CLK and RX_CLK connections between PHY and MAC. Remove R46 and R62.

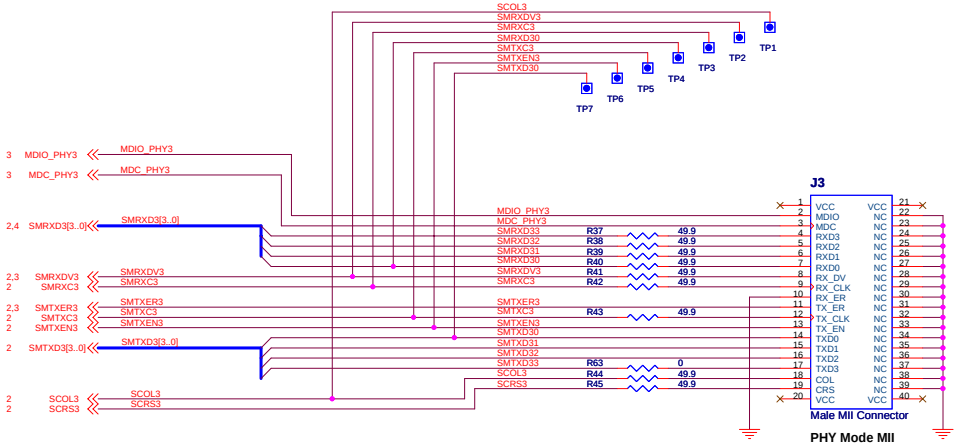
3. Connect RMII PHY (e.g. Micrel KS8721B) to MAC Mode MII port.

External PHY RMII (with respect to PHY)		KSZ8873MML RMII (with respect to MAC)		
Signal	**Type**	**Signal**	**Pin #**	**Type**
REF_CLK	Input	SMTXC3	26	Input
CRS_DV	Output	SMTXEN3	19	Input
RXD[1]	Output	SMTXD31	22	Input
RXD[0]	Output	SMTXD30	23	Input
TX_EN	Input	SMRXDV3	28	Output
TXD[1]	Input	SMRXD31	31	Output
TXD[0]	Input	SMRXD30	32	Output
RX_ER	Output	SMTXER3	27	Input



SMTXD33	Reference Clock selection Port 3 RMII
1	Enable REFCLKO Output
0	Disable REFCLKO





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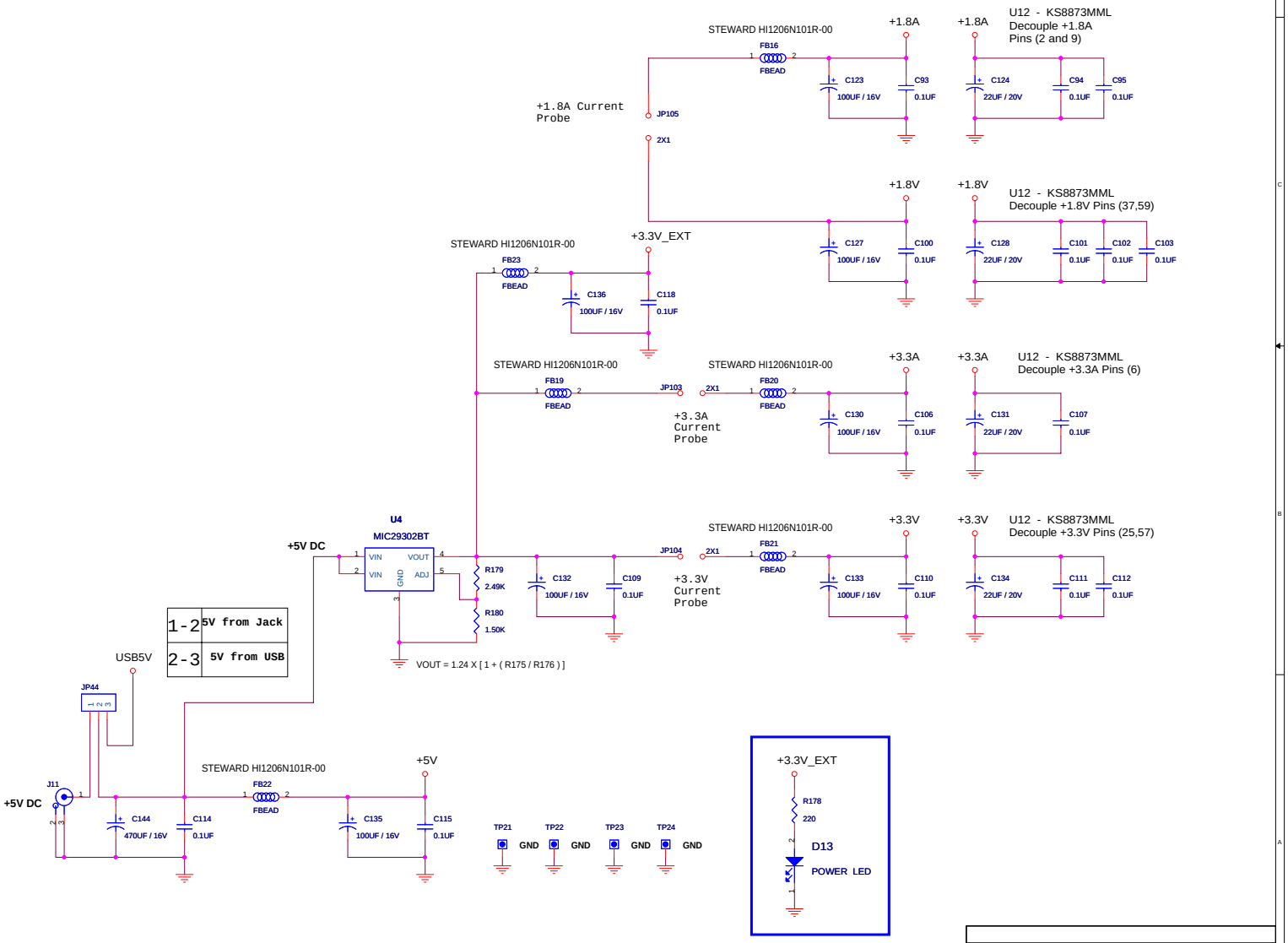

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