

Calypso Customer EVB 324 BGA Daughter Card (X-MPC574XG-324DS)

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Revision Information

Rev	Date	Designer	Comments
X1	28 Feb 2013	Alasdair Robertson	Initial release sent for review
X2	11 Mar 2013	Alasdair Robertson	Final Review
X3	13 Mar 2013	Alasdair Robertson	Version sent to Pre Layout, incorporating fixes from review
X4	15 Mar 2013	Alasdair Robertson	Component consolidation, Few minor changes. Sent to Layout
X5	29 Mar 2013	Alasdair Robertson	Changes made during layout to Daughtercard Connectors
X6	15 Apr 2013	Alasdair Robertson	CIS CAD Database update & SCH Back-Annotate
A	15 Apr 2015	Alasdair Robertson	Post Layout (Back Annotated), Matches PCB RevA

Caution:

These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points are denoted TPx
- Test point Vias are denoted TPVx

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS


3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hole Pad Large (for standard 0.1" header).

TPX - Surface Mount Wire Loop



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Drawn by: A. Robertson	Page Title: <h4 style="text-align: center;">Index and Title Page</h4>				
Approved: A. Robertson	Size B	Document Number SCH-27900 PDF: SPF-27900		Rev A	
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Calypso MCU Power Connections

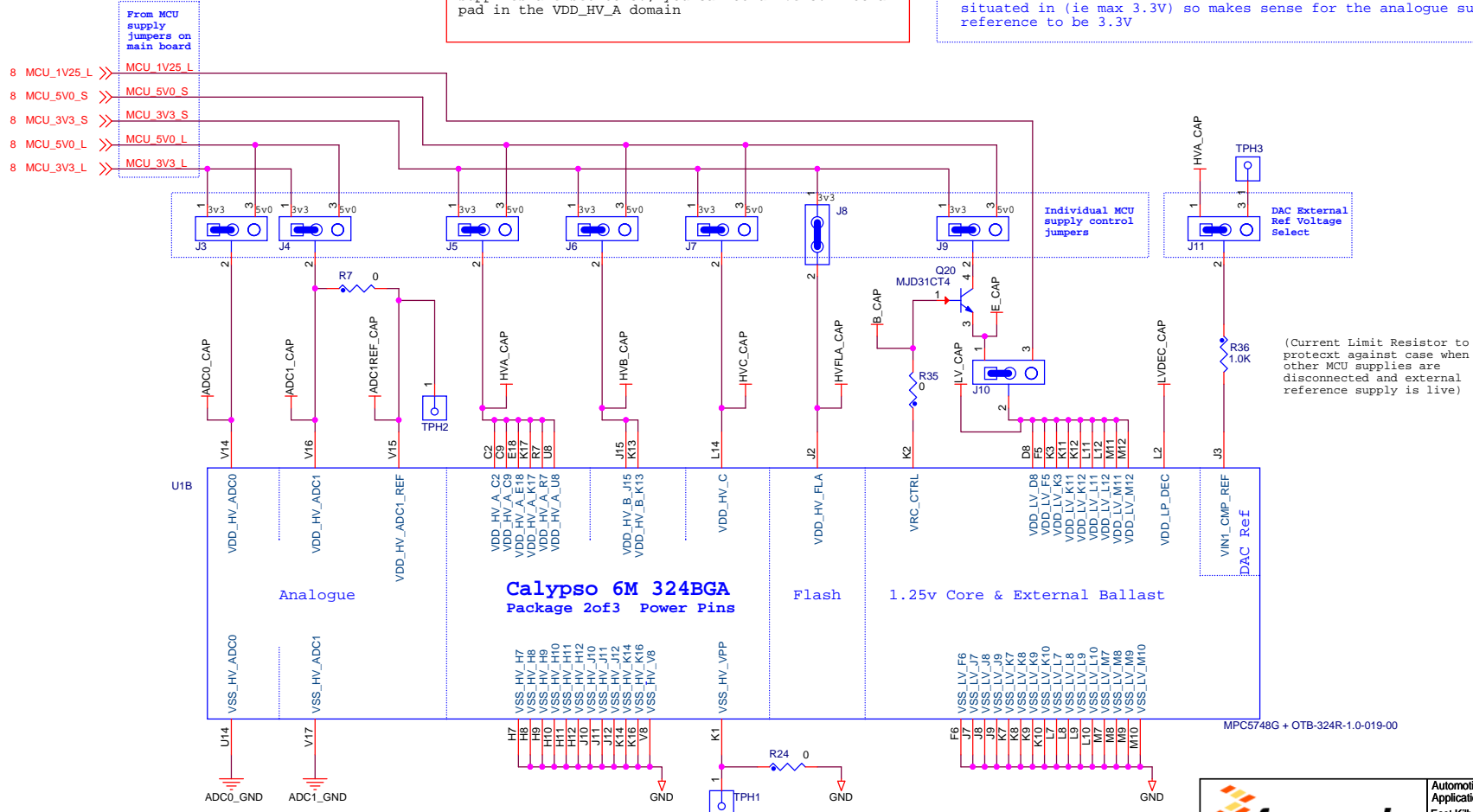
Caution:

- If VDD_HV_A is driven from 5V, the VDD_HV_FL A pin must not be supplied from 3.3V (remove the HVA_FL A jumper)
- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain

Default Configuraiton:

- ALL MCU supply voltages are set to 3.3V (ADC0, ADC1, VDD_HV_A, VDD_HV_B, VDD_HV_C, VBallast)
- VDD_HV_FL A = External 3.3V supplied (jumper fitted)
- VDD_LV Supplied from ballast transistor

This is not necessarily the same as the default shown in the RM. All VDD_HV_x domains have at least one peripheral that only functions at 3.3V. Therefore the default is to run these from 3.3V. The analogue pins can only be driven to the same voltage as the VDD_HV_x domain they are situated in (ie max 3.3V) so makes sense for the analogue supply and reference to be 3.3V

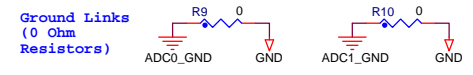


From MCU supply jumpers on main board

- 8 MCU_1V25_L >> MCU_1V25_L
- 8 MCU_5V0_S >> MCU_5V0_S
- 8 MCU_3V3_S >> MCU_3V3_S
- 8 MCU_5V0_L >> MCU_5V0_L
- 8 MCU_3V3_L >> MCU_3V3_L

Individual MCU supply control jumpers

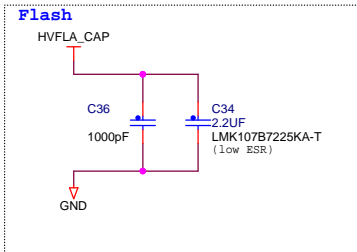
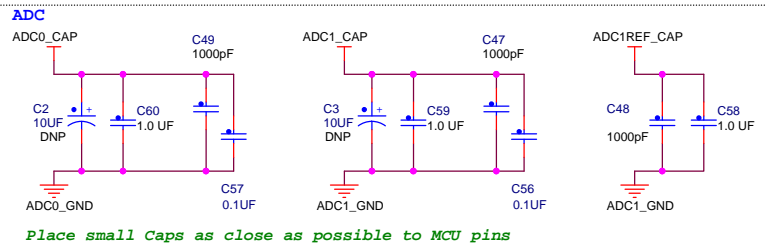
(Current Limit Resistor to protect against case when other MCU supplies are disconnected and external reference supply is live)



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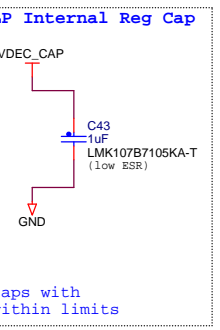
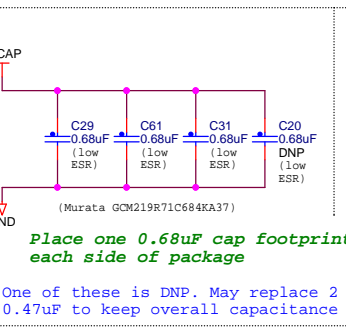
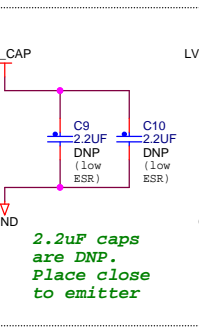
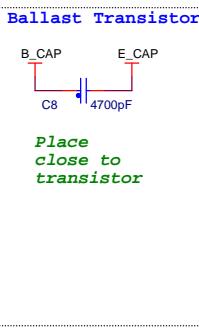
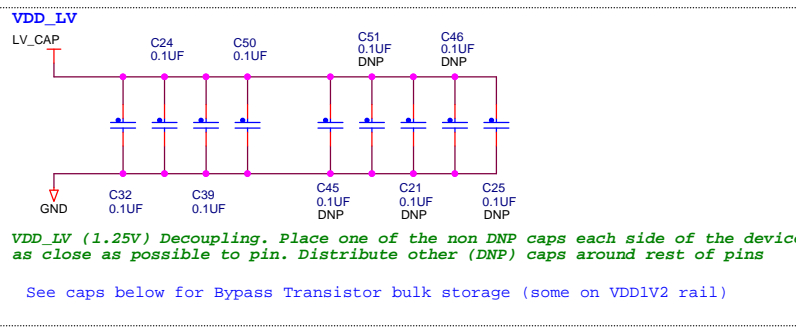
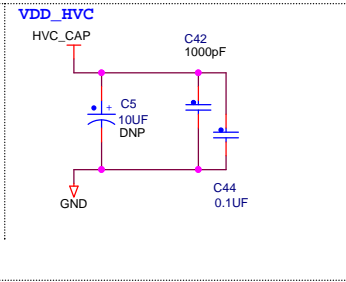
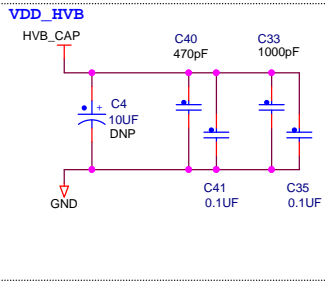
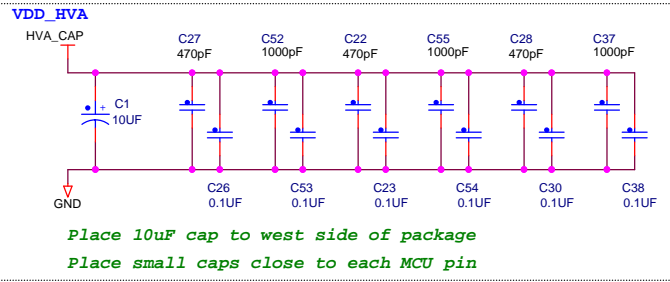
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Calypso MCU Decoupling and bulk storage



Capacitor Types:

- 470pF - Ceramic COG, 50V 5% 0402
- 1000pF - Ceramic COG, 50V 5% 0402
- 4700pF - Ceramic X7R, 50V 10% 0402
- 0.01uF - Ceramic X7R, 50V 10% 0402
- 0.1uF - Ceramic X7R, 16V 10% 0402
- 0.68uF - Ceramic X7R 16V 10% 0805 (Murata GCM219R71C684KA37)
- 1.0uF - Ceramic X7R, 10V 10% 0603 (Taiyo Yuden LMK107B7105KA-T)
- 2.2uF - Ceramic X7R, 10V, 10%, 0603 (Taiyo Yuden LMK107B7225KA-TR)
- 4.7uF - TANT, 12.5V 20% ESR=0.08R 7343
- 10uF - TANT, 35V 10% ESR=0.125R CC7343-31
- 4.7uF Alternative (150-78844)- Polymer ALU, 16V 20% ESR=0.08R 7343-18



Calypso GPIO 1 of 2

U1A

Calypso 324 BGA Package 1of3 GPIO Pins1


** PA1 is also NMI. Routed to I/O Matrix (WKPU2 / NMI0) (WKPU3)

Key to text colours:
 Purple - Comms Physical Interfaces
 Orange - Other Peripherals and I/O
 Blue - Debug (JTAG & Nexus)
 Black - Clock, Reset and Control
 RED - I/O Matrix and other functions (eg LED)
 Green - I/O Matrix (dedicated)

8	PA0	(SD_CD - WKPU19)	PA0	L5	PA0
8	PA1	(SW1 & GPIO**)	PA1	K6	PA1
8	PA2	(SW2 & GPIO)	PA2	J6	PA2
8	PA3	(MII_RXCLK)	PA3	M17	PA3
8	PA4	(CMP1_13 / IO)	PA4	P6	PA4
8	PA5	(SAI_GPIO)	PA5	A14	PA5
8	PA6	(MLB_GPIO)	PA6	A13	PA6
8	PA7	(MII_RXD2)	PA7	F17	PA7
8	PA8	(RMI1_RXD1)	PA8	F18	PA8
8	PA9	(RMI1_RXD0)	PA9	F17	PA9
8	PA10	(MII_COL)	PA10	D18	PA10
8	PA11	(RMI1_RXER)	PA11	D17	PA11
8	PA12	(CMP1_15 / IO)	PA12	N8	PA12
8	PA13	(CMP1_14 / IO)	PA13	P7	PA13
8	PA14	(CMP1_12 / IO)	PA14	T3	PA14
8	PA15	(CMP1_10 / IO)	PA15	N7	PA15
8	PB0	(CAN0_TX)	PB0	N1	PB0
8	PB1	(CAN0_RX)	PB1	N2	PB1
8	PB2	(LIN0_TX)	PB2	G9	PB2
8	PB3	(LIN0_RX)	PB3	G8	PB3
8	PB4	(ADC_F0T)	PB4	N11	PB4
8	PB5	(GPIO)	PB5	R14	PB5
8	PB6	(GPIO)	PB6	N12	PB6
8	PB7	(GPIO)	PB7	P14	PB7
8	PB8	(XTAL32)	PB8	V10	PB8/XTAL32
6	PB9	(EXTAL32)	PB9	V9	PB9/EXTAL32
8	PB10	(SAI0_SYNC)	PB10	P9	PB10
8	PB11	(GPIO)	PB11	P13	PB11
8	PB12	(GPIO)	PB12	N13	PB12
7	PB13	(MLB_DM)	PB13	T18	PB13
7	PB14	(MLB_SN)	PB14	R17	PB14
7	PB15	(MLB_CN / SIG)	PB15	R18	PB15
8	PC0	(TDI)	PC0	F9	PC0
8	PC1	(TDO)	PC1	F10	PC1
8	PC2	(USB1_CLK)	PC2	C13	PC2
8	PC3	(USB1_D18)	PC3	D11	PC3
8	PC4	(FR_B_TX_EN)	PC4	B12	PC4
8	PC5	(FR_A_TX)	PC5	A11	PC5
8	PC6	(LIN1_TX)	PC6	R3	PC6
8	PC7	(LIN1_RX)	PC7	U2	PC7
8	PC8	(RS232_TX)	PC8	D5	PC8
8	PC9	(RS232_RX)	PC9	D4	PC9
8	PC10	(CANL_TX)	PC10	M5	PC10
8	PC11	(CANL_RX)	PC11	M4	PC11
8	PC12	(FR_DBG1)	PC12	D6	PC12
8	PC13	(FR_DBG2)	PC13	E6	PC13
8	PC14	(FR_DBG3)	PC14	B2	PC14
8	PC15	(FR_DBG3)	PC15	C3	PC15
8	PD0	(HEX1 & GPIO)	PD0	R12	PD0
8	PD1	(HEX2 & GPIO)	PD1	T13	PD1
8	PD2	(HEX3 & GPIO)	PD2	T14	PD2
8	PD3	(HEX4 & GPIO)	PD3	R13	PD3
8	PD4	(GPIO)	PD4	P11	PD4
8	PD5	(GPIO)	PD5	T15	PD5
8	PD6	(GPIO)	PD6	R15	PD6
8	PD7	(GPIO)	PD7	R15	PD7
8	PD8	(GPIO)	PD8	P12	PD8
8	PD9	(GPIO)	PD9	N15	PD9
8	PD10	(GPIO)	PD10	P15	PD10
8	PD11	(GPIO)	PD11	V18	PD11
8	PD12	(GPIO)	PD12	N16	PD12
8	PD13	(GPIO & MLB_ST)	PD13	N14	PD13
7	PD14	(MLB_DP)	PD14	T17	PD14
7	PD15	(MLB_SP / DAT)	PD15	P17	PD15
8	MCU-RSTx	MCU-RSTx	L1		RESET
8	PORSTx	PORSTx	C12		PORST
6	MCU-XTAL	MCU-XTAL	V6		XTAL
6	MCU-EXTAL	MCU-EXTAL	V7		EXTAL

PE0	H3	PE0	(MLB_T2C1_SCL)	PE0	8
PE1	H2	PE1	(MLB_T2C1_SDA)	PE1	8
PE2	A12	PE2	(FR_A_TX_EN)	PE2	8
PE3	D10	PE3	(FR_A_RX)	PE3	8
PE4	B11	PE4	(FR_B_TX)	PE4	8
PE5	A10	PE5	(FR_B_RX)	PE5	8
PE6	F8	PE6	(SD_CMD)	PE6	8
PE7	D7	PE7	(SD_CLK)	PE7	8
PE8	K5	PE8	(SAI_T2C2_SDA)	PE8	8
PE9	K4	PE9	(SAI_T2C2_SCL)	PE9	8
PE10	H1	PE10	(SAI_T2C3_SDA)	PE10	8
PE11	J1	PE11	(SAI_T2C3_SCL)	PE11	8
PE12	C18	PE12	(MII_CRS)	PE12	8
PE13	G17	PE13	(MII_RXD3)	PE13	8
PE14	C15	PE14	(USB1_D2)	PE14	8
PE15	E12	PE15	(USB1_D1)	PE15	8
PF0	N9	PF0	(SAI0_MCLK)	PF0	8
PF1	R9	PF1	(SAI0_BCLK)	PF1	8
PF2	P10	PF2	(SAI0_D3)	PF2	8
PF3	U10	PF3	(SAI0_D2)	PF3	8
PF4	N10	PF4	(SAI0_D1)	PF4	8
PF5	V12	PF5	(SAI0_D0)	PF5	8
PF6	T11	PF6	(SAI1_SYNC)	PF6	8
PF7	R10	PF7	(SAI1_MCLK)	PF7	8
PF8	T2	PF8	(GPIO)	PF8	8
PF9	T1	PF9	(SW3 & GPIO) WKPU2	PF9	8
PF10	R5	PF10	(CMP1_8 / IO)	PF10	8
PF11	P5	PF11	(SW4 & GPIO) WKPU1	PF11	8
PF12	N5	PF12	(GPIO)	PF12	8
PF13	N6	PF13	(CMP1_11 / IO)	PF13	8
PF14	G18	PF14	(RMI1_MDI0)	PF14	8
PF15	H17	PF15	(RMI1_RXDV)	PF15	8
PG0	H18	PG0	(RMI1_MDC)	PG0	7
PG1	J16	PG1	(RMI1_TXCLK)	PG1	8
PG2	J4	PG2	(LED1 & GPIO)	PG2	8 (eMIOS E11C_11_H)
PG3	J5	PG3	(LED2 & GPIO)	PG3	8 (eMIOS E11C_12_H)
PG4	G2	PG4	(LED3 & GPIO)	PG4	8 (eMIOS E11C_13_H)
PG5	F2	PG5	(LED4 & GPIO)	PG5	8 (eMIOS E11C_14_H)
PG6	M2	PG6	(CLKOUT1 GPIO)	PG6	8
PG7	M1	PG7	(CLKOUT0 GPIO)	PG7	8
PG8	M3	PG8	(GPIO)	PG8	8
PG9	L3	PG9	(MLB_IRQ - WKPU21)	PG9	8
PG10	D14	PG10	(USB1_D4)	PG10	8
PG11	D13	PG11	(USB1_D5)	PG11	8
PG12	L18	PG12	(MII_RXD2)	PG12	7
PG13	M18	PG13	(MII_RXD3)	PG13	7
PG14	F12	PG14	(USB1_D0)	PG14	8
PG15	C16	PG15	(USB1_D1)	PG15	8
PH0	L17	PH0	(RMI1_TXD1)	PH0	7
PH1	K18	PH1	(RMI1_TXD0)	PH1	7
PH2	J18	PH2	(RMI1_TXEN)	PH2	7
PH3	J17	PH3	(eMIOS1_UC_5H)	PH3	8
PH4	C10	PH4	(eMIOS1_UC_6H)	PH4	8
PH5	B10	PH5	(eMIOS1_UC_7H)	PH5	8
PH6	A9	PH6	(MLB_RST)	PH6	8
PH7	D9	PH7	(MLB_PWR)	PH7	8
PH8	E8	PH8	(SD_WP)	PH8	8
PH9	E9	PH9	(TCK)	PH9	8
PH10	E10	PH10	(TMS)	PH10	8
PH11	C14	PH11	(USB1_D6)	PH11	8
PH12	D12	PH12	(USB1_D7)	PH12	8
PH13	F3	PH13	(GPIO)	PH13	8
PH14	E2	PH14	(GPIO)	PH14	8
PH15	G4	PH15	(GPIO)	PH15	8

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Calypso GPIO 2 of 2


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 Purple - Comms Physical Interfaces
 Orange - Other Peripherals and I/O
 Blue - Debug (JTAG & Nexus)
 Black - Clock, Reset and Control
 Red - I/O Matrix and other functions (eg LED)
 Green - I/O Matrix (dedicated)

Pin	Function	Pin	Function
8 P10	(SD_D3)	P10	C6
8 P11	(SD_D2)	P11	E7
8 P12	(SD_D1)	P12	C7
8 P13	(SD_D0)	P13	C8
8 P14	(USB1_STP)	P14	A18
8 P15	(USB1_NXT)	P15	E11
8 P16	(USB0_RST)	P16	H4
8 P17	(USB1_RST)	P17	G3
7 P18	(MLB_CP / CLK)	P18	P18
8 P19	(GPIO)	P19	T12
8 P110	(GPIO)	P110	U18
8 P111	(ENET_RST)	P111	N18
8 P112	(GPIO & MLB_P50)	P112	N17
8 P113	(GPIO & MLB_P51)	P113	M16
8 P114	(SAI2_D0)	P114	R16
8 P115	(SAI2_NCLK)	P115	P16
8 PJ0	(SAI2_SYNC)	PJ0	U18
8 PJ1	(SAI2_BCLK)	PJ1	V13
8 PJ2	(SAI1_D0)	PJ2	R11
8 PJ3	(SAI1_BCLK)	PJ3	U11
8 PJ4	(GPIO)	PJ4	A1
8 PJ5	(GPIO)	PJ5	T16
8 PJ6	(GPIO)	PJ6	U16
8 PJ7	(GPIO)	PJ7	U17
8 PJ8	(GPIO)	PJ8	U13
8 PJ9	(GPIO)	PJ9	V5
8 PJ10	(GPIO)	PJ10	V4
8 PJ11	(GPIO)	PJ11	U3
8 PJ12	(GPIO)	PJ12	V3
8 PJ13	(GPIO)	PJ13	T6
8 PJ14	(GPIO)	PJ14	R6
8 PJ15	(GPIO)	PJ15	U4
8 PK0	(GPIO)	PK0	T4
8 PK1	(GPIO)	PK1	N3
8 PK2	(GPIO)	PK2	N4
8 PK3	(GPIO)	PK3	P1
8 PK4	(GPIO)	PK4	P2
8 PK5	(GPIO)	PK5	P3
8 PK6	(GPIO)	PK6	P4
8 PK7	(GPIO)	PK7	R1
8 PK8	(GPIO)	PK8	R2
8 PK9	(GPIO)	PK9	B7
8 PK10	(GPIO)	PK10	A6
8 PK11	(GPIO)	PK11	B6
8 PK12	(GPIO)	PK12	A5
8 PK13	(GPIO)	PK13	B5
8 PK14	(GPIO)	PK14	C5
8 PK15	(GPIO)	PK15	A4
8 PL0	(GPIO)	PL0	B4
8 PL1	(GPIO)	PL1	L15
8 PL2	(MDO0)	PL2	E15
8 PL3	(MDO1)	PL3	E14
8 PL4	(MDO2)	PL4	F13
8 PL5	(MDO3)	PL5	F14
8 PL6	(MDO4)	PL6	F15
8 PL7	(MDO5)	PL7	G13
8 PL8	(EV1)	PL8	D15
8 PL9	(MSE00)	PL9	E13
8 PL10	(MCK0)	PL10	G12
8 PL11	(MSE01)	PL11	E16
8 PL12	(EVTO)	PL12	D16
8 PL13	(MDO6)	PL13	F16
8 PL14	(MDO7)	PL14	G16
8 PL15	(MDO8)	PL15	G15
8 PQ0	(USB0_STP)	PQ0	C11
8 PQ1	(USB0_CLK)	PQ1	B13
8 PQ2	(USB0_DIR)	PQ2	B14
8 PQ3	(USB0_NXT)	PQ3	F11
8 PQ4	(USB0_D7)	PQ4	A15
8 PQ5	(USB0_D6)	PQ5	A16
8 PQ6	(USB0_D5)	PQ6	B15
8 PQ7	(USB0_D4)	PQ7	A17

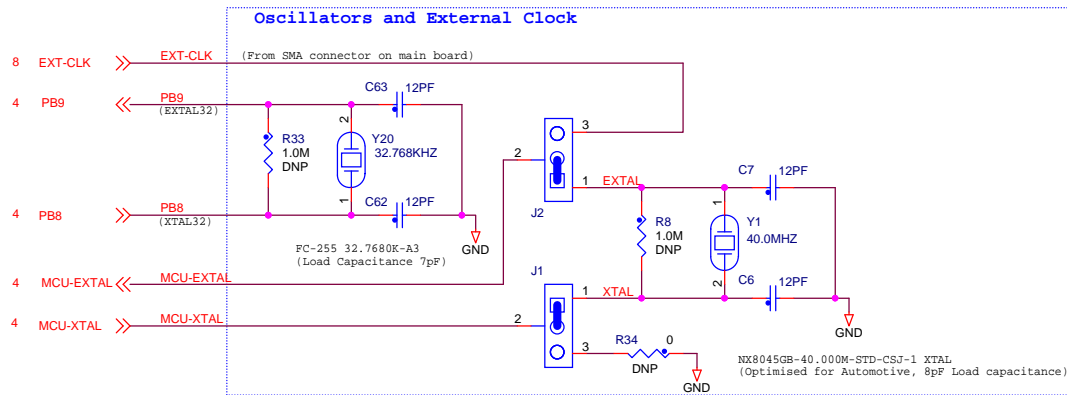
Calypso 324 BGA Package 3of3 GPIO Pins2


PM0	G14	PM0	(MDO9)
PM1	H13	PM1	(MDO10)
PM2	H15	PM2	(MDO11)
PM3	L13	PM3	(GPIO)
PM4	K15	PM4	(GPIO)
PM5	M14	PM5	(GPIO)
PM6	L16	PM6	(GPIO)
PM7	H16	PM7	(MDO12)
PM8	J13	PM8	(MDO13)
PM9	H14	PM9	(MDO14)
PM10	J14	PM10	(MDO15)
PM11	G10	PM11	(GPIO)
PM12	G11	PM12	(GPIO)
PM13	M13	PM13	(GPIO)
PM14	M15	PM14	(GPIO)
PM15	T10	PM15	(GPIO)
PN0	T9	PN0	(GPIO)
PN1	V11	PN1	(GPIO)
PN2	U9	PN2	(GPIO)
PN3	T8	PN3	(GPIO)
PN4	U7	PN4	(GPIO)
PN5	R8	PN5	(GPIO)
PN6	P8	PN6	(GPIO)
PN7	U8	PN7	(GPIO)
PN8	T5	PN8	(GPIO)
PN9	T7	PN9	(GPIO)
PN10	V2	PN10	(GPIO)
PN11	V1	PN11	(GPIO)
PN12	U1	PN12	(GPIO)
PN13	R4	PN13	(GPIO)
PN14	L4	PN14	(GPIO)
PN15	L4	PN15	(GPIO)
PO0	G1	PO0	(GPIO)
PO1	F1	PO1	(GPIO)
PO2	M6	PO2	(GPIO)
PO3	L6	PO3	(GPIO)
PO4	E1	PO4	(GPIO)
PO5	H6	PO5	(GPIO)
PO6	H5	PO6	(GPIO)
PO7	D1	PO7	(GPIO)
PO8	D2	PO8	(GPIO)
PO9	E3	PO9	(GPIO)
PO10	D3	PO10	(GPIO)
PO11	C1	PO11	(GPIO)
PO12	B1	PO12	(GPIO)
PO13	E4	PO13	(GPIO)
PO14	F4	PO14	(GPIO)
PO15	G6	PO15	(GPIO)
PP0	G5	PP0	(GPIO)
PP1	B3	PP1	(GPIO)
PP2	C4	PP2	(GPIO)
PP3	F7	PP3	(GPIO)
PP4	E5	PP4	(GPIO)
PP5	G7	PP5	(GPIO)
PP6	A2	PP6	(GPIO)
PP7	A3	PP7	(GPIO)
PP8	B8	PP8	(GPIO)
PP9	A7	PP9	(GPIO)
PP10	A8	PP10	(GPIO)
PP11	B9	PP11	(GPIO)
PP12	B17	PP12	(USB0_D3)
PP13	B16	PP13	(USB0_D2)
PP14	C17	PP14	(USB0_D1)
PP15	B18	PP15	(USB0_D0)

MPC5748G + OTB-324R-1.0-019-00

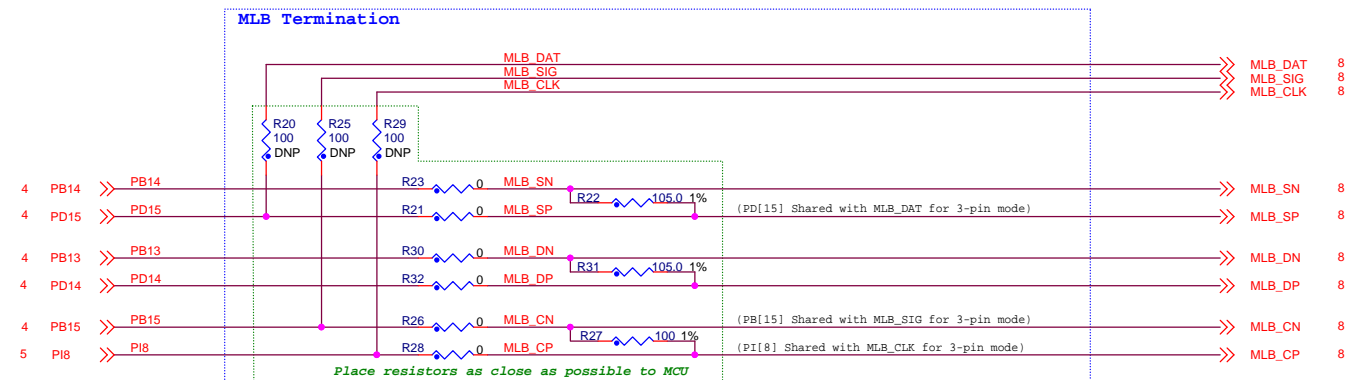
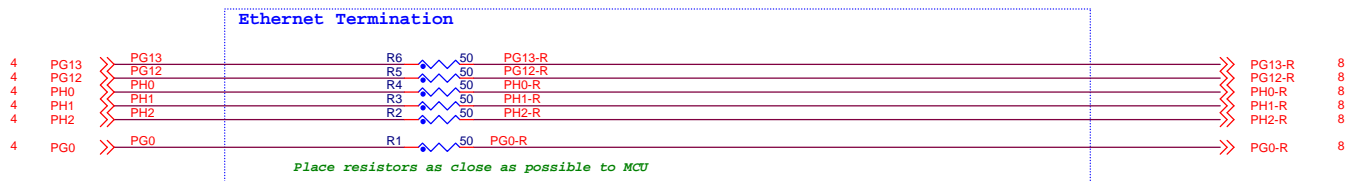
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Drawing Title: Calypso 324 BGA Daughter Card			
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Clocks



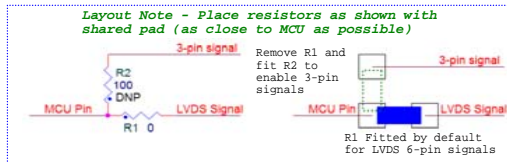
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Drawing Title: Calypso 324 BGA Daughter Card			
Page Title: Clocks			
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High Speed Signal Termination



From MCU

To Daughtercard

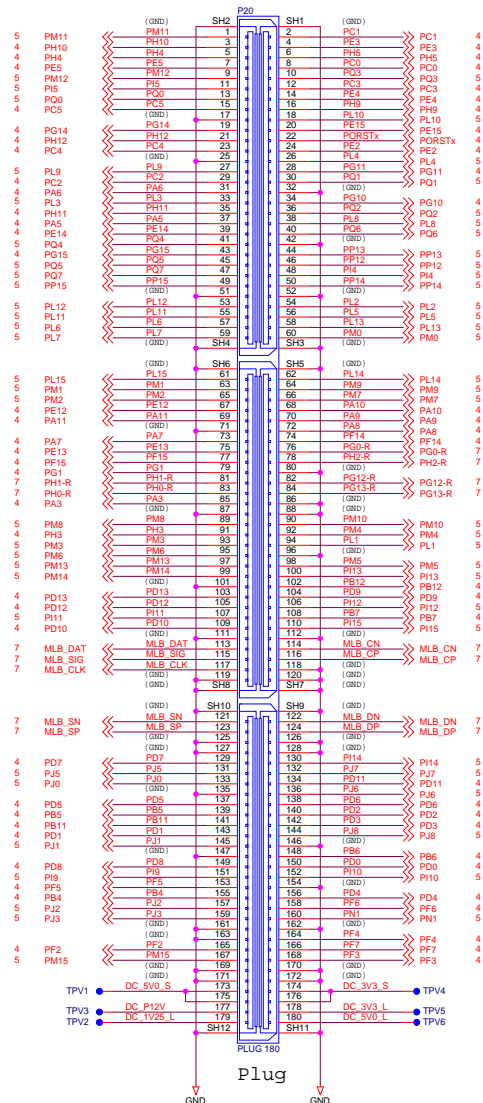
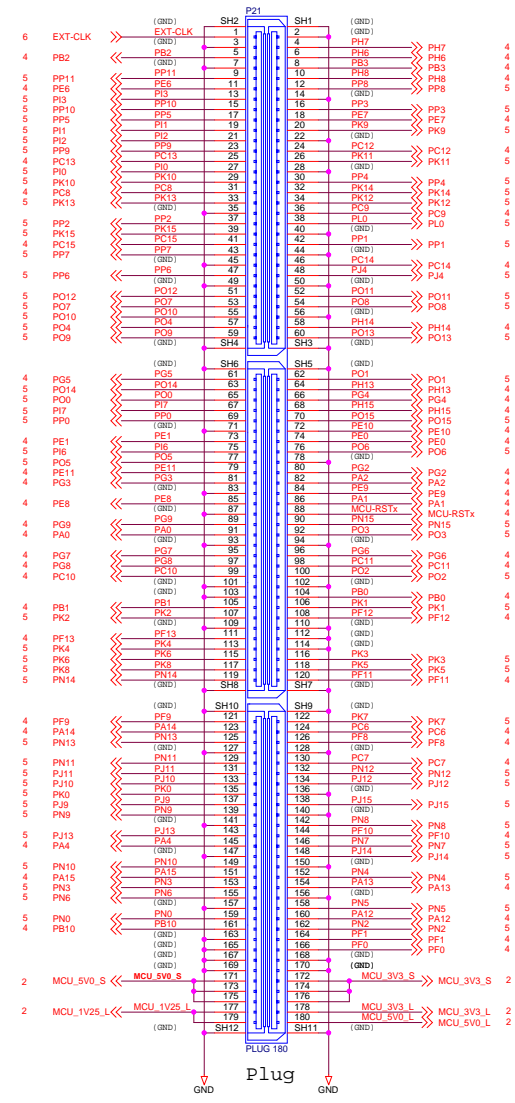
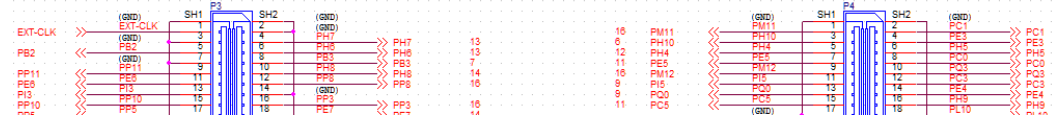


Daughter Card Connectors (Plugs)

Notes:

- there was no neat way to fit these connectors onto a B sized sheet so unfortunately the sheet size has been increased to C so will need to be printed on larger paper.
- The Crystal Signals are NOT routed via the daughtercard connectors
- The Specific MCU power pins are not routed via the daughter card however the jumpered MCU supply lines are brought up from the main board (see the top pins of the connector on the left)
- The connector schematic symbols have been horizontally mirrored so they match the main EVB connector. This has no bearing on the PCB placement or footprint. Pin1 on the receptacle mates with pin 1 on the plug.

Connectors on Main board (Shown for reference)



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Drawing Title: **Calypso 324 BGA Daughter Card**

Page Title: **Daughter Card Connectors (Plugs)**

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