MPC574xx Customer Evaluation Board (X-MPC574XG-MB)

Table Of Contents:

Revision Information

Rev	Date	Designer	Comments
0.1	01 Feb 2012	Alasdair Robertson	Start of capture, Working version
X1	19 Feb 2012	Alasdair Robertson	1st release for internal review (Complete Board)
X2	28 Feb 2012	Alasdair Robertson	2nd release for internal review (split into main board and DC)
X3	11 Mar 2013	Alasdair Robertson	Final review (including new USB transceiver)
X4	13 Mar 2013	Alasdair Robertson	Version sent to Pre Layout, incorporating fixes from review
X5	14 Mar 2013	Alasdair Robertson	Component consolodation, Few minor changes. Sent to Layout
X6	29 Mar 2013	Alasdair Robertson	Changes made during layout to Daughtercard Connectors
X7	02 Apr 2013	Alasdair Robertson	LAY RefDes Resequence and SCH BackAnnotate
A	17 Apr 2013	Alasdair Robertson	Post Layout (Back Annotated). Matches PCB RevA
AX1	24 Jun 2013	Alasdair Robertson	Fixes and changes to RevA Prototype design
AX2	10 July 2013	Alasdair Robertson	Added CAN Term (DNP)
AX3	12 July 2013	Alasdair Robertson	Corrected ground on ADC Pot
B	12 July 2013	Alasdair Robertson	Production Release
BX1	20 Aug 2013	Alasdair Robertson	Change to Ethernet 50MHz clock control
C	20 Aug 2013	Alasdair Robertson	Production Release
CX1	18 Dec 2013	Alasdair Robertson	CAN transceivers -> MC33901, ENET clock in RMII mode
CX2	05 May 2014	Alasdair Robertson	Added comment about LM1117 VREG output
CX3	25 June 2014	Alasdair Robertson	PH3..5 now GPIO matrix (was SAI), PM4, PD13, PM3 to SAI
CX4	26 June 2014	Alasdair Robertson	Minor changes made during layout (no component changes)
CX5	26 June 2014	Alasdair Robertson	Part Manager Tidy up
CX6	18 Aug 2014	Alasdair Robertson	Added additional connector with DSPI Signals for AVB
CX7	03 Sept 2014	Alasdair Robertson	Added additional TWRPI header (Sheet 12)
D	24 Sept 2014	Alasdair Robertson	Released to Production (RevD PCB)

Caution:

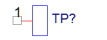
These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hile Pad Large (for standard 0.1" header).
Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop



Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2. 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

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Designer: A. Robertson	Drawing Title: MPC574XG-MB		
Drawn by: A. Robertson	Page Title: Index and Title Page		
Approved: A. Robertson	Size B	Document Number SCH-27897 PDF: SPF-27897	Rev D
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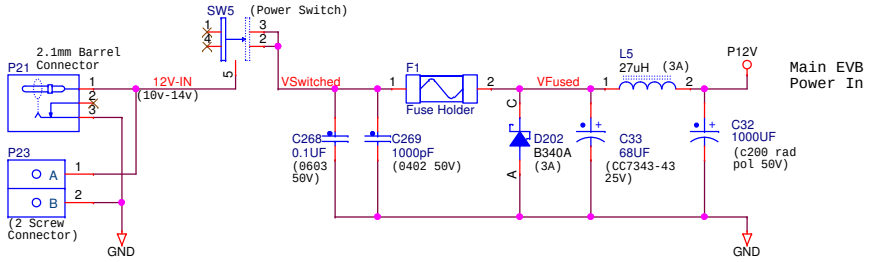
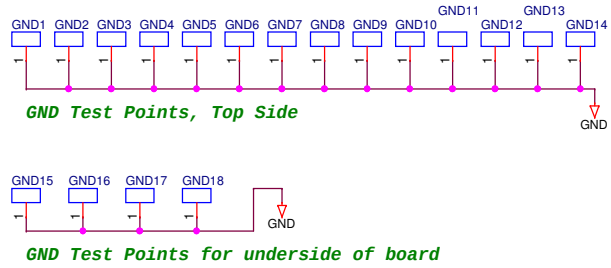
Power Input and Linear Voltage Regulators

Input 12V DC nominal (range 10v - 14v)
See note on schematic sheet 3 regarding 3.3V regulator when running at < 11V)

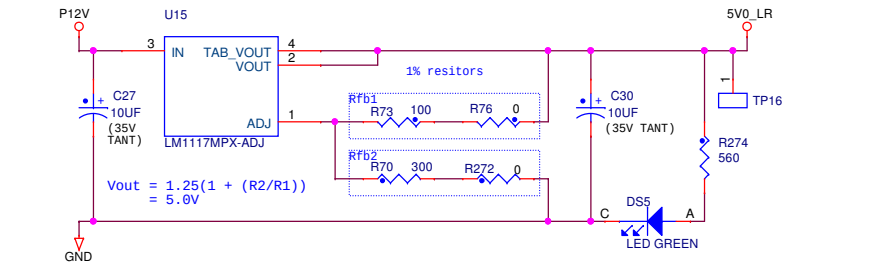
Power Supply Input and Filter



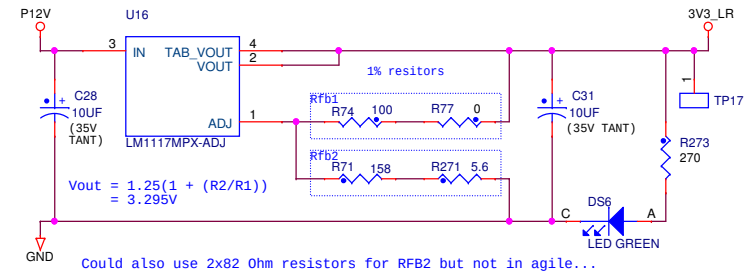
Test and reference points



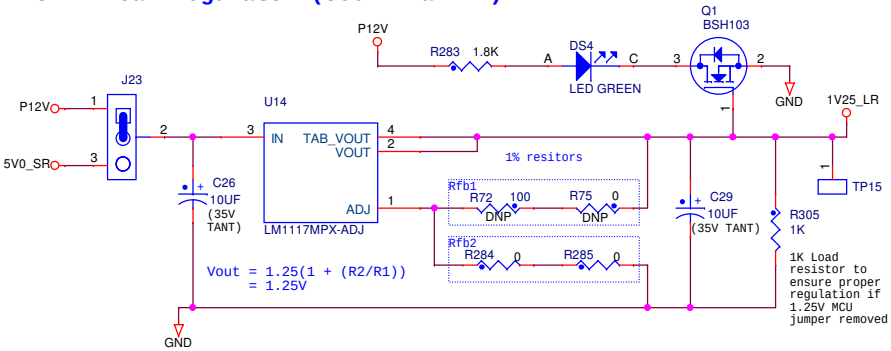
5.0V Linear Regulator (800mA Max **)



3.3V Linear Regulator (800mA Max **)



1.25V Linear Regulator (800mA Max **)



1.25V for External core supply. Simpler to use linear rather than switcher so can safely power from 5V switcher (slight ripple not an issue) for reduced heat dissipation

** Notes on Linear Regulator LM1117

The LM1117 linear regulators provide a maximum output current of 800mA in ideal conditions. The current requirement for each regulator is in the region of 10's of mA (significantly under the maximum rating) so these regulators will run cool on the EVB.

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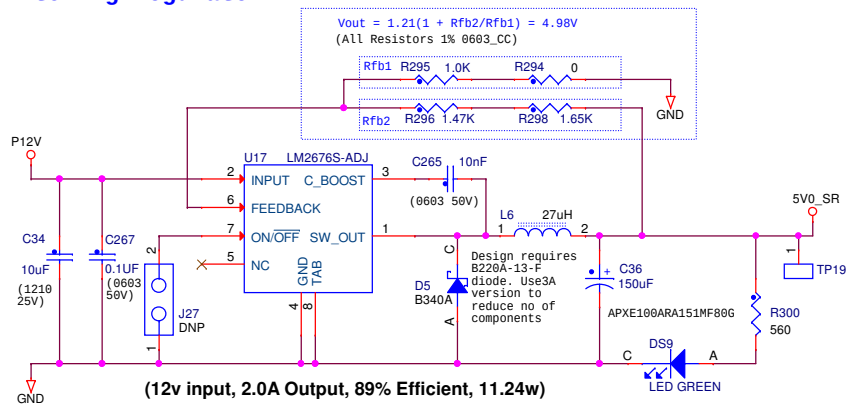
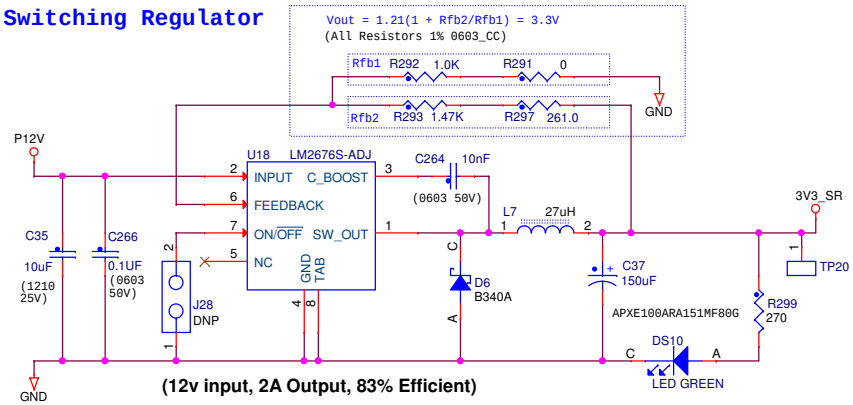
Switching Voltage Regulators and Supply Jumpers

5.0v Switching Regulator



(12v input, 2.0A Output, 89% Efficient, 11.24w)

3.3v Switching Regulator



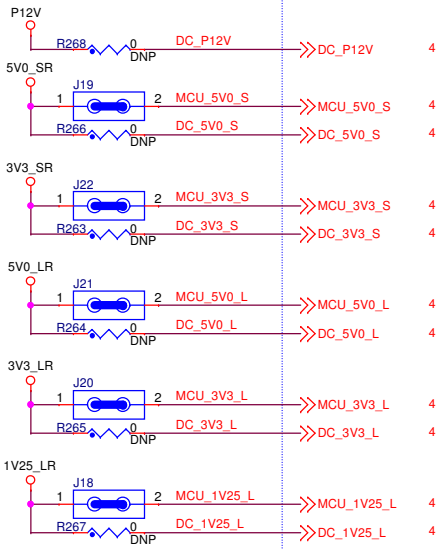
(12v input, 2A Output, 83% Efficient)

Caution The 3.3v regulator design is optimised for an input voltage of 12V. If the input voltage drops below approx 11V, the 3.3v output voltage ripple may increase. This can be reduced by increasing the bulk storage capacitor if required.

Using Adjustable version of LM2676 rather than fixed 3.3V / 5V regulators to reduce number of components in BOM.

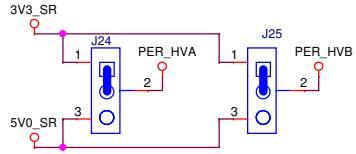
Where possible, components have been shared accross the regulator designs to further reduce component count.

Global MCU Daughtercard Supply Jumpers and DC power



To Daughtercard Connectors

Peripheral Power Control



These jumpers control the voltage of the peripherals connected to MCU pads in the VDD_HV_A / HV_B domains and are required so the respective jumpers at the MCU can be used for MCU current measurement.

The settings on these jumpers must mirror the setting of the respective MCU VDD_HV_A / HB_V jumpers

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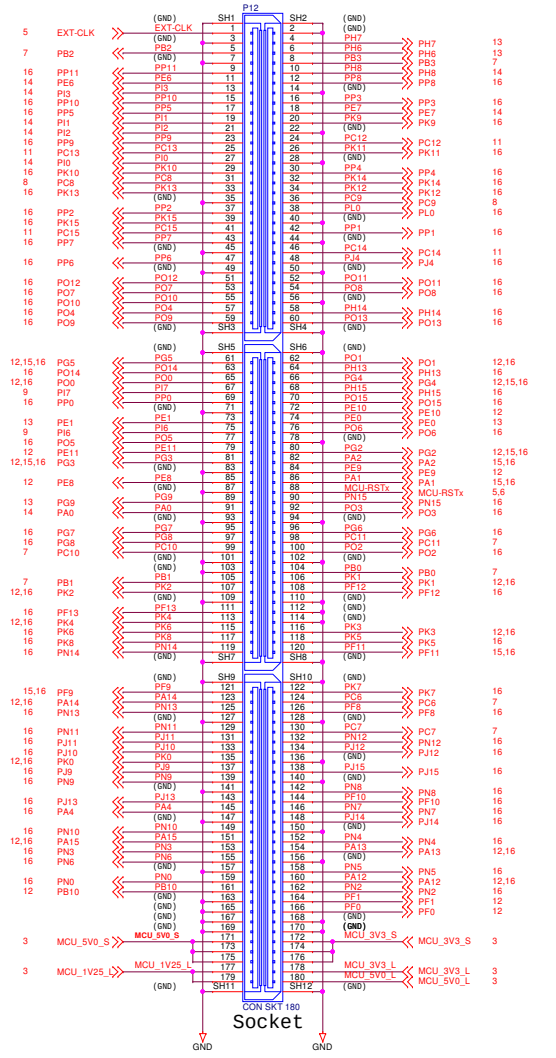
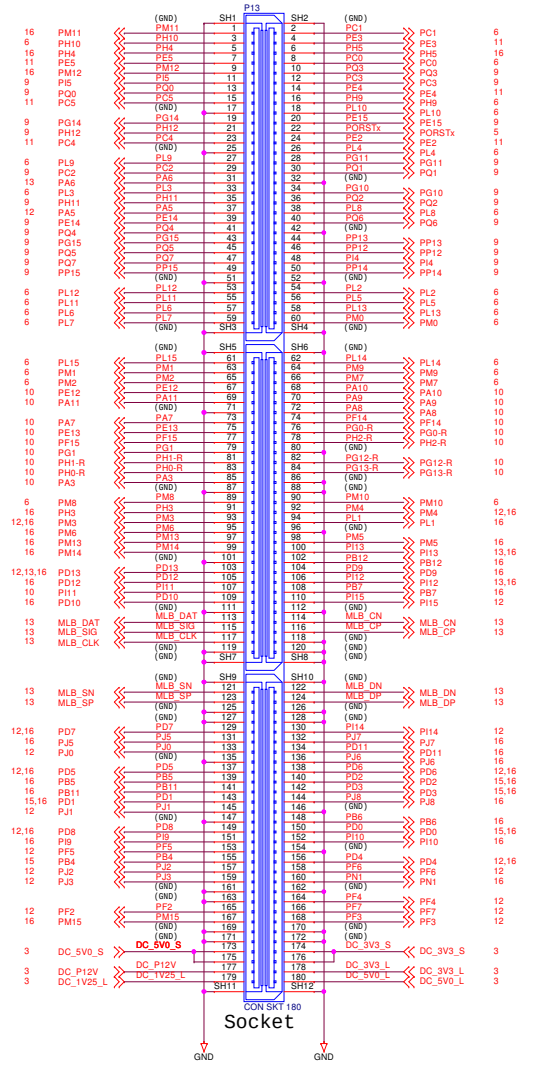
Daughter Card Connectors (Sockets)

Notes:

- there was no neat way to fit these connectors onto a B sized sheet so unfortunately the sheet size has been increased to C so will need to be printed on larger paper.

- The MCU Clock circuitry (apart from external clock) is local to the daughtercard so not pinned out on the connectors
- Power is supplied to the daughtercard via MCU specific jumpered supplies (left connector) or direct supplies from the regulators (right connector)





Not routed through the connectors:
- Crystal signals
- Specific MCU power pins (Power supplies are however taken to daughtercard)

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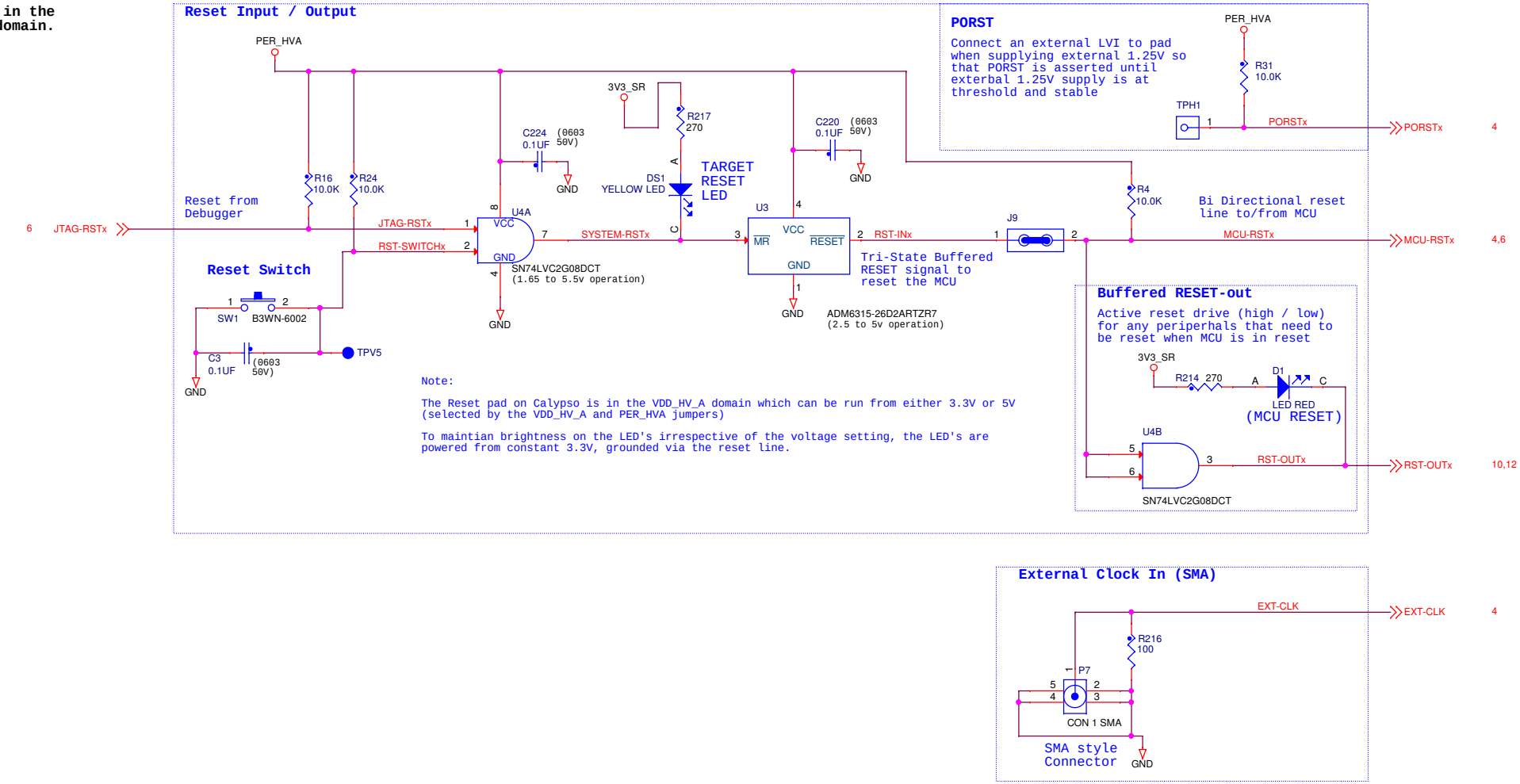
Reset and External Clock In

Reset is in the VDD_HVA domain.



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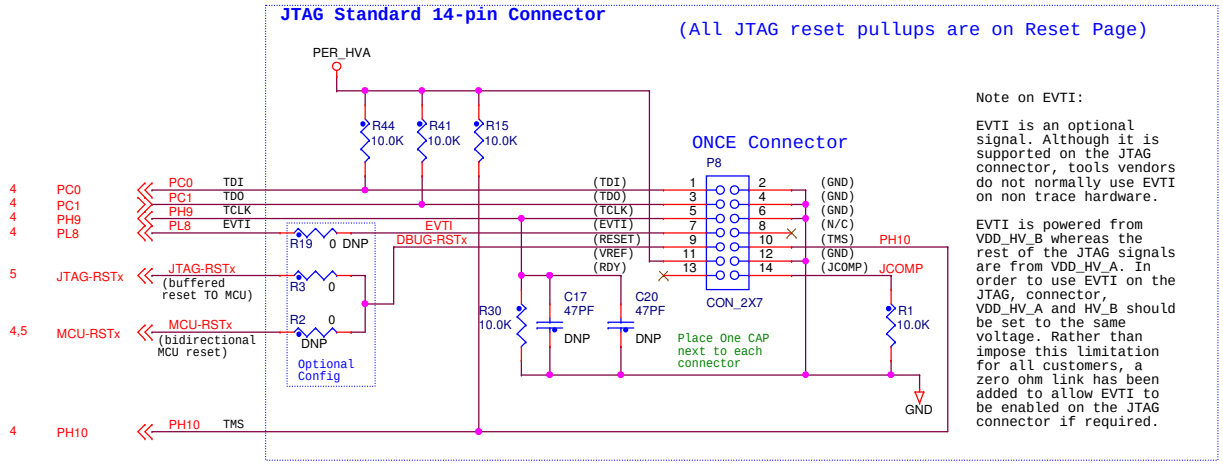
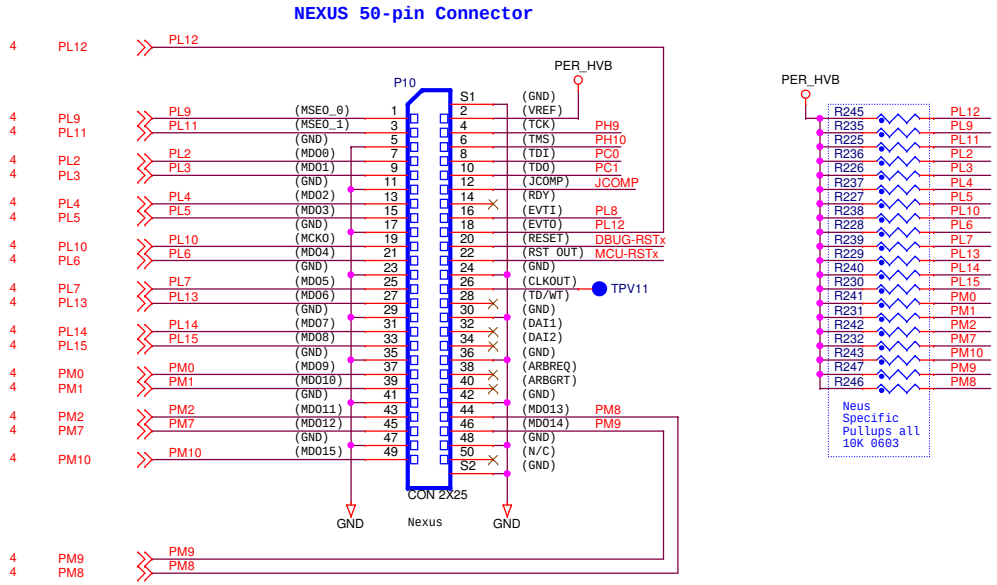
Debug Connectors (JTAG and NEXUS)





Voltage Domains:

All of the signals used for JTAG (with the exception of EVTI, see note) are powered from the VDD_HV_A domain. All of the additional signals used for Nexus are powered from VDD_HV_B.

If you are using Nexus, you need to ensure that the VDD_HV_A and VDD_HV_B domains are at the same voltage as well as ensuring that the peripheral supplies PER_HVA and PER_HVB match VDD_HV_A / B. See the MCU power page for configuration jumpers.

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CAN & LIN Physical

All CAN and LIN signals are in power domain VDD_HV_A.

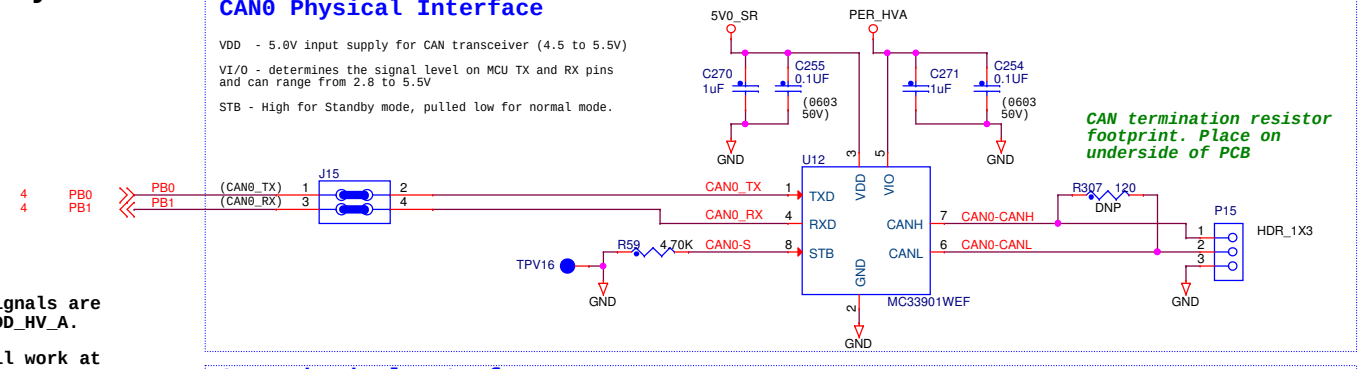
All interfaces will work at 3.3V or 5.0V (PER_HVA jumper)

CAN0 Physical Interface

VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)

VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V

STB - High for Standby mode, pulled low for normal mode.

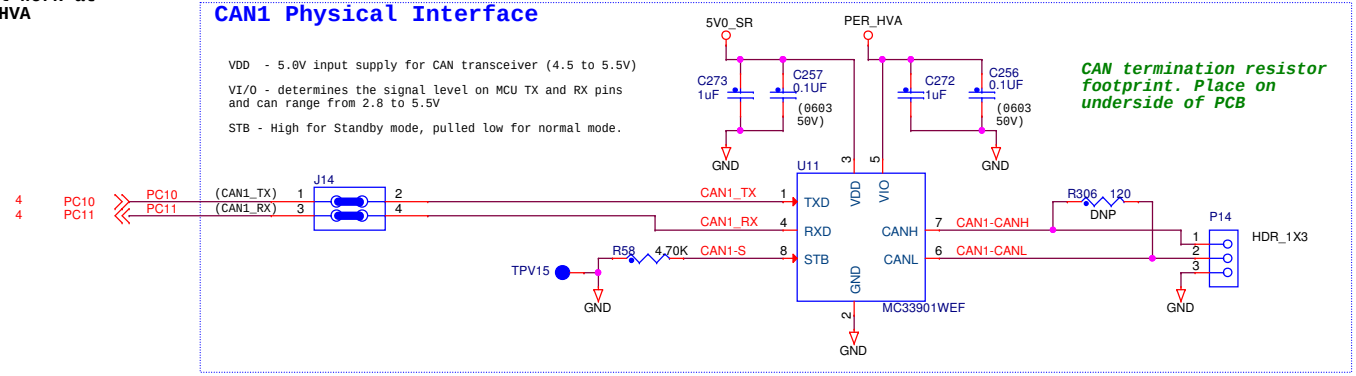


CAN1 Physical Interface

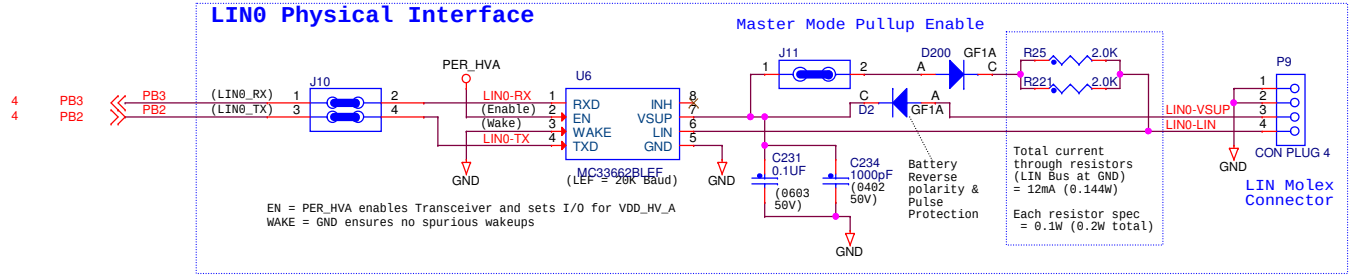
VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)

VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V

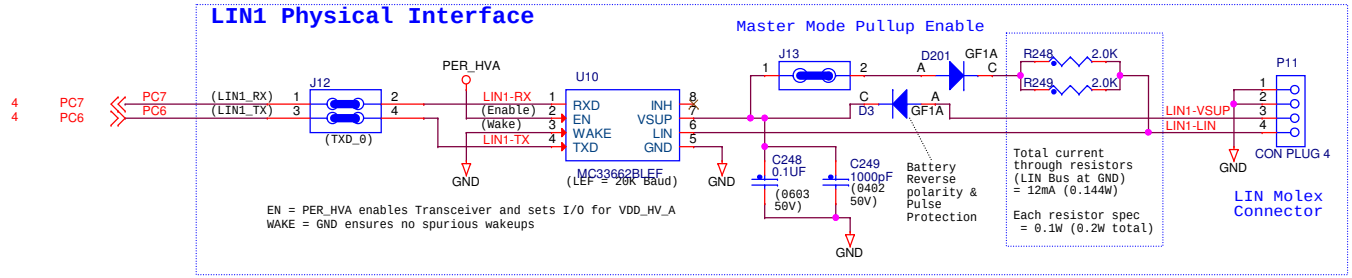
STB - High for Standby mode, pulled low for normal mode.



LIN0 Physical Interface



LIN1 Physical Interface



MC33662LEF LIN transceiver is newer version of 33661 offering:

- Full LIN compliance (33661 no longer compliant)
- Improved ESD protection on LIN pin up to 15KV
- Improved ESD on Wake and VSUP Pins
- Other EMC and performance improvements

See freescale.com for more details

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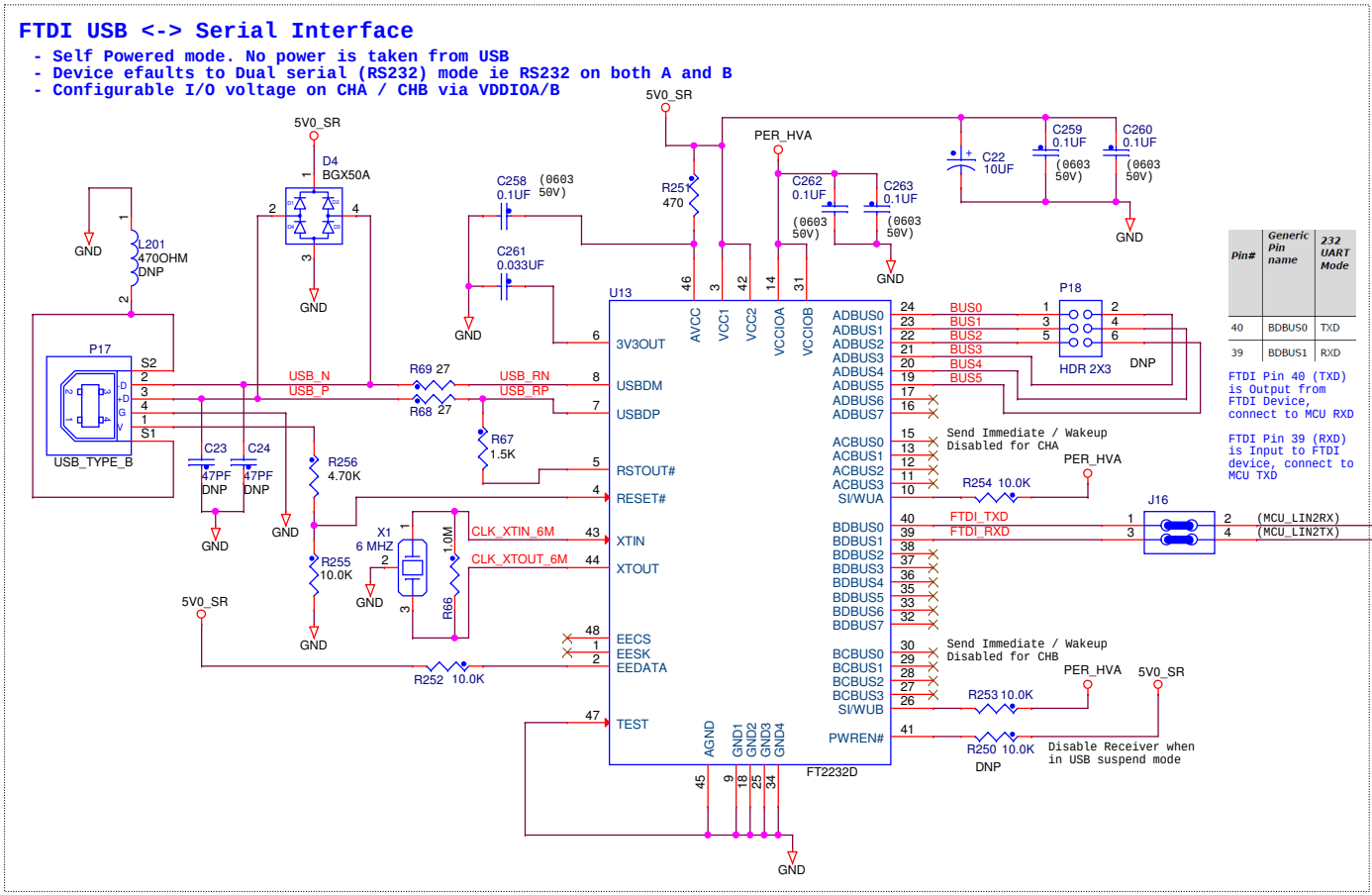
USB RS232 (serial) Interface

All Signals are in power domain VDD_HV_A.

FTDI interface will work at 3.3V or 5.0V (PER_HVA jumper)



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USB (Type A Host and Type AB OTG)

USB Signals are in power domain VDD_HV_A

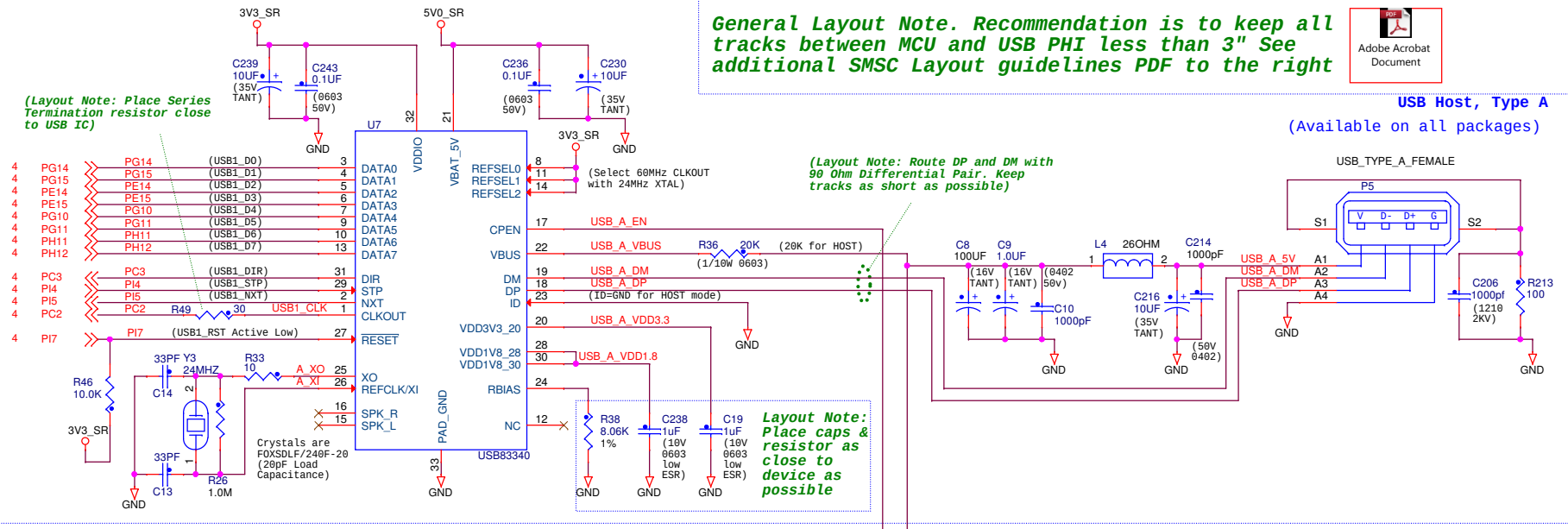
The USB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, USB MCU pads must be left as tri-state with no pullups.

General Layout Note. Recommendation is to keep all tracks between MCU and USB PHI less than 3" See additional SMSC Layout guidelines PDF to the right

Adobe Acrobat Document

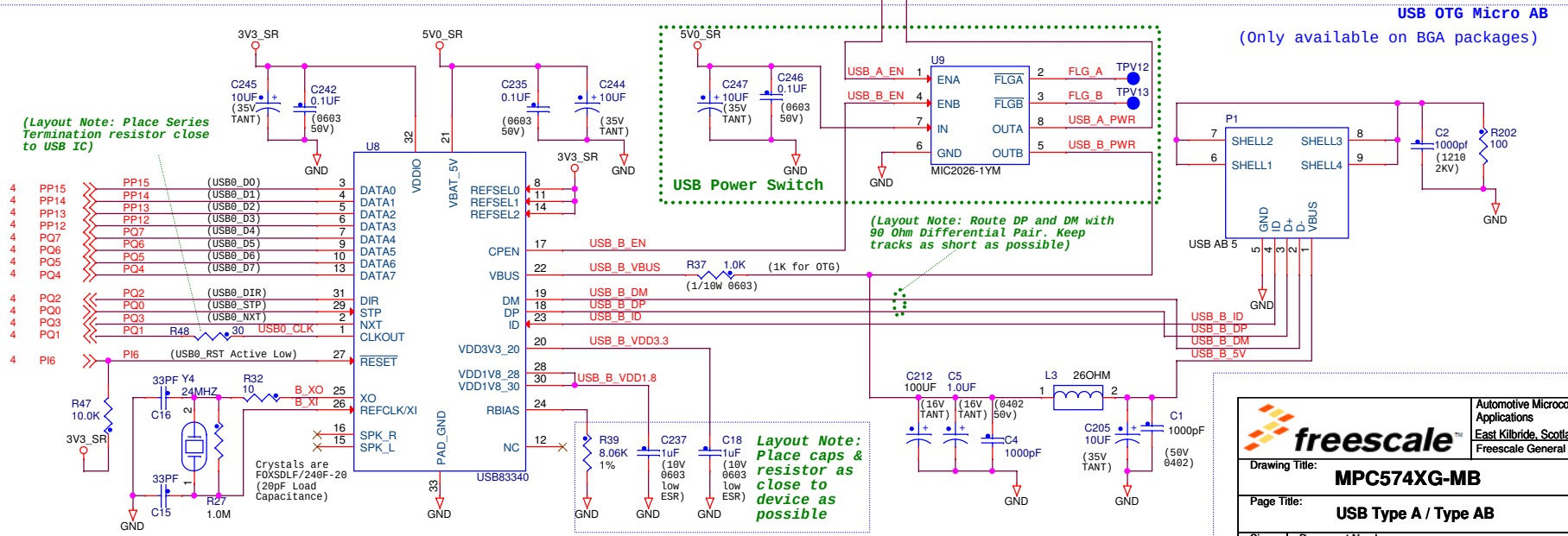
USB Host, Type A

(Available on all packages)



USB OTG Micro AB

(Only available on BGA packages)



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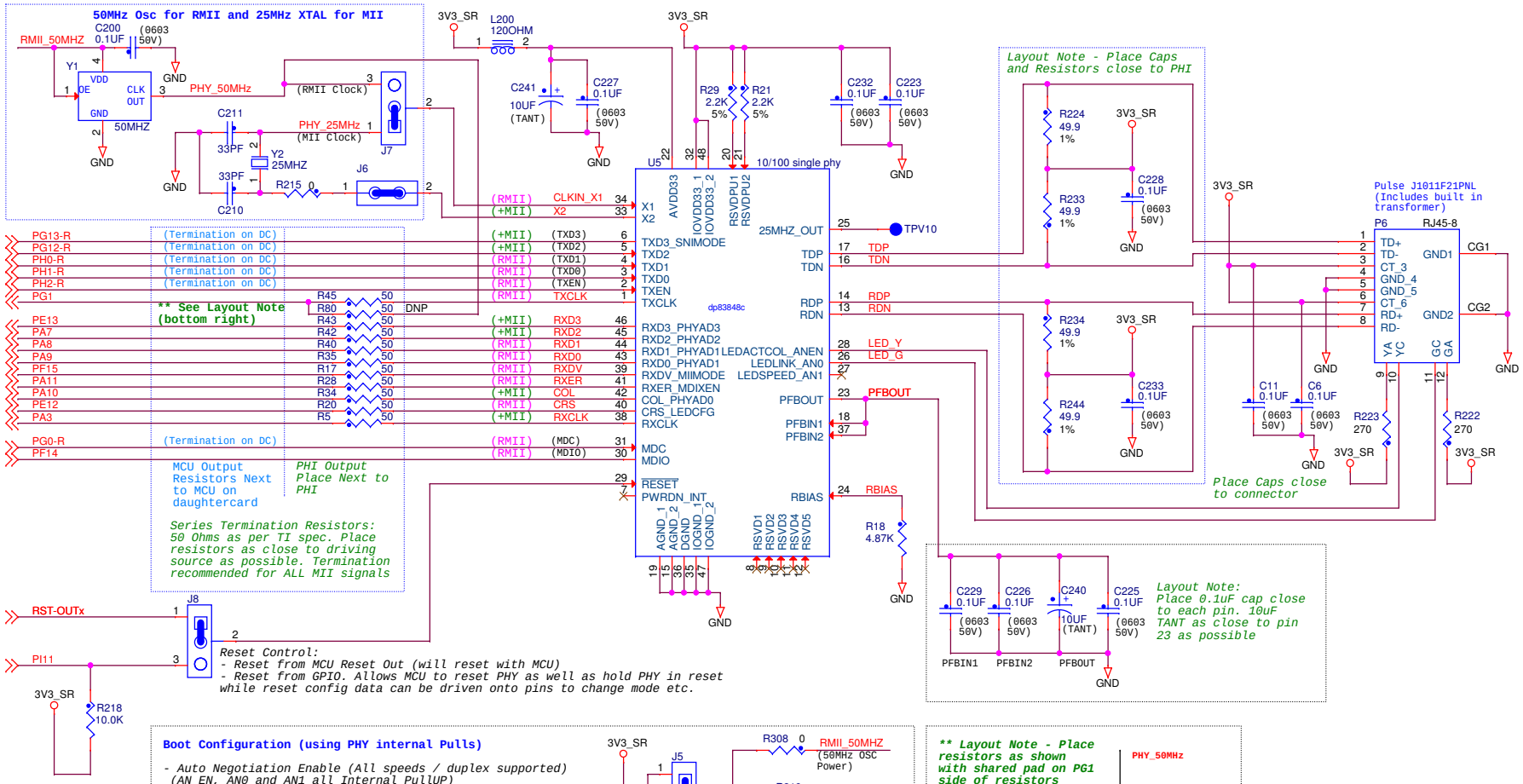
Ethernet

All Ethernet Signals are in power domain VDD_HV_B

The Ethernet interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, Ethernet MCU pads must be left as tri-state with no pullups.



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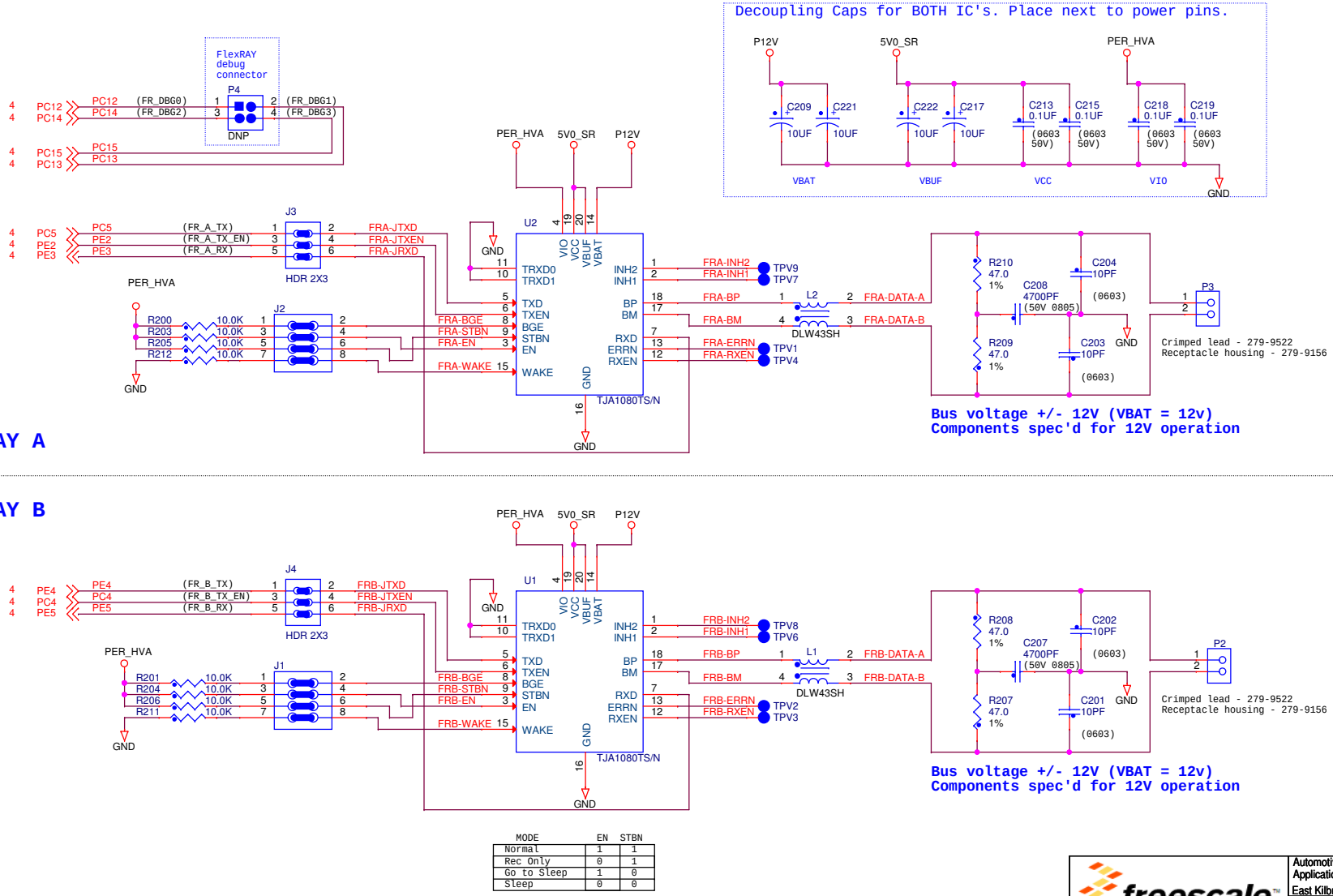
FlexRAY Physical Interface

All Signals are in power domain VDD_HV_A.

FlexRAY interface will work at 3.3V or 5.0V (PER_HVA jumper)



MODE	EN	STBN
Normal	1	1
Rec Only	0	1
Go to Sleep	1	0
Sleep	0	0

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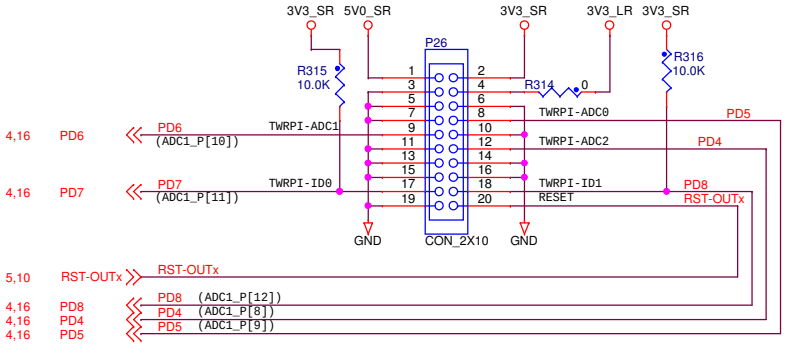
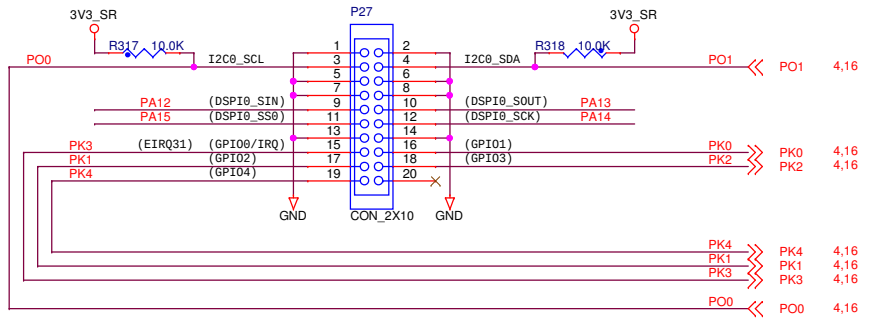
SAI Audio, AVB & TWRPI Connectors

General Purpose TWRPI

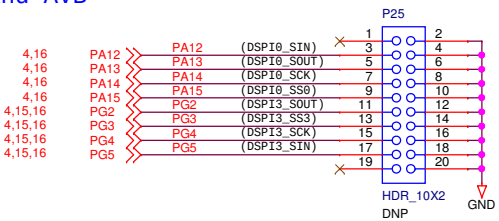


Note: Ports PD[4..8] are shared with the GPIO Matrix



Note: Ports PK[0..5] are shared with the GPIO Matrix

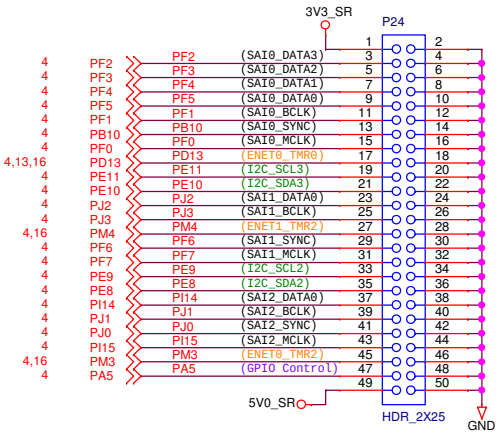
SAI Audio and AVB



Pins used on this header are also at GPIO Matrix

PA12 - DSPI0_SIN (Also shared with TWRPI)
PA13 - DSPI0_SOUT (Also shared with TWRPI)
PA14 - DSPI0_SCK (Also shared with TWRPI)
PA15 - DSPI0_SS0 (Also shared with TWRPI)

PG2 - DSPI3_SOUT (Also shared with User LED)
PG3 - DSPI3_SS3 (Also shared with User LED)
PG4 - DSPI3_SCLK (Also shared with User LED)
PG5 - DSPI3_SIN (Also shared with User LED)



Differences to RevC
Pin 17 was PH5, now PD13** (PH5 now routed to GPIO Matrix)
Pin 27 was PH4, now PM4 (PH4 now routed to GPIO Matrix)
Pin 45 was PH3, now PM3 (PH3 now routed to GPIO Matrix)

** Note PD13 is also routed to MLB header via DNP link

Black - SAI Channels
Green - I2C Channels
Orange - ENET TMRx channels

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Drawing Title: **MPC574XG-MB**

Page Title: **SAI Audio, AVB & TWRPI Headers**

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MLB (SMSC) Daughtercard Connector

Layout Note: MLB track lengths should be < 80mm (from MCU through daughter card to connector)

All MLB Signals are in power domain VDD_HV_C.

The MLB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVC is set to 5V, MLB MCU pads must be left as tri-state with no pullups.

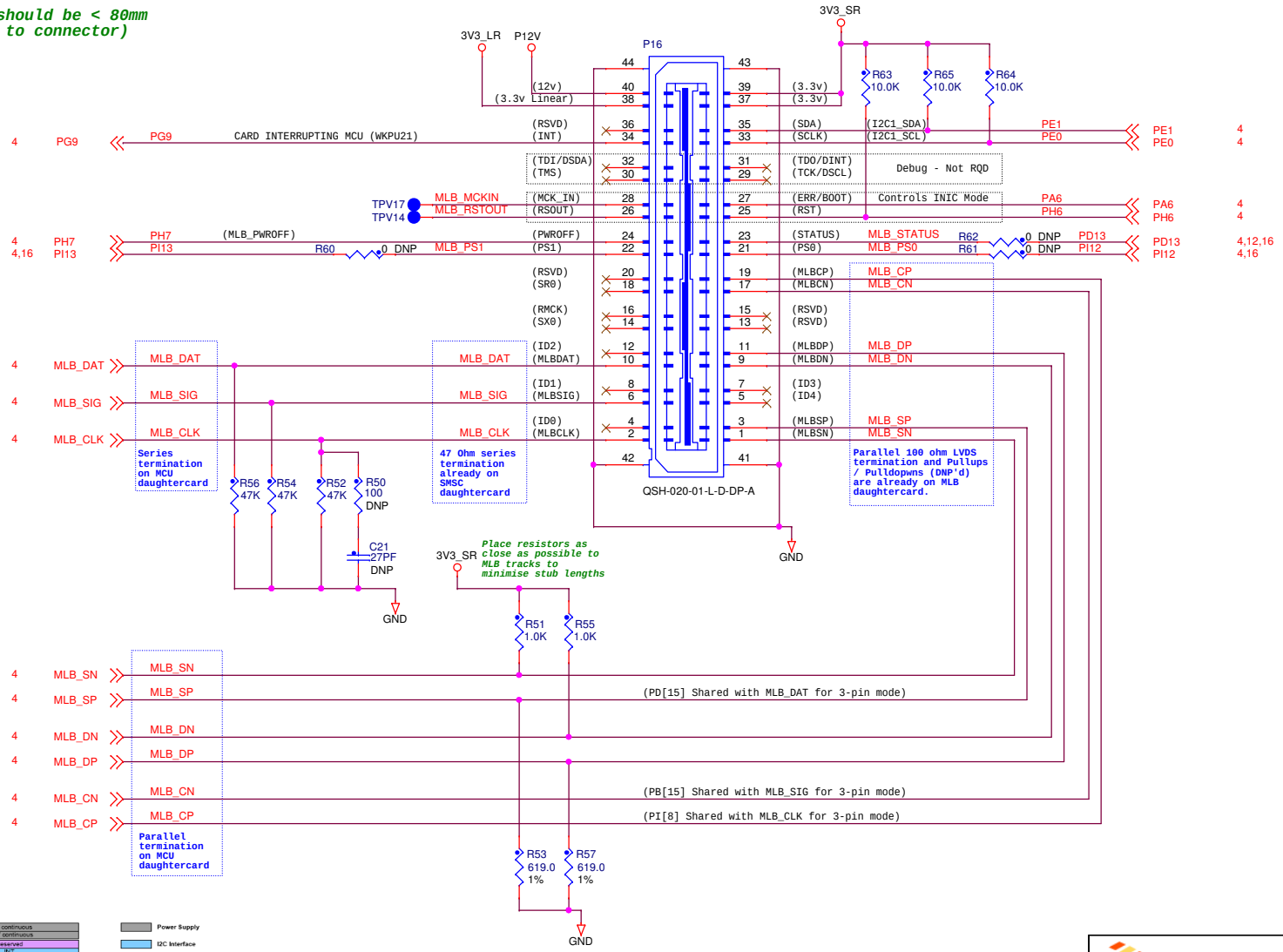

Figure 5-1. Connector Interface to Main Board

Pin 39	3.3 V switched
Pin 37	3.3 V switched
Pin 35	SDA
Pin 33	SCL
Pin 31	TDO/DINT
Pin 29	TCK/DSCL
Pin 27	ERR/BOOT
Pin 25	RST
Pin 23	STATUS (STATUS/NDACT/SCSUB)
Pin 21	PS0
Pin 19	Reserved
Pin 17	Reserved
Pin 15	Reserved (MOST_RXP)
Pin 13	Reserved (MOST_RXN)
Pin 11	FSY
Pin 9	SCK
Pin 7	PhyIntfBrd_ID3
Pin 5	PhyIntfBrd_ID4
Pin 3	Reserved
Pin 1	Reserved

Pin 40	12 V continuous
Pin 38	3.3 V continuous
Pin 36	Reserved
Pin 34	INT
Pin 32	TDI/DSDA
Pin 30	TMS
Pin 28	MCK_IN
Pin 26	RSOUT
Pin 24	PWROFF
Pin 22	PS1
Pin 20	Reserved
Pin 18	RST
Pin 16	RMCK
Pin 14	SDA
Pin 12	PhyIntfBrd_ID2
Pin 10	MLBDAT
Pin 8	PhyIntfBrd_ID1
Pin 6	MLBSIG
Pin 4	PhyIntfBrd_ID0
Pin 2	MLBCLK

- Power Supply
- I2C Interface
- Debug & JTAG Interface
- Misc Signals
- Board ID
- Network Interface
- RMCK
- I2S Interface
- MediaLB 3-Pin

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Drawing Title: **MPC574XG-MB**

Page Title: **MLB SMSC Daughtercard Connector**

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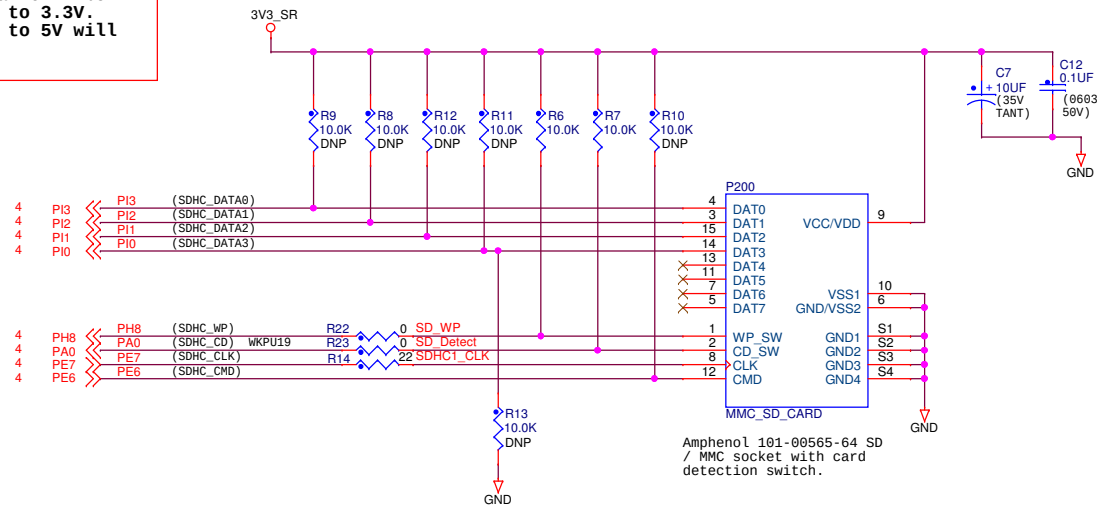
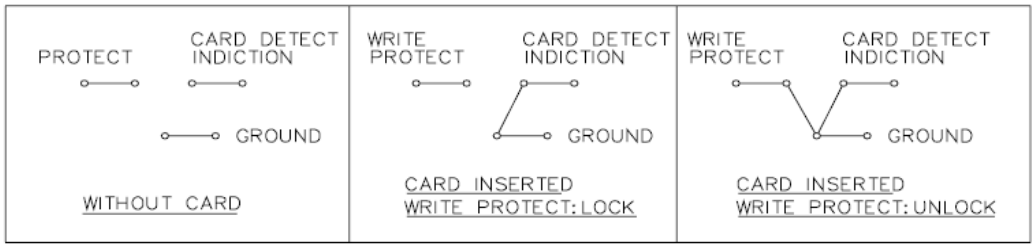
SD Connector

Caution

The SD card specification details an operating voltage of between 2.7 and 3.6V. If using the SD card, it can ONLY be used when VDD_HV_A (and PER_HVA) jumpers are set to 3.3V. Inserting an SD card with VDD_HV_A / PER_HVA set to 5V will result in card damage.





Card Detect: **Grounded when Card Inserted, Pulled high when card removed**
Write Protect: **Grounded when NOT protected, Pulled high when protected (or card removed)**

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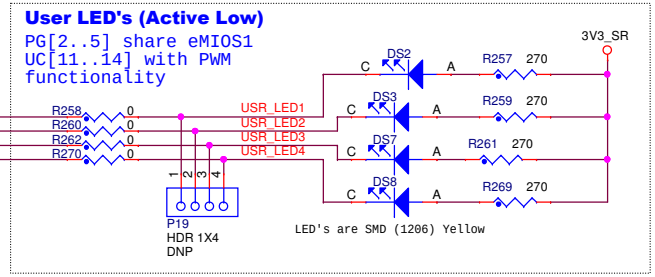
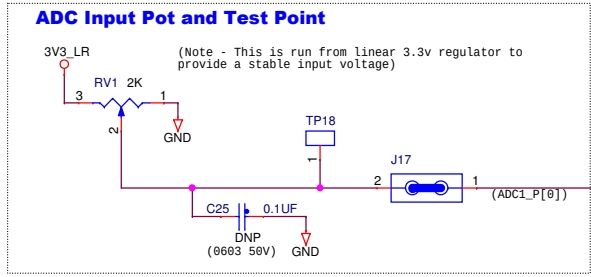
User Peripherals, Audio Controls and GPIO

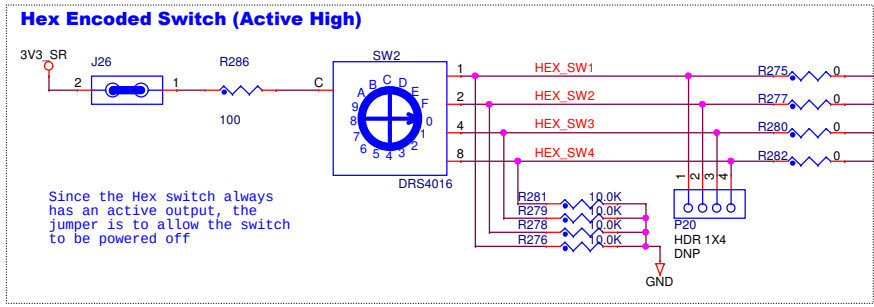
Switches are hard wired to 3.3V rather than 5V so it's not possible to drive 5V into a 3.3V pad (which would cause damage)
Similarly, the LED's are active low with 3.3v supply so can be safely coupled to pads on either 3.3V or 5V domains
The ADC input is limited to 3.3V, again to prevent driving 5V into a 3.3V pad which would cause damage

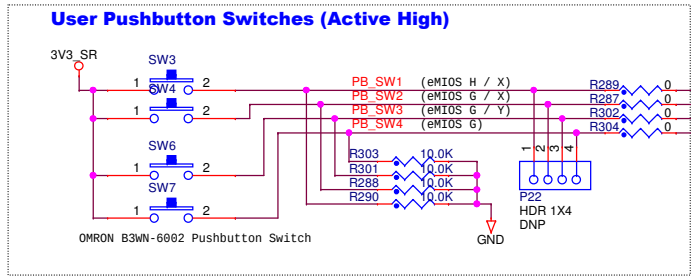
Note that LED2 and LED4 (PG3 and PG5) can be controlled in LPU_RUN mode (and also have pad keepers in LPU_STANDBY)





The LED's, Hex switches and push-button switches are connected to MCU pads vvia zero ohm links. If desired these can be removed and direct connection made to the LED or switch. All of the ports used for LED's / Switches are also bonded out to the GPIO matrix





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GPIO Pin Matrix

All pads are DNP (Do Not Populate) 0.1" pitch headers placed on a 0.1" grid

PA[1,2] shared with user switches

PA[12..15] shared with SAI Audio and TWRPI

PD[0..3] shared with Hex Switch

PD[4..8] shared with TWRPI connector with pullup on PD[7], PD[8]

PD[13] shared with SAI Audio and MLB headers

PI[12,13] shared with MLB header

PK[0..4] shared with TWRPI header

PORTA

PA1	1	IOM7	
PA2	1	IOM14	
PA4	1	IOM28	
PA12	1	IOM96	
PA13	1	IOM106	
PA14	1	IOM116	
PA15	1	IOM123	

PORTB

PB5	1	IOM37	
PB6	1	IOM46	
PB7	1	IOM55	
PB11	1	IOM87	
PB12	1	IOM97	

PORTC

No spare pins on PortE

PORTD

PD0	1	IOM1	
PD1	1	IOM8	
PD2	1	IOM15	
PD3	1	IOM21	
PD4	1	IOM29	
PD5	1	IOM38	
PD6	1	IOM47	
PD7	1	IOM56	
PD8	1	IOM63	
PD9	1	IOM71	
PD10	1	IOM79	
PD11	1	IOM88	
PD12	1	IOM98	
PD13	1	IOM107	

PORTE

No spare pins on PortE

PORTF

PF8	1	IOM64	
PF9	1	IOM72	
PF10	1	IOM80	
PF11	1	IOM89	
PF12	1	IOM99	
PF13	1	IOM108	

PORTG

PG2	1	IOM16	
PG3	1	IOM22	
PG4	1	IOM30	
PG5	1	IOM39	
PG6	1	IOM48	
PG7	1	IOM57	
PG8	1	IOM65	

PORTH

PH3	1	IOM132	
PH4	1	IOM131	
PH5	1	IOM130	
PH13	1	IOM109	
PH14	1	IOM117	
PH15	1	IOM124	

PORTI

PI9	1	IOM73	
PI10	1	IOM81	
PI12	1	IOM100	
PI13	1	IOM110	

PORTJ

PJ4	1	IOM31	
PJ5	1	IOM40	
PJ6	1	IOM49	
PJ7	1	IOM58	
PJ8	1	IOM66	
PJ9	1	IOM74	
PJ10	1	IOM82	
PJ11	1	IOM90	
PJ12	1	IOM101	
PJ13	1	IOM111	
PJ14	1	IOM118	
PJ15	1	IOM125	

PORTK

PK0	1	IOM2	
PK1	1	IOM9	
PK2	1	IOM17	
PK3	1	IOM23	
PK4	1	IOM32	
PK5	1	IOM41	
PK6	1	IOM50	
PK7	1	IOM59	
PK8	1	IOM67	
PK9	1	IOM75	
PK10	1	IOM83	
PK11	1	IOM91	
PK12	1	IOM102	
PK13	1	IOM112	
PK14	1	IOM119	
PK15	1	IOM126	

PORTL

PL0	1	IOM3	
PL1	1	IOM10	

PORTM

PM3	1	IOM24	
PM4	1	IOM33	
PM5	1	IOM42	
PM6	1	IOM51	
PM11	1	IOM92	
PM12	1	IOM103	
PM13	1	IOM113	
PM14	1	IOM120	
PM15	1	IOM127	

PORTN

PN0	1	IOM4	
PN1	1	IOM11	
PN2	1	IOM18	
PN3	1	IOM25	
PN4	1	IOM34	
PN5	1	IOM43	
PN6	1	IOM52	
PN7	1	IOM60	
PN8	1	IOM68	
PN9	1	IOM76	
PN10	1	IOM84	
PN11	1	IOM93	
PN12	1	IOM104	
PN13	1	IOM114	
PN14	1	IOM121	
PN15	1	IOM128	

PORTO

PO0	1	IOM5	
PO1	1	IOM12	
PO2	1	IOM19	
PO3	1	IOM26	
PO4	1	IOM35	
PO5	1	IOM44	
PO6	1	IOM53	
PO7	1	IOM61	
PO8	1	IOM69	
PO9	1	IOM77	
PO10	1	IOM85	
PO11	1	IOM94	
PO12	1	IOM105	
PO13	1	IOM115	
PO14	1	IOM122	
PO15	1	IOM129	

PORTP

PP0	1	IOM6	
PP1	1	IOM13	
PP2	1	IOM20	
PP3	1	IOM27	
PP4	1	IOM36	
PP5	1	IOM45	
PP6	1	IOM54	
PP7	1	IOM62	
PP8	1	IOM70	
PP9	1	IOM78	
PP10	1	IOM86	
PP11	1	IOM95	

PORTQ

No spare pins on PortQ

PF[9,11] shared with user switches

PG[2..5] shared with user LED's, SAI and TWRPI headers

PM[3..4] shared with SAI Audio header

PO[0..1] shared with TWRPI header

Busses are not used on ports as it makes it harder to see which pins are shared with other functions

14 GND Pads (one at bottom of each colum)

TPH2 TPH3 TPH4 TPH5 TPH6 TPH7 TPH8 TPH9 TPH10 TPH11 TPH12 TPH13 TPH14 TPH15 → GND

Layout Notes:

Pads must be placed in a 13 x 16 matrix pattern, 2.54 mm pitch

- 13 wide (one column for each port EXCLUDING those with no available pads ie C, E, H, Q)

- 16 tall (1 row for each port number from 0 to 15).

- GND pad at bottom of each colum

- After production, pads should be through hole (not solder filled)

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