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Revisions			
Rev	Description	Date	Approved
X1	Initial Draft	18/09/13	David Erasmus
X2	Memory section updated (A070 release)	24/09/13	David Erasmus
X3	1. J23 changed as 1X2 header to sel only 3.3V 2. Transistor&Diode, changed from SQ2301 & SS8P3L to PMV65XP & STPS8L30B in 1.25V onboard reg section	26/09/13	David Erasmus
X4	1. Reset Section buffer updated and circuit modified to reduce a jumper	07/10/13	David Erasmus
X5	1. extra TP on net 1.25V_SR removed	14/10/13	David Erasmus
A	1. Back Annatated 2. A085 release	16/10/13	David Erasmus

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<small>ICAP Classification:</small> FCP: FIUQ: X PUBI:		<small>Designer:</small> John Paul Franklin	
<small>Design Title:</small>		X-MPC5777C-516DS	
<small>Drawn by:</small> John Paul Franklin		<small>Page Title:</small>	
Table of Contents/Revisions			
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1. Unless Otherwise Specified:
 All resistors are in ohms, 5%, 1/8 Watt
 All capacitors are in uF, 20%, 50V
 All voltages are DC
 All polarized capacitors are aluminum electrolytic
2. Intruded lines coded with the same letter or letter combinations are electrically connected.
3. Device type numberis for reference only. the number varies with te manufacturer.
4. Special signal usage:
 _B Denotes - Active-Low Signal
 <> or [] Denotes - Vectored Signals
5. Inteeprer diagram in accordance with american National Standards Institute specifications, current revision, with the exception of logic block symbology

DEFAULT JUMPER SETTINGS

REFDES	Default settings	Description	Header	Jumper Type
J00	1 & 2	VDDA_B0 Selection	HR 1X2 TH	100H1L
J24	OPEN	VDDPLA Selection	HR 1X2 TH	100H1L
J7	1 & 2 (5.0V)	VDDA_MISC Select	HR 1X2 TH	100H1L
J8	1 & 2	VDDA_B0 Selection	HR 1X2 TH	100H1L
J9	1 & 2	VDDA_B0 Selection	HR 1X2 TH	100H1L
J10	1 & 2	VDDA_B0 Selection	HR 1X2 TH	100H1L
J11	1 & 2	VDDA_B0 Selection	HR 1X2 TH	100H1L
J12	1 & 2	VDDA_B0 Selection	HR 1X2 TH	100H1L
J13	1 & 2	VDDA_B0 Selection	HR 1X2 TH	100H1L
J14	2 & 3 (5.0V)	VDDA_B0 Selection	HR 1X3	200
J15	1 & 2	Reset Enable	1X2	200
J16	2 & 3 (3.3V)	5V SR Selection	HR 1X3	200
J17	1 & 2 (3.3V)	VDDB2 Selection	HR 1X3	200
J18	2 & 3 (5V)	VDDPWR Selection	HR 1X3	200
J19	2 & 3 (5.0V)	VDDPWR Selection	HR 1X3	200
J20	2 & 3 (5.0V)	5V SR Selection	HR 1X3	200
J21	2 & 3 (5.0V)	VDDERMA Selection	HR 1X3	200
J22	2 & 3	PMU to PM2A	HR 1X3	200
J23	1 & 2 (3.3V)	VDDB2A Selection	HR 1X3	200
J4	2 & 3 (00#1)	SRAM Chip Select	HR 1X3	200
J24	2 & 3 (5.0V)	VDD_B0 to B0IN	HR 1X3	200
J11	1 & 2 (3.3V)	TIAG VDD Selection	HR 1X3	200
J12	2 & 3 (00#)	RESSEL to 00#	HR 1X3	200
J25	2 & 3	RESSEL to 00#	HR 1X3	200
J6	1 & 2 (5.0V LB)	VDDA Selection	HR 1X3	200
J26	3 & 3	1.25V SR SR	HR 2X3	200
J15	3 & 5 (00#)	VDDV Selection	HR 2X3	200
J13	OPEN (00#)	3.3V Regulator Off	1X2	200
J14	OPEN (00#)	3V Regulator Off	1X2	200

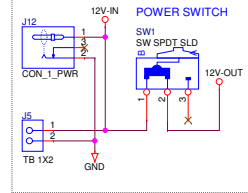


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 Drawing Title: **X-MPC5777C-516DS**
 Page Title: **NOTES**

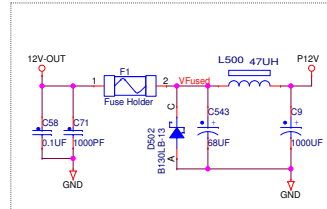
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Power supply : Connectors and Regulators

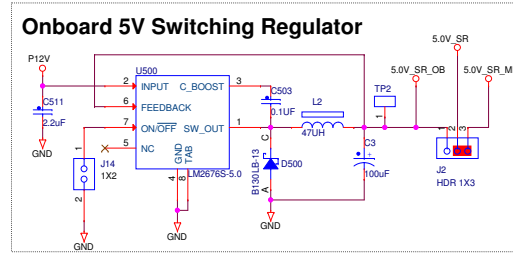
Input Power Connectors



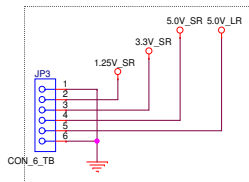
Power supply input and filter



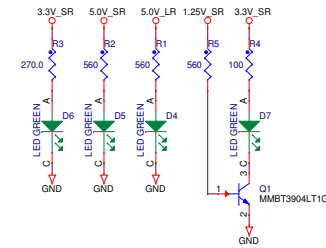
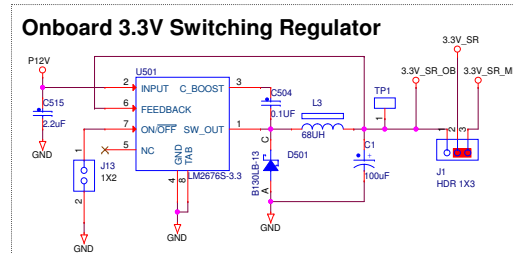
Onboard 5V Switching Regulator



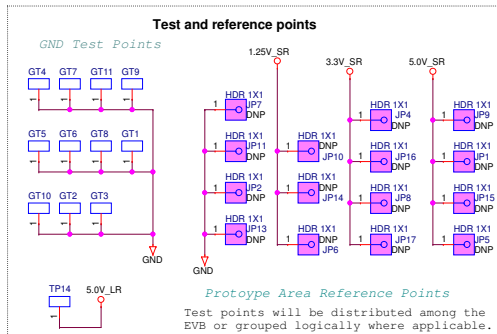
External Power feed



Onboard 3.3V Switching Regulator



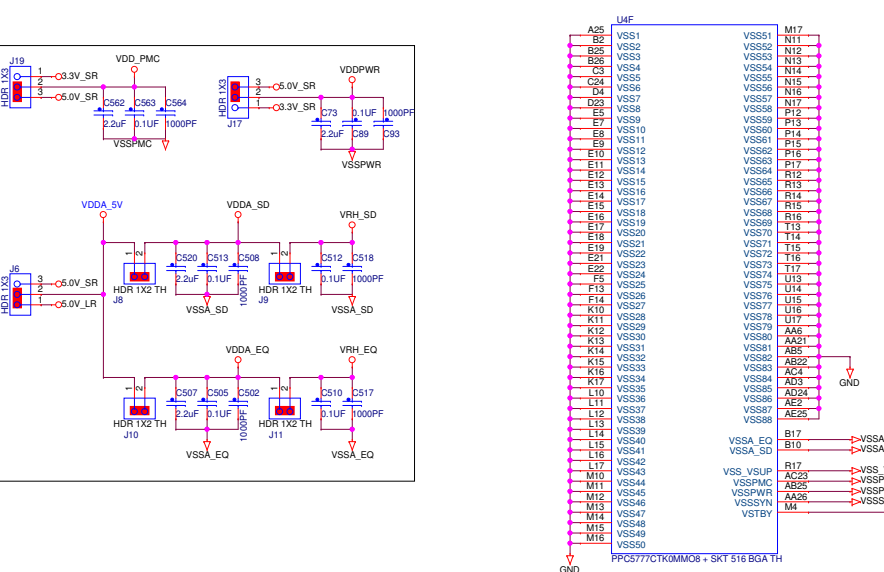
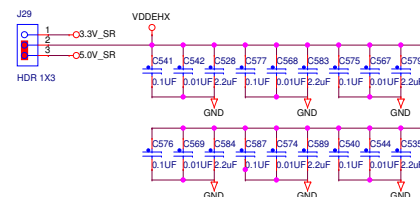
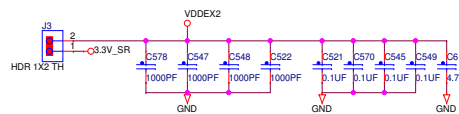
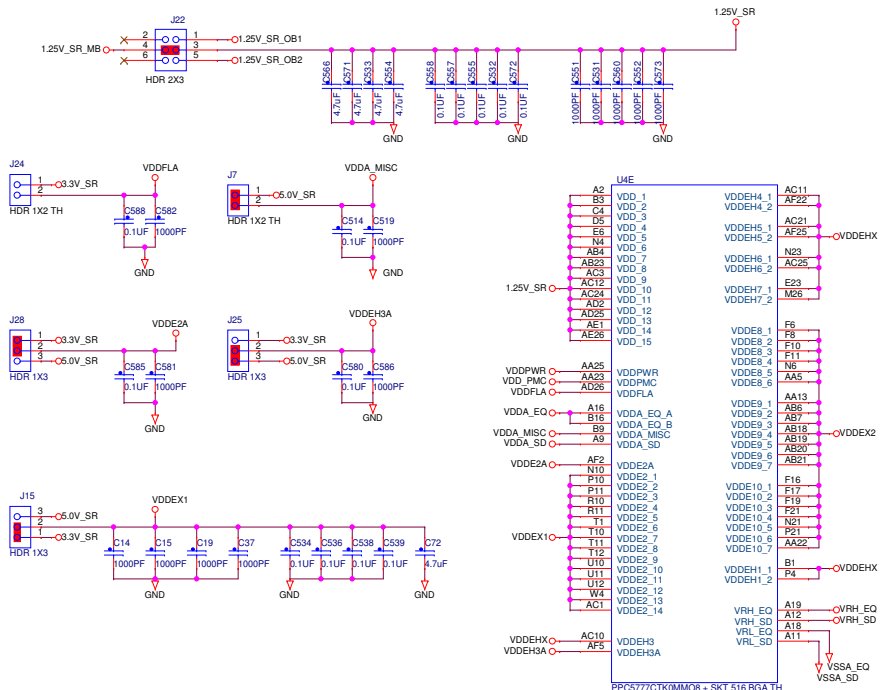
Test and reference points



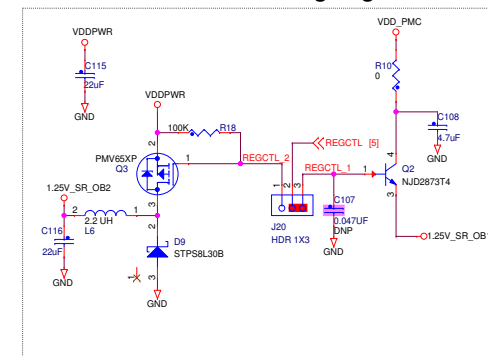
MCU Power and 1.2V Regulator

DEFAULT JUMPER SETTINGS

REFDES	Default settings	Description	Header	Jumper Type
J10	1 & 2	VDDA_EQ Selection	HDR 1X2 TH	100MIL
J24	OPEN	VDDPA Selection	HDR 1X2 TH	100MIL
J7	1 & 2 (5.0V)	VDDA_MISC Select	HDR 1X2 TH	100MIL
J8	1 & 2	VDDA_SD Selection	HDR 1X2 TH	100MIL
J9	1 & 2	VDDA_VS Selection	HDR 1X2 TH	100MIL
J11	1 & 2	VRH_EQ Selection	HDR 1X2 TH	100MIL
J29	2 & 3 (5.0V)	VDDER2_VDD Select	HDR 1X2 TH	100MIL
J3	1 & 2	Reset Enable	1X2	2981
J13	2 & 3 (4.3V)	VDDER3_VDD Select	HDR 1X3	2981
J17	2 & 3 (3V)	VDDPWR Selection	HDR 1X3	2981
J18	2 & 3 (5.0V)	VDDPWR Selection	HDR 1X3	2981
J22	2 & 3 (5.0V_MB)	5V_SR Selection	HDR 1X3	2981
J25	2 & 3 (5.0V)	VDDER3A Selection	HDR 1X3	2981
J26	2 & 3	VDDER3B Select	HDR 1X3	2981
J28	1 & 2 (3.3V)	VDDER2A Selection	HDR 1X3	2981
J4	2 & 3 (CS#1)	SRAM Chip Select	HDR 1X3	2981
J16	2 & 3 (18.0V)	VDD_VDDPWR	HDR 1X3	2981
J31	1 & 2 (3.3V)	JTAG VDD Selection	HDR 1X3	2981
J18	2 & 3 (GND)	REGSEL to GND	HDR 1X3	2981
J20	2 & 3	REGCTL1_25V_Ost	HDR 1X3	2981
J6	1 & 2 (5.0V_LR)	VDDA Selection	HDR 1X3	2981
J22	4 & 5	1.25V_SR_MB	HDR 2X3	2981
J16	3 & 5 (GND)	VREG Selection	HDR 2X3	2981
J11	OPEN (ON)	5.3V Regulator OFF	1X2	2981
J14	OPEN (ON)	5V Regulator OFF	1X2	2981



Onboard 1.25V Switching Regulator



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Drawing Title: X-MPC577C-516DS

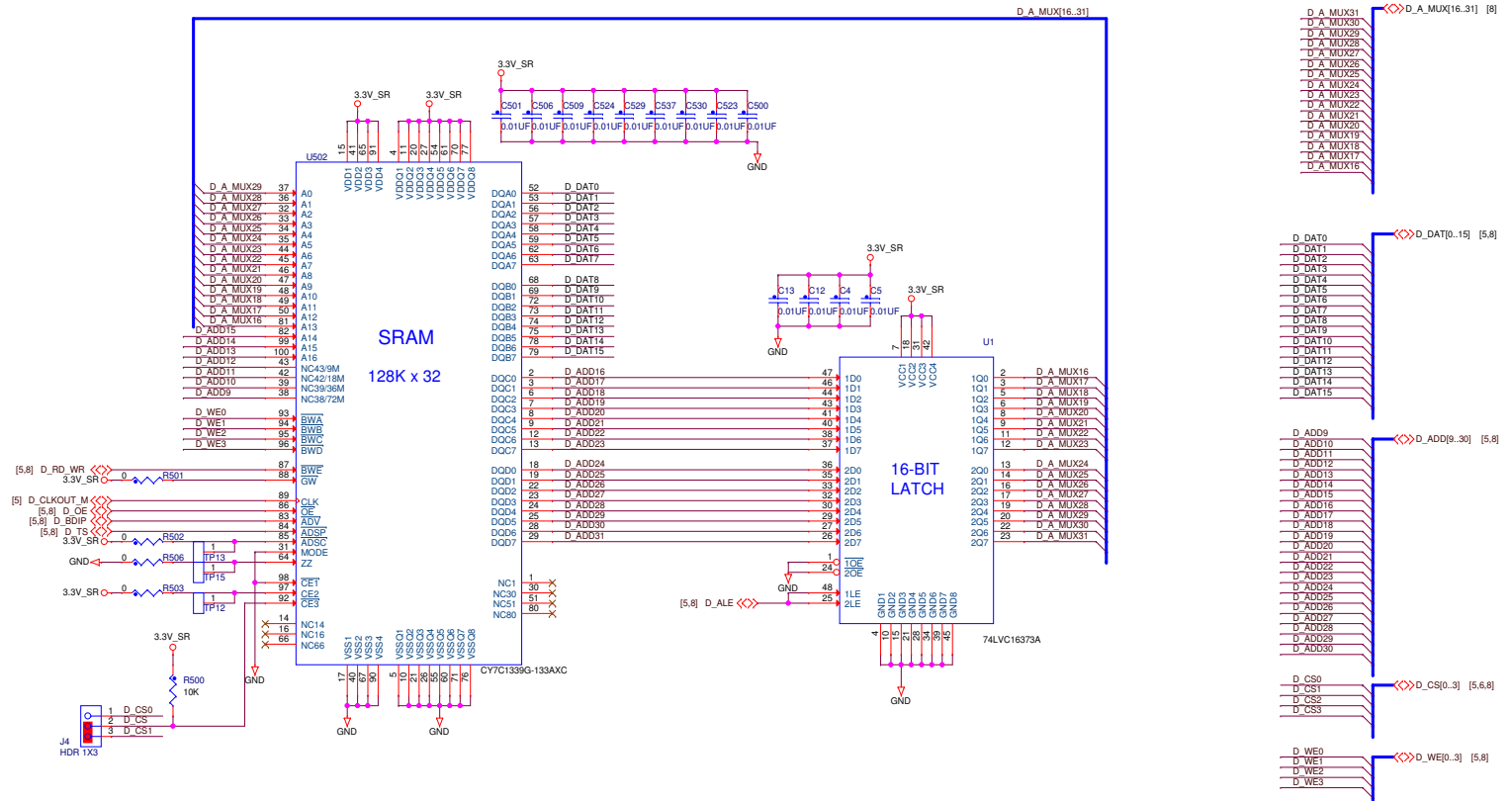
Page Title: CONTROLLER POWER

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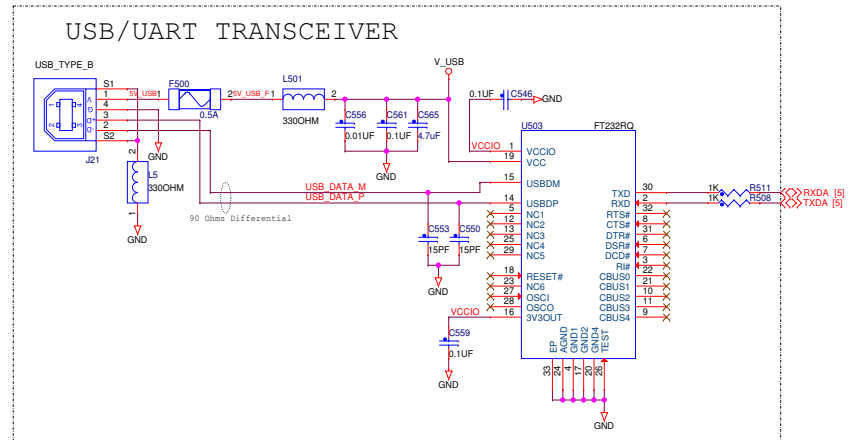
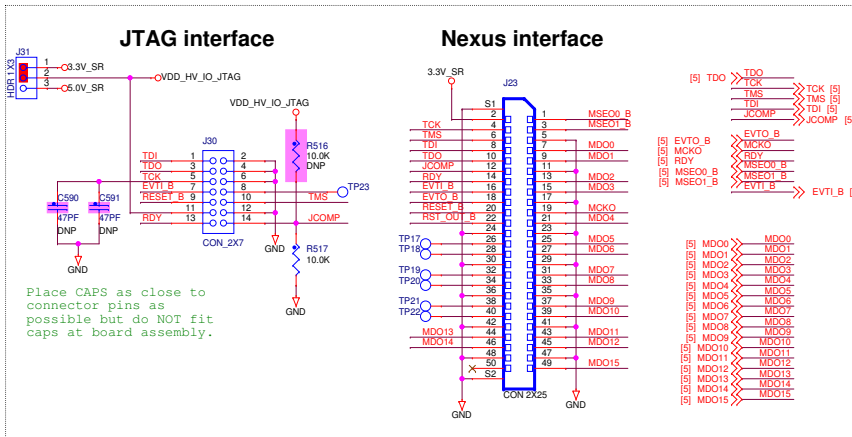
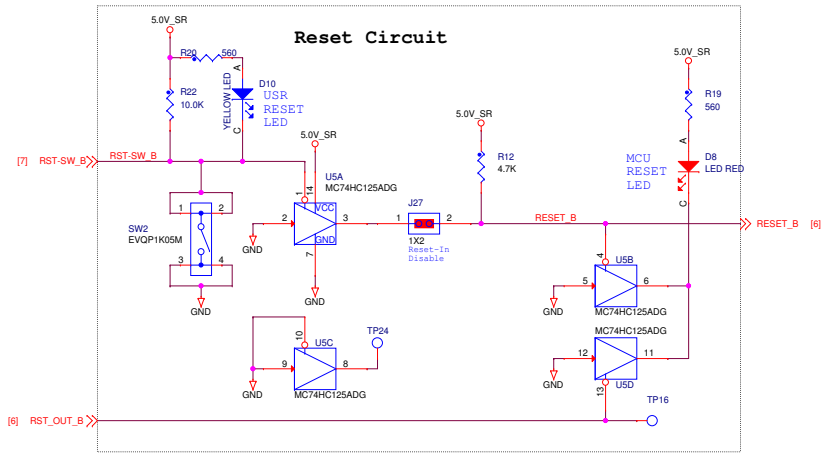
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ON BOARD MEMORY

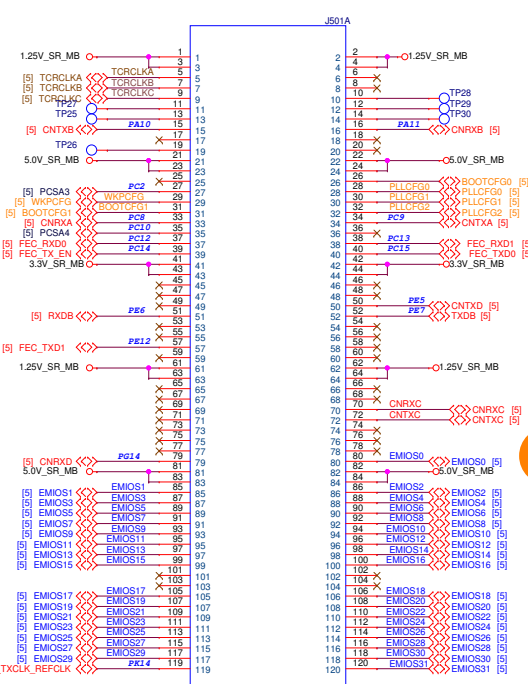


RESET, JTAG, NEXUS & UART



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DAUGHTER CARD TO MOTHERBOARD CONNECTOR



i SHD match J56 on the mother board

