LNK302/304-306 LinkSwitch-TN Family

Lowest Component Count, Energy Efficient Off-Line Switcher IC



Product Highlights

Cost Effective Linear/Cap Dropper Replacement

- Lowest cost and component count buck converter solution
- Fully integrated auto-restart for short-circuit and open loop fault protection saves external component costs
- LNK302 uses a simplified controller without auto-restart for very low system cost
- 66 kHz operation with accurate current limit allows low cost off-the-shelf 1 mH inductor for up to 120 mA output current
- Tight tolerances and negligible temperature variation
- High breakdown voltage of 700 V provides excellent input surge withstand
- Frequency jittering dramatically reduces EMI (~10 dB)
 minimizes EMI filter cost
- High thermal shutdown temperature (+135 °C minimum)

Much Higher Performance over Discrete Buck and Passive Solutions

- Supports buck, buck-boost and flyback topologies
- System level thermal overload, output short-circuit and open control loop protection
- Excellent line and load regulation even with typical configuration
- High bandwidth provides fast turn-on with no overshoot
- Current limit operation rejects line ripple
- Universal input voltage range (85 VAC to 265 VAC)
- Built-in current limit and hysteretic thermal protection
- Higher efficiency than passive solutions
- Higher power factor than capacitor-fed solutions
- Entirely manufacturable in SMD

EcoSmart - Extremely Energy Efficient

- Consumes typically only 50/80 mW in self-powered buck topology at 115/230 VAC input with no load (opto feedback)
- Consumes typically only 7/12 mW in flyback topology with external bias at 115/230 VAC input with no load
- Meets California Energy Commission (CEC), Energy Star, and EU requirements

Applications

- Appliances and timers
- LED drivers and industrial controls

Description

LinkSwitch-TN is specifically designed to replace all linear and capacitor-fed (cap dropper) non-isolated power supplies in the

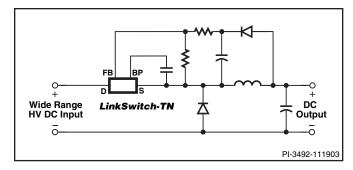


Figure 1. Typical Buck Converter Application (See Application Examples Section for Other Circuit Configurations).

OUTPUT CURRENT TABLE ¹								
PRODUCT⁴	230 VA	C ±15%	85-265 VAC					
PRODUCT	MDCM ²	CCM ³	M³ MDCM² CCI					
LNK302P [63 { A	80 { A	63 { A	80 { A				
LNK304P [120 { A	170 { A	120 { A	170 { A				
LNK305P [175 { A	280 { A	175 { A	280 { A				
LNK306P [¦ G	225 { A	360 { A	225 { A	360 { A				

Table 1. Notes: 1. Typical output current in a non-isolated buck converter. Output power capability depends on respective output voltage. See Key Applications Considerations Section for complete description of assumptions, including fully discontinuous conduction mode (DCM) operation. 2. Mostly discontinuous conduction mode. 3. Continuous conduction mode. 4. Packages: P: DIP-8B, G: SMD-8B. For lead-free package options, see Part Ordering Information.

under 360 mA output current range at equal system cost while offering much higher performance and energy efficiency.

LinkSwitch-TN devices integrate a 700 V power MOSFET, oscillator, simple On/Off control scheme, a high voltage switched current source, frequency jittering, cycle-by-cycle current limit and thermal shutdown circuitry onto a monolithic IC. The start-up and operating power are derived directly from the voltage on the DRAIN pin, eliminating the need for a bias supply and associated circuitry in buck or flyback converters. The fully integrated auto-restart circuit in the LNK304-306 safely limits output power during fault conditions such as short-circuit or open loop, reducing component count and system-level load protection cost. A local supply provided by the IC allows use of a non-safety graded optocoupler acting as a level shifter to further enhance line and load regulation performance in buck and buck-boost converters, if required.

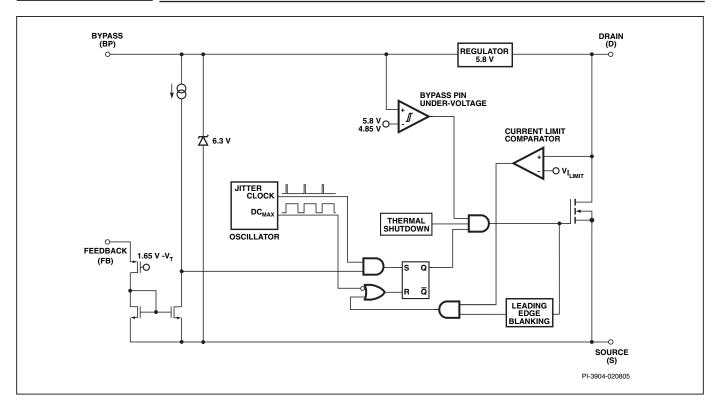


Figure 2a. Functional Block Diagram (LNK302).

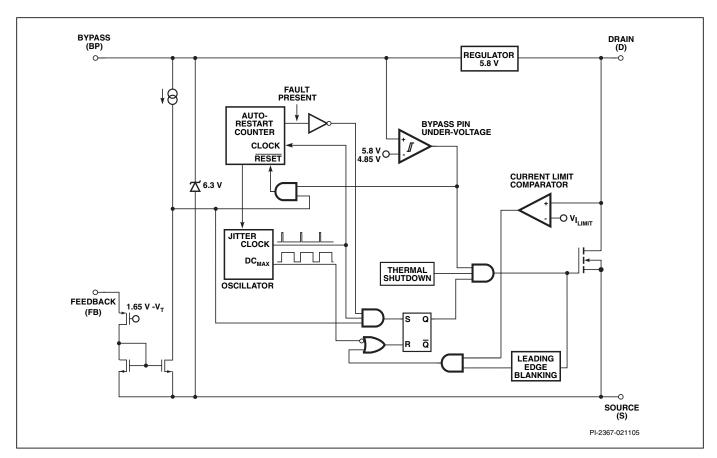


Figure 2b. Functional Block Diagram (LNK304-306).

Pin Functional Description

DRAIN (D) Pin:

Power MOSFET drain connection. Provides internal operating current for both start-up and steady-state operation.

BYPASS (BP) Pin:

Connection point for a $0.1\,\mu F$ external bypass capacitor for the internally generated $5.8\,V$ supply.

FEEDBACK (FB) Pin:

During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is terminated when a current greater than 49 μ A is delivered into this pin.

SOURCE (S) Pin:

This pin is the power MOSFET source connection. It is also the ground reference for the BYPASS and FEEDBACK pins.

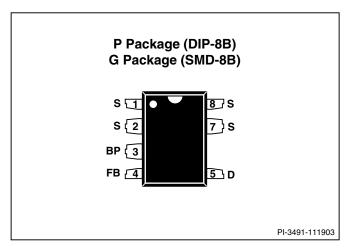


Figure 3. Pin Configuration.

LinkSwitch-TN Functional Description

LinkSwitch-TN combines a high voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM (pulse width modulator) controllers, LinkSwitch-TN uses a simple ON/OFF control to regulate the output voltage. The LinkSwitch-TN controller consists of an oscillator, feedback (sense and logic) circuit, 5.8 V regulator, BYPASS pin undervoltage circuit, over-temperature protection, frequency jittering, current limit circuit, leading edge blanking and a 700 V power MOSFET. The LinkSwitch-TN incorporates additional circuitry for auto-restart.

Oscillator

The typical oscillator frequency is internally set to an average of 66 kHz. Two signals are generated from the oscillator: the maximum duty cycle signal ($\mathrm{DC}_{\mathrm{MAX}}$) and the clock signal that indicates the beginning of each cycle.

The *LinkSwitch-TN* oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 4 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 4 illustrates the frequency jitter of the *LinkSwitch-TN*.

Feedback Input Circuit

The feedback input circuit at the FB pin consists of a low impedance source follower output set at 1.65 V. When the current delivered into this pin exceeds $49\,\mu\text{A}$, a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the FB pin voltage or current during the remainder of the cycle are ignored.

5.8 V Regulator and 6.3 V Shunt Voltage Clamp

The 5.8 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.8 V by drawing a current from the voltage on the DRAIN, whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node for the LinkSwitch-TN. When the MOSFET is on, the LinkSwitch-TN runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows the LinkSwitch-TN to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 0.1 μF is sufficient for both high frequency decoupling and energy storage.

In addition, there is a 6.3 V shunt regulator clamping the BYPASS pin at 6.3 V when current is provided to the BYPASS pin through an external resistor. This facilitates powering of *LinkSwitch-TN* externally through a bias winding to decrease the no-load consumption to about 50 mW.

BYPASS Pin Under-Voltage

The BYPASS pin under-voltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below 4.85 V. Once the BYPASS pin voltage drops below 4.85 V, it must rise back to 5.8 V to enable (turn-on) the power MOSFET.

Over-Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is set at 142 °C typical with a 75 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point it is re-enabled.

Current Limit

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the



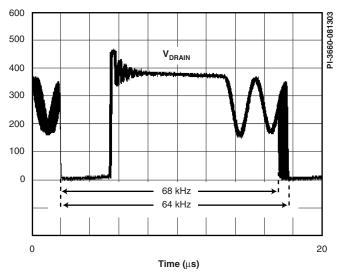


Figure 4. Frequency Jitter.

power MOSFET is turned off for the remainder of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the switching pulse.

Auto-Restart (LNK304-306 only)

In the event of a fault condition such as output overload, output short, or an open loop condition, *LinkSwitch-TN* enters into autorestart operation. An internal counter clocked by the oscillator gets reset every time the FB pin is pulled high. If the FB pin is not pulled high for 50 ms, the power MOSFET switching is disabled for 800 ms. The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed.

Applications Example

A 1.44 W Universal Input Buck Converter

The circuit shown in Figure 5 is a typical implementation of a

12 V, 120 mA non-isolated power supply used in appliance control such as rice cookers, dishwashers or other white goods. This circuit may also be applicable to other applications such as night-lights, LED drivers, electricity meters, and residential heating controllers, where a non-isolated supply is acceptable.

The input stage comprises fusible resistor RF1, diodes D3 and D4, capacitors C4 and C5, and inductor L2. Resistor RF1 is a flame proof, fusible, wire wound resistor. It accomplishes several functions: a) Inrush current limitation to safe levels for rectifiers D3 and D4; b) Differential mode noise attenuation; c) Input fuse should any other component fail short-circuit (component fails safely open-circuit without emitting smoke, fire or incandescent material).

The power processing stage is formed by the *LinkSwitch-TN*, freewheeling diode D1, output choke L1, and the output capacitor C2. The LNK304 was selected such that the power supply operates in the mostly discontinuous-mode (MDCM). Diode D1 is an ultra-fast diode with a reverse recovery time (t_{rr}) of approximately 75 ns, acceptable for MDCM operation. For continuous conduction mode (CCM) designs, a diode with a t_{rr} of \leq 35 ns is recommended. Inductor L1 is a standard off-the-shelf inductor with appropriate RMS current rating (and acceptable temperature rise). Capacitor C2 is the output filter capacitor; its primary function is to limit the output voltage ripple. The output voltage ripple is a stronger function of the ESR of the output capacitor than the value of the capacitor itself.

To a first order, the forward voltage drops of D1 and D2 are identical. Therefore, the voltage across C3 tracks the output voltage. The voltage developed across C3 is sensed and regulated via the resistor divider R1 and R3 connected to U1's FB pin. The values of R1 and R3 are selected such that, at the desired output voltage, the voltage at the FB pin is 1.65 V.

Regulation is maintained by skipping switching cycles. As the output voltage rises, the current into the FB pin will rise. If this exceeds I_{FB} then subsequent cycles will be skipped until the current reduces below I_{FB} . Thus, as the output load is reduced, more cycles will be skipped and if the load increases, fewer

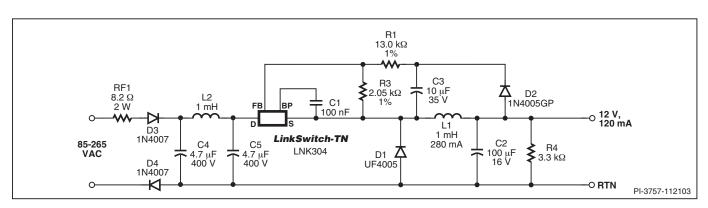


Figure 5. Universal Input, 12 V, 120 mA Constant Voltage Power Supply Using LinkSwitch-TN.

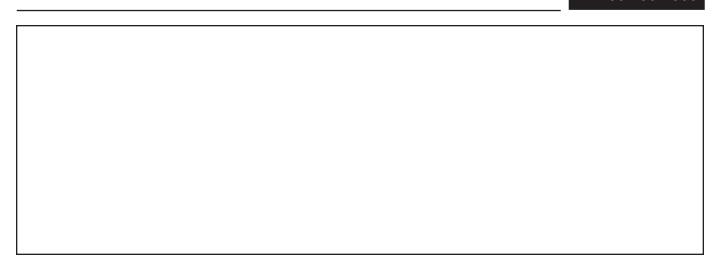


Figure 6. Recommended Printed Circuit Layout for LinkSwitch-TN in a Buck Converter Configuration.

cycles are skipped. To provide overload protection if no cycles are skipped during a 50 ms period, LinkSwitch-TN will enter auto-restart (LNK304-306), limiting the average output power to approximately 6% of the maximum overload power. Due to tracking errors between the output voltage and the voltage across C3 at light load or no load, a small pre-load may be required (R4). For the design in Figure 5, if regulation to zero load is required, then this value should be reduced to $2.4 \, \mathrm{k}\Omega$.

Key Application Considerations LinkSwitch-TN Design Considerations

Output Current Table

Data sheet maximum output current table (Table 1) represents the maximum practical continuous output current for both mostly discontinuous conduction mode (MDCM) and continuous conduction mode (CCM) of operation that can be delivered from a given *LinkSwitch-TN* device under the following assumed conditions:

- 1) Buck converter topology.
- The minimum DC input voltage is ≥70 V. The value of input capacitance should be large enough to meet this criterion.
- 3) For CCM operation a KRP* of 0.4.
- 4) Output voltage of 12 VDC.
- 5) Efficiency of 75%.
- 6) A catch/freewheeling diode with t_{rr} ≤75 ns is used for MDCM operation and for CCM operation, a diode with t_{rr} ≤35 ns is used.
- 7) The part is board mounted with SOURCE pins soldered to a sufficient area of copper to keep the SOURCE pin temperature at or below 100 °C.
- *KRP is the ratio of ripple to peak inductor current.

LinkSwitch-TN Selection and Selection Between MDCM and CCM Operation

Select the LinkSwitch-TN device, freewheeling diode and output inductor that gives the lowest overall cost. In general, MDCM provides the lowest cost and highest efficiency converter. CCM designs require a larger inductor and ultra-fast ($t_{rr} \le 35$ ns) freewheeling diode in all cases. It is lower cost to use a larger LinkSwitch-TN in MDCM than a smaller LinkSwitch-TN in CCM because of the additional external component costs of a CCM design. However, if the highest output current is required, CCM should be employed following the guidelines below.

Topology Options

LinkSwitch-TN can be used in all common topologies, with or without an optocoupler and reference to improve output voltage tolerance and regulation. Table 2 provide a summary of these configurations. For more information see the Application Note – LinkSwitch-TN Design Guide.

Component Selection

Referring to Figure 5, the following considerations may be helpful in selecting components for a *LinkSwitch-TN* design.

Freewheeling Diode D1

Diode D1 should be an ultra-fast type. For MDCM, reverse recovery time $t_{rr} \le 75$ ns should be used at a temperature of 70 °C or below. Slower diodes are not acceptable, as continuous mode operation will always occur during startup, causing high leading edge current spikes, terminating the switching cycle prematurely, prereat ere uttut pr

ere



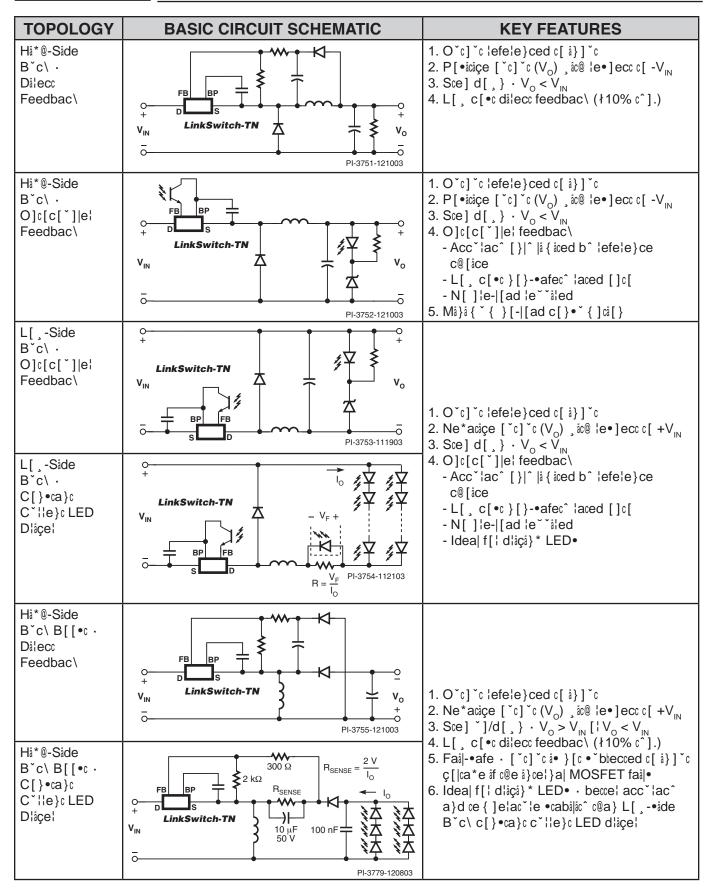


Table 2. Common Circuit Configurations Using LinkSwitch-TN. (continued on next page)

TOPOLOGY	BASIC CIRCUIT SCHEMATIC	KEY FEATURES
L[,-Side B`c\B[[•c· O]:[c[`] el Feedbac\		1. O c c lefele ced c c i lefele ced c c i lefele ced c c i lefele ced c c lefele ced c c lefele ced c c c c c c c c c c c c c c c c c

Table 2 (cont). Common Circuit Configurations Using LinkSwitch-TN.

leading edge current spikes, terminating the switching cycle prematurely and preventing full power delivery.

Fast and slow diodes should never be used as the large reverse recovery currents can cause excessive power dissipation in the diode and/or exceed the maximum drain current specification of *LinkSwitch-TN*.

Feedback Diode D2

Diode D2 can be a low-cost slow diode such as the 1N400X series, however it should be specified as a glass passivated type to guarantee a specified reverse recovery time. To a first order, the forward drops of D1 and D2 should match.

Inductor L1

Choose any standar	rd off-the-she	lf inductor	that meet	ts the							
design requirements.	. A "drum" or "	dog bone" "	'I" core ind	luctor							
is recommended wi	ith a single fe	rrite elemen	nt due to	to its							
low cost and very le	ow audible no	oi 🗆	M	off- tha	m						
-	o m	of of		0		m		aurM	2	eve	m
Inn 1r	mM						r				

isrrent □ r dorr wp M

lon □ e M



thauoose I

be included for better EMI performance and higher line surge withstand capability.

Quick Design Checklist

As with any power supply design, all *LinkSwitch-TN* designs should be verified for proper functionality on the bench. The following minimum tests are recommended:

- 1) Adequate DC rail voltage check that the minimum DC input voltage does not fall below 70 VDC at maximum load, minimum input voltage.
- 2) Correct Diode Selection UF400x series diodes are recommended only for designs that operate in MDCM at an ambient of 70 °C or below. For designs operating in continuous conduction mode (CCM) and/or higher ambients, then a diode with a reverse recovery time of 35 ns or better, such as the BYV26C, is recommended.
- 3) Maximum drain current verify that the peak drain current is below the data sheet peak drain specification under

- worst-case conditions of highest line voltage, maximum overload (just prior to auto-restart) and highest ambient temperature.
- 4) Thermal check at maximum output power, minimum input voltage and maximum ambient temperature, verify that the *LinkSwitch-TN* SOURCE pin temperature is 100 °C or below. This figure ensures adequate margin due to variations in R_{DS(ON)} from part to part. A battery powered thermocouple meter is recommended to make measurements when the SOURCE pins are a switching node. Alternatively, the ambient temperature may be raised to indicate margin to thermal shutdown.

In a *LinkSwitch-TN* design using a buck or buck boost converter topology, the SOURCE pin is a switching node. Oscilloscope measurements should therefore be made with probe grounded to a DC voltage, such as primary return or DC input rail, and not to the SOURCE pins. The power supply input must always be supplied from an isolated source (e.g. via an isolation transformer).

	ABSOLUTE MAXI	MUM RATINGS(1,5)
DRAIN Voltage	0.3 V to 700 V	Notes:
Peak DRAIN Current (LNK302)	200 mA (375 mA) ⁽²⁾	1. All voltages reference
Peak DRAIN Current (LNK304)	400 mA (750 mA) ⁽²⁾	2. The higher peak DRA
Peak DRAIN Current (LNK305)	800 mA(1500 mA) ⁽²⁾	to SOURCE voltage of
Peak DRAIN Current (LNK306)	1400 mA(2600 mA) ⁽²⁾	3. Normally limited by i
FEEDBACK Voltage	0.3 V to 9 V	4. 1/16 in. from case for
FEEDBACK Current	100 mA	5. Maximum ratings spe
BYPASS Voltage	0.3 V to 9 V	without causing perm
Storage Temperature	65 °C to 150 °C	Exposure to Absolute
Operating Junction Temperature ⁽³⁾	40 °C to 150 °C	extended periods of ti
Lead Temperature ⁽⁴⁾	260 °C	

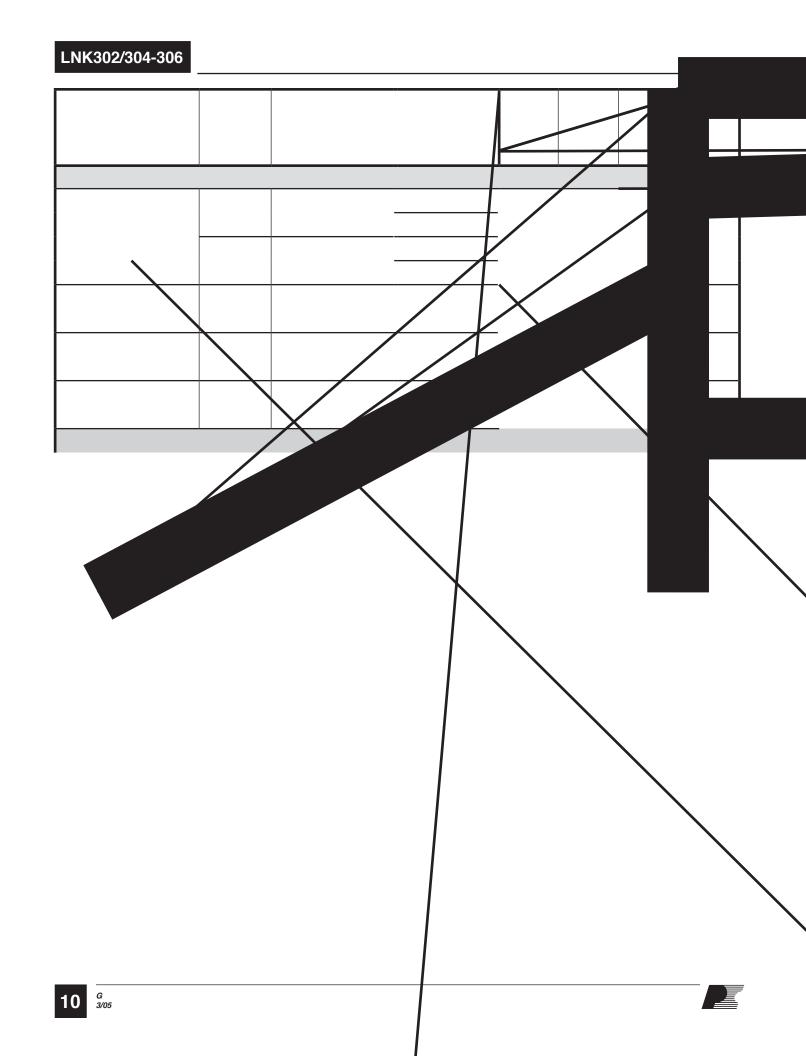
Notes:

- 1. All voltages referenced to SOURCE, $T_A = 25$ °C.
- 2. The higher peak DRAIN current is allowed if the DRAIN to SOURCE voltage does not exceed 400 V.
- 3. Normally limited by internal circuitry.
- 4. 1/16 in. from case for 5 seconds.
- 5. Maximum ratings specified may be applied, one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

THERMAL IMPEDANCE							
Thermal Impedance: P or G Package:	Notes:						
(θ_{IA}) 70 °C/W ⁽²⁾ ; 60 °C/W ⁽³⁾	1. Measured on pin 2 (SOURCE) close to plastic interface.						
$(\theta_{\rm IC})^{(1)}$	2. Soldered to 0.36 sq. in. (232 mm ²), 2 oz. (610 g/m ²) copper clad.						
	3. Soldered to 1 sq. in. (645 mm ²), 2 oz. (610 g/m ²) copper clad.						

Parameter	Symbol	Conditions SOURCE = 0 V; T _J = -40 c[125 »C See Fi* ie 7 (U} e•• Oc@el ; i•e S]eci ed)		Min	Тур	Max	Units	
CONTROL FUNCT	TIONS							
O c] c	f _{osc}	T ₁ = 25 »C	Açe¦a*e	62	66	70	\H:	
F¦eĭĕ}c^	'osc	1 _J = 25 %	Pea\-Pea\ Jiccel		4		\□.	
Ma¢ã { ັ { Dັĉ C^c e	DC _{MAX}	S2 O]e}		66	69	72	%	
FEEDBACK På} Tˇ¦}[ff T@¦e•@[d Cˇ¦le}c	I _{FB}	T _J = 25 »C		30	49	68	μΑ	
FEEDBACK Pa} V[ca*e ac T* }[ff T@ e•@[d	V _{FB}			1.54	1.65	1.76	V	
	I _{s1}	V _{FB} ⁻ 2 V (MOSFET N[c S¸ācc@ā}*) See N[ce A			160	220	μΑ	
DRAIN Sˇ]] ^ Cˇ¦le}:		FEEDBACK O]e} (MOSFET	LNK302/304		200	260		
o nego	I _{S2}		(MOSFET	LNK305		220	280	μΑ
		S¸icc@i}*) See N[ce∙ A, B			250	310		





Parameter	Symbol	Conditions SOURCE = 0 V; T _J = -40 c[125 »C See Fi* * le 7 (U} e•• Oc@el ; i•e S]eci led)		Min	Тур	Max	Units
CIRCUIT PROTEC	CIRCUIT PROTECTION (cont.)						
Leadã}* Ed*e B a}\ã}* Tã{e	C _{LEB}	T _J = 2 See N		170	215		}•
T@el{a S@`cd[,} Te{]elac`le	T _{SD}			135	142	150	°C
T@el{a S@~cd[,} H^•cele•i•	T _{SHD}	See N	[ce G		75		°C
OUTPUT						•	
		LNK302	T _J = 25 °C		48	55.2	
		I _D = 13 { A	T _J = 100 °C		76	88.4	
		LNK304	T _J = 25 °C		24	27.6	
ON-Scace	R _{DS(ON)}	I _D = 25 { A	T _J = 100 °C		38	44.2	Ω
Re•ã•ca}ce	DS(ON)	LNK305 I _D = 35 { A LNK306	T _J = 25 °C		12	13.8	
			T _J = 100 °C		19	22.1	
			T _J = 25 °C		7	8.1	
		I _D = 45 { A	T _J = 100 °C		11	12.9	
OFF-Scace Dlai}		$V_{BP} = 6.2 \text{ V}, V_{FB}^{-2}$	V, LNK302/304			50	
Lea\a*e Cˇ¦¦e}c	DSS	$V_{DS} = 560 \text{ V},$ $T_{J} = 25 ^{\circ}\text{C}$	LNK305 LNK306			70 90	μΑ
B¦ea\d[¸} V[a*e	BV _{DSS}	$V_{BP} = 6.2 \text{ V}, V_{FB}^{-2} \text{ V},$ $T_{J} = 25 \text{ °C}$		700			V
Rã•e Tã { e	C _R	Mea∙ ˇled i} a	T^]aca B*c\		50		}•
Fa Tã { e	C _F	C[}çekek	\]] acaca[}		50		}•
DRAIN Sˇ]] ^ V[a*e				50			V
Oˇc]ˇc E}ab e De aˆ	C _{EN}	See Fi	*			10	μ•
Oˇc]ˇc Dà•ab e Secˇ] Tã { e	C _{DST}				0.5		μ•
A c[-Re•calc		T _J = 25 °C	LNK302	N	[cA]] ãcab	e	(-
ON-Tã { e	C _{AR}	See N[ce H	LNK304-306		50		{•
A c[-Re•calc	5.0		LNK302	N	[cA]] ãcab	e	2,
D c C C e	DC _{AR}		LNK304-306		6		%



NOTES:

- A. $T[ca|c^*]= c[e^*]= c[e^*]$
- B Si}ce c@e ['c]'c MOSFET i•• , icc@i}*, ic i• dif'c'|c c[i•[|ace c@e , icc@i}* c'lle}c fl[{ c@e ']]|^ c'lle}c ac c@e DRAIN. A} a|cel}aciçe i• c[{ ea•'le c@e BYPASS]i} c'lle}c ac 6 V.
- C. See T^|ica| Pelf[|{a}ce C@alacceliocico oecci[|Fi**le 14 f[|BYPASS]i} ocalco |color="1" acef[|{.
- D. T@i• c'ile}c i• [}|^ i}ce}ded c[']]|^ a} []ci[{a| []c[c[']|e| c[}}ecced bec_ee} c@e BYPASS a}d FEEDBACK]i}• a}d }[ca}^ (cae' e¢cei}a| cilc'ici^.
- E. F[|c||e]c||a||ac ac [c@e||da/dc||e||, lefe||c||Fa*||e 13.
- F. T@i•]ala { ecel i• * ala}ceed b de•i*}.
- G. T@i•]ala { ecel i• deliçed fl [{ c@alacceli:aci[}.
- H. A c[-le•calc [] ci { e @a• c@e •a { e ce {]elac le c@alacceli•cic• a• c@e [•ci||ac[l (i)çel•e|^]![][!ci[]a|c[fle e]c^).

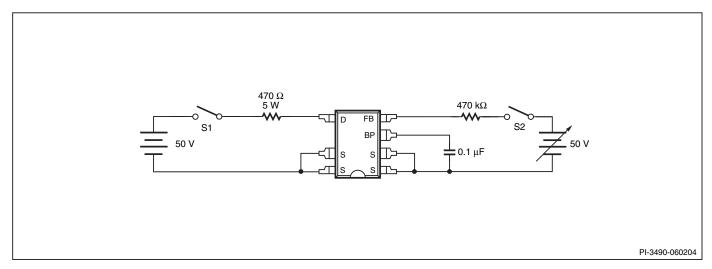


Figure 7. LinkSwitch-TN General Test Circuit.

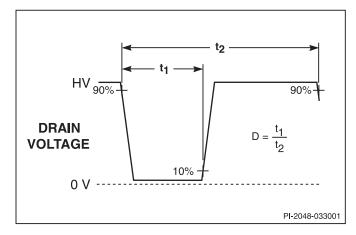


Figure 8. LinkSwitch-TN Duty Cycle Measurement.

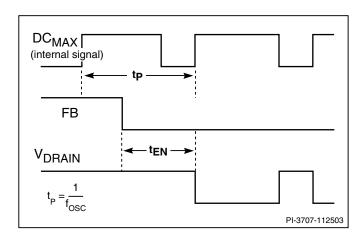


Figure 9. LinkSwitch-TN Output Enable Timing.



Typical Performance Characteristics

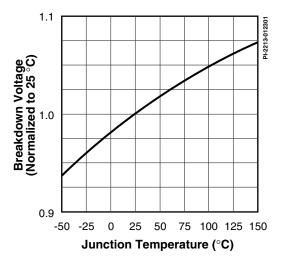


Figure 10. Breakdown vs. Temperature.

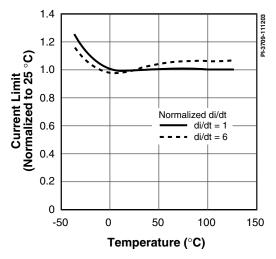


Figure 12. Current Limit vs. Temperature at Normalized di/dt.

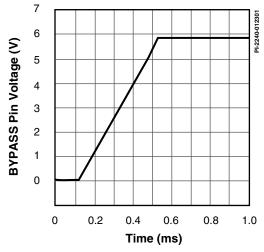


Figure 14. BYPASS Pin Start-up Waveform.

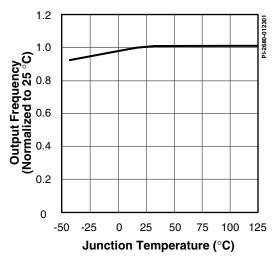


Figure 11. Frequency vs. Temperature.

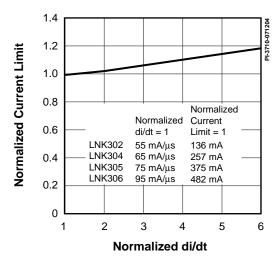


Figure 13. Current Limit vs. di/dt.

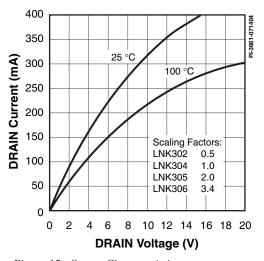


Figure 15. Output Characteristics.



Typical Performance Characteristics (cont.)

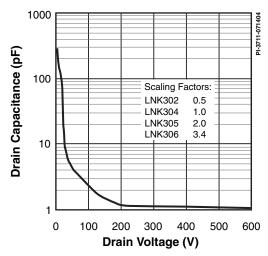
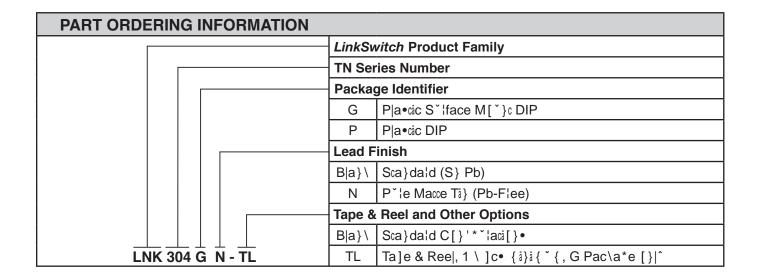
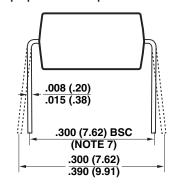


Figure 16. C_{oss} vs. Drain Voltage.



DIP-8B ⊕DS .004 (.10) .137 (3.48) MINIMUM -E-.240 (6.10) .260 (6.60) Pin 1 .367 (9.32) -D-.387 (9.83) .057 (1.45) .068 (1.73) (NOTE 6) .125 (3.18) .015 (.38) .145 (3.68) MINIMUM -T-**SEATING PLANE** .120 (3.05) .140 (3.56) .100 (2.54) BSC .048 (1.22) .053 (1.35) .014 (.36) .022 (.56) (TED (.010 (.25) ()

- 1. Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.
- 2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
- Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
- 4. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 6 is omitted.
- 5. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
- Lead width measured at package body.
- 7. Lead spacing measured with the leads constrained to be perpendicular to plane T.



P08B

PI-2551-121504

SMD-8B ⊕ DS .004 (.10) .137 (3.48) 1. Controlling dimensions are MINIMUM inches. Millimeter sizes are -Eshown in parentheses. 2. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .372 (9.45) .240 (6.10) .006 (.15) on any side. .420 3. Pin locations start with Pin 1, .388 (9.86) .260 (6.60) ⊕ ES .010 (.25) and continue counter-clock-.060 .046 .046 .060 wise to Pin 8 when viewed from the top. Pin 6 is omitted. 4. Minimum metal to metal .080 spacing at the package body Pin 1 Pin 1 for the omitted lead location is .137 inch (3.48 mm). 086 -.100 (2.54) (BSC) 5. Lead width measured at .186 package body. .286 D and E are referenced .367 (9.32) -D-Solder Pad Dimensions datums on the package .387 (9.83) body. .057 (1.45) .068 (1.73) .125 (3.18) (NOTE 5) .145 (3.68) <u>_.004 (.10)</u> .032 (.81) .048 (1.22) 0°- 8° .009 (.23) .036 (0.91) .037 (.94) .053 (1.35) .004 (.10) .044 (1.12) .012 (.30) **G08B** PI-2546-121504

LNK302/304-306

Revision	Notes	Date
С	1) Released Final Data Sheet.	3/03
D	1) Corrected Minimum On Time.	1/04
Е	1) Added LNK302.	8/04
F	1) Added lead-free ordering information.	12/04
G	 Minor error corrections. Renamed Feedback Pin Voltage parameter to Feedback Pin Voltage at Turnoff Threshold and removed condition. 	3/05

For the latest updates, visit our website: www.powerint.com

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.powerint.com/ip.htm.

LIFE SUPPORT POLICY

POWER INTEGRATIONS' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF POWER INTEGRATIONS. As used herein:

- 1. A Life support device or system is one which, (i) is intended for surgical implant into the body, or (ii) supports or sustains life, and (iii) whose failure to perform, when properly used in accordance with instructions for use, can be reasonably expected to result in significant injury or death to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

The PI logo, **TOPSwitch**, **TinySwitch**, **LinkSwitch**, **DPA-Switch**, **EcoSmart**, **PI Expert** and **PI FACTS** are trademarks of Power Integrations, Inc. Other trademarks are property of their respective companies. ©Copyright 2005, Power Integrations, Inc.

Power Integrations Worldwide Sales Support Locations

Mil:

