

PCADADIO

Multi-Function Digital/Analogue I/O Board

Technical Manual

Product Information

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FREE Windows NT4.0 Drivers

Visit the 'PC(ISA)bus Boards' page on the Arcom Website,
www.arcom.co.uk/ntdrv10_AR.exe to download.

Preface

Packing List

This product is shipped as follows:

- Board
- User Manual
- Utility Disk

If any of the above appear to be missing, please telephone Arcom 01223 411200. Throughout this document “/” denotes that a signal is active low. All address and data values are in hexadecimal.

Utility Disk

This product is shipped with a utility disk which contains:

- PCbus Library
- Source code (written in 'C') and sample executable files to aid in calibrating the board
- Also supplied is a programming resistor which is required for the 0-5V range of the ADC

Handling (ESD/Packaging)

This board contains CMOS devices which could be damaged in the event of static electricity being discharged through them. At all times please observe anti-static precautions when handling the board and always unpack and install the board in an anti-static working area.

Please ensure that should a board need to be returned to Arcom, it is adequately packed and if a battery is fitted, that it is isolated.

Revision History

Manual	PCB	Comments	
Issue A	V1 Iss 2	960731	First released in this format. ECO2684.
Issue B	V1 Iss 2	980115	

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Introduction

The PCADADIO is a low-cost, multi-purpose I/O board for PC-compatibles. It has eight differential (PCADADIOCD) or 16 single-ended (PCADADIOCS) multiplexed analogue inputs, two analogue outputs, 16 digital I/Os and three counter-timer channels. The operation of each of these functions is controlled using the PC XT bus and link options.

Features

- CE compliant design
- 8 differential or 16 single-ended, multiplexed 12-bit ADC channels
- 10kHz channel-to-channel acquisition rate (buffered input)
- 100kHz repeat rate (back-to-back single channel conversion)
- 10 μ s typical conversion rate
- $\pm 5V$, $\pm 10V$, 0-5V, 0-10V selectable input ranges
- Two 12-bit (± 1 -bit accuracy) analogue output channels
- $\pm 5V$, 0-5V, 0-10V channel-by-channel selectable output ranges
- 10 μ s settling time to 12-bit accuracy
- Intel 8254-compatible 3-channel counter-timer
- 1 ADC timer, 1 interrupt timer, 1 general-purpose timer
- 1MHz master operating frequency
- 16 TTL nibble-configurable digital I/O lines
- Input: 1K pulled to 0.8V resistor input low
- Output: 24mA at 0-45V, sources from 1K resistor at +5V
- Selectable power-up states
- Compact I/O addressing scheme (4 bytes)
- 8-bit ISA bus interface
- Board access user LEDs: ID byte = 2Dh
- I/O connector conforms to Arcom Signal Conditioning System (SCS)
- Operating temperature range, 0°C to +55°C
- Power required: $\pm 5V$ @ 330mA ($\pm 5\%$) typical, +12V @ 200mA ($\pm 10\%$) typical
- MTBF: 172,706 hours (using generic figures from MIL-HDBK-217F at ground benign)
- Dimensions: 289 x 120 x 25mm
- Weight: 266g

Getting Started

- Switch off PC
- Install board in supplied configuration
- Switch on PC and observe the LEDs while it powers up. You may see the red LED flash once. This simply means that the BIOS start-up program in your PC is checking through I/O space to see if any boards are there. It is nothing to worry about. On the other hand, if your PC fails to boot or the red LED flashes continuously, you will need to change the PCADADIO base address.
- Run EXAMP-01 (utility disk)
- The Green User LED should flash

The utility disk supplied with PCADADIO contains example software to help get you started. PCADADIO.EXE will run with the standard link settings and displays the ADC inputs, scrolls an active bit along the digital I/O and allows setting of the DACs. Decrementing CTC data and incrementing interrupt counts are also shown. In order for these to run, it is necessary to add a link to LK2A between pins 9 and 10 on PL3.

Operation

Reading from or Writing to the Board

Control of the PCADADIO is achieved by writing to a pointer register and then accessing a data register to read or write the required function. The pointer register need only be written with a new value if a different data register is next to be accessed. ADC and DAC data is handled by a dedicated pair of registers. The board occupies only four bytes of PCbus I/O space. Each time the board is accessed, the Red LED will flash momentarily.

Base Address Selection

The switches set the address of the lowest of the four bytes of the board control registers (the base address) and the three remaining bytes occupy sequential addresses above this location in PCbus I/O space. Therefore, the base address must be set-up on four byte boundaries, i.e SW3 should be set to 0, 4, 8 or C. The address switches should be set to read from left to right (SW1 to SW3) to correspond with the hex switches. For example for address 180hex (the deepest PCbus I/O base address) SW1 is set to 1, SW2 to 8 and SW3 to 0.

The I/O Pointer Scheme

To access a function on the PCADADIO, you must set-up the 'pointer register' to point to it. This is achieved by writing a pointer value byte to the I/O base address. Once a particular device is pointed at, it can be accessed by writing/reading the relevant access register. The pointer value need not be re-written for every access to the same access register.

All control and diagnostic functions, including ADC control, are accessed using the byte (8 bit) access register located at Base +1. The ADC and DAC data are accessed using the low and high access registers located at Base + 2 and Base + 3. This feature can be used to optimise data acquisition using software word access, since this results in two contiguous bus cycles (Base + 2 followed by Base + 3). There is no need to write a new pointer value before access is made to read ADC data.

I/O Address	Function	Read/Write
Base	Pointer Register	Write Only
Base + 1	Diagnostic and Control Access Byte	Read/Write
Base + 2	DAC and ADC Low Access Byte	Read/Write
Base + 3	DAC and ADC High Access Byte	Read/Write

Pointer Values and Register Function

Pointer Value (hex)	Read/Write	Function Register Name	Data Bit	Function
00	Read Base +1	Status Flag - ADC	0	ADC ready 0 = conversion completed since last read of ADC Data - High Byte
00	Read Base +1	Status Flag - CTC	1	Counter-Timer ready 0 = OUTB has transitioned low-high since Clear CTC Ready last accessed
00	Write Base +1	ADC Start Conversion		Writing any data starts conversion
00	Read Base +2	ADC Data - Low Byte	4-7	AD0-3 ADC data from last conversion
00	Read Base +3	ADC Data - High Byte	0-7	AD4-11 ADC data from last conversion
01	Write Base +1	Multiplexer Channel Select	0-3	Multiplexer channel address 0-15 for PCADADIOCS 0-7 for PCADADIOCD
02	Write Base +2	DACA Register	4-7	DA0-3 DACA low data
02	Write Base +3	DACB Register	0-7	DA4-11 DACA high data
03	Write Base +2	DACB Register	4-7	DB0-3 DACB low data
03	Write Base +3	CTC Counter A	0-7	DB4-11 DACB high data
04	R/W Base +1	CTC Counter B	0-7	See Intel 8254 data sheet
05	R/W Base +1	CTC Counter C	0-7	See Intel 8254 data sheet
06	R/W Base +1	CTC Counter Control	0-7	See Intel 8254 data sheet
07	R/W Base +1	Word Clear CTC Ready	0-7	See Intel 8254 data sheet
08	Write Base +1	Digital I/O Configuration		Writing any data sets Status Flag - CTC to 1 and clears CTC interrupt (if enabled)
09	Write Base +1		0-3	NBEN0-3 0 = nibble configured as output 1 = nibble configured as input
0A	R/W Base +1	Digital I/O Group 2	0-7	PL7 Digital I/O Dig0-7
0B	R/W Base +1	Digital I/O Group 3	0-7	PL7 Digital I/O Dig8-15
0C-7F		Not Used		
80	Write Base +1	User LED	0	Green User LED Control 0 = LED off 1 = LED on
81	Read Base +1	Board ID	0-7	Reads as 2Dh

Installing Multiple PCADADIOS

This is just like installing a single PCADADIO, except that each must be installed at a different address. The base address must be set in 4-byte boundaries.

ADC Sequence

The PCADADIO is shipped calibrated for the $\pm 5V$ range, and requires re-calibration if used on other ranges. The ADC may be triggered from three alternative sources, selected by a jumper:

- Software trigger, from writing the register
- Hardware trigger, from an external TTL input, approximately 1-2 μ sec low pulse
- Periodic timer, programmed from the on-board CTC

In the second two cases an interrupt should be used to signal that a new value is ready.

With a software trigger all timing can be done from the program using this sequence:

- Select channel register and write channel value
- Delay for input settling (about 50 μ sec)
- Select software trigger register and write to trigger (value not defined)
- Delay for ADC conversion (about 20 μ sec)
- Select status register and read to check that new value is ready
- Read ADC data registers

DAC Sequence

Before writing a 12-bit DAC value to the data registers at Base + 2 and Base + 3, the DAC channel must be selected. Write value 02 to the Pointer register for DAC A and value 03 for DAC B.

Digital I/Os

Before connecting any inputs to the digital I/Os, check that the links (LK12-15) which control the reset state of the individual nibbles are correctly configured as inputs, otherwise damage may occur, either to the PCADADIO or external equipment.

The direction of individual nibbles can be switched by writing to the digital configuration register. Access to the individual outputs and inputs is via the digital I/O group 2 and 3 registers. If a nibble is configured as an input a write to the output register will have no effect on the input, unless the state of the configuration register is changed to an output. In this case the last value written to the nibble will be transferred to the output. It is therefore important to ensure that the correct value is written to the output register before switching from an input to an output.

Counter/Timers

The PCADADIO contains three 16-bit counter/timers in an Intel 8254-compatible Counter Timer Chip (CTC).

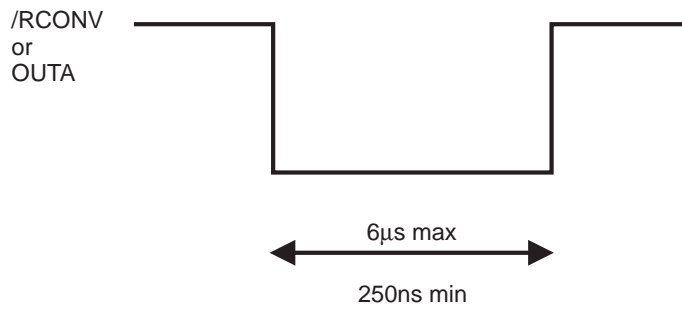
To offer maximum flexibility, the PCADADIO has a 10-way connector (PL3) with the facility to link the inputs to external and internal clock sources including the outputs of other counter/timer channels. Additionally, channel A can be used to start ADC conversion and channel B to generate interrupts on IRQ2 or 3 when links LK10 and LK4 are selected respectively.

Counter A should always be programmed in mode 2 which ensures that OUTA is only active for a single clock cycle (i.e. 1 μ s when connected to the 1MHz clock). When OUTC is connected to CLKA, the time between rising edges on OUTC must not exceed 6 μ s or be less than 250ns.

ADC Triggering

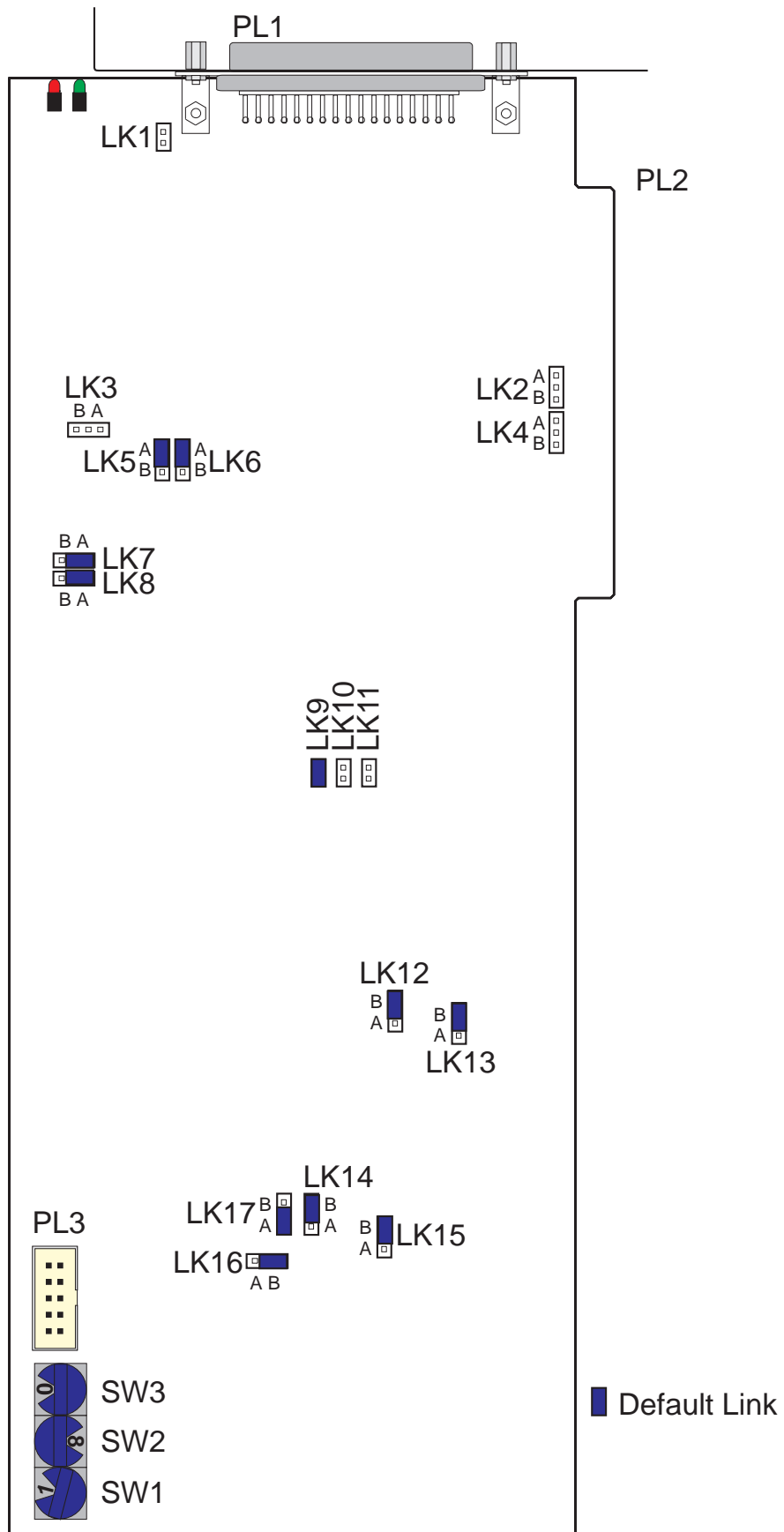
The counter/timer trigger uses channel A and the hardware strobe the /RCONV pin on PL1. Conversion is started from these sources when OUTA signal or /RCONV are low. To ensure that the ADC does not perform multiple conversions it must be ensured that hardware and CTC trigger pulses are greater than 250nS, but less than 6 μ S.

Maximum data throughput can be obtained by triggering a new conversion before data from the last conversion is read and processed. To ensure that the ADC data registers contain data from the last conversion they must be read within 6 μ S of triggering a new conversion.



Links & Options

Default Link Position Diagram



Board Functions

Throughout this section '+' indicates a factory set default link.

Link LK1: Pseudo Differential Ground Connection

Fit	PCADADIOCS. Fit only if inputs are isolated from 0VA
Omit	PCADADIOCD, differential inputs

Link LK2: ADC Interrupt Selection

Link LK2 selects an interrupt source for the ADC which generates an interrupt signal after conversion is complete and indicates ADC data is ready for reading:

LK2A	Sends an interrupt at conversion complete to IRQ2
LK2B	Sends an interrupt at conversion complete to IRQ3

ADC conversion complete is also indicated by the status flag register, whether or not a link is fitted.

Link LK3: Differential/Single-Ended Input Selection

A	PCADADIOCD
B	PCADADIOCS

Link LK4: Counter/Timer Interrupt Selection

Link LK4 selects an interrupt source for the counter/timer channel B. An interrupt will be generated whenever the OUTB pin of the counter/timer (8254) strobes low to high.

LK4A	Sends an interrupt to the counter/timer OUTB to IRQ2
LK4B	Sends an interrupt from the counter/timer OUTB to IRQ3

CTC OUTB strobing high is also indicated by the status flag register, whether or not a link is fitted.

Links LK5, LK6: DAC Output Range

Links LK5 and LK6 selects the output range for DAC1 and DAC0 respectively. The range settings are as below:

+ LKA	-5V to +5V
LKB	0V to 5V
None	0V to 10V

Links LK7, LK8 and R15: ADC Input Ranges

Links LK7, LK8 and R15 select the input range to the ADC. The range settings are as below:

LK7	LK8	R15	Range
+A	+A	+Omit	-5V to +5V
A	B	Omit	0V to +10V
B	A	Omit	-10V to +10V
A	B	49.9K	0V to +5V

Under no circumstances should both links be fitted to position B

Link LK9, LK10 and LK11: ADC Trigger Sources

These three links enable the three different ADC trigger sources. Each trigger source is enabled when a link is fitted.

Please note that only one link should be fitted for reliable operation

+LK9 fitted	Enable software triggering
LK10 fitted	Enable hardware triggering
LK11 fitted	Enable counter/timer channel A triggering

Links LK12, LK13, LK14, LK15: Digital I/O Reset State

These links select the state of the digital I/O lines at reset in nibble (4 bit) groups.

Reset high should be used when the digital I/Os are to be used as inputs, otherwise the lines will be driven low as outputs which may cause damage. The link associated with each nibble is shown below.

- LK15** **Digital I/O lines DIG0-3**
- LK14** **Digital I/O lines DIG4-7**
- LK13** **Digital I/O lines DIG8-11**
- LK12** **Digital I/O lines DIG12-15**

LKxxxA fitted	Sets the nibble low
+ LKxxxB fitted	Sets the nibble high

Link LK16: Counter/Timer Channel A Clock Source

Link LK16 selects the clock source for counter/timer channel A

LK16A	Clocked by the output of counter/timer channel C output
+ LK16B	1MHz Clock

Link LK17: Digital I/O Reset Test Link

Used for automated board testing of the digital I/Os, to ensure they reset into the correct states and should be left in position A.

User Configuration Record Sheet

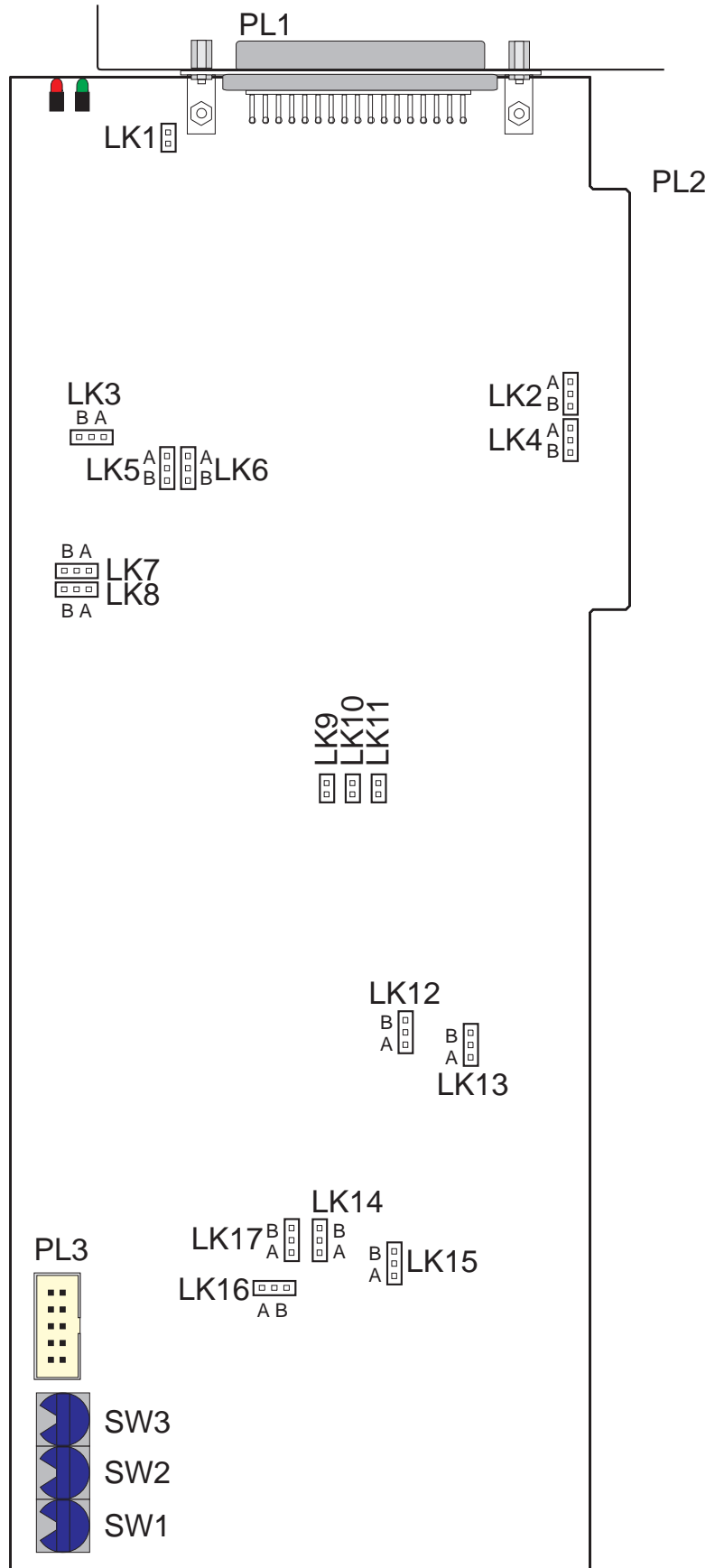
This sheet may be duplicated

Links

Pseudo Differential Ground	LK1	
ADC Interrupt	LK2	
Differential Single-Ended Input	LK1	
Counter/Timer Interrupt	LK2	
DAC Output	LK5 LK6	
ADC Input	LK7 LK8	
ADC Trigger Sources	LK9 LK10 LK11	
Digital I/O Reset State	LK12 LK13 LK14 LK15	
Counter/Timer Channel A Clock	LK16	
Digital I/O Reset Test	LK17	

Base Address Switches

SW1	
SW2	
SW3	



Calibration

Calibrating the ADC

In order to calibrate the ADC it is necessary to have a precision digital voltmeter (DVM) with at least 5 digit resolution and a high stability low noise DC signal source. To monitor adjustments, it is necessary to continually read and display the ADC data. There is a program on the Utility Disk which provides this facility, PCADADIO.EXE.

Two trim adjusters, VR7 and VR1, are provided for trimming the zero offset and gain respectively. These trims are for fine-adjusting the standard ranges.

Unipolar Calibration

Set the necessary links for unipolar mode and the required voltage range. Run the screen display software.

Zero Offset Adjust

- 1) Set the input voltage to exactly zero.
- 2) Adjust VR7 to give 000 to 001 hex.

Full Scale Gain Adjust

- 1) Set the input voltage to full scale positive minus 1 LSB:-
+4.9985 for the 5V range.
+9.9975 for the 10V range.
- 2) Adjust VR1 to give FFE to FFF.

Bipolar Calibration

Set the necessary links for bipolar mode and the required voltage range. Run the screen display software.

Bipolar Offset Adjust

- 1) Set the input voltage to full scale negative plus 1 LSB:-
-4.9975 for the 5V range.
-9.995 for the 10V range.
- 2) Adjust VR7 to give 000 to 001 hex.

Full Scale Gain Adjust

- 1) Set the input voltage to full scale positive minus 1 LSB:-
+4.9975 for the 5V range.
+9.995 for the 10V range.
- 2) Adjust VR1 to give FFE to FFF.

Calibrating the DACs

In order to calibrate the DACs it is necessary to have a DVM with at least 5 digit resolution. On the demonstration disk there is a facility useful for calibrating the DACs. This allows each DAC to be set to the required value for calibration.

A single trim (VR2) is provided to trim the reference voltage used by the DACs. Additionally, two trimmers are provided for adjusting the zero offset and gain of each DAC channel. VR5 and VR3 trim the zero offset and gain of DAC channel A and VR6 and VR4 DAC channel B respectively. These trims are for fine adjust only within standard ranges.

Set the necessary links for the required mode and voltage ranges. Run the screen display software. Put the DVM on the AGND and VREF test point and adjust VR2 to read 5.02V.

Note: If the gain adjust trimmers (VR3 & 4) have insufficient range, adjust VR2 to read 5.01V and repeat the calibration procedure.

Unipolar Calibration

For DAC channel A.

Zero Offset Adjust

- 1) Set DAC A output to 000 hex.
- 2) Measure between the DAC A output on PL1 and analogue ground and adjust VR5 to give 0.000V.

Full Scale Gain Adjust

- 1) Set the DAC A output to 800 hex.
- 2) Measure between the DAC A output on PL1 and adjust VR3 to exactly give half scale output (2.500V for the 0V to 5V output and 5.000V for the 0V to 10V output).
- 3) Set DAC A to FFF hex and check full scale is:-
 - 9.9975 for 0V to 10V range.
 - 4.9985 for the 0V to 5V range.
- 4) Adjust VR3 if necessary.

Repeat for DAC channel B replacing VR5 with VR6, and VR3 with VR4.

Bipolar Calibration

For DAC channel A.

Zero Offset Adjust

- 1) Set DAC A output to 000 hex.
- 2) Measure between the DAC A output on PL1 and analogue ground and adjust VR5 to give full scale negative i.e. -5.000V.

Full Scale Gain Adjust

- 1) Set the DAC A output to 800 hex.
- 2) Measure between the DAC A output on PL1 and adjust VR3 to give half scale output 0.000V.
- 3) Set DAC A to FFF hex and check full scale is 4.9975V.

Repeat for DAC channel B replacing VR5 and VR6, and VR3 and VR4.

Utility Disk

A Utility Disk containing example software is supplied with the PCADADIO to help you get started.

README.TXT File

The file README.TXT is the first one you should look at. It contains up-to-date information on the whole disk.

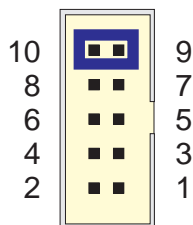
PCADADIO.INI

The demonstration program uses a file (PCADADIO.INI) which allows the user to initialise the base address, ADC and DAC ranges, etc. This file may be edited to reflect changes in the board settings.

PCADADIO.EXE

This program displays the ADC inputs, scrolls an active bit along the digital I/O and allows setting of the DACs. These will all run with the standard link settings.

Decrementing CTC data and incrementing interrupt counts are also shown. In order for these to run, it is necessary to add a link to LK2A between pins 9 and 10 on PL3 as shown.



Connectors

PL1. Front Panel 50-way D-type

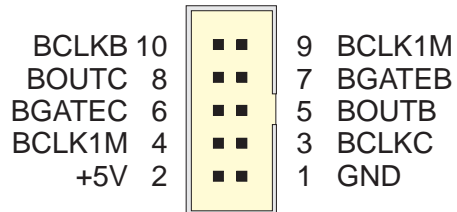
The PCADADIO has two user connectors PL1 and PL3. PL2 is the edge connector on the PCB used to connect to the PC bus.

PL1 is located on the board front panel and the pinout is compatible with the Arcom Signal Conditioning System (SCS). For this reason the pinout is listed both for the 50-way D-type and a 50-way ribbon cable. The pin locations for these connectors are shown below:

Ribbon Cable No.	D-50 Pin No.	Signal Title
1	1	0VA
2	34	PDIFF
3	18	Ch0+
4	2	Ch0-/CH8+
5	35	Ch1+
6	19	Ch1-/Ch9+
7	3	Ch2+
8	36	Ch2-/Ch10+
9	20	Ch3+
10	4	Ch3-/Ch11+
11	37	0VA
12	21	PDIFF
13	5	Ch4+
14	38	Ch4-/Ch12+
15	22	Ch5+
16	6	Ch5-/Ch13+
17	39	Ch6+
18	23	Ch6-/Ch14+
19	7	Ch7+
20	40	Ch7-/Ch15+
21	24	GND
22	8	PDIFF
23	41	Dig0
24	25	Dig1
25	9	Dig2
26	42	Dig3
27	26	Dig4
28	10	Dig5
29	43	Dig6
30	27	Dig7
31	11	GND
32	44	Not Used
33	28	Dig8
34	12	Dig9
35	45	Dig10
36	29	Dig11
37	13	Dig12
38	46	Dig13
39	30	Dig14
40	14	Dig15
41	47	0VA
42	31	Reserved
43	15	DAC0
44	48	DAC1
45	32	Not Used
46	16	Not Used
47	49	-12V
48	33	+12V
49	17	+5V
50	50	-5V

PL3. 10-way IDC Header

PL3 is used for connecting external signals to buffered versions of the CTC inputs and outputs for channels B and C. For maximum flexibility the connections have been arranged to allow clock inputs to be linked to the standard 1MHz clock or other channel outputs using jumper links. The pinout of the 10-way header and connections are shown below:



Installation for CE Compliance

To maintain compliance with the requirements of the EMC Directive (89/336/EEC), this product must be correctly installed. The PC in which the board is housed must be CE compliant as declared by the PC manufacturer. The external I/O cable should be the Arcom CAB50CE, or a fully screened cable to the same pattern.

1. Remove the cover of the PC observing any additional instructions of the PC manufacturer
2. Locate the board in a spare ISA slot and press gently but firmly into place
3. Ensure that the metal bracket attached to the board is fully seated
4. Fit the bracket clamping screw and firmly tighten this on the bracket

NOTE: Good contact of the bracket to chassis is essential

5. Fit the screened I/O cable to the 50-way board connector
6. Ensure that the jack screws for the cable connector are tightened (use a screw driver)
7. Replace the cover of the PC observing any additional instructions of the PC manufacturer

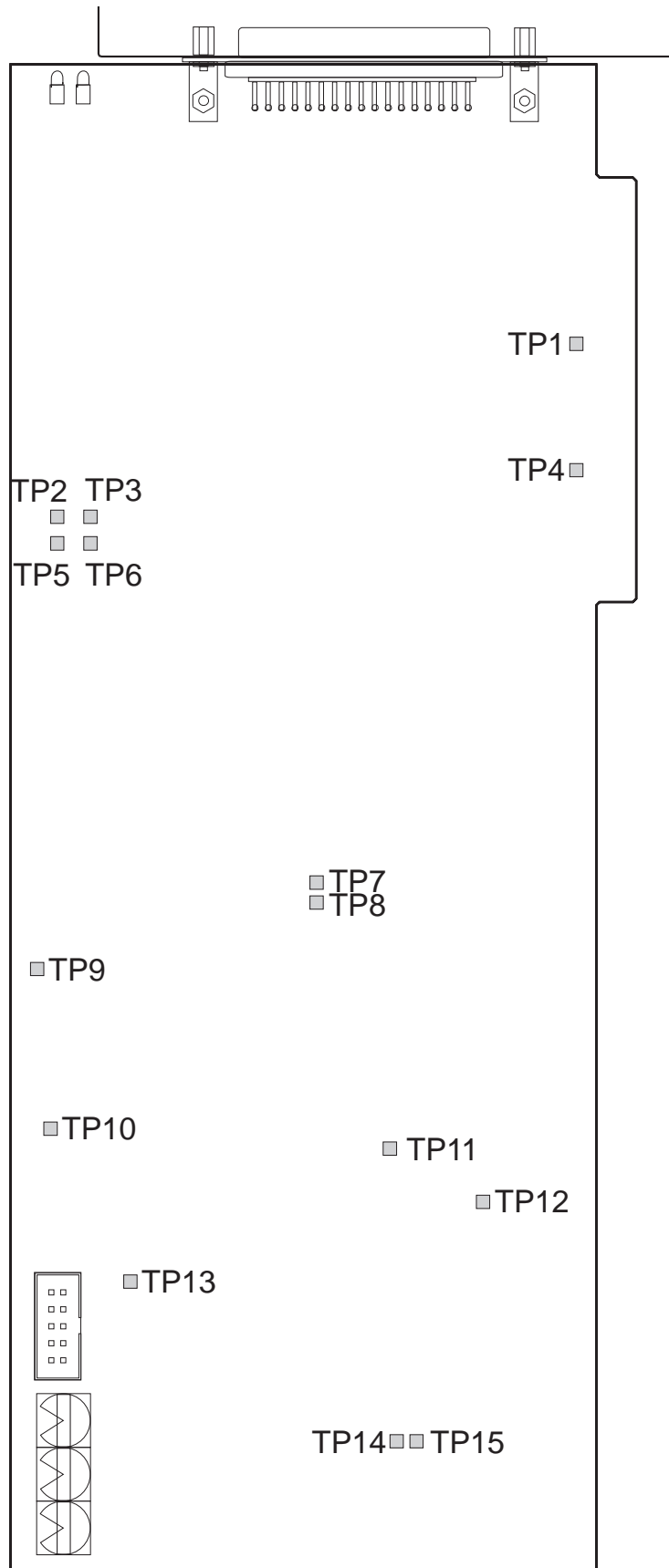
The following standards have been applied to this product:

BS EN50081-1: 1992	Generic Emissions Standard, Residential, Commercial, Light Industry
BS EN50082-1: 1992	Generic Immunity Standard, Residential, Commercial, Light Industry
BS EN55022 : 1995	ITE Emissions, Class B, Limits and Methods

Reference

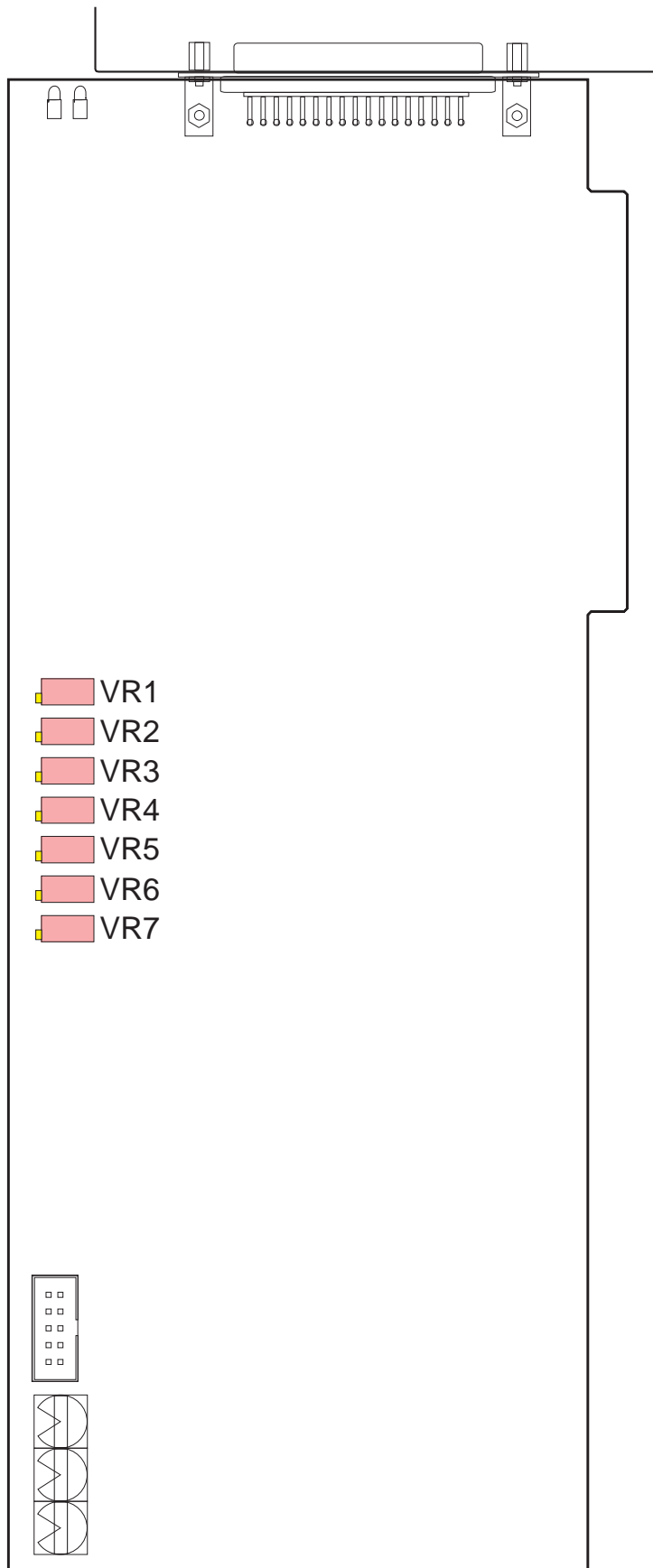
Test Point Locations

Test Point	Description
TP1	PCbus IRQ2
TP2	DAC Voltage Reference
TP3	+5V Analogue
TP4	PCbus IRQ3
TP5	Analogue + Supply (Approx. 15V)
TP6	Analogue - Supply (Approx. -15V)
TP7	ADC Chip Enable
TP8	ADC Status Line
TP9	Analogue Ground
TP10	Digital Ground
TP11	Buffered Reset Active Low
TP12	I/O Address Match
TP13	+5V Digital
TP14	Device Write Active Low
TP15	Device Read Active Low

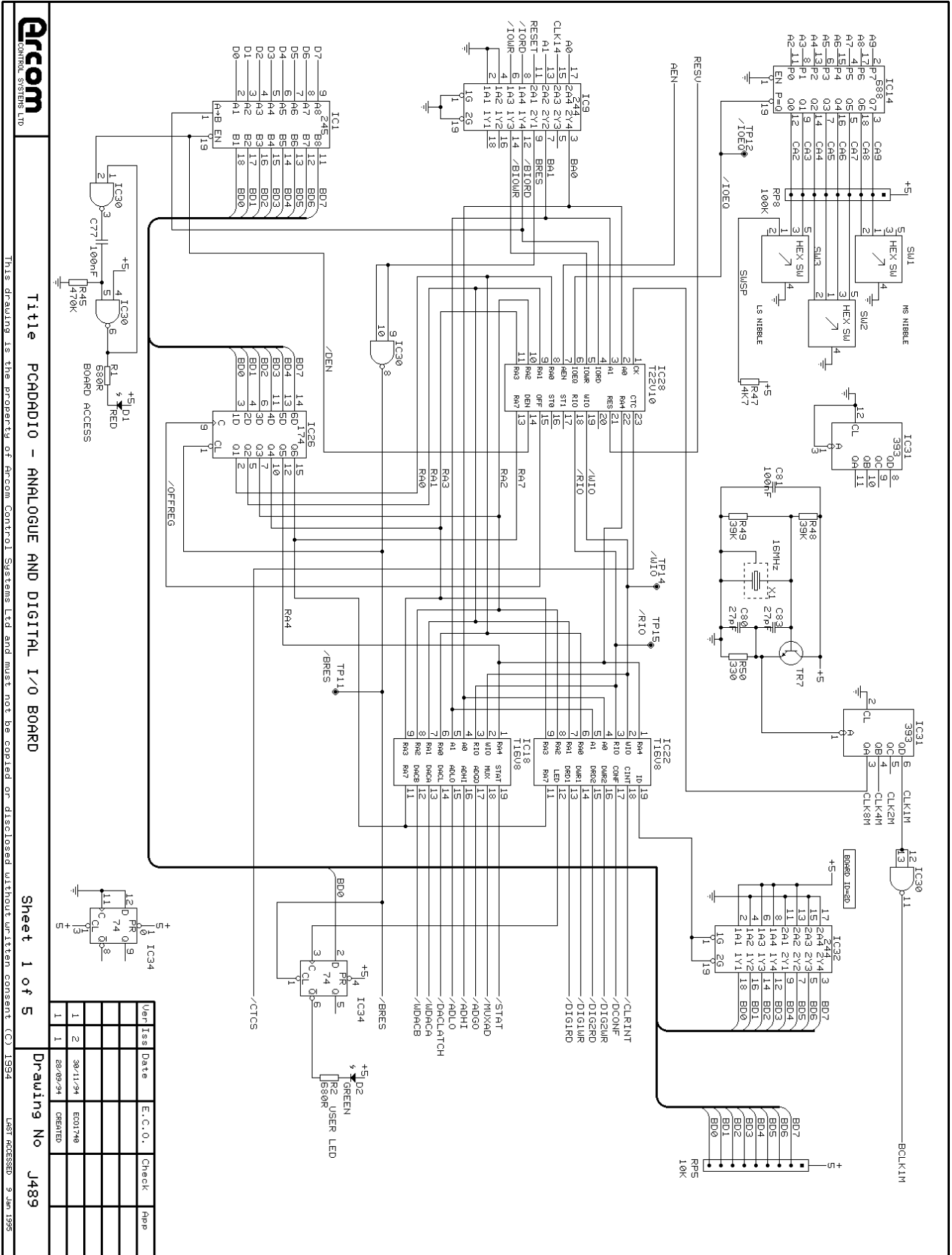


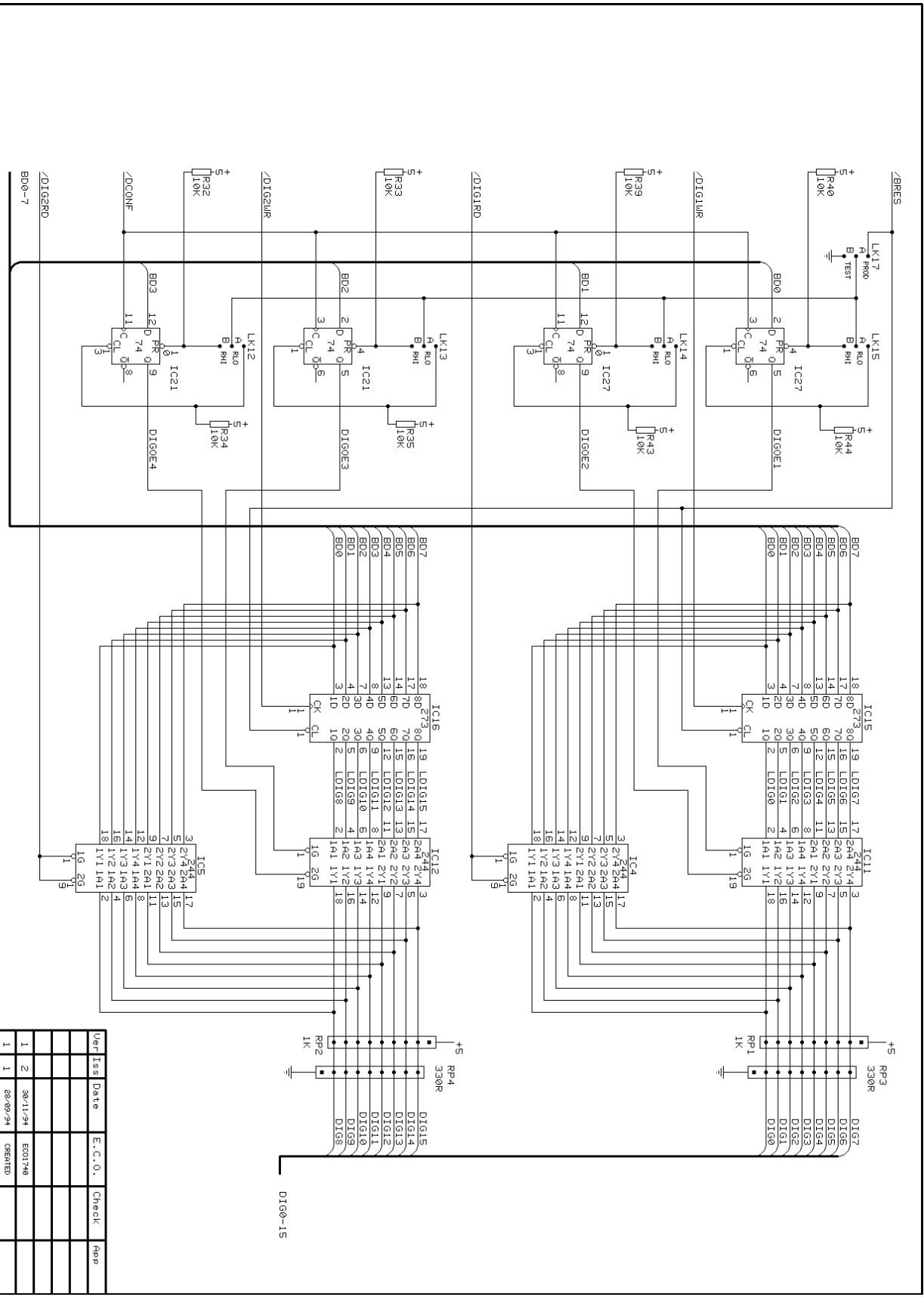
Trimmer Locations

Trimmer	Function
VR1	ADC Gain
VR2	DAC Reference Voltage
VR3	DAC Ch A Gain
VR4	DAC Ch B Gain
VR5	DAC Ch A Zero Offset
VR6	DAC Ch B Zero Offset
VR7	ADC Zero Offset



Circuit Diagrams





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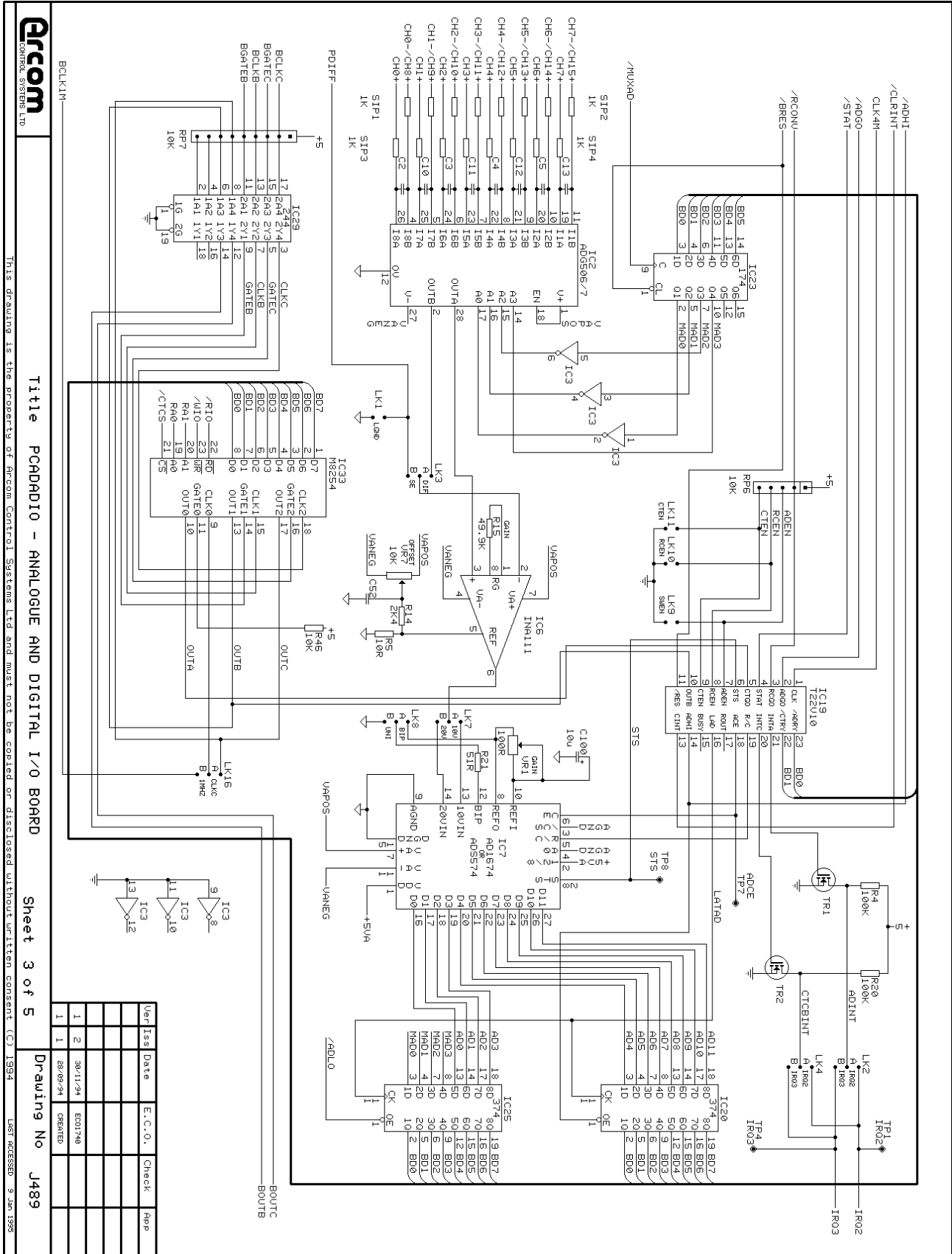
Sheet 2 of 5

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U87 PROCESSOR 9 Jun 1995

Ver	Iss	Date	E.C.O.	Check	App
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1	1	28/09/94	0801748		





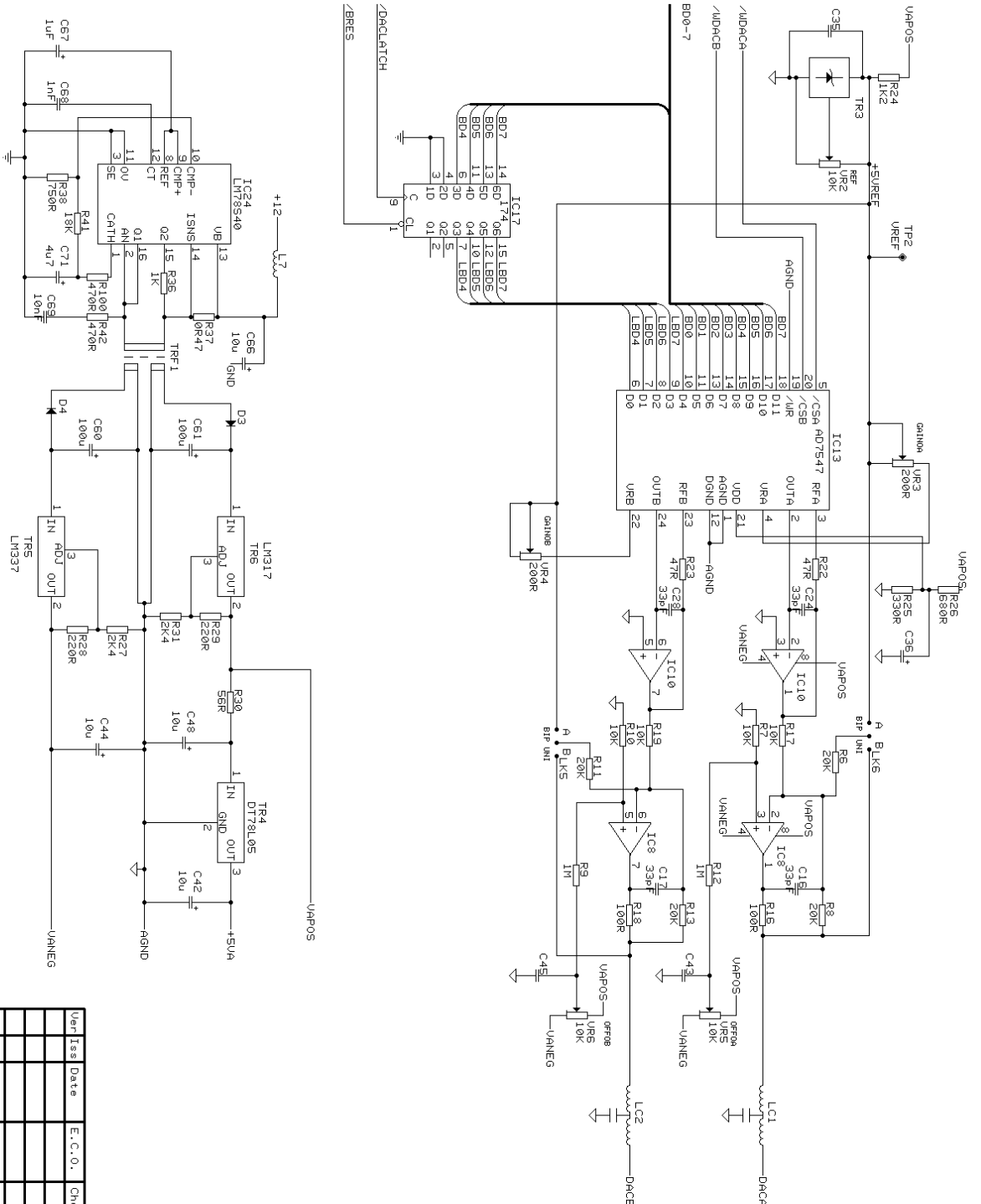
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1	1	30/11/94	ED01746		
1	1	28/09/94	CREATED		

