MOTOROLA

4-Bit Arithmetic Logic Unit

ELECTRICALLY TESTED PER:
MIL-M-35810/30801

Military 54LS181

The 54LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

- Provides 16 Arithmetic Operations Add, Subtract, Compare, Double, Plus Twelve Other Arithmetic Operations
- Provides All 16 Logic Operations of Two Variables Exclusive-OR, Compare, AND, NAND, OR, NOR, Plus Ten Other Logic Operations
- Full Lookahead For High-Speed Arithmetic Operation On Long Words
- Input Clamp Diodes

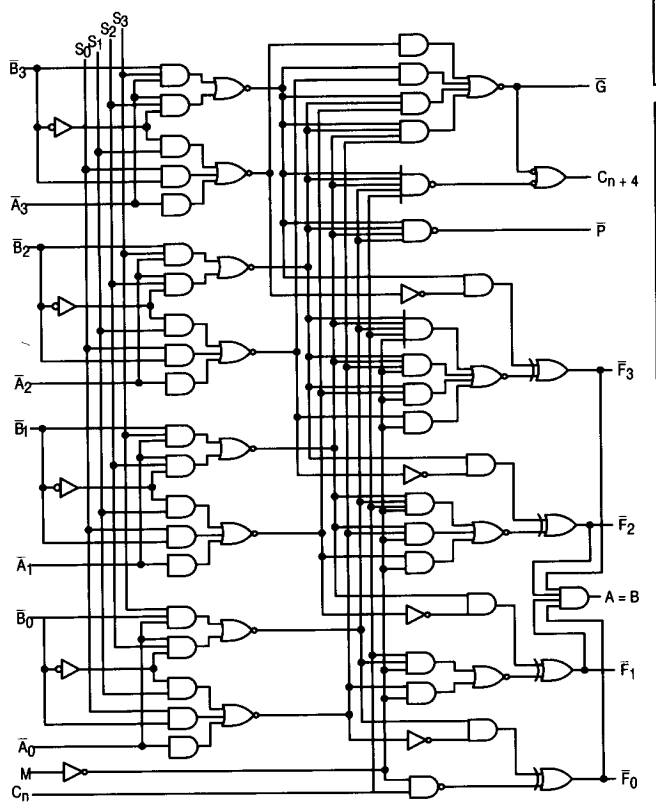
AVAILABLE AS:

1) JAN: JM38510/30107BXA
2) SMD: N/A
3) 883: 54LS175/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: J
CERFLAT: K

THE LETTER "M" APPEARS BEFORE THE / ON LCC

LOGIC DIAGRAM



PIN ASSIGNMENTS

FUNCT.	DIL 623-05	FLATS 652-02	BURN-IN (COND. A)
$\overline{B}_0$	1	1	GND
$\overline{A}_0$	2	2	GND
S_3	3	3	GND
S_2	4	4	GND
S_1	5	5	GND
S_0	6	6	GND
C_n	7	7	GND
M	8	8	V_{CC}
$\overline{F}_0$	9	9	V_{CC}
$\overline{F}_1$	10	10	V_{CC}
$\overline{F}_2$	11	11	V_{CC}
GND	12	12	GND
$\overline{F}_3$	13	13	V_{CC}
A = B	14	14	V_{CC}
$\overline{P}$	15	15	V_{CC}
C_{n+4}	16	16	V_{CC}
$\overline{G}$	17	17	V_{CC}
$\overline{B}_3$	18	18	GND
$\overline{A}_3$	19	19	GND
$\overline{B}_2$	20	20	GND
$\overline{A}_2$	21	21	GND
$\overline{B}_1$	22	22	GND
$\overline{A}_1$	23	23	GND
V_{CC}	24	24	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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FUNCTIONAL DESCRIPTION

The 'LS181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0-S_3) and the Mode control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-HIGH or active-LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} Output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the 'LS181 can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operations the 'LS181 is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four 'LS181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = 8 output is open collector and can be wired-AND with other A = 8 outputs to give a comparison for more than four bits. The A = B signal can be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus 8 minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow, thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active-LOW inputs producing active-LOW outputs or with active-HIGH inputs producing active-HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

Mode Select Inputs				Active-Low Operands & F_n Outputs		Active-High Operands & F_n Outputs	
				Logic (M = H)	Arithmetic** (M = L) (C_n = L)	Logic (M = H)	Arithmetic** (M = H) (C_n = H)
S_3	S_2	S_1	S_0				
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A+B}$	A$\overline{B}$ minus 1	$\overline{AB}$	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A $\oplus$ B	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	A$\overline{B}$	A$\overline{B}$ minus 1
H	L	L	L	$\overline{AB}$	A plus (A + B)	$\overline{A}$ + B	A plus AB
H	L	L	H	A $\oplus$ B	A plus 8	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	A$\overline{B}$ minus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

*Each bit is shifted to the next more significant position.

**Arithmetic operations expressed in 2s complement notation.

H = HIGH Voltage Level

L = LOW Voltage Level

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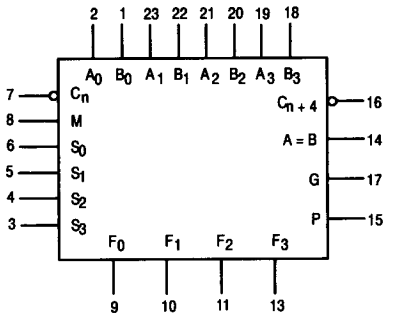
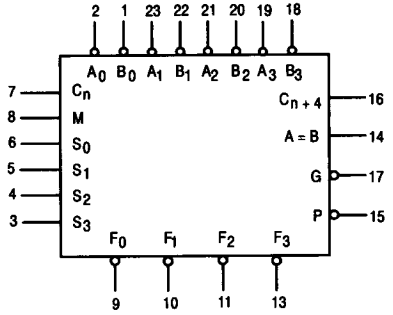
LOGIC SYMBOLS

Active-High Operands



Active-Low Operands



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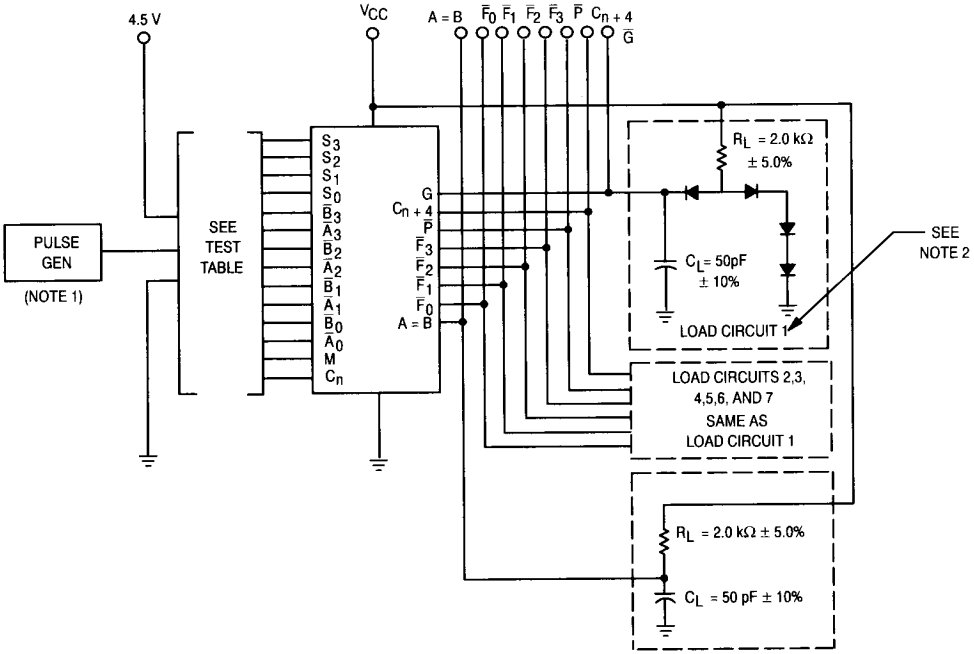
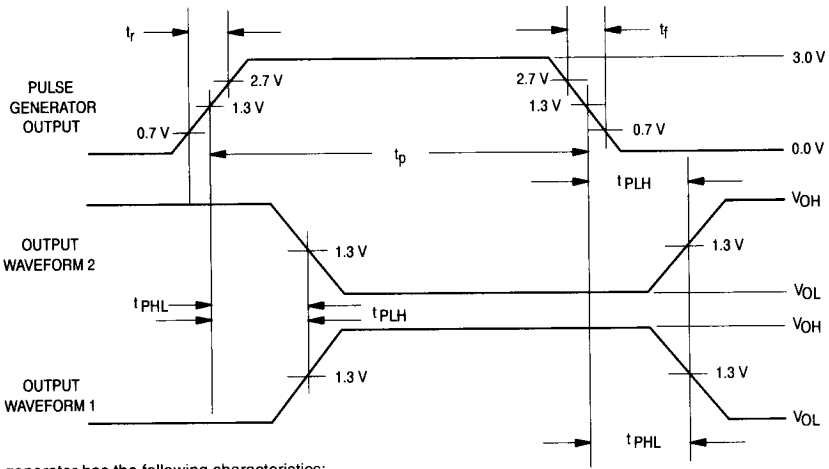
AC TEST CIRCUIT AND WAVEFORMS





NOTES:

1. The pulse generator has the following characteristics: PRR = 1.0 MHz ± 10%, $Z_{OUT} \approx 50\ \Omega$, Pulse width = 200 ns ± 10%, $t_r \leq 15$ ns, and $t_f \leq 6.0$ ns.
2. Load circuits on a given output are only required where the specific test in table indicates. Load circuits may otherwise be omitted.
3. $C_L = 50$ pF ± 10%, including scope probe and jig capacitance.
4. $R_L = 2.0\ k\Omega \pm 5.0\%$
5. All diodes are 1N3064, or equivalent.
6. The limits specified for $C_L = 15$ pF are guaranteed but not tested.
7. Terminal conditions (pins not designated may be high ≥ 2.0 V, or low ≤ 0.7 V, or open).

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 400 µA, V_{IH} = 2.0 V, V_{IL} = 0.8 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V.
I_{IH1}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, $V_{IH(M)}$ = 2.7 V, C_n = 5.5 V, other inputs are GND.
I_{IH2}	Logical "1" Input Current		60		60		60	µA	V_{CC} = 5.5 V, $V_{IH(An, Bn)}$ = 2.7 V, C_n = GND or 5.5 V, other inputs are GND.
I_{IH3}	Logical "1" Input Current		80		80		80	µA	V_{CC} = 5.5 V, $V_{IH(S0, S1)}$ = 2.7 V, B_n = 5.5 V, other inputs are GND.
I_{IH4}	Logical "1" Input Current		80		80		80	µA	V_{CC} = 5.5 V, $V_{IH(S1,S2)}$ = 2.7 V, B_n = 5.5 V, other inputs are open.
I_{IH5}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, $V_{IH(Cn)}$ = 2.7 V, other inputs = 5.5 V.
I_{IHH1}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, $V_{IHH(M)}$ = 5.5 V, other inputs are GND.
I_{IHH2}	Logical "1" Input Current		300		300		300	µA	V_{CC} = 5.5 V, $V_{IHH(An, Bn)}$ = 5.5 V, other inputs are GND.
I_{IHH3}	Logical "1" Input Current		400		400		400	µA	V_{CC} = 5.5 V, $V_{IHH(S0, S3)}$ = 5.5 V, other inputs are GND.
I_{IHH4}	Logical "1" Input Current		400		400		400	µA	V_{CC} = 5.5 V, $V_{IHH(S1, S2)}$ = 5.5 V, B_n = 5.5 V, other inputs are GND.
I_{IHH5}	Logical "1" Input Current		500		500		500	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V (all inputs).
I_{CCH}	Power Supply Current Off		35		35		35	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (S_n, M), other inputs are GND.
I_{CCL}	Power Supply Current Off		32		32		32	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (S_n, M, A_n), other inputs are GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{OS1}	Output Short Circuit Current	−15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, $V_{IN(S3, A3, B3)}$ = 5.5 V, other inputs are GND, V_{OUT} = GND.
I_{OS2}	Output Short Circuit Current	−15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), V_{OUT} = GND.
I_{OS3}	Output Short Circuit Current	−15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), V_{OUT}= GND.
I_{IL1}	Logical "0" Input Current	− 0.15	− 0.38	− 0.15	− 0.38	− 0.15	− 0.38	mA	V_{CC} = 5.5 V, $V_{IN(M)}$ = 0.4 V, other inputs = 5.5 V.
I_{IL2}	Logical "0" Input Current	− 0.45	− 1.14	− 0.45	− 1.14	− 0.45	− 1.14	mA	V_{CC} = 5.5 V, $V_{IN(Bn)}$ = 0.4 V or 5.5 V, other inputs = 5.5 V.
I_{IL3}	Logical "0" Input Current	− 0.6	− 1.52	− 0.6	− 1.52	− 0.6	− 1.52	mA	V_{CC} = 5.5 V, $V_{IN(S0,S3)}$ = 0.4 V, other inputs = 5.5 V.
I_{IL4}	Logical "0" Input Current	− 0.6	− 1.52	− 0.6	− 1.52	− 0.6	− 1.52	mA	V_{CC} = 5.5 V, $V_{IN(S1,S2)}$ = 0.4 V, B_n = GND, An = 5.5 V.
I_{IL5}	Logical "0" Input Current	− 0.75	− 1.9	− 0.75	− 1.9	− 0.75	− 1.9	mA	V_{CC} = 5.5 V, $V_{IN(Cn)}$ = 0.4 V, other inputs are GND.
I_{IL6}	Logical "0" Input Current	− 0.3	− 0.76	− 0.3	− 0.76	− 0.3	− 0.76	mA	V_{CC} = 5.5 V, $V_{IN(An)}$ = 0.4 V, B_n = 5.5 V or GND, other inputs = 5.5 V.
I_{CEX}	Open Collector Input Current		100		100		100	µA	V_{CC} = 4.5 V, $V_{IN(A = B)}$ = 5.5 V, other inputs = 2.0 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$	2.0 —	25 20	2.0 —	37 25	2.0 —	37 25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH1} t_{PLH1}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$	2.0 —	56 32	2.0 —	55 40	2.0 —	55 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL2} t_{PHL2}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$	2.0 —	30 32	2.0 —	55 40	2.0 —	55 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH2} t_{PLH2}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$	2.0 —	32 32	2.0 —	55 40	2.0 —	55 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL3} t_{PHL3}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	2.0 —	32 30	2.0 —	52 38	2.0 —	52 38	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH3} t_{PLH3}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	2.0 —	30 30	2.0 —	52 38	2.0 —	52 38	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL4} t_{PHL4}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	2.0 —	33 33	2.0 —	57 41	2.0 —	57 41	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH4} t_{PLH4}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	2.0 —	30 30	2.0 —	52 38	2.0 —	52 38	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL5} t_{PHL5}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$	2.0 —	28 23	2.0 —	42 29	2.0 —	42 29	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH5} t_{PLH5}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$	2.0 —	32 29	2.0 —	51 36	2.0 —	51 36	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL6} t_{PHL6}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$	2.0 —	30 32	2.0 —	55 40	2.0 —	55 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH6} t_{PLH6}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$	2.0 —	32 32	2.0 —	55 40	2.0 —	55 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL7} t_{PHL7}	Propagation Delay C_n or $\overline{F}$	2.0 —	25 20	2.0 —	37 25	2.0 —	37 25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH7} t_{PLH7}	Propagation Delay C_n or $\overline{F}$	2.0 —	26 26	2.0 —	46 33	2.0 —	46 33	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL8} t_{PHL8}	Propagation Delay $\overline{A}$ or $\overline{B}$ to A = B	2.0 —	75 62	2.0 —	96 78	2.0 —	96 78	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH8} t_{PLH8}	Propagation Delay $\overline{A}$ or $\overline{B}$ to A = B	2.0 —	80 50	2.0 —	100 63	2.0 —	100 63	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL9} t_{PHL9}	Propagation Delay C_n to C_{n+4}	2.0 —	25 20	2.0 —	37 25	2.0 —	37 25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH9} t_{PLH9}	Propagation Delay C_n to C_{n+4}	2.0 —	26 27	2.0 —	48 34	2.0 —	48 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL10} t_{PHL10}	Propagation Delay C_n to C_{n+4}	2.0 —	25 20	2.0 —	37 25	2.0 —	37 25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH10} t_{PLH10}	Propagation Delay C_n to C_{n+4}	2.0 —	26 27	2.0 —	48 34	2.0 —	48 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL11} t_{PHL11}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}	2.0 —	40 38	2.0 —	64 48	2.0 —	64 48	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH11} t_{PLH11}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}	2.0 —	38 38	2.0 —	64 48	2.0 —	64 48	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL12} t_{PHL12}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}	2.0 —	46 41	2.0 —	60 51	2.0 —	60 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH12} t_{PLH12}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}	2.0 —	40 41	2.0 —	69 51	2.0 —	69 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL13} t_{PHL13}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$	2.0 —	38 38	2.0 —	48 48	2.0 —	48 48	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH13} t_{PLH13}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$	2.0 —	33 33	2.0 —	57 51	2.0 —	57 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.