LM2685
Dual Output Regulated Switched Capacitor Voltage Converter

General Description
The LM2685 CMOS charge-pump voltage converter operates as an input voltage doubler, +5V regulator and inverter for an input voltage in the range of +2.85V to +6.5V. Five low cost capacitors are used in this circuit to provide up to 50mA of output current at +5V (+5%), and 15mA at −5V. The LM2685 operates at a 130 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 800µA (operating efficiency greater than 80% with most loads) and 6µA typical shutdown current, the LM2685 is ideal for use in battery powered systems. The device is in a small 14-pin TSSOP package.

Features
- +5V regulated output
- Inverts V<sub>IN</sub>(+5V) to V<sub>NEG</sub>(−5V)
- Doubles input supply voltage
- TSSOP-14 package
- 80% typical conversion efficiency at 25mA
- Input voltage range of 2.85V to 6.5V
- Independent shutdown control pins

Applications
- Cellular phones
- Pagers
- PDAs
- Handheld instrumentation
- 3.3V to 5V voltage conversion applications

Typical Application and Connection Diagram

Ordering Information

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package Type</th>
<th>NSC Package Drawing</th>
<th>Supplied As</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2685MTC</td>
<td>TSSOP-14</td>
<td>MTC14</td>
<td>94 Units, Rail</td>
</tr>
<tr>
<td>LM2685MTCX</td>
<td>TSSOP-14</td>
<td>MTC14</td>
<td>2.5k Units, Tape and Reel</td>
</tr>
<tr>
<td>Pin No.</td>
<td>Name</td>
<td>Function</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>--------</td>
<td>---------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>$V_{IN}$</td>
<td>Power supply input voltage.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Power supply ground.</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>$V_{NEG}$</td>
<td>Negative output voltage created by inverting $V_{05}$.</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>$V_{NSW}$</td>
<td>$V_{NEG}$ output connected through a series switch, NSW.</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>CE</td>
<td>Chip enable input. This pin is high for normal operation and low for shutdown. (See Shutdown and Load Disconnect section in the Detailed Device Description division).</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>SDP</td>
<td>Positive side shutdown input. This pin is low for normal operation and high for positive side shutdown and $V_{PSW}$ load disconnect. (See Shutdown and Load Disconnect section in the Detailed Device Description division).</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>SDN</td>
<td>Negative side shutdown input. This pin is low for normal operation and high for negative side shutdown and $V_{NSW}$ load disconnect. (See Shutdown and Load Disconnect section in the Detailed Device Description division).</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>$C_2^-$</td>
<td>The negative terminal of inverting charge-pump capacitor, $C_2$.</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>$C_2^+$</td>
<td>The positive terminal of inverting charge-pump capacitor, $C_2$.</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>$V_{05}$</td>
<td>Regulated +5V output.</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>$V_{PSW}$</td>
<td>$V_{05}$ output connected through a series switch, PSW.</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>$V_{DBL}$</td>
<td>Voltage Doubler Output. (2.85V $\leq V_{IN} \leq$ 5.4V. See Voltage Doubler section).</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>$C_1^+$</td>
<td>The positive terminal of doubling charge-pump capacitor, $C_1$.</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>$C_1^-$</td>
<td>The negative terminal of doubling charge-pump capacitor, $C_1$.</td>
<td></td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Supply Voltage (V_IN to GND or GND to V_NEG) 6.8V
- SDN, SDP, CE (GND − 0.3V) to (V_IN + 0.3V)
- Continuous Output Current 80mA
- Short-Circuit Duration to GND (Note 2) Indefinite

Continuous Power Dissipation (T_A = 25˚C) (Note 3) 600mW
- T_JMAX (Note 3) 150˚C
- θ_JA (Note 3) 140˚C/W
- Operating Ambient Temp. Range −40˚C to 85˚C
- Operating Junction Temp. Range −40˚C to 125˚C
- Storage Temp. Range −65˚C to 150˚C
- Lead Temp. (Soldering, 10 sec.) 300˚C
- ESD Rating (Note 4) 2kV

Electrical Characteristics

Limits with standard typeface apply for T_J = 25˚C, and limits in boldface type apply over the full temperature range. Unless otherwise specified V_IN = 3.6V, C_1 = C_2 = C_3 = C_5 = 2.2µF, C_4 = 4.7µF (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V^-</td>
<td>Supply Voltage</td>
<td>2.85</td>
<td>6.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_Q</td>
<td>Supply Current</td>
<td>No Load</td>
<td>800</td>
<td>1600</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>No Load, V_IN = 6.5V</td>
<td>300</td>
<td>600</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>I_SSD</td>
<td>Shutdown Supply Current</td>
<td>V_IN = 6.5V</td>
<td>6</td>
<td>30</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>V_SD</td>
<td>Shutdown Pin Input Voltage for CE, SDP, SDN</td>
<td>Logic Input High @6.5V</td>
<td>2.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Logic Input Low @6.5V</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_L (+5V)</td>
<td>Output Current at V_05</td>
<td>2.85V &lt; V_IN &lt; 6.5V</td>
<td>50</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_O (−5V)</td>
<td>Output Resistance at V_NEG</td>
<td>I_L = 15mA (Note 6)</td>
<td>20</td>
<td>40</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>F_SW</td>
<td>Switch Frequency</td>
<td>85</td>
<td>130</td>
<td>180</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>η_P</td>
<td>Average Power Efficiency at V_05</td>
<td>2.85V ≤ V_IN ≤ 6.5V</td>
<td>82</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_L = 25mA to GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_05</td>
<td>Output Regulation</td>
<td>1mA &lt; I_L &lt; 50mA, V_IN = 6.5V (Note 7)</td>
<td>5.05</td>
<td>5.252</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1mA &lt; I_L &lt; 50mA, V_IN = 6.5V (Note 7)</td>
<td>4.848</td>
<td>5.05</td>
<td>5.303</td>
<td></td>
</tr>
<tr>
<td>G_LINE</td>
<td>Line Regulation</td>
<td>2.85V &lt; V_IN &lt; 3.6V</td>
<td>0.25</td>
<td></td>
<td>%/V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.6V &lt; V_IN &lt; 6.5V</td>
<td>0.05</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G_LOAD</td>
<td>Load Regulation</td>
<td>1mA &lt; I_L &lt; 50mA, V_IN = 6.5V</td>
<td>0.3</td>
<td>1.0</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>R_S</td>
<td>Series Switch Resistance V_NEG to V_PSW</td>
<td>V_IN &gt; 2.85V</td>
<td>1.5</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_05 to V_PSW</td>
<td>5.0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: V_05 may be shorted to GND without damage. However, shorting V_NEG to V_05 may damage the device. Also, for temperature above 85˚C, V_05 must not be shorted to GND or device may be damaged.

Note 3: The maximum allowable power dissipation is calculated by using P_DMAX = (T_JMAX — T_A) / θ_JA, where T_JMAX is the maximum junction temperature, T_A is the ambient temperature and θ_JA is the junction-to-ambient thermal resistance of the specified package.

Note 4: The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

Note 5: In the typical operating circuit, capacitors C_1 and C_2 are 2.2µF, 0.3Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.

Note 6: Specified output resistance includes internal switch resistance and ESR of capacitors. See the Detailed Device Description section.

Note 7: The 50 mA maximum current assumes no current is drawn from V_DBL pin. See Voltage Doubler section in the Detailed Device Description.
Typical Performance Characteristics  Unless otherwise specified, $T_A = 25^\circ C$, $V_{IN} = 3.6V$. 

Supply Current vs Input Voltage

Supply Current vs Temperature

Efficiency vs Load Current

Output Voltage ($V_{05}$) vs. Load Current

$V_{05}$ Voltage vs. Input Voltage

Output Resistance ($V_{NEG}$) vs. Temperature

Output Resistance ($V_{DBL}$) vs. Input Voltage

Output Resistance ($V_{DBL}$) vs. Temperature

Switch Frequency vs. Temperature
Typical Performance Characteristics

Unless otherwise specified, $T_A = 25\^\circ C$, $V_{IN} = 3.6V$. (Continued)

**Line Transient Response (with 5mA Load)**

A: INPUT VOLTAGE: $V_{IN} = 3.2V$ to $6.0V$, 5V/div
B: OUTPUT VOLTAGE: $V_{PSW}$: 100mV/div
C: OUTPUT VOLTAGE: $V_{NSW}$: 100mV/div

**V_{PSW} and V_{NSW} Response to CE (with 5mA Load)**

A: CE INPUT: 5V/div
B: OUTPUT VOLTAGE: $V_{PSW}$: 5V/div
C: OUTPUT VOLTAGE: $V_{NSW}$: 5V/div

**V_{NSW} Response to SDP (with 5mA Load)**

A: SDP INPUT: 5V/div
B: OUTPUT VOLTAGE: 5V/div

**V_{NSW} Response to SDN (with 5mA Load)**

A: SDN INPUT: 5V/div
B: OUTPUT VOLTAGE ($V_{NSW}$): 5V/div
Detailed Device Description

The LM2685 CMOS charge pump voltage converter operates as an input voltage doubler, +5V regulator and inverter for an input voltage in the range of +2.85V to +6.5V. It delivers maximum load currents of 50mA and 15mA for the regulated +5V and the inverted output voltages respectively, with an operating current of only 800µA. It also has a typical shutdown current of 6µA. All these performance qualities make the LM2685 an ideal device for battery powered systems.

The LM2685 has three main functional blocks: a voltage doubler, a low dropout (LDO) regulator, and a voltage inverter. Figure 1 shows the LM2685 functional block diagram.

Voltage Doubler

The voltage doubler stage doubles the input voltage \( V_{IN} \) within the range of +2.85V to +5.4V. For \( V_{IN} \) above 5.4V, the doubler shuts off and the input voltage is passed directly to \( V_{DBL} \) via an internal power switch.

The doubler contains four large CMOS switches which are switched in a sequence to double the input supply voltage. Figure 2 illustrates the voltage conversion scheme. When S2 and S4 are closed, C1 charges to the supply voltage \( V_{IN} \). During this time interval, switches S1 and S3 are open. In the next time interval, S2 and S4 are opened at the same time, S1 and S3 are closed, the sum of the input voltage \( V_{IN} \) and the voltage across C1 gives the \( 2V_{IN} \) and the voltage across C2 gives the \( 2V_{IN} \) at \( V_{DBL} \) output. \( V_{DBL} \) supplies the LDO regulator. It is recommended not to load \( V_{DBL} \) when \( V_{OS} \) has a load of 50mA. For proper operation, the sum of \( V_{DBL} \) and \( V_{OS} \) loads must not be more than 50mA.

The Schottky diode D1 is only needed for start-up. The internal oscillator circuit uses the \( V_{DBL} \) and GND pins. The voltage across them must be larger than 1.8V to ensure the operation of the oscillator. During start-up, D1 is used to charge up the voltage at \( V_{DBL} \) pin to start the oscillator; it also protects the device from turning on its own parasitic diode and potentially latching up. The diode should have enough current carrying capability to change capacitor C3 at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning on. A Schottky diode like 1N5817 can be used for most applications. If the input ramp is less than 10V/ms, a smaller schottky diode like MBR0520LT1 can be used to reduce the circuit size.

+5 LDO Regulator

\( V_{DBL} \) is the input to an LDO regulator that regulates it to a +5 output voltage at \( V_{OS} \). \( V_{PSW} \) is tied to \( V_{OS} \) through a series switch PSW. The LDO output capacitor (4.7µF Tantalum) may be tied to either \( V_{OS} \) or \( V_{PSW} \).

Inverter

From the \( V_{OS} \) output, a −5V output is created at \( V_{NEG} \) by means of an inverting charge pump. This negative output is unregulated, meaning that it’s output will droop as the load current at \( V_{NEG} \) increases. The inverter contains four large CMOS switches which are in a sequence to invert the input supply voltage. Figure 3 illustrates the voltage conversion scheme. When S1 and S3 are closed, C1 charges to the supply voltage \( V_{OS} \). During this time interval, switches S2 and S4 are open. In the second time interval, S1 and S3 are open; at the same time, S2 and S4 are closed, C1 is charging C2. After a number of cycles, the voltage across C2 will be pumped to \( V_{OS} \). Since the anode of C2 is connected to ground, the output at the cathode of C2 equals \( -(V_{OS}) \) when there is no load current. The output voltage drop when a load...
Detailed Device Description

(Continued)

is added is determined by the parasitic resistance \( R_{ds(on)} \) of the MOSFET switches and the ESR of the capacitors and the charge transfer loss between capacitors.

\[ R_{ds(on)} \times \text{ESR} \]

**Shutdown and Load Disconnect**

In addition to the nominal charge pump and regulator functions, the LM2685 features shutdown and load disconnect circuitry. CE (chip enable) and SDP (shutdown positive) perform the same task with opposite input polarities. When CE is low or SDP is high, all circuit blocks are disabled and \( V_{05} \) falls to ground potential. This is the same result as when the die temperature exceeds 150˚C (typical), and the device’s internal thermal shutdown is triggered.

Forcing SDN (shutdown negative) high disables only the inverting charge pump. The doubling charge pump and the LDO regulator continue to operate, so the \( V_{05} \) and the \( V_{PSW} \) remain at 5V.

The LM2685 incorporates two low impedance switches tied to the \( V_{05} \) and \( V_{NEG} \) outputs, because some special applications require load disconnect and this is achievable via the switches. Switch PSW connects \( V_{05} \) to \( V_{PSW} \), and switch NSW connects \( V_{NEG} \) to \( V_{NSW} \). In normal operation, these switches are closed, allowing 5V loads to be tied to either \( V_{05} \) or \( V_{PSW} \) and −5V loads to be tied to either \( V_{NEG} \) or \( V_{NSW} \). Driving SDN high opens switch NSW only, while forcing CE low or SDP high, opens both the PSW and NSW.

**Application Information**

**Capacitor Selection**

The output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors.

**Voltage Doubler External Capacitors**

The selection of capacitors are based on the specifications of the dropout voltage (which equals \( I_{OUT} \times R_{OUT} \)), the output voltage ripple, and the converter efficiency.

\[ R_{OUT} = 2 R_{SW} + \frac{2}{f_{OSC}} \times C_1 + 4 \times \text{ESR}_C + \text{ESR}_3 \]

where \( R_{SW} \) is the sum of the ON resistance of the internal MOSFET switches as shown in Figure 2.

The peak-to-peak output voltage ripple is determined by the oscillator frequency, the capacitance and ESR of the capacitor C3.

\[ V_{\text{RIPPLE}} = \frac{i_l}{f_{OSC} \times C_2} + 2 \times i_L \times \text{ESR}_C \]

High capacitance (2.2µF to higher), low ESR capacitors can reduce the output resistance and the voltage ripple.

\[ \text{Power efficiency of} \quad P_{\text{OUT}} = \frac{V^2}{L} R_L \]

where \( I_{Q}(V+) \) is the quiescent power loss of the IC device, and \( P_{IN} \) is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs. Low ESR capacitors (table to be referenced) are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

**+5 LDO Regulator External Capacitors**

The voltage doubler output capacitor, \( C_3 \), serves as the input capacitor of the +5 LDO regulator. The output capacitor \( C_4 \), must meet the requirement for minimum amount of capacitance and appropriate ESR (Equivalent Serving Resistance) for proper operation. The ESR value must remain within the regions of stability as shown in Figure 4, Figure 5 and Figure 6 to ensure output’s stability. A minimum capacitance of 1µF is required at the output. This can be increased without limit, but a 4.7µF tantalum capacitor is recommended for loads ranging up to the maximum specification. With lighter loads of less or equal to 10mA, ceramic capacitor of at least 1µF and ESR in the milliohms can be used. This has to be connected to \( V_{PSW} \) pin instead of the \( V_{05} \) pin.

Any output capacitor used should have a good tolerance over temperature for capacitance and ESR values. The larger the capacitor, with ESR within the stable region, the better the stability and noise performance.

**FIGURE 3. Voltage Inverter Principle**

**FIGURE 4. ESR Curve for C\text{OUT} = 2.2\mu\text{F}**
Inverter External Capacitors

As discussed in the +5 LDO Regulator External Capacitors section, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. A minimum of 1µF capacitor with good tolerance over temperature for capacitance and ESR values. The capacitance value can be increased without limit while still maintain high low ESR value. 2.2µF capacitors are recommended for the two external capacitors, C2 and C5 of the inverter.

FIGURE 5. ESR Curve for C\textsubscript{OUT} = 4.7µF

FIGURE 6. ESR Curve for C\textsubscript{OUT} = 10µF
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