■ CPM2C General Specifications

Item	CPU Units with 10 I/O points		CPU Units with 20 I/O points (Transistor outputs)	Expansion I/O Units	
	Relay outputs	Transistor outputs		10 I/O points (Relay outputs)	24 I/O points (Transistor outputs)
Supply voltage	24 VDC				
Operating voltage range	20.4 to 26.4 VDC				
Power consumption	4 W			1 W	
Inrush current	21 A max.				
Insulation resistance	20 MΩ min. (at 500 VDC) between insulated circuits				
Dielectric strength	2,300 VAC for 1 min (between insulated circuits)				
Noise immunity	1,500 Vp-p, pulse width: 0.1 to 1 μs, rise time: 1-ns pulse (via noise simulator)				
Vibration resistance	10 to 57 Hz, 0.075-mm amplitude, 57 to 150 Hz, acceleration: 9.8 m/s^2 in X, Y, and Z directions for 80 minutes each (Time coefficient; 8 minutes × coefficient factor 10 = total time 80 minutes)				
Shock resistance	147 m/s^2 three times each in X, Y, and Z directions				
Ambient temperature	Operating: 0° to 55°C Storage: −20° to 75°C (except for the battery)				
Humidity	10% to 90% (with no condensation)				
Atmosphere	Must be free from corrosive gas				

I/O interface

CPM2C Specifications

■ CPM2C Characteristics

Item		CPU Unit Specification		
		10 I/O points (Relay outputs)	**10 I/O points (Transistor outputs)**	**20 I/O points (Transistor outputs)**
Control method		Stored program method		
I/O control method		Cyclic scan with direct output (Immediate refreshing can be performed with IORF(97).)		
Programming language		Ladder diagram		
Instruction length		1 step per instruction, 1 to 5 words per instruction		
Instructions		Basic instructions: 14 Special instructions: 105 instructions, 185 variations		
Execution time		Basic instructions: 0.64 µs (LD instruction) Special instructions: 7.8 µs (MOV instruction)		
Program capacity		4,096 words		
I/O capacity	CPU Unit only	10 points		20 points
	With Expansion I/O Units	130 points max.		140 points max.
Input bits		IR 00000 to IR 00915 (Words not used for input bits can be used for work bits.)		
Output bits		IR 01000 to IR 01915 (Words not used for output bits can be used for work bits.)		
Work bits		928 bits: IR 02000 to IR 04915 (Words IR 020 to IR 049) and IR 20000 to IR 22715 (Words IR 200 to IR 227)		
Special bits (SR area)		448 bits: SR 22800 to SR 25515		
Temporary bits (TR area)		8 bits (TR0 to TR7)		
Holding bits (HR area)		320 bits: HR 0000 to HR 1915 (Words HR 00 to HR 19)		
Auxiliary bits (AR area)		384 bits: AR 0000 to AR 2315 (Words AR 00 to AR 23)		
Link bits (LR area)		256 bits: LR 0000 to LR 1515 (Words LR 00 to LR 15)		
Timers/Counters		256 timers/counters (TIM/CNT 000 to TIM/CNT 255) 1-ms timers: TMHH(—) 10-ms timers: TIMH(15) 100-ms timers: TIM 1-s/10-s timers: TIML(—) Decrementing counters: CNT Reversible counters: CNTR(12)		
Data memory		Read/Write: 2,048 words (DM 0000 to DM 2047)* Read-only: 456 words (DM 6144 to DM 6599) PC Setup: 56 words (DM 6600 to DM 6655) *The Error Log is contained in DM 2000 to DM 2021.		
Basic interrupts	Interrupt processing	2 interrupts	2 interrupts	4 interrupts
		Shared by the external interrupt inputs (counter mode) and the quick-response inputs.		
	Interval timer interrupts	1 (Scheduled Interrupt Mode or Single Interrupt Mode)		
High-speed counter	High-speed counter	One high-speed counter: 20 kHz single-phase or 5 kHz two-phase (linear count method)		
		Counter interrupt: 1 (set value comparison or set-value range comparison)		
	Interrupt Inputs (Counter mode)	2 inputs	2 inputs	4 inputs
		Shared by the external interrupt inputs and the quick-response inputs.		
		Count-up interrupts: Shared by the external interrupt inputs and the quick-response inputs.		
Pulse output		Two points with no acceleration/deceleration, 10 Hz to 10 kHz each, and no direction control. One point with trapezoid acceleration/deceleration, 10 Hz to 10 kHz, and direction control. Two points with variable duty-ratio outputs (using PWM(—)). (Pulse outputs can be used with transistor outputs only, they cannot be used with relay outputs.)		

CPM2C Specifications

Item	CPU Unit Specification		
	10 I/O points (Relay outputs)	**10 I/O points (Transistor outputs)**	**20 I/O points (Transistor outputs)**
Synchronized pulse control	One point: A pulse output can be created by combining the high-speed counter with pulse outputs and multiplying the frequency of the input pulses from the high-speed counter by a fixed factor. (This output is possible with transistor outputs only, it cannot be used with relay outputs.)		
Quick-response inputs	2 inputs	2 inputs	4 inputs
	Shared by the external interrupt inputs and the interrupt inputs (counter mode). Min. input pulse width: 50 μs max.		
Input time constant (ON response time = OFF response time)	Can be set for all input points. (1 ms, 2 ms, 3 ms, 5 ms, 10 ms, 20 ms, 40 ms, or 80 ms)		
Clock function	Shows the year, month, day of the week, day, hour, minute, and second. (Battery backup) The following CPU Units have a built-in clock: CPM2C-10C1DR-D, CPM2C-10C1DTC-D, CPM2C-10C1DT1C-D, CPM2C-20C1DTC-D, and CPM2C-20C1DT1C-D.		
Communications functions	Peripheral port: Supports Host Link, peripheral bus, no-protocol, or Programming Console connections. RS-232C port: Supports Host Link, no-protocol, 1:1 Slave Unit Link, 1:1 Master Unit Link, or 1:1 NT Link connections. A CPM2C-CN111, CS1W-CN114, or CS1W-CN118 Connecting Cable is required to connect to the CPM2C's communications port.		
Memory protection	HR area, AR area, program contents, read/write DM area contents, and counter values are maintained during power interruptions.		
Memory backup	Flash memory: Program, read-only DM area, and PC Setup Memory backup: The read/write DM area, HR area, AR area, and counter values are backed up. When a battery is installed, its lifetime is approximately 2 years at 25°C. When a battery is not installed, the internal capacitor will backup memory for 10 days at 25°C. (See note.)		
Self-diagnostic functions	CPU Unit failure (watchdog timer), I/O bus error, battery error, and memory failure		
Program checks	No END instruction, programming errors (checked when operation is started)		

Note: A CPM2C-BAT01 Battery can be installed in CPU Units that are not equipped with a clock to backup the contents of the read/write DM area, HR area, AR area, and counter values. Memory can be backed up for up to 2 years.

CPM2C Specifications

■ CPM2C I/O Specifications

1. CPU Unit Input Specifications

Item	Inputs	Specification
Input voltage	All	24 VDC $^{+10\%}/_{-15\%}$
Input impedance	IN00000 to IN00001	2.7 kΩ
	IN00002 to IN00006	3.9 kΩ
	IN00007 and up	4.7 kΩ
Input current	IN00000 to IN00001	8 mA typical
	IN00002 to IN00006	6 mA typical
	IN00007 and up	5 mA typical
ON voltage/current	IN00000 to IN00001	17 VDC min., 5.0 mA
	IN00002 and up	14.4 VDC min., 3.5 mA
OFF voltage/current	All	5.0 VDC max., 1.1 mA
ON delay	All	1 to 80 ms max. Default: 10 ms (See note.)
OFF delay	All	1 to 80 ms max. Default: 10 ms (See note.)
Circuit configuration	IN00000 to IN00001	
	IN00002 to IN00006	
	IN00007 to IN00011	

Note: The input time constant can be set to 1, 2, 3, 5, 10, 20, 40, or 80 ms in the PC Setup.

High-speed Counter Inputs

The following CPU Unit input bits can be used as high-speed counter inputs. The maximum count frequency is 5 kHz in differential phase mode and 20 kHz in the other modes.

Input	Function			
	Differential phase mode	Pulse plus direction input mode	Up/down input mode	Increment mode
IN00000	A-phase pulse input	Pulse input	Increment pulse input	Increment pulse input
IN00001	B-phase pulse input	Direction input	Decrement pulse input	Normal input
IN00002	Z-phase pulse input or hardware reset input (IN00002 can be used as a normal input when it is not used as a high-speed counter input.)			

Interrupt Inputs

CPM2C PCs have inputs that can be used as interrupt inputs (interrupt input mode or counter mode) and quick-response inputs. The minimum pulse width for these inputs is 50 μs.
In CPU Units with 10 I/O points, inputs IN00003 and IN00004 can be used as interrupt inputs. In CPU Units with 20 I/O points, inputs IN00003 through IN00006 can be used as interrupt inputs.

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2. Expansion I/O Unit Input Specifications

Item	Specification
Input voltage	24 VDC $^{+10\%}/_{-15\%}$
Input impedance	4.7 kΩ
Input current	5 mA typical
ON voltage	14.4 VDC min., 3.5 mA
OFF voltage	5.0 VDC max., 1.1 mA
ON delay	1 to 80 ms max. Default: 10 ms (See note.)
OFF delay	1 to 80 ms max. Default: 10 ms (See note.)
Circuit configuration	

Note: The input time constant can be set to 1, 2, 3, 5, 10, 20, 40, or 80 ms in the PC Setup.
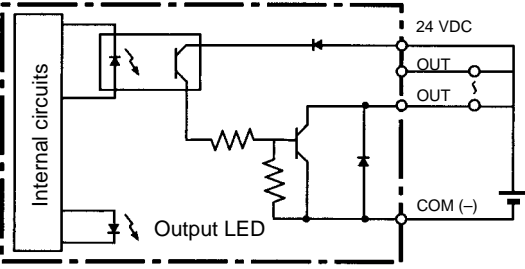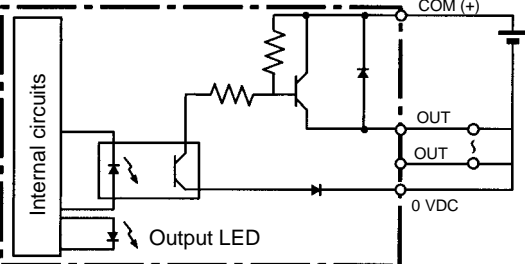
■ CPM2C Output Specifications (CPU Unit and Expansion I/O Unit)

1. Relay Output

Item	Specification
Max. switching capacity	2 A, 250 VAC (cosϕ = 1) 2 A, 24 VDC (4 A/common)
Min. switching capacity	10 mA, 5 VDC
Service life of relay	Electrical: 150,000 operations (30-VDC resistive load) 100,000 operations (240-VAC inductive load, cosϕ = 0.4) Mechanical: 20,000,000 operations
ON delay	15 ms max.
OFF delay	15 ms max.
Circuit configuration	

CPM2C Specifications

2. Transistor Output (Sinking or Sourcing)

Item	Specification
Max. switching capacity	40 mA/4.5 VDC to 300 mA/20.4 VDC, 300 mA (20.4 VDC to 26.4 VDC), 0.3 A/output
Min. switching capacity	0.5 mA
Max. inrush current	0.9 A for 10 ms (charging and discharging waveform)
Leakage current	0.1 mA max.
Residual voltage	0.8 V max.
ON delay	OUT01000 and OUT01001: 20 μs max. OUT01002 and up: 0.1 ms max.
OFF delay	OUT01000 and OUT01001: 40 μs max. for 4.5 to 26.5 V, 10 to 300 mA 0.1 ms max. for 4.5 to 30 V, 0.5 to 10 mA OUT01002 and up: 1 ms max.
Fuse	1 fuse for each 2 outputs (The fuse cannot be replaced by the user.)
Circuit configuration	