



MICROCHIP

PIC18F242/252/442/452

28/40-Pin *Enhanced* FLASH Microcontroller Product Brief

High Performance RISC CPU:

- C compiler optimized architecture/instruction set
 - Source code compatible with the PIC16CXXX instruction set
- Linear program memory addressing to 32 Kbytes
- Linear data memory addressing to 1.5 Kbytes
- 256 bytes of Data EEPROM
- Up to 10 MIPS operation:
 - DC - 40 MHz osc./clock input
 - 4 MHz - 10 MHz osc./clock input with PLL active
- 16-bit wide instructions, 8-bit wide data path
- Priority levels for interrupts
- 31-level, software accessible hardware stack
- 8 x 8 Single Cycle Hardware Multiplier
- Pinout compatible with:
 - PIC16CXXX and PIC16FXXX families
 - PIC18CXXX and PIC18FXXX families

Peripheral Features:

- High current sink/source 25 mA/25 mA
- Three external interrupt pins
- Timer0 module: 8-bit/16-bit timer/counter
- Timer1 module: 16-bit timer/counter
- Timer2 module: 8-bit timer/counter
- Timer3 module: 16-bit timer/counter
- Secondary low power oscillator clock option - Timer1/Timer3
- Two Capture/Compare/PWM (CCP) modules:
 - Capture is 16-bit, max. resolution 6.25 ns (Tcy/16)
 - Compare is 16-bit, max. resolution 100 ns (Tcy)
 - PWM output: PWM resolution is 1- to 10-bit.
- Master Synchronous Serial Port (MSSP) module. Two modes of operation:
 - 3-wire SPI™ (supports all 4 SPI modes)
 - I²C™ Master and Slave mode
- Addressable USART module:
 - Supports RS485 and RS232
- Parallel Slave Port (PSP) module

Analog Features:

- 10-bit with up to 8-ch Analog-to-Digital Converter (A/D):
 - Conversion available during SLEEP
- Programmable 16-level Low Voltage Detection (LVD) module
 - Supports interrupt-on-low voltage detection
- Programmable Brown-out Reset (BOR)

Special Microcontroller Features:

- 1000 erase/write cycle Enhanced FLASH program memory
- 1 second programming time
- 100K erase/write cycle Data EEPROM memory
- Data EEPROM/FLASH Retention: > 40 years
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options including:
 - 4X Phase Lock Loop (of primary oscillator)
 - Secondary Oscillator (32 kHz) clock input
- In-Circuit Serial Programming™ (ICSP™) via two pins
- MPLAB® In-Circuit Debug (ICD) via two pins

CMOS Technology:

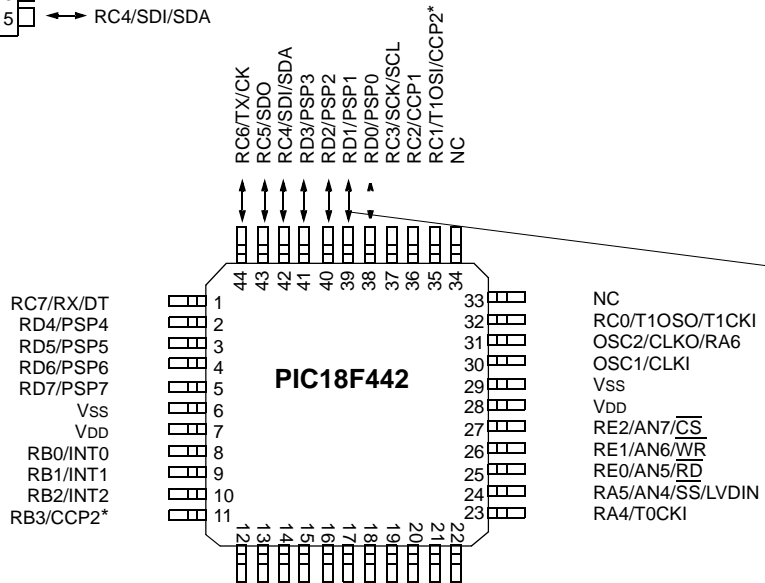
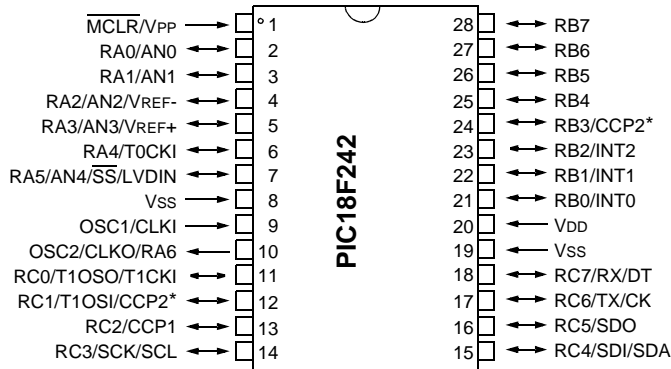
- Low power, high speed FLASH technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Industrial temperature range

Device	Program Memory		Data Memory		I/O	10-bit A/D (ch)	CCP (PWM)	MSSP		USART	Timers 8-bit/16-bit
	Bytes	# Single Word Instructions	SRAM (bytes)	EEPROM (bytes)				SPI	Master I ² C		
PIC18F242	16K	8192	768	256	23	5	2	Y	Y	Y	1/3
PIC18F252	32K	16384	1536	256	23	5	2	Y	Y	Y	1/3
PIC18F442	16K	8192	768	256	34	8	2	Y	Y	Y	1/3
PIC18F452	32K	16384	1536	256	34	8	2	Y	Y	Y	1/3

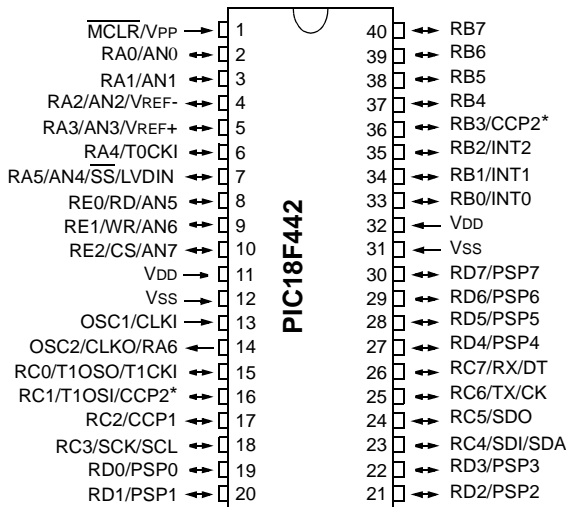
PIC18F242/252/442/452

Pin Diagrams

DIP, SOIC



DIP



* RB3 is the alternate pin for the CCP2 pin multiplexing.

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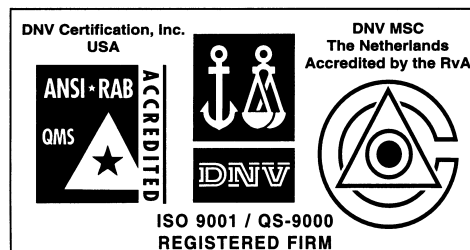
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