CMOS, Low-Voltage, 3-Wire Serially-Controlled, Matrix Switches

ADG738/ADG739

FEATURES
3-Wire Serial Interface
2.7 V to 5.5 V LblfD1Tt©5Ros5ly
2.5 Ω On Resistance
0.75 Ω On-Resistance Flatness
100 pA LeakaD1Te Currents
LblfD1Tt©58-to-15Multiplexer5ADG738
Dual 4-to-15Multiplexer5ADG739
Power-On Reset
TTL/CMOS-Compatible

APPLICATIONS
Data Acquisition Systems
Communication Systems
Relay Replacement

REV. 0

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ADG738/ADG739–SPECIFICATIONS[1] (V_{DD} = 5 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
	4.5	5	Ω max	Test Circuit 1
On-Resistance Match Between		0.4	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
Channels (ΔR_{ON})		0.8	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.75		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
		1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±0.3	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±1	nA max	Test Circuit 3
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_D = V_S = 1 V/4.5 V, Test Circuit 4
	±0.1	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	3		pF typ	
DIGITAL OUTPUT				
Output Low Voltage		0.4	max	I_{SINK} = 6 mA
C_{OUT}, Digital Output Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	20		ns typ	R_L = 300 Ω, C_L = 35 pF, Test Circuit 5;
		32	ns max	V_{S1} = 3 V
t_{OFF}	10		ns typ	R_L = 300 Ω, C_L = 35 pF, Test Circuit 5;
		17	ns max	V_{S1} = 3 V
Break-Before-Make Time Delay, t_D	9		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_{S1} = V_{S8} = 3 V, Test Circuit 5
Charge Injection	±3		pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 6
Off Isolation	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
–3 dB Bandwidth				
ADG738	65		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 8
ADG739	100		MHz typ	
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG738	85		pF typ	
ADG739	42		pF typ	
C_D, C_S (ON)				
ADG738	96		pF typ	
ADG739	48		pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 5.5 V
		20	μA max	

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	6		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
	11	12	Ω max	Test Circuit 1
On-Resistance Match Between		0.4	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
Channels (ΔR_{ON})		1.2	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)		3.5	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.1	±0.3	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_D = 3 V/1 V, V_D = 1 V/3 V;
	±0.1	±1	nA max	Test Circuit 3
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_D = V_S = 3 V/1 V, Test Circuit 4
	±0.1	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	3		pF typ	
DIGITAL OUTPUT				
Output Low Voltage		0.4	max	I_{SINK} = 6 mA
C_{OUT}, Digital Output Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	40		ns typ	R_L = 300 Ω, C_L = 35 pF, Test Circuit 5;
		70	ns max	V_{S1} = 2 V
t_{OFF}	14		ns typ	R_L = 300 Ω, C_L = 35 pF, Test Circuit 5;
		25	ns max	V_{S1} = 2 V
Break-Before-Make Time Delay, t_D	12		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 2 V, Test Circuit 5
Charge Injection	±3		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 6
Off Isolation	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
–3 dB Bandwidth				
ADG738	65		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 8
ADG739	100		MHz typ	
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG738	85		pF typ	
ADG739	42		pF typ	
C_D, C_S (ON)				
ADG738	96		pF typ	
ADG739	48		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.3 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 3.3 V
		20	μA max	

NOTES

[1]Temperature ranges are as follows: B Versions: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = 2.7 V to 5.5 V. All specifications –40°C to +85°C, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
f_{SCLK}	30	MHz max	SCLK Cycle Frequency
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	0	ns min	$\overline{SYNC}$ to SCLK Active Edge Setup Time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	0	ns min	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge
t_8	33	ns min	Minimum $\overline{SYNC}$ High Time
t_9[3]	20	ns min	SCLK Rising Edge to DOUT Valid

NOTES
[1]See Figure 1.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3]C_L = 20 pF, R_L = 1 kΩ.

Specifications subject to change without notice.

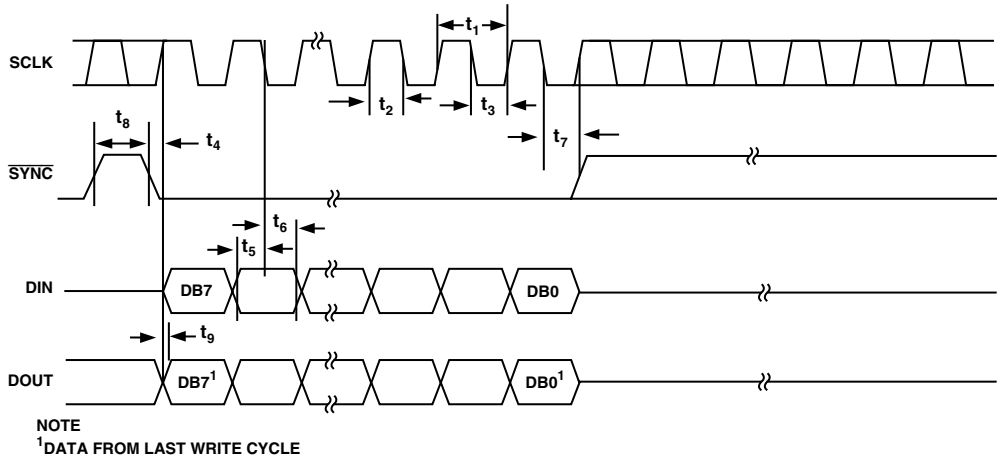
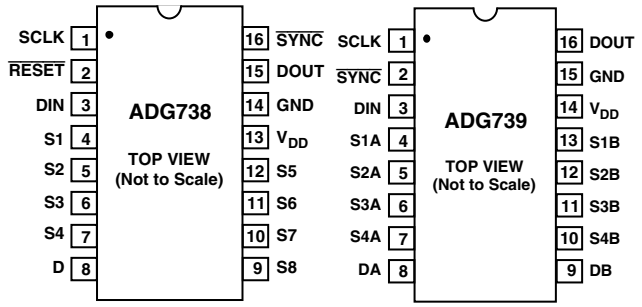


Figure 1. 3-Wire Serial Interface Timing Diagram

PIN FUNCTION DESCRIPTIONS

ADG738	ADG739	Mnemonic	Function
1	1	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz.
2		$\overline{\text{RESET}}$	Active low control input that clears the input register and turns all switches to the OFF condition.
3	3	DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
4, 5, 6, 7	4, 5, 6, 7	Sxx	Source. May be an input or output.
8	8, 9	Dx	Drain. May be an input or output.
9, 10, 11, 12	10, 11, 12, 13	Sxx	Source. May be an input or output.
13	14	V_{DD}	Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V.
14	15	GND	Ground Reference.
15	16	DOUT	Data Output. This allows a number a parts to be daisy-chained. Data is clocked out of the input shift register on the rising edge of SCLK. This is an open drain output which should be pulled to the supply with an external resistor.
16	2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following clocks. Taking $\overline{\text{SYNC}}$ high updates the switch conditions.

PIN CONFIGURATIONS



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG738BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG739BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-16

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted.)

V_{DD} to GND ..... –0.3 V to +7 V
Analog, Digital Inputs[2] ..... –0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D ..... 100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, Each S ..... 30 mA
Continuous Current D, ADG739 ..... 80 mA
Continuous Current D, ADG738 ..... 120 mA
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
TSSOP Package
θ_{JA} Thermal Impedance ..... 150.4°C/W
θ_{JC} Thermal Impedance ..... 27.6°C/W
Lead Temperature, Soldering (10 seconds) ..... 300°C
IR Reflow, Peak Temperature ..... 220°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG738/ADG739 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
I_{DD}	Positive Supply Current.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
V_D (V_S)	Analog Voltage on Terminals D, S.
R_{ON}	Ohmic Resistance between D and S.
ΔR_{ON}	On Resistance Match Between any Two Channels, i.e., R_{ON}max – R_{ON}min.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch "OFF."
I_D (OFF)	Drain Leakage Current with the Switch "OFF."
I_D, I_S (ON)	Channel Leakage Current with the Switch "ON."
V_{INL}	Maximum Input Voltage for Logic "0."
V_{INH}	Minimum Input Voltage for Logic "1."
I_{INL}(I_{INH})	Input Current of the Digital Input.
C_S (OFF)	"OFF" Switch Source Capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" Switch Drain Capacitance. Measured with reference to ground.
C_D, C_S (ON)	"ON" Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance.
t_{ON}	Delay time between the 50% and 90% points of the $\overline{SYNC}$ rising edge and the switch "ON" condition.
t_{OFF}	Delay time between the 50% and 90% points of the $\overline{SYNC}$ rising edge and the switch "OFF" condition.
t_D	"OFF" time measured between the 80% points of both switches when switching from one switch to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Bandwidth	The frequency at which the output is attenuated by 3 dBs.
On Response	The frequency response of the "ON" switch.
Insertion Loss	The loss due to the ON resistance of the switch.

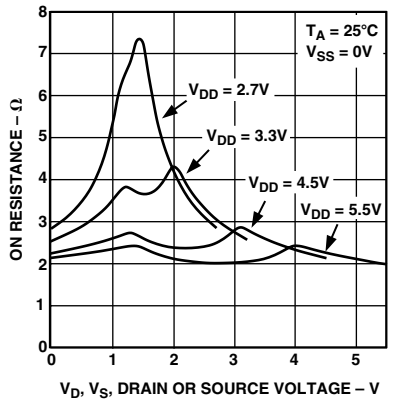


Figure 2. On Resistance as a Function of V_D (V_S)

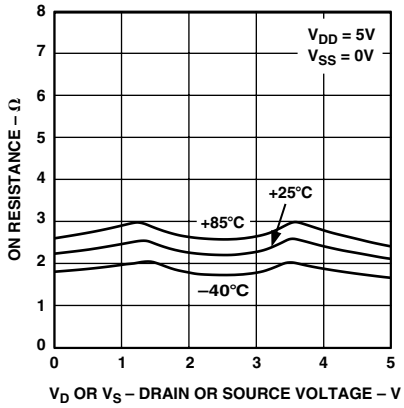


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures

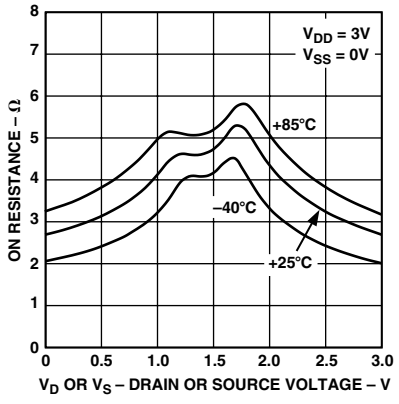


Figure 4. On Resistance as a Function of V_D (V_S) for Different Temperatures

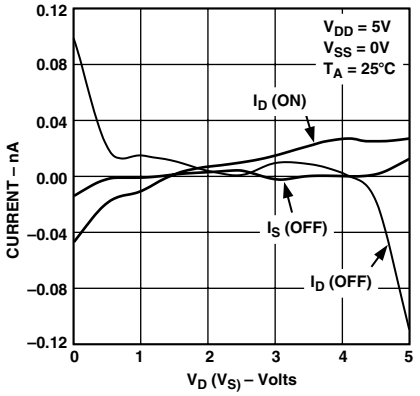


Figure 5. Leakage Currents as a Function of V_D (V_S)

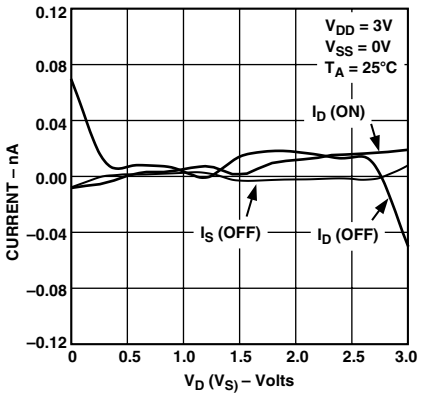


Figure 6. Leakage Currents as a Function of V_D (V_S)

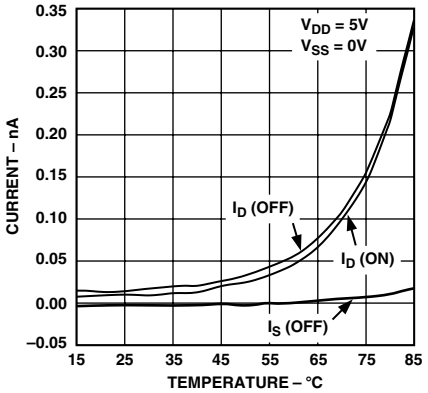


Figure 7. Leakage Currents as a Function of Temperature

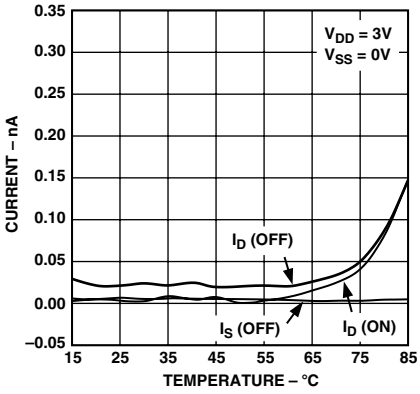


Figure 8. Leakage Currents as a Function of Temperature

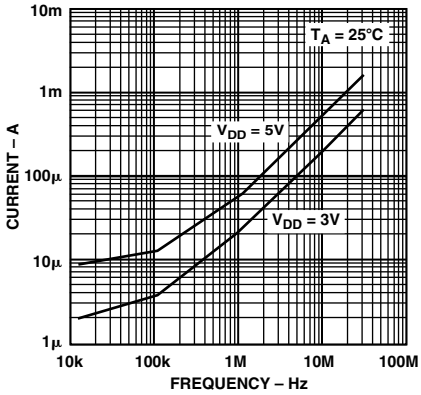


Figure 9. Input Currents vs. Switching Frequency

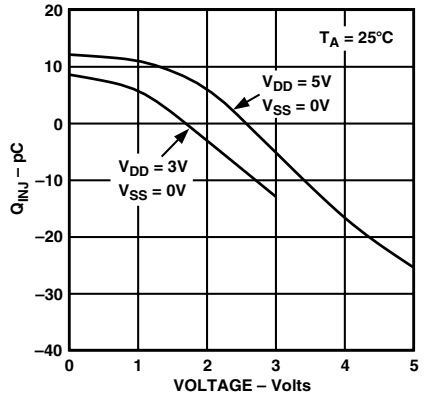


Figure 10. Charge Injection vs. Source Voltage

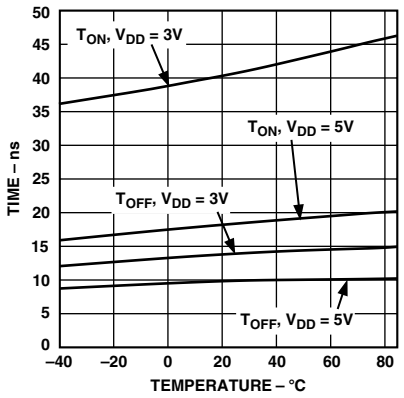


Figure 11. T_{ON}/T_{OFF} Times vs. Temperature

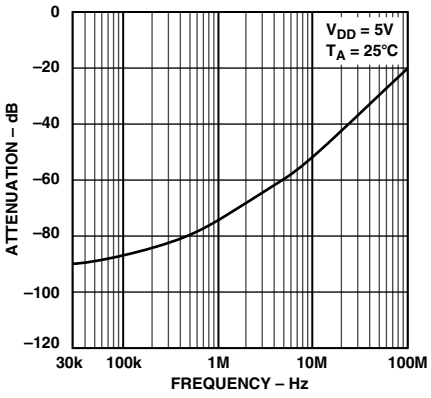


Figure 12. Off Isolation vs. Frequency

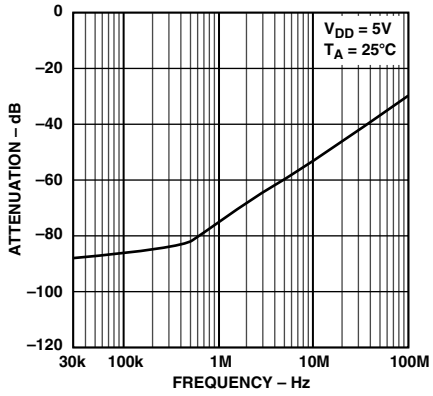


Figure 13. Crosstalk vs. Frequency

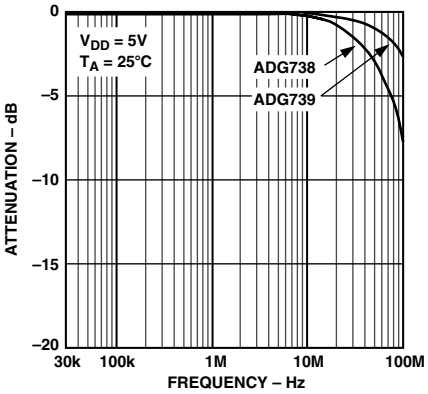


Figure 14. On Response vs. Frequency

GENERAL DESCRIPTION

The ADG738 and ADG739 are serially controlled, 8-channel and dual 4-channel Matrix Switches respectively. While providing the normal multiplexing and demultiplexing functions, these parts also provide the user with more flexibility as to where their signal may be routed. Each bit of the 8-bit serial word corresponds to one switch of the part. A Logic 1 in the particular bit position turns on the switch, while a Logic 0 turns the switch off. Because each switch is independently controlled by an individual bit, this provides the option of having any, all, or none of the switches ON. This feature may be particularly useful in the demultiplexing application where the user may wish to direct one signal from the drain to a number of outputs (sources). Care must be taken, however, in the multiplexing situation where a number of inputs may be shorted together (separated only by the small on resistance of the switch).

When changing the switch conditions, a new 8-bit word is written to the input shift register. Some of the bits may be the same as the previous write cycle, as the user may not wish to change the state of some switches. In order to minimize glitches on the output of these switches, the part cleverly compares the state of switches from the previous write cycle. If the switch is already in the ON condition, and is required to stay ON, there will be minimal glitches on the output of the switch.

POWER-ON RESET

On power-up of the device, all switches will be in the OFF condition and the internal shift register is filled with zeros and will remain so until a valid write takes place.

SERIAL INTERFACE

The ADG738 and ADG739 have a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN), which is compatible with SPI, QSPI, MICROWIRE interface standards and most DSPs. Figure 1 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit shift register via DIN under the control of the $\overline{SYNC}$ and SCLK signals. Data may be written to the shift register in more or less than eight bits. In each case the shift register retains the last eight bits that were written.

When $\overline{SYNC}$ goes low, the input shift register is enabled. Data from DIN is clocked into the shift register on each falling edge of SCLK. Each bit of the 8-bit word corresponds to one of the eight switches. Figure 15 shows the contents of the input shift register. Data appears on the DOUT pin on the rising edge of SCLK suitable for daisy-chaining, delayed, of course, by eight bits. When all eight bits have been written into the shift register, the $\overline{SYNC}$ line is brought high again. The switches are updated with the new configuration and the input shift register is disabled. With $\overline{SYNC}$ held high, any further data or noise on the DIN line will have no effect on the shift register.

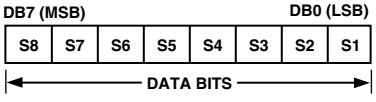


Figure 15. Input Shift Register Contents

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the ADG738/ADG739 is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a synchronization signal. The ADG738/ADG739 requires an 8-bit data word with data valid on the falling edge of SCLK.

Data from the previous write cycle is available on the DOUT pin. The following figures illustrate simple 3-wire interfaces with popular microcontrollers and DSPs.

ADSP-21xx to ADG738/ADG739

An interface between the ADG738/ADG739 and the ADSP-21xx is shown in Figure 16. In the interface example shown, SPORT0 is used to transfer data to the Matrix Switch. The SPORT control register should be configured as follows: internal Clock operation, alternate framing mode; active low framing signal.

Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. As the data is clocked out of the DSP on the rising edge of SCLK, no glue logic is required to interface the DSP to the Matrix Switch. The update of each switch condition takes place automatically when $\overline{TFS}$ is taken high.

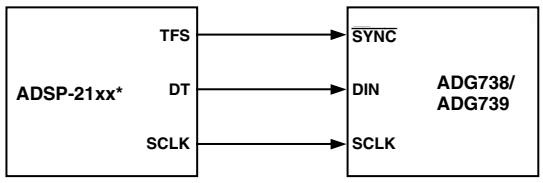


Figure 16. ADSP-21xx to ADG738/ADG739 Interface

8051 Interface to ADG738/ADG739

A serial interface between the ADG738/ADG739 and the 8051 is shown in Figure 17. TXD of the 8051 drives SCLK of the ADG738/ADG739, while RXD drives the serial data line, DIN. P3.3 is a bit-programmable pin on the serial port and is used to drive $\overline{SYNC}$.

The 8051 provides the LSB of its SBUF register as the first bit in the data stream. The user will have to ensure that the data in the SBUF register is arranged correctly as the switch expects MSB first.

When data is to be transmitted to the Matrix Switch, P3.3 is taken low. Data on RXD is clocked out of the microcontroller on the rising edge of TXD and is valid on the falling edge. As a result no glue logic is required between the ADG738/ADG739 and microcontroller interface.

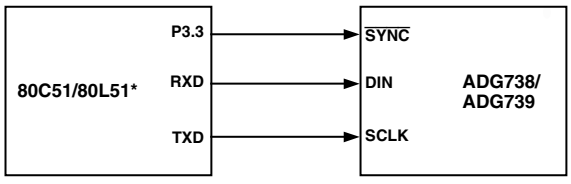


Figure 17. 8051 Interface to ADG738/ADG739

MC68HC11 Interface to ADG738/ADG739

Figure 18 shows an example of a serial interface between the ADG738/ADG739 and the MC68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the Matrix Switch, while the MOSI output drives the serial data line, DIN. $\overline{\text{SYNC}}$ is driven from one of the port lines, in this case PC7.

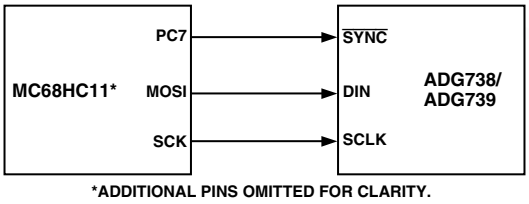


Figure 18. MC68HC11 Interface to ADG738/ADG739

The 68HC11 is configured for master mode; MSTR = 1, CPOL = 0 and CPHA = 1. When data is transferred to the part, PC7 is taken low, data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK.

If the user wishes to verify the data previously written to the input shift register, the DOUT line could be connected to MISO of the MC68HC11, and with $\overline{\text{SYNC}}$ low, the shift register would clock data out on the rising edges of SCLK.

APPLICATIONS

Expand the Number of Selectable Serial Devices Using an ADG739

The dual 4-channel ADG739 multiplexer can be used to multiplex a single chip select line in order to provide chip selects for up to four devices on the SPI bus. Figure 19 illustrates the ADG739 in such a typical configuration. All devices receive the same serial clock and serial data, but only one device will receive the $\overline{\text{SYNC}}$ signal at any one time. The ADG739 is a serially controlled device also. One bit programmable pin of the microcontroller is used to enable the ADG739 via $\overline{\text{SYNC2}}$, while another bit programmable pin is used as the chip select for the other serial devices, $\overline{\text{SYNC1}}$. Driving $\overline{\text{SYNC2}}$ low enables changes to be made to the addressed serial devices. By bringing $\overline{\text{SYNC1}}$ low, the selected serial device hanging from the SPI bus will be enabled and data will be clocked into its shift register on the falling edges of SCLK. The convenient design of the matrix switch allows for different combinations of the four serial devices to be addressed at any one time. If more devices need to be addressed via one chip select line, the ADG738 is an 8-channel device and would allow further expansion of the chip select scheme. There may be some digital feedthrough from the digital input lines because SCLK and DIN are permanently connected to each device. Using a burst clock will minimize the effects of digital feedthrough on the analog channels.

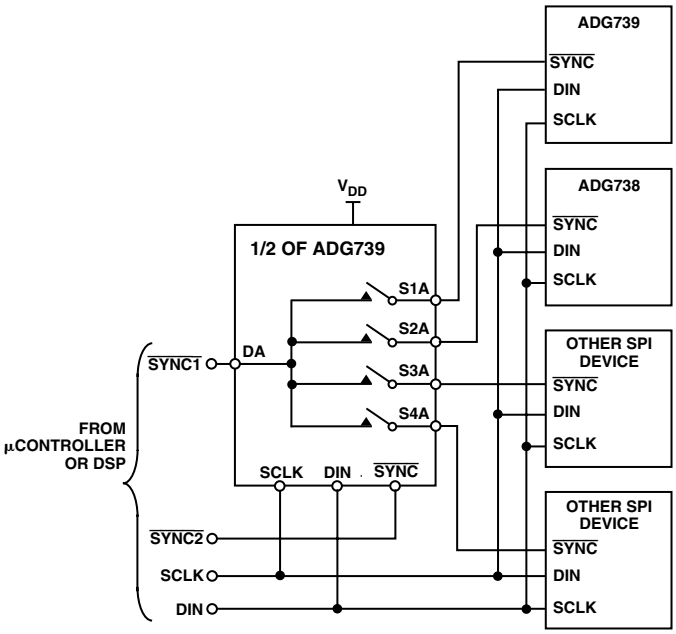


Figure 19. Addressing Multiple Serial Devices Using an ADG739

Daisy-Chaining Multiple ADG738s

A number of ADG738 matrix switches may be daisy-chained simply by using the DOUT pin. DOUT is an open drain output that should be pulled to the supply with an external resistor. Figure 20 shows a typical implementation. The $\overline{\text{SYNC}}$ pin of all three parts in the example are tied together. When $\overline{\text{SYNC}}$ is brought low, the input shift registers of all parts are enabled, data is written to the parts via DIN, and clocked through the shift registers. When the transfer is complete, $\overline{\text{SYNC}}$ is brought high and all switches are updated simultaneously. Further shift registers may be added in series.

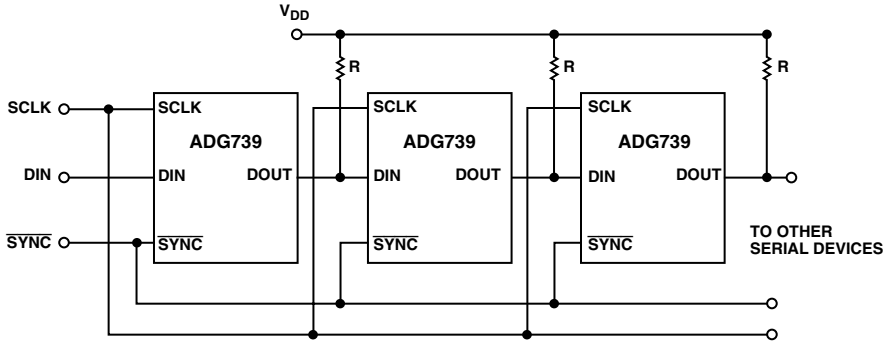
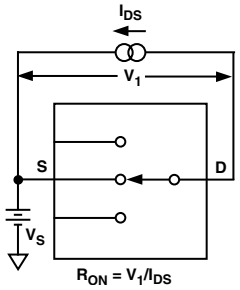
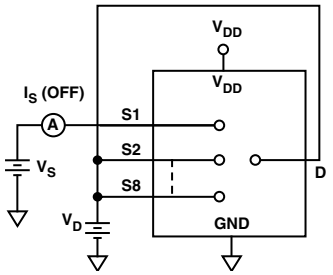


Figure 20. Multiple ADG739 Devices in a Daisy-Chained Configuration

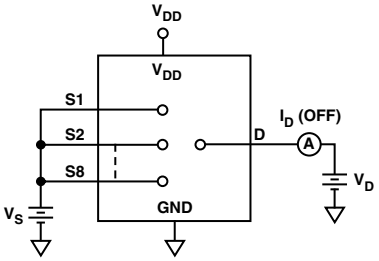
TEST CIRCUITS



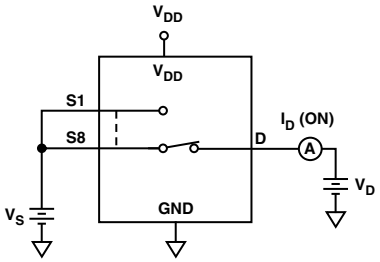
Test Circuit 1. On Resistance



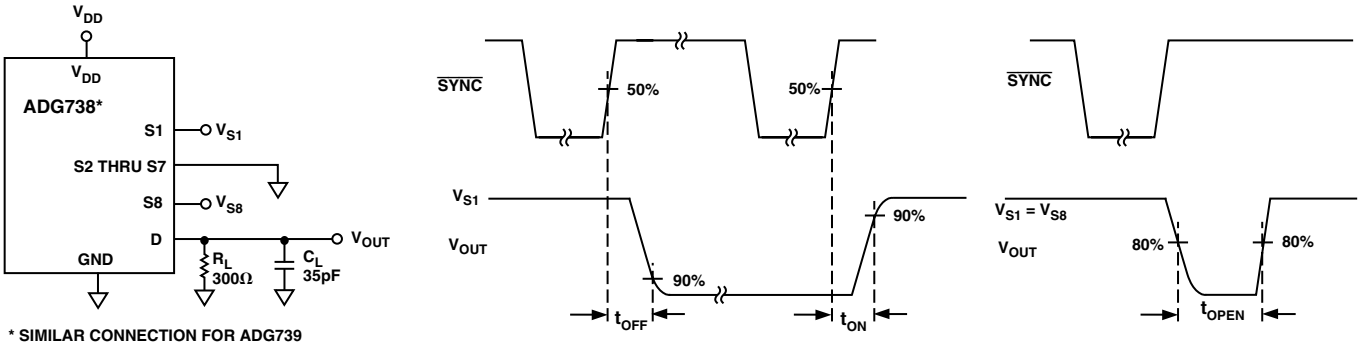
Test Circuit 3. I_S (OFF)



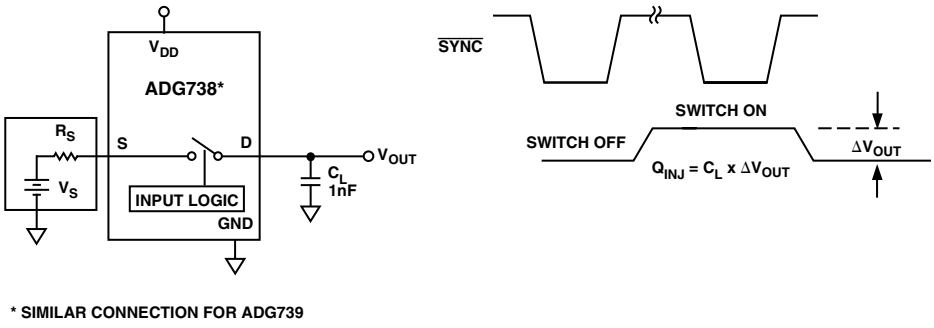
Test Circuit 2. I_D (OFF)



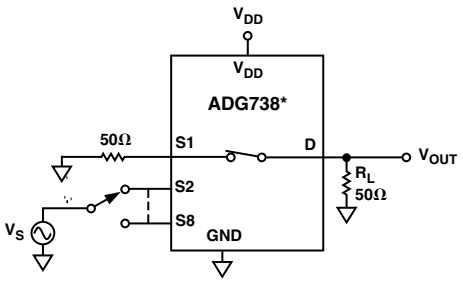
Test Circuit 4. I_D (ON)



Test Circuit 5. Switching Times and Break-Before-Make Times



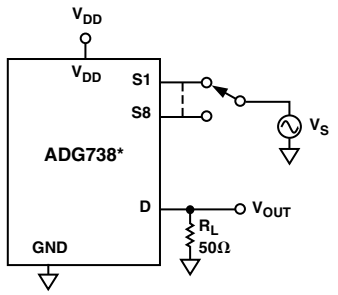
Test Circuit 6. Charge Injection



* SIMILAR CONNECTION FOR ADG739

CHANNEL-TO-CHANNEL CROSSTALK = $20LOG_{10}(V_{OUT}/V_S)$

Test Circuit 7. Channel-to-Channel Crosstalk



*SIMILAR CONNECTION FOR ADG739

S1 IS SWITCHED OFF FOR OFF ISOLATION MEASUREMENTS AND ON FOR BANDWIDTH MEASUREMENTS

OFF ISOLATION = $20LOG_{10}(V_{OUT}/V_S)$

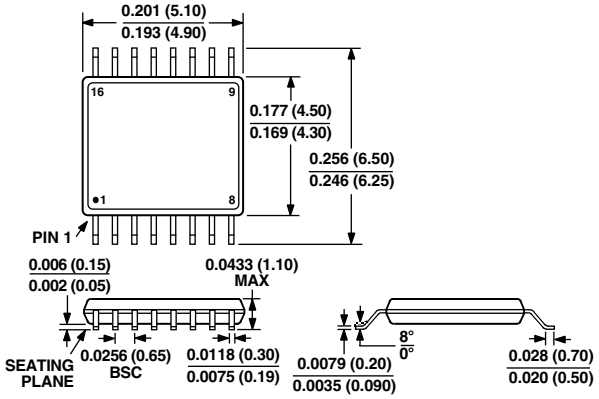
INSERTION LOSS = $20LOG_{10}\left(\frac{V_{OUT}\text{ WITH SWITCH}}{V_{OUT}\text{ WITHOUT SWITCH}}\right)$

Test Circuit 8. Off Isolation and Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP
(RU-16)



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