NEC

MOS INTEGRATED CIRCUIT

78K0R/KE3

16-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The 78K0R/KE3 is a 16-bit single-chip microcontroller that incorporates a 78K0R core.

This is an All Flash microcontroller, which has a single power supply flash memory with a self programming function as well as various other functions.

FEATURES

○ Internal ROM and RAM

Part Number \ Item	Program Memory (ROM)	Data Memory (RAM)
μPD78F1146[Note 1]	256 KB (flash memory)	12 KB
μPD78F1145[Note 1]	192 KB (flash memory)	10 KB
μPD78F1144[Note 2]	128 KB (flash memory)	8 KB
μPD78F1143[Note 2]	96 KB (flash memory)	6 KB
μPD78F1142[Note 2]	64 KB (flash memory)	4 KB

Notes 1. Under development

2. Under planning

○ Minimum instruction execution time
  0.05 μs (20 MHz@2.7 to 5.5 V)
  0.2 μs (5 MHz@1.8 to 5.5 V)

○ Operating clock
  • Main system clock
    - Internal high-speed oscillation clock: 8 MHz (TYP.)
    - Ceramic/crystal resonator/external clock: 2 to 20 MHz
  • Subsystem clock
    - 32.768 kHz
  • Watchdog timer (WDT) clock
    - Internal low-speed oscillation clock: 240 kHz (TYP.)

○ Peripheral function
  • Power-on-clear (POC) circuit
  • Low-voltage detector (LVI)
  • Timer
    - 16-bit timer: 8 channels
    - Real-time counter: 1 channel
    - Watchdog timer: 1 channel
  • Serial interface:
    - UART/CSI: 1 channel
    - UART/CSI/simplified I^2C: 1 channel
    - UART (LIN-bus supported): 1 channel
    - I^2C: 1 channel
  • Key interrupt: 8 channels
  • A/D converter
    - 10-bit resolution A/D converter: 8 channels
  • DMA controller: 2 channels
  • I/O port
    - Total: 55
    - CMOS I/O: 46
    - CMOS input: 4
    - CMOS output: 1
    - N-ch open-drain I/O: 4
  • Multiplier
    - 16 bits × 16 bits
  • Other
    - Self programming
    - Buzzer output/clock output
    - On-chip debug function
    - Safety function
    - BCD adjustment

Interrupt
  - Internal: 25 channels
  - External: 13 channels

Operating voltage range
  - 1.8 V to 5.5 V

Package
  - 64-pin plastic LQFP (10 × 10)
  - 64-pin plastic LQFP (12 × 12)

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Document No. U17846EJ1V0PM00 (1st edition)
Date Published June 2006 NS CP(K)
Printed in Japan

APPLICATIONS

Home appliances (laser printer motors, clothes washers, air conditioners, refrigerators)

Home audio systems

Digital cameras, digital video cameras

OVERVIEW OF FUNCTIONS

(1/2)

Item		μPD78F1142[Note 1]	μPD78F1143[Note 1]	μPD78F1144[Note 1]	μPD78F1145[Note 2]	μPD78F1146[Note 2]
Internal memory	Flash memory (self-programming supported)	64 KB	96 KB	128 KB	192 KB	256 KB
	RAM	4 KB	6 KB	8 KB	10 KB	12 KB
Memory space		1 MB				
Main system clock (Oscillation frequency)	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 2 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 2 to 5 MHz: V_{DD} = 1.8 to 5.5 V				
	Internal high-speed oscillation clock	Internal oscillation 8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V				
Subsystem clock (Oscillation frequency)		XT1 (crystal) oscillation 32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V				
Internal low-speed oscillation clock (For WDT)		Internal oscillation 240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V				
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)				
		0.125 μs (Internal high-speed oscillation clock: f_{IH} = 8 MHz (TYP.) operation)				
		61 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)				
Instruction set		• 8-bit operation, 16-bit operation • Multiply (16 bits × 16 bits) • Bit manipulation (Set, reset, test, and Boolean operation), etc.				
I/O port		Total: 55 CMOS I/O: 46 CMOS input: 4 CMOS output: 1 N-ch open-drain I/O (6 V tolerance): 4				
Timer		• 16-bit timer: 8 channels • Watchdog timer: 1 channel • Real-time counter: 1 channel				
	Timer output	7 (PWM output: 6)				
	RTC output	2 • 1 Hz (Subsystem clock: f_{SUB} = 32.768 kHz) • 512 Hz, 16.384 kHz, or 32 kHz (Subsystem clock: f_{SUB} = 32.768 kHz)				
Clock output/buzzer output		2 • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (peripheral hardware clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)				
A/D converter		10-bit resolution × 16 channels (AV_{REF} = 2.3 to 5.5 V)				

Notes 1. Under planning

2. Under development

(2/2)

Item		μPD78F1142[Note 1]	μPD78F1143[Note 1]	μPD78F1144[Note 1]	μPD78F1145[Note 2]	μPD78F1146[Note 2]
Serial interface		• UART supporting LIN-bus: 1 channel • UART/CSI: 1 channel • UART/CSI/simplified I^2C: 1 channel • I^2C bus: 1 channel				
Multiplier		16 bits × 16 bits = 32 bits				
DMA controller		2 channels				
Vectored interrupt sources	Internal	25				
	External	13				
Key interrupt		Key interrupt (INTKR) occurs by detecting falling edge of the key input pins (KR0 to KR7).				
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-clear • Internal reset by low-voltage detector • Internal reset by illegal instruction execution[Note 3]				
On-chip debug function		Provided				
Power supply voltage		V_{DD} = 1.8 to 5.5 V				
Operating ambient temperature		T_A = −40 to +85°C				
Package		64-pin plastic LQFP (10 × 10) (0.5 mm pitch) 64-pin plastic LQFP (12 × 12) (0.65 mm pitch)				

Notes 1. Under planning

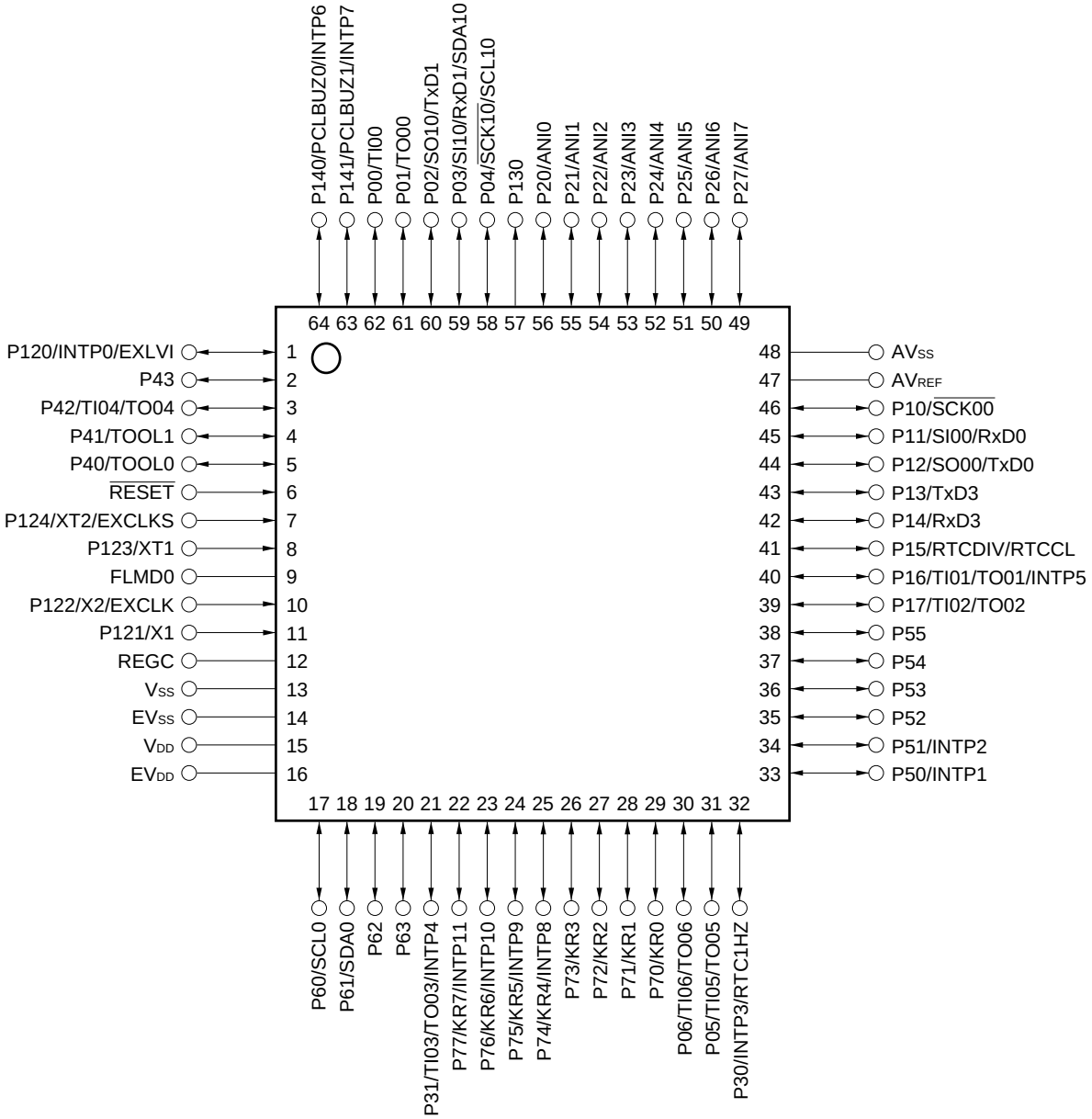
2. Under development

3. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution cannot be emulated by the in-circuit emulator or on-chip debug emulator.

CONTENTS

1. PIN CONFIGURATION (Top View)

- 64-pin plastic LQFP (10 × 10)
- 64-pin plastic LQFP (12 × 12)



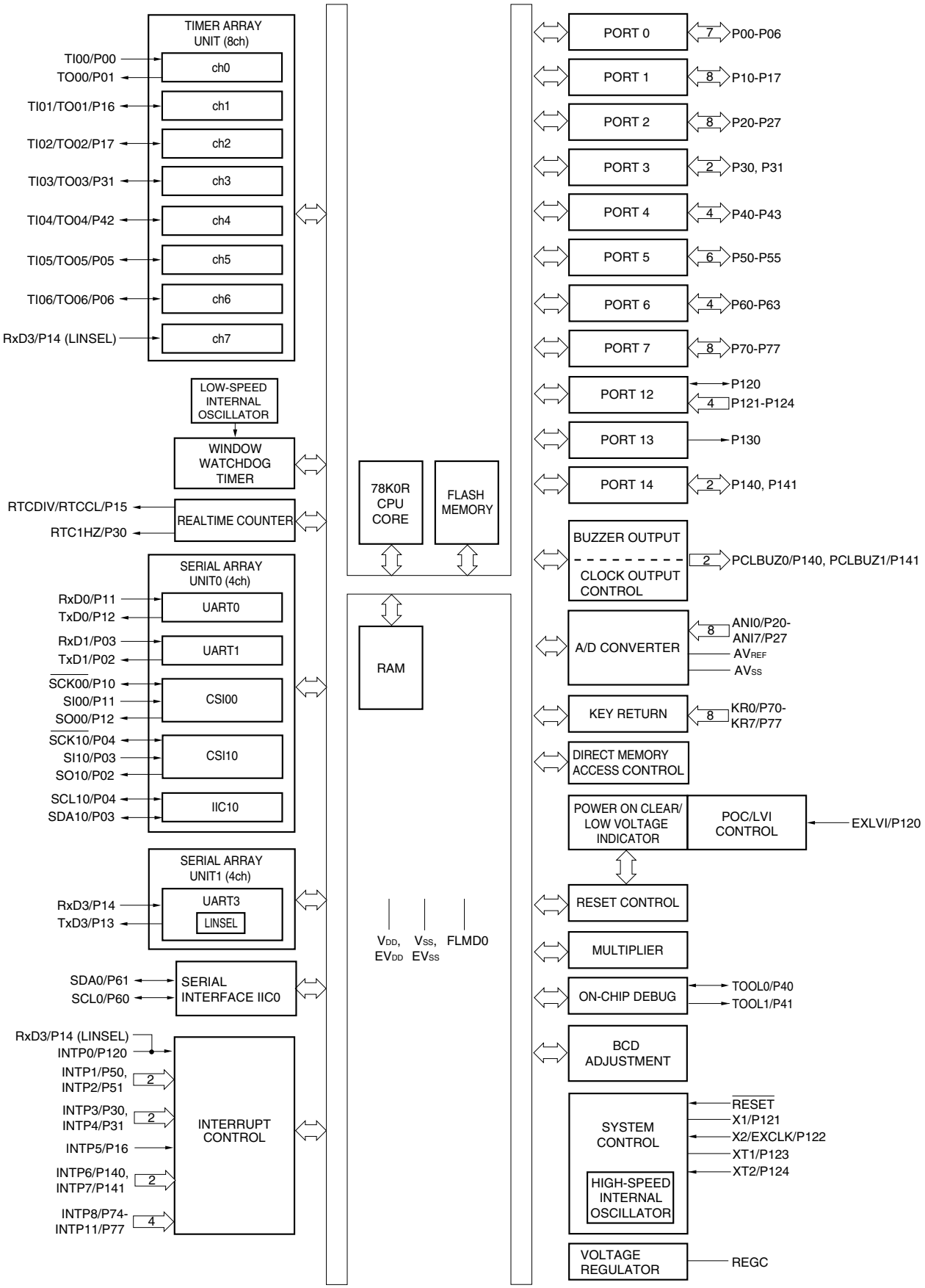
Cautions 1. Make AVSS the same potential as EVSS and VSS.

2. Make EVDD the same potential as VDD.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF: target).

ANI0-ANI7:	Analog Input
AV_{REF}:	Analog Reference Voltage
AV_{SS}:	Analog Ground
EV_{DD}:	Power Supply for Port
EV_{SS}:	Ground for Port
EXCLK:	External Clock Input (Main System Clock)
EXLVI:	External potential Input for Low-voltage detector
FLMD0:	Flash Programming Mode
INTP0-INTP11:	External Interrupt Input
KR0-KR7:	Key Return
P00-P06:	Port 0
P10-P17:	Port 1
P20-P27:	Port 2
P30, P31:	Port 3
P40-P43:	Port 4
P50-P55:	Port 5
P60-P63:	Port 6
P70-P77:	Port 7
P120-P124:	Port 12
P130:	Port 13
P140, P141:	Port 14
PCLBUZ0, PCLBUZ1:	Programmable Clock Output/ Buzzer Output
REGC:	Regulator Capacitance
RESET:	Reset
RTC1HZ:	Real-time Counter Correction Clock (1 Hz) Output
RTCCL:	Real-time Counter Clock (32 kHz Original Oscillation) Output
RTCDIV:	Real-time Counter Clock (32 kHz Divided Frequency) Output
RxD0, RxD1	
RxD3:	Receive Data
SCK00, SCK10:	Serial Clock Input/Output
SCL0, SCL10:	Serial Clock Input/Output
SDA0, SDA10:	Serial Data Input/Output
SI00, SI10:	Serial Data Input
SO00, SO10:	Serial Data Output
TI00-TI06:	Timer Input
TO00-TO06:	Timer Output
TOOL0:	Data Input/Output for Tool
TOOL1:	Clock Output for Tool
TxD0, TxD1, TxD3:	Transmit Data
V_{DD}:	Power Supply
V_{SS}:	Ground
X1, X2:	Crystal Oscillator (Main System Clock)
XT1, XT2:	Crystal Oscillator (Subsystem Clock)

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Functions

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 7-bit I/O port. Input of P03 and P04 can be set to TTL buffer. Output of P02 to P04 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI00
P01				TO00
P02				SO10/TxD1
P03				SI10/RxD1/SDA10
P04				$\overline{\text{SCK10}}$/SCL10
P05				TI05/TO05
P06				TI06/TO06
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK00}}$
P11				SI00/RxD0
P12				SO00/TxD0
P13				TxD3
P14				RxD3
P15				RTCDIV/RTCCL
P16				TI01/TO01/INTP5
P17				TI02/TO02
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input	ANI0 to ANI7
P30	I/O	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	RTC1HZ/INTP3
P31				TI03/TO03/INTP4
P40	I/O	Port 4. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TOOL1
P42				TI04/TO04
P43				–
P50	I/O	Port 5. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1
P51				INTP2
P52				–
P53				–
P54				–
P55				–

(2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P60	I/O	Port 6. 4-bit I/O port. Output of P60 to P63 can be set to N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0
P62				–
P63				–
P70 to P73	I/O	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0 to KR3
P74 to P77				KR4/INTP8 to KR7/ INTP11
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P130	Output	Port 13. 1-bit output port.	Output port	–
P140	I/O	Port 14. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0/INTP6
P141				PCLBUZ1/INTP7

3.2 Non-Port Functions

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
ANI0-ANI7	Input	A/D converter analog input	Digital input	P20 to P27
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P50
INTP2				P51
INTP3				P30/RTC1HZ
INTP4				P31/TI03/TO03
INTP5				P16/TI01/TO01
INTP6				P140/PCLBUZ0
INTP7				P141/PCLBUZ1
INTP8				P74/KR4 to P77/KR7
INTP9				
INTP10				
INTP11				
KR0-KR3	Input	Key interrupt input	Input port	P70 to P73
KR4-KR7				P74/INTP8 to P77/INTP11
PCLBUZ0	Output	Clock output/buzzer output	Input port	P140/INTP6
PCLBUZ1				P141/INTP7
REGC	–	Connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF: target).	–	–
RTCDIV	Output	Real-time counter clock (32 kHz divided frequency) output	Input port	P15/RTCCL
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P15/RTCDIV
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P30/INTP3
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to UART0	Input port	P11/SI00
RxD1	Input	Serial data input to UART1	Input port	P03/SI10/SDA10
RxD3	Input	Serial data input to UART3	Input port	P14
$\overline{\text{SCK00}}$	I/O	Clock input/output for CSI00 and CSI10	Input port	P10
$\overline{\text{SCK10}}$				P04/SCL10
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P04/$\overline{\text{SCK10}}$
SDA0	I/O	Serial data I/O for I^2C	Input port	P61
SDA10		Clock input/output for simplified I^2C	Input port	P03/SI10/RxD1
SI00	I/O	Serial data input to CSI00 and CSI10	Input port	P11/RxD0
SI10				P03/RxD1/SDA10
SO00	Output	Serial data output from CSI00 and CSI10	Input port	P12/TxD0
SO10				P02/TxD1

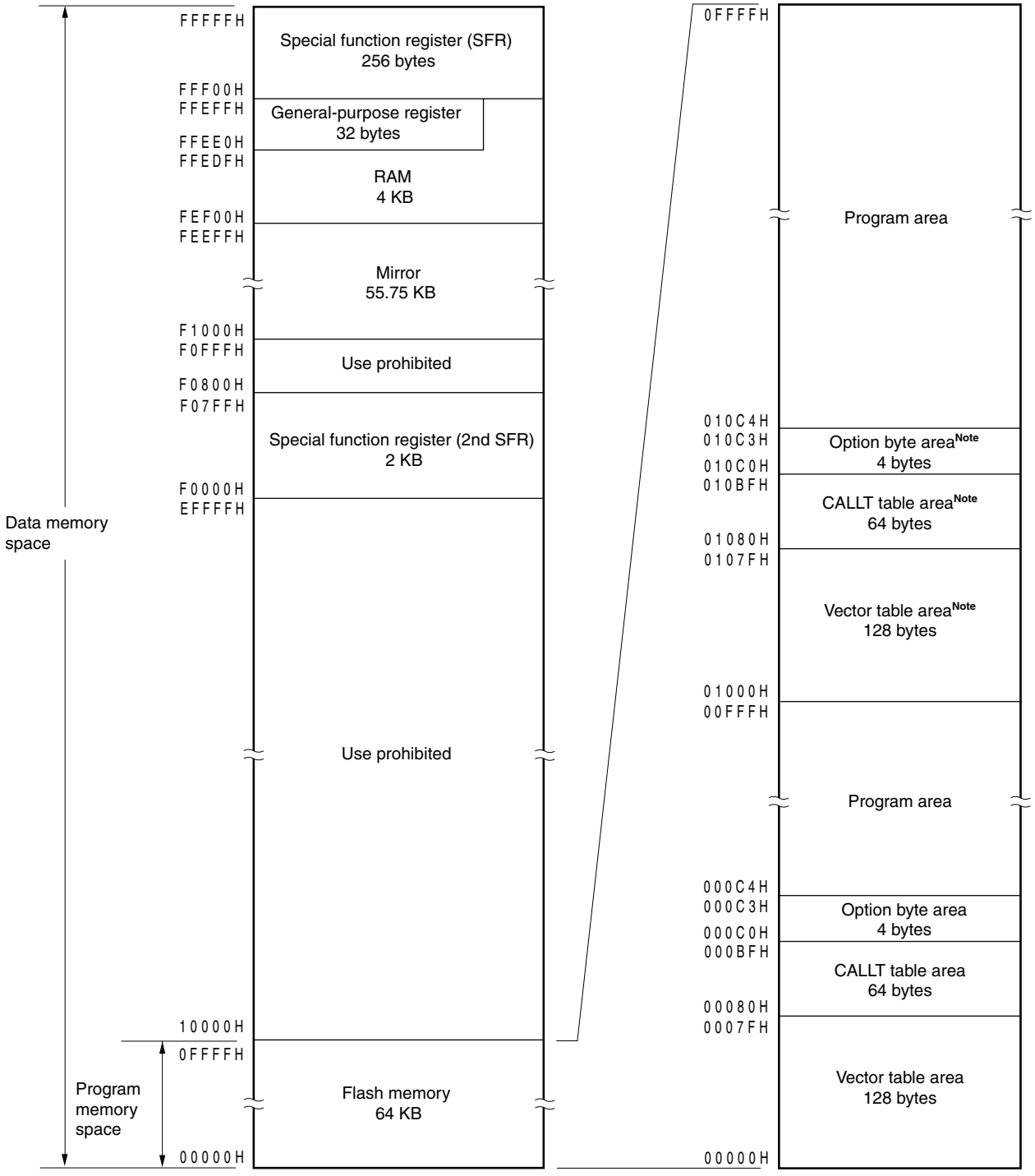
(2/2)

Function Name	I/O	Function	After Reset	Alternate Function
TI00		External count clock input to 16-bit timer 00		P00

4. MEMORY SPACE

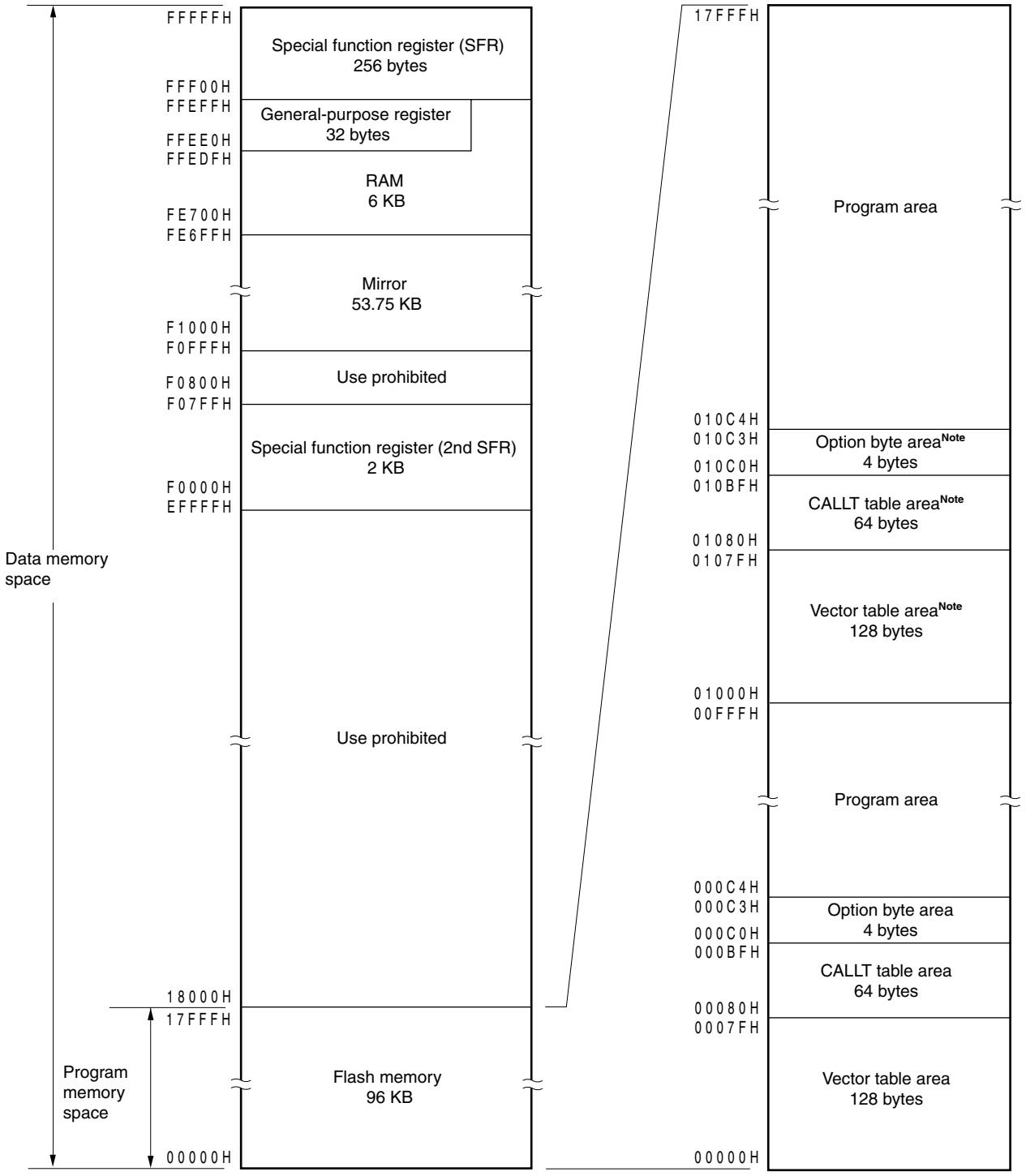
Memory maps of μPD78F1142, 78F1143, 78F1144, 78F1145, and 78F1146 are shown in Figures 4-1 to 4-5.

Figure 4-1. Memory Map (μPD78F1142)



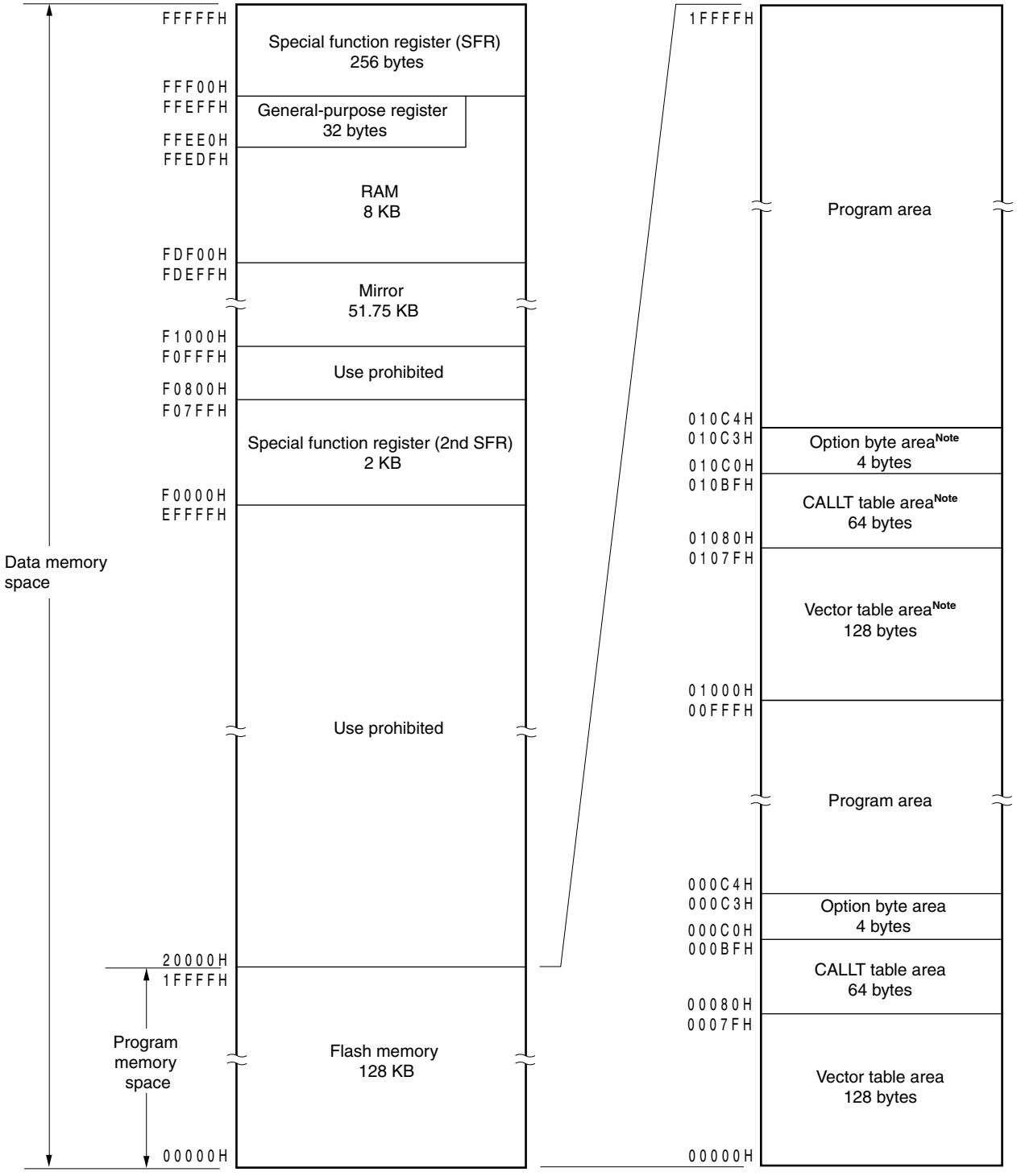
Note When using boot swap, write the contents of 00000H to 00FFFH in 01000H to 01FFFH.

Figure 4-2. Memory Map (μPD78F1143)



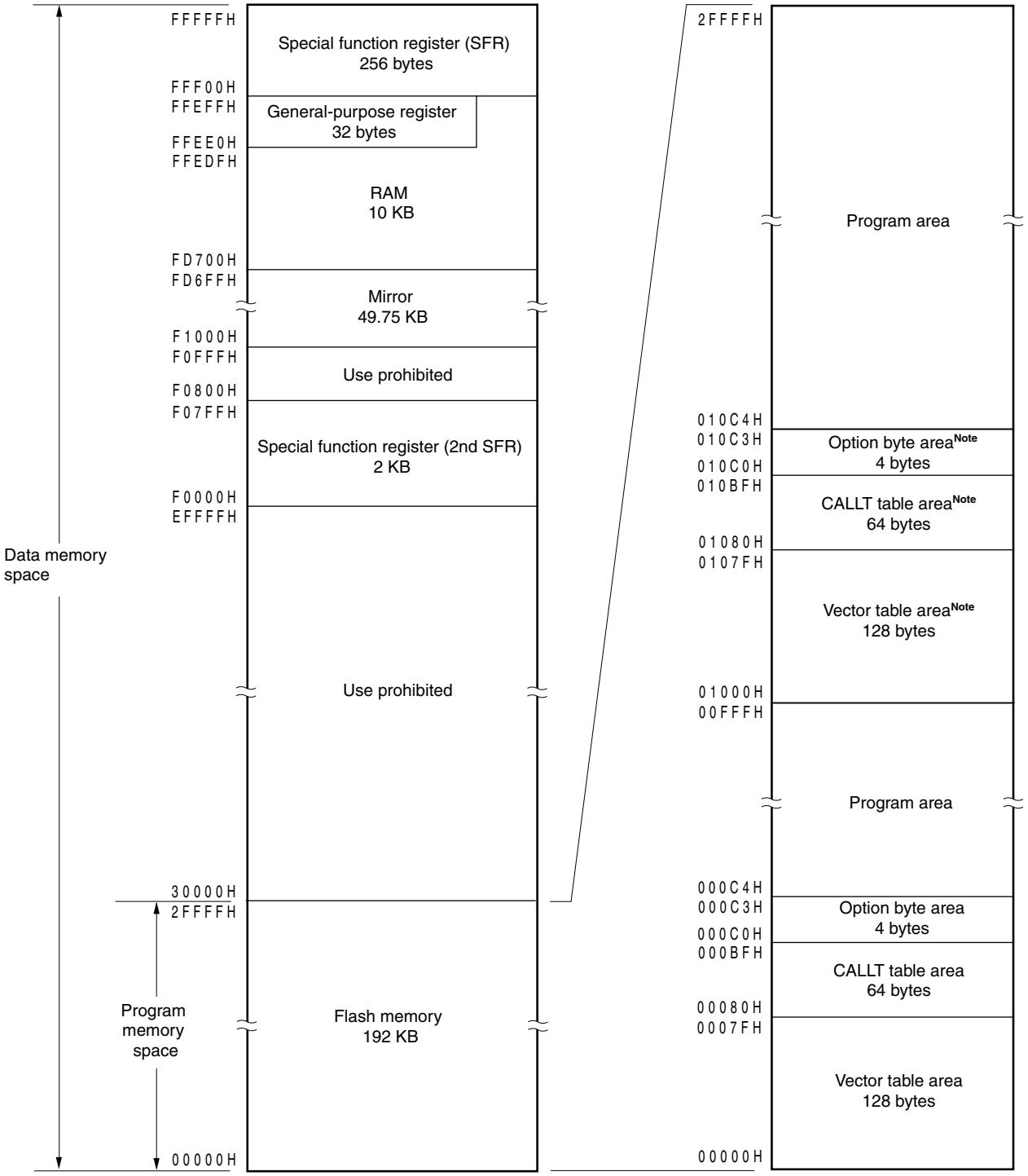
Note When using boot swap, write the contents of 00000H to 00FFFH in 01000H to 01FFFH.

Figure 4-3. Memory Map (μPD78F1144)



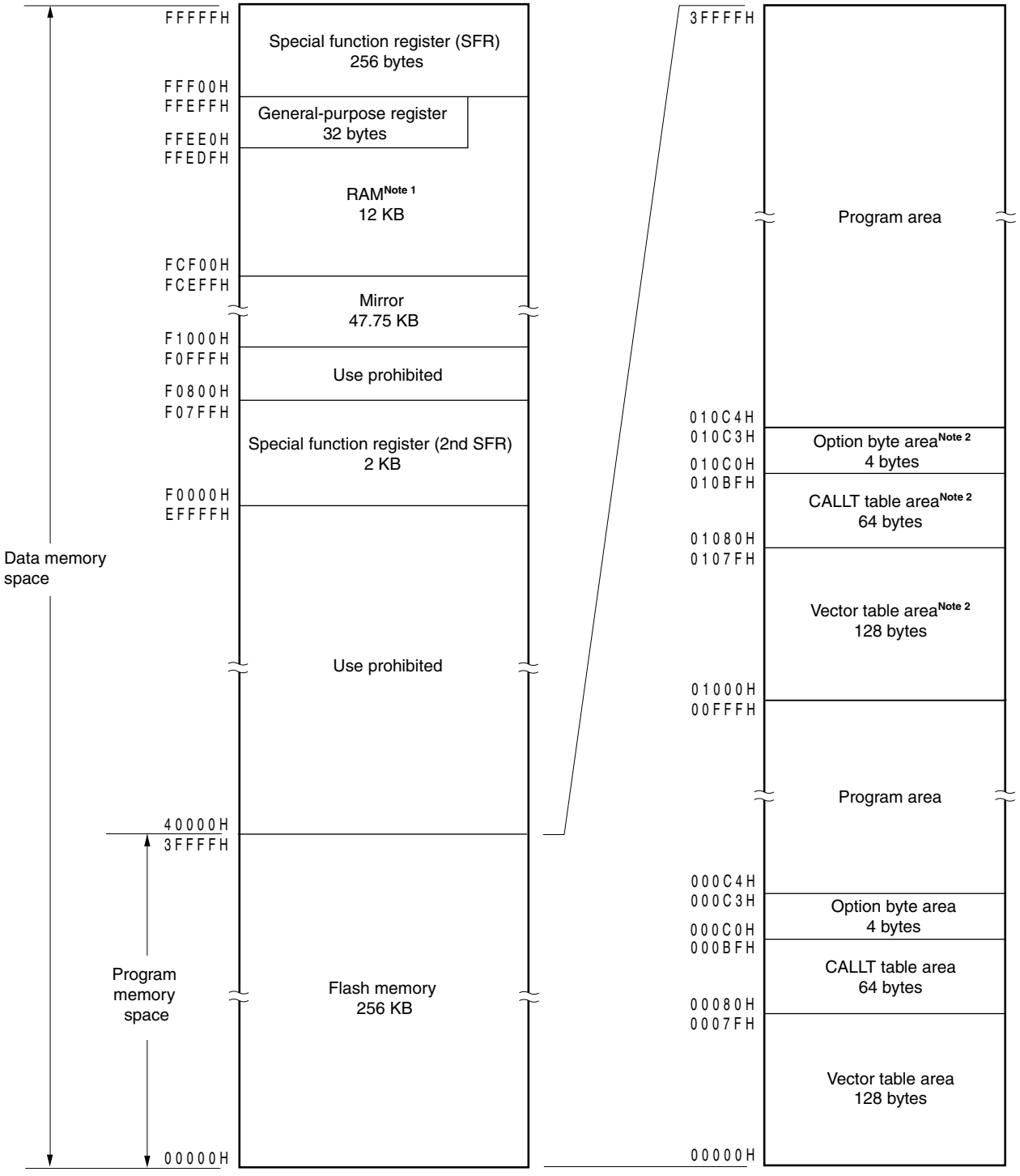
Note When using boot swap, write the contents of 00000H to 00FFFH in 01000H to 01FFFH.

Figure 4-4. Memory Map (μPD78F1145)



Note When using boot swap, write the contents of 00000H to 00FFFH in 01000H to 01FFFH.

Figure 4-5. Memory Map (μPD78F1146)



Notes 1. Use of the area FCF00H to FD6FFH is prohibited when using the self-programming function.

2. When using boot swap, write the contents of 00000H to 00FFFH in 01000H to 01FFFH.

5. SPECIAL FUNCTION REGISTERS (SFRs)

Unlike a general-purpose register, each SFR has a special function.

SFRs are allocated to the FFF00H to FFFFFH area.

SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit). This manipulation can also be specified with an address.
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr). This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (sfrp). When specifying an address, describe an even address.

Table 5-1 gives a list of the SFRs. The meanings of items in the table are as follows.

- Symbol
  Symbol indicating the address of a SFR. It is a reserved word in the RA78K0R, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0R. When using the RA78K0R, debugger, and simulator, symbols can be written as an instruction operand.
- R/W
  Indicates whether the corresponding SFR can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulable bit units
  "√" indicates the manipulable bit unit (1, 8, or 16). "–" indicates a bit unit for which manipulation is not possible.
- After reset
  Indicates each register status upon reset signal generation.

Remark For extended SFRs (2nd SFRs), see **6. EXTENDED SPECIAL FUNCTION REGISTERS (2nd SFRs: 2nd Special Function Registers)**.

Table 5-1. SFR List (1/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
FFF00H	Port register 0	P0		R/W	√	√	–	00H
FFF01H	Port register 1	P1		R/W	√	√	–	00H
FFF02H	Port register 2	P2		R/W	√	√	–	00H
FFF03H	Port register 3	P3		R/W	√	√	–	00H
FFF04H	Port register 4	P4		R/W	√	√	–	00H
FFF05H	Port register 5	P5		R/W	√	√	–	00H
FFF06H	Port register 6	P6		R/W	√	√	–	00H
FFF07H	Port register 7	P7		R/W	√	√	–	00H
FFF0CH	Port register 12	P12		R/W	√	√	–	00H
FFF0DH	Port register 13	P13		R/W	√	√	–	00H
FFF0EH	Port register 14	P14		R/W	√	√	–	00H
FFF10H	Serial data register 00	TxD0/ SIO00	SDR00	R/W	–	√	√	0000H
FFF11H		–			–	–		
FFF12H	Serial data register 01	RxD0	SDR01	R/W	–	√	√	0000H
FFF13H		–			–	–		
FFF14H	Serial data register 12	TxD3	SDR12	R/W	–	√	√	0000H
FFF15H		–			–	–		
FFF16H	Serial data register 13	RxD3	SDR13	R/W	–	√	√	0000H
FFF17H		–			–	–		
FFF18H	Timer data register 00	TDR00		R/W	–	–	√	0000H
FFF19H								
FFF1AH	Timer data register 01	TDR01		R/W	–	–	√	0000H
FFF1BH								
FFF1EH	10-bit A/D conversion result register	ADCR		R	–	–	√	0000H
FFF1FH	8-bit A/D conversion result register	ADCRH		R	–	√	–	00H
FFF20H	Port mode register 0	PM0		R/W	√	√	–	FFH
FFF21H	Port mode register 1	PM1		R/W	√	√	–	FFH
FFF22H	Port mode register 2	PM2		R/W	√	√	–	FFH
FFF23H	Port mode register 3	PM3		R/W	√	√	–	FFH
FFF24H	Port mode register 4	PM4		R/W	√	√	–	FFH
FFF25H	Port mode register 5	PM5		R/W	√	√	–	FFH
FFF26H	Port mode register 6	PM6		R/W	√	√	–	FFH
FFF27H	Port mode register 7	PM7		R/W	√	√	–	FFH
FFF2CH	Port mode register 12	PM12		R/W	√	√	–	FFH
FFF2EH	Port mode register 14	PM14		R/W	√	√	–	FFH

Table 5-1. SFR List (2/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
FFF30H	A/D converter mode register	ADM		R/W	√	√	–	00H
FFF31H	Analog input channel specification register	ADS		R/W	√	√	–	00H
FFF37H	Key return mode register	KRM		R/W	√	√	–	00H
FFF38H	External interrupt rising edge enable register 0	EGP0		R/W	√	√	–	00H
FFF39H	External interrupt falling edge enable register 0	EGN0		R/W	√	√	–	00H
FFF3AH	External interrupt rising edge enable register 1	EGP1		R/W	√	√	–	00H
FFF3BH	External interrupt falling edge enable register 1	EGN1		R/W	√	√	–	00H
FFF3CH	Input switch control register	ISC		R/W	√	√	–	00H
FFF3EH	Timer input select register 0	TIS0		R/W	√	√	–	00H
FFF44H	Serial data register 02	TxD1/ SIO10	SDR02	R/W	–	√	√	0000H
FFF45H		–			–	–		
FFF46H	Serial data register 03	RxD1	SDR03	R/W	–	√	√	0000H
FFF47H		–			–	–		
FFF50H	IIC shift register 0	IIC0		R/W	–	√	–	00H
FFF51H	IIC flag register 0	IICF0		R/W	√	√	–	00H
FFF52H	IIC control register 0	IICC0		R/W	√	√	–	00H
FFF53H	IIC slave address register 0	SVA0		R/W	–	√	–	00H
FFF54H	IIC clock select register 0	IICCL0		R/W	√	√	–	00H
FFF55H	IIC function expansion register 0	IICX0		R/W	√	√	–	00H
FFF56H	IIC status register 0	IICS0		R	√	√	–	00H
FFF64H	Timer data register 02	TDR02		R/W	–	–	√	0000H
FFF65H								
FFF66H	Timer data register 03	TDR03		R/W	–	–	√	0000H
FFF67H								
FFF68H	Timer data register 04	TDR04		R/W	–	–	√	0000H
FFF69H								
FFF6AH	Timer data register 05	TDR05		R/W	–	–	√	0000H
FFF6BH								
FFF6CH	Timer data register 06	TDR06		R/W	–	–	√	0000H
FFF6DH								
FFF6EH	Timer data register 07	TDR07		R/W	–	–	√	0000H
FFF6FH								

Table 5-1. SFR List (3/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
FFF90H	Sub-count register	RSUBC	R	–	–	√	0000H
FFF91H							
FFF92H	Second count register	SEC	R/W	–	√	–	00H
FFF93H	Minute count register	MIN	R/W	–	√	–	00H
FFF94H	Hour count register	HOUR	R/W	–	√	–	12H Note 1
FFF95H	Week count register	WEEK	R/W	–	√	–	00H
FFF96H	Day count register	DAY	R/W	–	√	–	01H
FFF97H	Month count register	MONTH	R/W	–	√	–	01H
FFF98H	Year count register	YEAR	R/W	–	√	–	00H
FFF99H	Watch error correction register	SUBCUD	R/W	–	√	–	00H
FFF9AH	Alarm minute register	ALARMWM	R/W	–	√	–	00H
FFF9BH	Alarm hour register	ALARMWH	R/W	–	√	–	12H
FFF9CH	Alarm week register	ALARMWW	R/W	–	√	–	00H
FFF9DH	Real-time counter control register 0	RTCC0	R/W	√	√	–	00H
FFF9EH	Real-time counter control register 1	RTCC1	R/W	√	√	–	00H
FFF9FH	Real-time counter control register 2	RTCC2	R/W	√	√	–	00H
FFFA0H	Clock operation mode control register	CMC	R/W	–	√	–	00H
FFFA1H	Clock operation status control register	CSC	R/W	√	√	–	C0H
FFFA2H	Oscillation stabilization time counter status register	OSTC	R	√	√	–	00H
FFFA3H	Oscillation stabilization time select register	OSTS	R/W	–	√	–	07H
FFFA4H	Clock control register	CKC	R/W	√	√	–	09H
FFFA5H	Clock output select register 0	CKS0	R/W	√	√	–	00H
FFFA6H	Clock output select register 1	CKS1	R/W	√	√	–	00H
FFFA8H	Reset control flag register	RESF	R	–	√	–	00H Note 2
FFFA9H	Low-voltage detection register	LVIM	R/W	√	√	–	00H Note 3
FFFAAH	Low-voltage detection level select register	LVIS	R/W	√	√	–	0EH Note 4
FFFABH	Watchdog timer enable register	WDTE	R/W	–	√	–	1A/9A Note 5
FFFACH	Temperature correction table H	TTBLH	R	–	–	√	**Note 6**
FFFADH							
FFFAEH	Temperature correction table L	TTBLL	R	–	–	√	**Note 6**
FFFAFH							

Notes 1. The value of this register is 00H if the AMPH bit (bit 0 of the CMC register) is set to 1 after reset.

2. The reset value of RESF varies depending on the reset source.

3. The reset value of LVIM varies depending on the reset source and the setting of the option byte.

4. The reset value of LVIS varies depending on the reset source.

5. The reset value of WDTE is determined by the setting of the option byte.

6. The values of these registers differ depending on the product.

Table 5-1. SFR List (4/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
FFFB0H	DMA SFR address register 0	DSA0		R/W	–	√	–	00H
FFFB1H	DMA SFR address register 1	DSA1		R/W	–	√	–	00H
FFFB2H	DMA RAM address register 0L	DRA0L	DRA0	R/W	–	√	√	00H
FFFB3H	DMA RAM address register 0H	DRA0H		R/W	–	√		00H
FFFB4H	DMA RAM address register 1L	DRA1L	DRA1	R/W	–	√	√	00H
FFFB5H	DMA RAM address register 1H	DRA1H		R/W	–	√		00H
FFFB6H	DMA byte count register 0L	DBC0L	DBC0	R/W	–	√	√	00H
FFFB7H	DMA byte count register 0H	DBC0H		R/W	–	√		00H
FFFB8H	DMA byte count register 1L	DBC1L	DBC1	R/W	–	√	√	00H
FFFB9H	DMA byte count register 1H	DBC1H		R/W	–	√		00H
FFFBAH	DMA mode control register 0	DMC0		R/W	√	√	–	00H
FFFBBH	DMA mode control register 1	DMC1		R/W	√	√	–	00H
FFFBCH	DMA operation control register 0	DRC0		R/W	√	√	–	00H
FFFBDH	DMA operation control register 1	DRC1		R/W	√	√	–	00H
FFFBEH	Back ground event control register	BECTL		R/W	√	√	–	00H
FFFBFH	BCD correction carry register	– Note		R	√	–	–	0
FFFD0H	Interrupt request flag register 2L	IF2L	IF2	R/W	√	√	√	00H
FFFD1H	Interrupt request flag register 2H	IF2H		R/W	√	√		00H
FFFD4H	Interrupt mask flag register 2L	MK2L	MK2	R/W	√	√	√	FFH
FFFD5H	Interrupt mask flag register 2H	MK2H		R/W	√	√		FFH
FFFD8H	Priority specification flag register 02L	PR02L	PR02	R/W	√	√	√	FFH
FFFD9H	Priority specification flag register 02H	PR02H		R/W	√	√		FFH
FFFDCH	Priority specification flag register 12L	PR12L	PR12	R/W	√	√	√	FFH
FFFDDH	Priority specification flag register 12H	PR12H		R/W	√	√		FFH
FFFE0H	Interrupt request flag register 0L	IF0L	IF0	R/W	√	√	√	00H
FFFE1H	Interrupt request flag register 0H	IF0H		R/W	√	√		00H
FFFE2H	Interrupt request flag register 1L	IF1L	IF1	R/W	√	√	√	00H
FFFE3H	Interrupt request flag register 1H	IF1H		R/W	√	√		00H
FFFE4H	Interrupt mask flag register 0L	MK0L	MK0	R/W	√	√	√	FFH
FFFE5H	Interrupt mask flag register 0H	MK0H		R/W	√	√		FFH
FFFE6H	Interrupt mask flag register 1L	MK1L	MK1	R/W	√	√	√	FFH
FFFE7H	Interrupt mask flag register 1H	MK1H		R/W	√	√		FFH
FFFE8H	Priority specification flag register 00L	PR00L	PR00	R/W	√	√	√	FFH
FFFE9H	Priority specification flag register 00H	PR00H		R/W	√	√		FFH
FFFEAH	Priority specification flag register 01L	PR01L	PR01	R/W	√	√	√	FFH
FFFEBH	Priority specification flag register 01H	PR01H		R/W	√	√		FFH
FFFECH	Priority specification flag register 10L	PR10L	PR10	R/W	√	√	√	FFH
FFFEDH	Priority specification flag register 10H	PR10H		R/W	√	√		FFH
FFFEEH	Priority specification flag register 11L	PR11L	PR11	R/W	√	√	√	FFH
FFFEFH	Priority specification flag register 11H	PR11H		R/W	√	√		FFH

Note This register can be manipulated only in 1-bit units. Therefore, no symbol is applied as an 8-bit register.

Table 5-1. SFR List (5/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
FFFF0H	Multiplication input data register A	MULA	R/W	–	–	√	0000H
FFFF1H							
FFFF2H	Multiplication input data register B	MULB	R/W	–	–	√	0000H
FFFF3H							
FFFF4H	Higher multiplication result storage register	MULOH	R	–	–	√	0000H
FFFF5H							
FFFF6H	Lower multiplication result storage register	MULOL	R	–	–	√	0000H
FFFF7H							
FFFFEH	Processor mode control register	PMC	R/W	√	√	–	00H

Remark For extended SFRs (2nd SFRs), see **Table 6-1 Extended SFR (2nd SFR) List**.

6. EXTENDED SPECIAL FUNCTION REGISTERS (2nd SFRs: 2nd Special Function Registers)

Unlike a general-purpose register, each extended SFR (2nd SFR) has a special function.

Extended SFRs are allocated to the F0000H to F07FFH area. SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

Extended SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (!addr16.bit). This manipulation can also be specified with an address.
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (!addr16). This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (!addr16). When specifying an address, describe an even address.

Table 6-1 gives a list of the extended SFRs (2nd SFRs). The meanings of items in the table are as follows.

- Symbol
  Symbol indicating the address of an extended SFR. It is a reserved word in the RA78K0R, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0R. When using the RA78K0R, debugger, and simulator, symbols can be written as an instruction operand.
- R/W
  Indicates whether the corresponding extended SFR can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulable bit units
  "√" indicates the manipulable bit unit (1, 8, or 16). "–" indicates a bit unit for which manipulation is not possible.
- After reset
  Indicates each register status upon reset signal generation.

Remark For SFRs in the SFR area, see **5. SPECIAL FUNCTION REGISTERS (SFRs)**.

Table 6-1. Extended SFR (2nd SFR) List (1/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F0017H	A/D port configuration register	ADPC		R/W	–	√	–	10H
F0030H	Pull-up resistor option register 0	PU0		R/W	√	√	–	00H
F0031H	Pull-up resistor option register 1	PU1		R/W	√	√	–	00H
F0033H	Pull-up resistor option register 3	PU3		R/W	√	√	–	00H
F0034H	Pull-up resistor option register 4	PU4		R/W	√	√	–	00H
F0035H	Pull-up resistor option register 5	PU5		R/W	√	√	–	00H
F0037H	Pull-up resistor option register 7	PU7		R/W	√	√	–	00H
F003CH	Pull-up resistor option register 12	PU12		R/W	√	√	–	00H
F003EH	Pull-up resistor option register 14	PU14		R/W	√	√	–	00H
F0040H	Port input mode register 0	PIM0		R/W	√	√	–	00H
F0050H	Port output mode register 0	POM0		R/W	√	√	–	00H
F0060H	Noise filter enable register 0	NFEN0		R/W	√	√	–	00H
F0061H	Noise filter enable register 1	NFEN1		R/W	√	√	–	00H
F00F0H	Peripheral enable register 0	PER0		R/W	√	√	–	00H
F00F2H	Internal high-speed oscillator trimming register	HIOTRM		R/W	–	√	–	10H
F00F3H	Operation speed mode control register	OSMC		R/W	–	√	–	00H
F00F4H	Regulator mode control register	RMC		R/W	–	√	–	00H
F00FEH	BCD adjust result register	BCDADJ		R	–	√	–	00H
F0100H	Serial status register 00	SSR00L	SSR00	R	–	√	√	0000H
F0101H		–			–	–		
F0102H	Serial status register 01	SSR01L	SSR01	R	–	√	√	0000H
F0103H		–			–	–		
F0104H	Serial status register 02	SSR02L	SSR02	R	–	√	√	0000H
F0105H		–			–	–		
F0106H	Serial status register 03	SSR03L	SSR03	R	–	√	√	0000H
F0107H		–			–	–		
F0108H	Serial flag clear trigger register 00	SIR00L	SIR00	R/W	–	√	√	0000H
F0109H		–			–	–		
F010AH	Serial flag clear trigger register 01	SIR01L	SIR01	R/W	–	√	√	0000H
F010BH		–			–	–		
F010CH	Serial flag clear trigger register 02	SIR02L	SIR02	R/W	–	√	√	0000H
F010DH		–			–	–		
F010EH	Serial flag clear trigger register 03	SIR03L	SIR03	R/W	–	√	√	0000H
F010FH		–			–	–		
F0110H	Serial mode register 00	SMR00		R/W	–	–	√	0020H
F0111H								
F0112H	Serial mode register 01	SMR01		R/W	–	–	√	0020H
F0113H								
F0114H	Serial mode register 02	SMR02		R/W	–	–	√	0020H
F0115H								
F0116H	Serial mode register 03	SMR03		R/W	–	–	√	0020H
F0117H								

Table 6-1. Extended SFR (2nd SFR) List (2/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F0118H	Serial communication operation setting register 00	SCR00		R/W	–	–	√	0087H
F0119H								
F011AH	Serial communication operation setting register 01	SCR01		R/W	–	–	√	0087H
F011BH								
F011CH	Serial communication operation setting register 02	SCR02		R/W	–	–	√	0087H
F011DH								
F011EH	Serial communication operation setting register 03	SCR03		R/W	–	–	√	0087H
F011FH								
F0120H	Serial channel enable status register 0	SE0L	SE0	R	√	√	√	0000H
F0121H		–			–	–		
F0122H	Serial channel start register 0	SS0L	SS0	R/W	√	√	√	0000H
F0123H		–			–	–		
F0124H	Serial channel stop register 0	ST0L	ST0	R/W	√	√	√	0000H
F0125H		–			–	–		
F0126H	Serial clock select register 0	SPS0L	SPS0	R/W	–	√	√	0000H
F0127H		–			–	–		
F0128H	Serial output register 0	SO0		R/W	–	–	√	0F0FH
F0129H								
F012AH	Serial output enable register 0	SOE0L	SOE0	R/W	√	√	√	0000H
F012BH		–			–	–		
F0134H	Serial output level register 0	SOL0L	SOL0	R/W	–	√	√	0000H
F0135H		–			–	–		
F0144H	Serial status register 12	SSR12L						
F0145H		–						

Table 6-1. Extended SFR (2nd SFR) List (4/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F01A0H	Timer status register 00	TSR00L	TSR00	R	–	√	√	0000H
F01A1H		–			–	–		
F01A2H	Timer status register 01	TSR01L	TSR01	R	–	√	√	0000H
F01A3H		–			–	–		
F01A4H	Timer status register 02	TSR02L	TSR02	R	–	√	√	0000H
F01A5H		–			–	–		
F01A6H	Timer status register 03	TSR03L	TSR03	R	–	√	√	0000H
F01A7H		–			–	–		
F01A8H	Timer status register 04	TSR04L	TSR04	R	–	√	√	0000H
F01A9H		–			–	–		
F01AAH	Timer status register 05	TSR05L	TSR0	R	–	√	√	0000H
F01ABH		–			–	–		
F01ACH	Timer status register 06	TSR06L	TSR06	R	–	√	√	0000H
F01ADH		–			–	–		
F01AEH	Timer status register 07	TSR07L	TSR07	R	–	√	√	0000H
F01AFH		–			–	–		
F01B0H	Timer channel enable status register 0	TE0L	TE0	R	√	√	√	0000H
F01B1H		–			–	–		
F01B2H	Timer channel start register 0	TS0L	TS0	R/W	√	√	√	0000H
F01B3H		–			–	–		
F01B4H	Timer channel stop register 0	TT0L	TT0	R/W	√	√	√	0000H
F01B5H		–			–	–		
F01B6H	Timer clock select register 0	TPS0L	TPS0	R/W	–	√	√	0000H
F01B7H		–			–	–		
F01B8H	Timer output register 0	TO0L	TO0	R/W	–	√	√	0000H
F01B9H		–			–	–		
F01BAH	Timer output enable register 0	TOE0L	TOE0	R/W	√	√	√	0000H
F01BBH		–			–	–		
F01BCH	Timer output level register 0	TOL0L	TOL0	R/W	–	√	√	0000H
F01BDH		–			–	–		
F01BEH	Timer output mode register 0	TOM0L	TOM0	R/W	–	√	√	0000H
F01BFH		–			–	–		

Remark For SFRs in the SFR area, see **Table 5-1 SFR List**.

7. PERIPHERAL HARDWARE FUNCTIONS

7.1 Ports

The following four types of I/O ports are available.

- CMOS input (Port 12 (P121 to P124)): 4
- CMOS output (Port 13): 1
- CMOS I/O (Port 0, Port 1, Port 2, Port 3, Port 4, Port 5, Port 7, Port 12 (P120), Port 14): 46
- N-ch open-drain I/O (Port 6): 4

Total: 55

Table 7-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P06	I/O port. Input of P03 and P04 can be set to TTL buffer. Output of P02 to P04 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.
Port 1	P10 to P17	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.
Port 2	P20 to P27	I/O port. Input/output can be specified in 1-bit units.
Port 3	P30, P31	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.
Port 4	P40 to P43	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.
Port 5	P50 to P55	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.
Port 6	P60 to P63	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.
Port 7	P70 to P77	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.
Port 12	P120 to P124	I/O port and input port. Input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.
Port 13	P130	Output port.
Port 14	P140, P141	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.

7.2 Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.
The following three kinds of system clocks and clock oscillators are selectable.

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of f_X = 2 to 20 MHz by connecting a resonator to X1 and X2.

<2> High-speed internal oscillator

This circuit oscillates a clock of f_{IH} = 8 MHz (TYP.). After a reset release, the CPU always starts operating with this internal high-speed oscillation clock.

An external main system clock (f_{EX} = 2 to 20 MHz) can also be supplied from the EXCLK/X2/P122 pin.

(2) Subsystem clock

- XT1 oscillator

This circuit oscillates a clock of f_{SUB} = 32.768 kHz by connecting a 32.768 kHz resonator across XT1 and XT2.

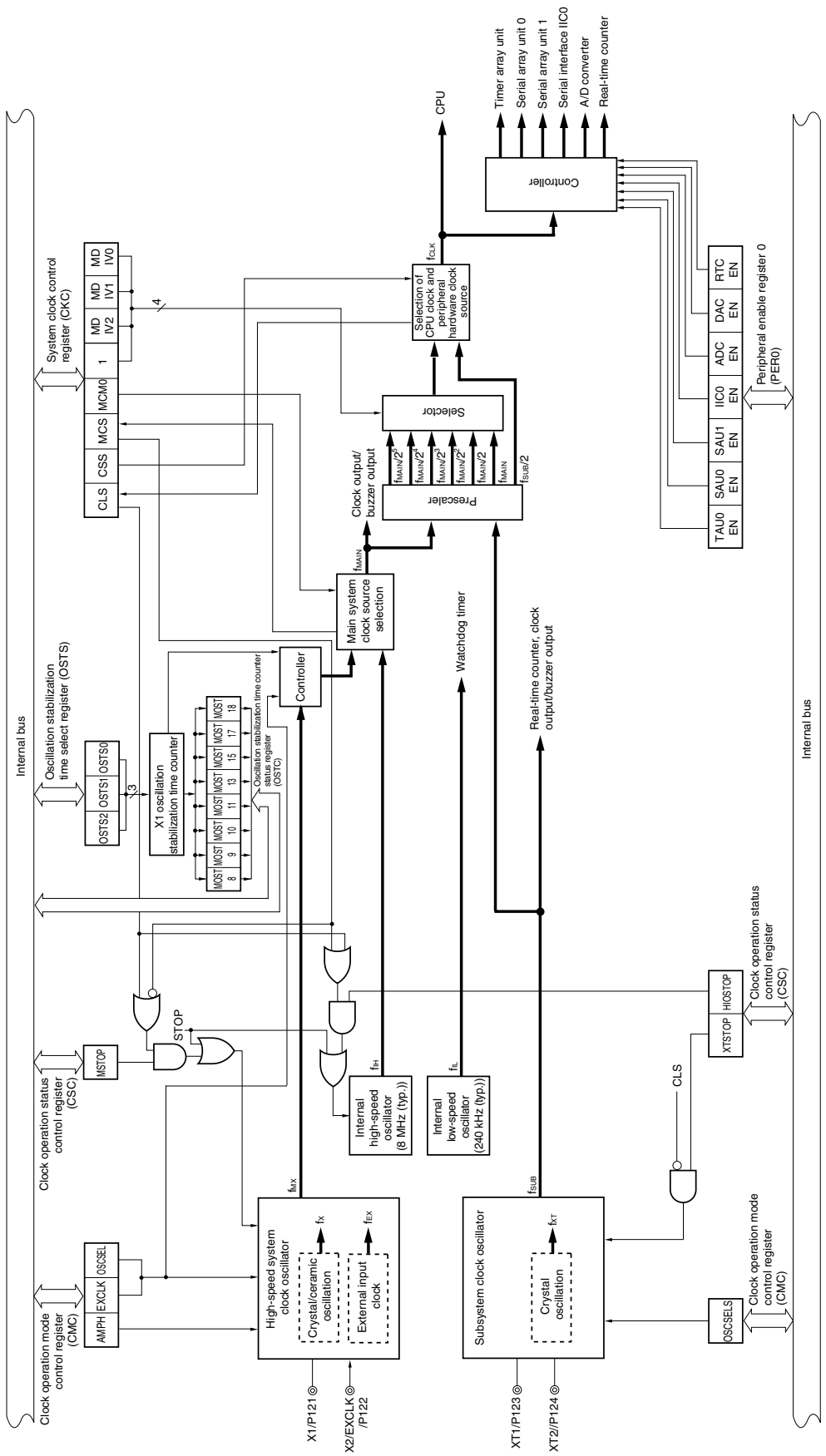
(3) Internal low-speed oscillation clock (clock for watchdog timer)

- Internal low-speed oscillator

This circuit oscillates a clock of f_{IL} = 240 kHz (TYP.). After a reset release, the internal low-speed oscillation clock operation is determined by setting the option byte.
The internal low-speed oscillation clock cannot be used as the CPU clock.

Remark f_X: X1 clock oscillation frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{EX}: External main system clock frequency
f_{SUB}: Subsystem clock frequency

Figure 7-1. Block Diagram of Clock Generator



The clock generator uses the following nine types of registers.

(1) Clock operation mode control register (CMC)
This register selects whether the X1 and X2 pins, and XT1 and XT2 pins are used to connect an oscillator or as input port pins.

(2) Clock operation status control register (CSC)
This register is used to set an operation mode of a clock source (except the internal low-speed oscillation clock).

(3) Oscillation stabilization time counter status register (OSTC)
This register indicates the counting status of the oscillation stabilization time counter of the X1 clock.
The X1 clock oscillation stabilization time can be checked in the following case,

- If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating.

(4) Oscillation stabilization time select register (OSTS)
This register is used to select the oscillation stabilization time of the X1 clock when the STOP mode is released.
If the X1 clock is selected as the CPU clock, the microcontroller waits for the time set by the OSTS.
If the internal high-speed oscillation clock is selected as the CPU clock, check if the oscillation stabilization time set by the OSTC register passes after the STOP mode is released. The time set by OSTS in advance can be checked with OSTC.

(5) System clock control register (CKC)
This register is used to select the system clock source and check the select state.

(6) Peripheral enable registers 0 (PER0)
These registers are used to control the peripheral macro clock.

(7) Operation speed mode control register (OSMC)
This register is used to control the step-up circuit of the flash memory for high-speed operation.
If the microcontroller operates at a low speed with a system clock of 10 MHz or less, the power consumption can be lowered by setting this register to the default value, 00H.

(8) Internal high-speed oscillator trimming register (HIOTRM)
This register is used to adjust the accuracy of the internal high-speed oscillator.
Temperature is measured by using the internal temperature sensor and A/D converter in combination, and a correction value calculated from the measured temperature is set to this register.

(9) Temperature correction tables H and L (TTBLH and TTBLL)
These registers store constants that are used to calculate a correction value to which the internal high-speed oscillator is adjusted depending on the temperature.
Values suitable for each product are written to these tables as a factory-set condition of the product (these registers can only be read after the product is shipped).

7.3 Timer Array Unit (TAU)

The timer array unit has eight 16-bit timers per unit. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more “channels” can be used to create a high-accuracy timer.

Independent Operation Function	Combination Operation Function
• Interval timer • Square wave output • External event counter • Divider function • Input pulse interval measurement • Measurement of high-/low-level width of input signal	• PWM output • One-shot pulse output • PWM output

Channel 7 can be used to realize LIN-bus reception processing in combination with UART3 of serial array unit 1.

7.3.1 Functional outline of timer array unit

<Functions of each channel when it operates independently>

Independent operation functions are those functions that can be used for any channel regardless of the operation mode of the other channel.

(1) Interval timer

Each timer of a unit can be used as a reference timer that generates an interrupt (INTTM0n) at fixed intervals.

(2) Square wave output

A toggle operation is performed each time INTTM0n is generated and a square wave with a duty factor of 50% is output from a timer output pin (TO0n).

(3) External event counter

Each timer of a unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TI0n) has reached a specific value.

(4) Divider function

A clock input from a timer input pin (TI0n) is divided and output from an output pin (TO0n).

(5) Input pulse interval measurement

Counting is started by the valid edge of a pulse signal input to a timer input pin (TI0n). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.

(6) Measurement of high-/low-level width of input signal

Counting is started by a single edge of the signal input to the timer input pin (TI0n), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured.

Remark n: Channel number (n = 0 to 7)

<Functions of each channel when it operates with another channel>

Combination operation functions are those functions that are attained by using the master channel (mostly the reference timer that controls cycles) and the slave channels (timers that operate following the master channel) in combination.

(1) PWM (Pulse Width Modulator) output
Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.

(2) One-shot pulse output
Two channels are used as a set to generate a one-shot pulse with a specified delay time and a specified pulse width.

(3) Multiple PWM (Pulse Width Modulator) output
By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.

<LIN-bus supporting function (channel 7 only)>

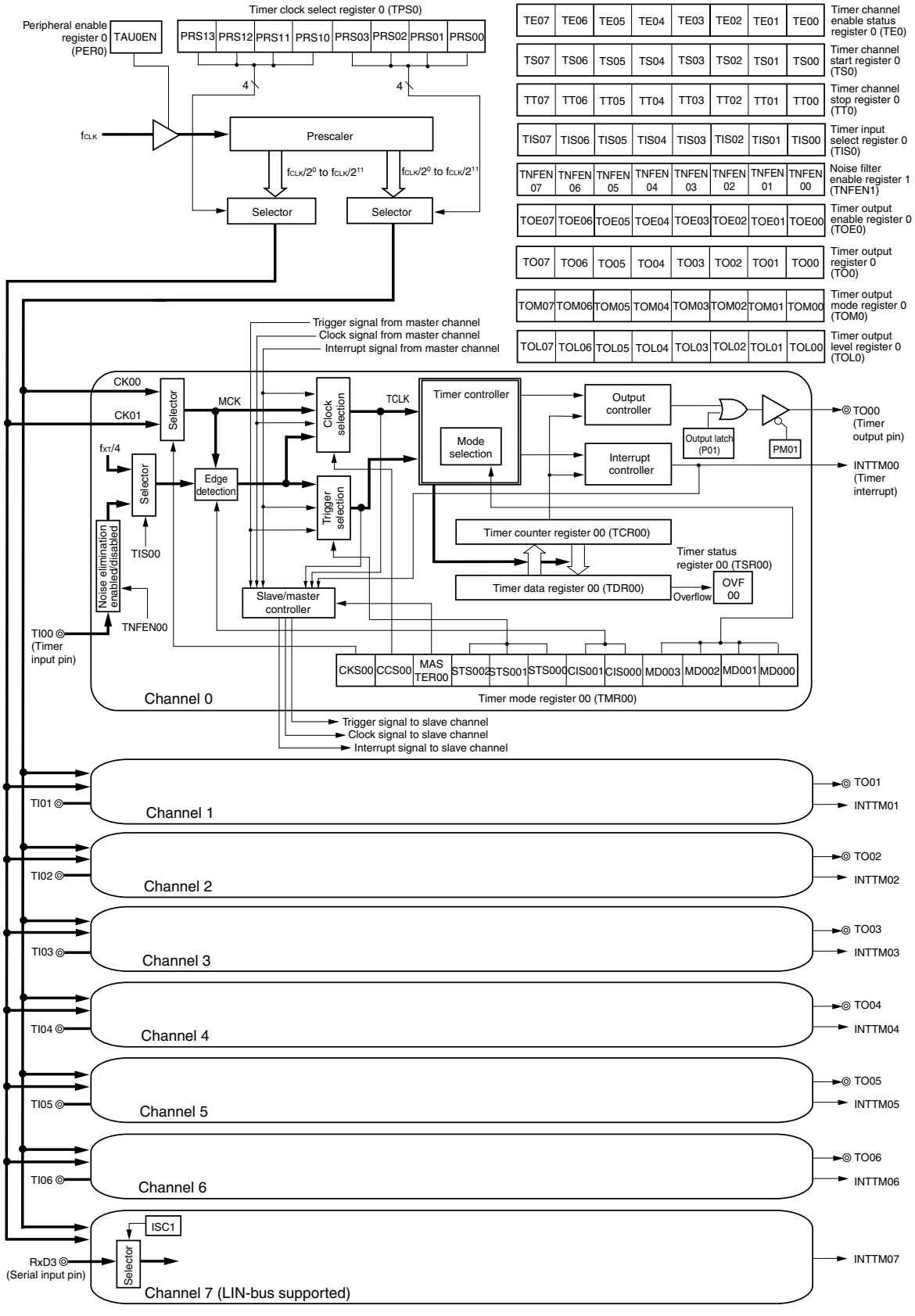
(1) Detection of wakeup signal
The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD3) of UART3 and the count value of the timer is captured at the rising edge. In this way, a low-level width can be measured. If the low-level width is greater than a specific value, it is recognized as a wakeup signal.

(2) Detection of sync break field
The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD3) of UART3 after a wakeup signal is detected, and the count value of the timer is captured at the rising edge. In this way, a low-level width is measured. If the low-level width is greater than a specific value, it is recognized as a sync break field.

(3) Measurement of pulse width of sync field
After a sync break field is detected, the low-level width and high-level width of the signal input to the serial data input pin (RxD3) of UART3 are measured. From the bit interval of the sync field measured in this way, a baud rate is calculated.

7.3.2 Timer array unit configuration

Figure 7-2. Block Diagram of Timer Array Unit



The timer array unit consists of the following registers.

<Registers of unit setting block>

(1) Peripheral enable register 0 (PER0)
Bit 0 of this register enables or stops operation of the timer array unit. The default value of this bit is set to stop the operation of the timer array unit.

(2) Timer clock select register 0 (TPS0)
This register is used to set a division ratio of the CK0 and CK1 clocks when they are generated, by dividing the peripheral hardware clock. The CK00 and CK01 clocks are commonly supplied to channels 0 to 7 of each unit.

(3) Timer channel enable status register 0 (TE0)
This register is used to enable or stop the timer operation of each channel.

(4) Timer channel start register 0 (TS0)
This is a trigger register that is used to clear a timer counter (TCR0n) and start the counting operation of each channel.

(5) Timer channel stop register 0 (TT0)
This is a trigger register that stops the counting operation of each channel.

(6) Timer input select register 0 (TIS0)
This register is used to select the input signal of a timer input pin (TI0n) or subsystem clock divided by 4 ($f_{XT}/4$) for each channel.

(7) Noise filter enable register 1 (NFEN1)
This register is used to set whether the noise filter can be used for the timer input signal to each channel.

(8) Timer output enable register 0 (TOE0)
This register is used to enable or stop the timer output of each channel.

(9) Timer output register 0 (TO0)
This is a buffer register of timer output. The value of each bit in this register is output from the timer output pin (TO0n) of each channel.

(10) Timer output level register 0 (TOL0)
TOL0 is a register that controls the timer output level of each channel.
The setting of the inverted output of channel n by this register is reflected at the timing of set or reset of the timer output signal while the timer output is enabled (TOE0n = 1) in the combination operation mode (TOM0n = 1).

(11) Timer output mode register 0 (TOM0)
This register is used to set an output mode of timer output (toggle operation or combination operation) for each channel.

<Registers of each channel> n: Channel number (n = 0 to 7)

(1) Timer data register 0n (TDR0n)
This is the data register of channel n. In the interval timer mode, it functions as a compare register (that sets an interval period). In the capture mode, it functions as a capture register (that stores a captured value).

(2) Timer counter register 0n (TCR0n)
This is the counter register of channel n. It counts down in the interval timer mode and counts up in the capture mode.

(3) Timer mode register 0n (TMR0n)
This register sets an operation mode of channel n. It is used to select an operating clock (MCK), a count clock, whether the timer operates as the master or a slave, a start trigger and a capture trigger, the valid edge of the timer input, and an operation mode (interval, capture, event counter, one-count, or capture & one-count).

(4) Timer status register 0n (TSR0n)
This register indicates the overflow status of the timer/counter of channel n.

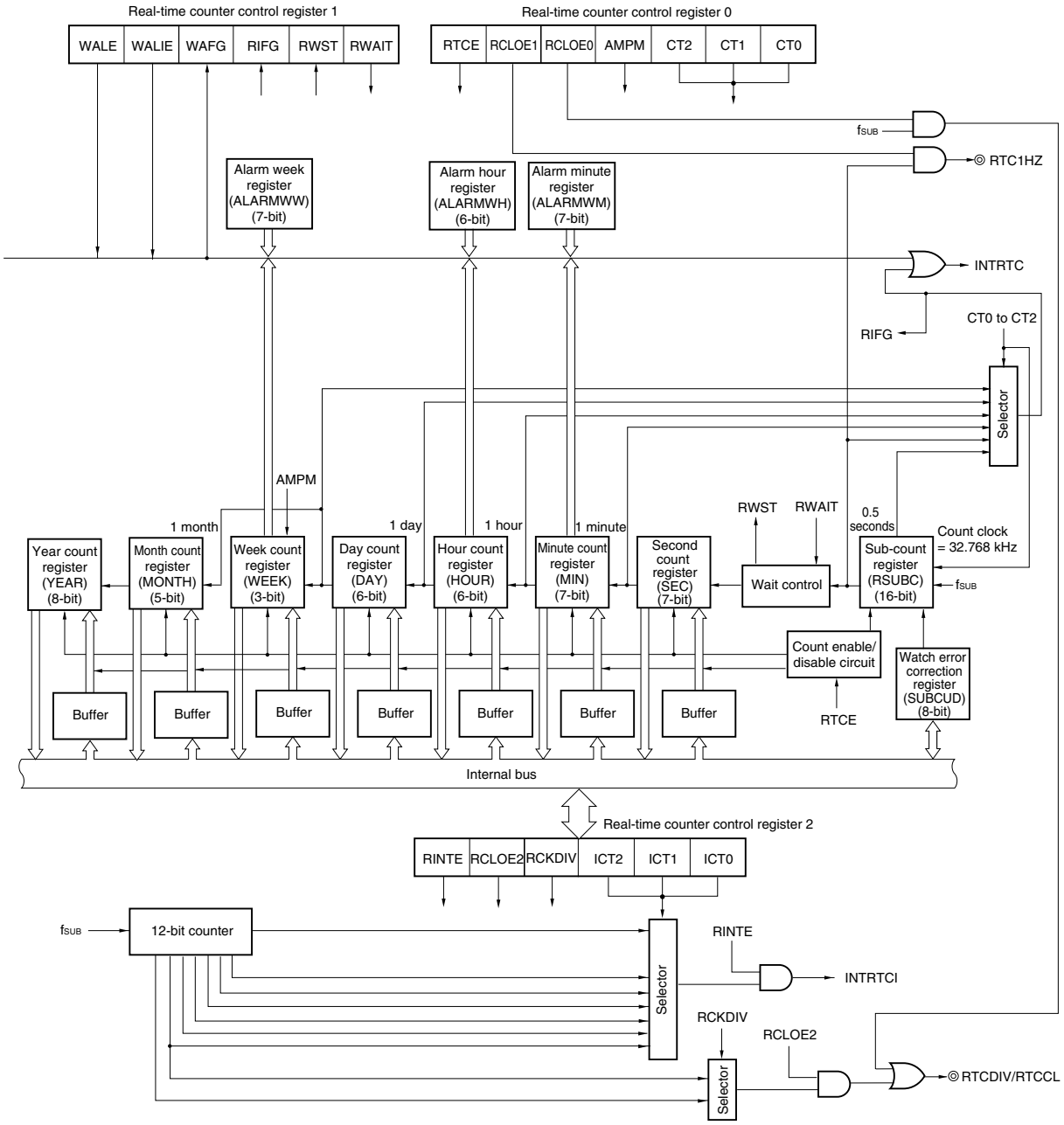
(5) Input switch control register (ISC) (channel 7 only)
This register is used to change the timer input signal of channel 7 to a signal input from the serial input pin (RxD3) of UART3. It is used to realize LIN-bus communication in combination with the serial array unit (SAU).

7.4 Real-Time Counter

The real-time counter has the following features.

- Having counters of year, month, week, day, hour, minute, and second, and can count up to 99 years.
- Constant-period interrupt function (period: 1 month to 0.5 seconds)
- Alarm interrupt function (alarm: week, hour, minute)
- Interval interrupt function
- Pin output function of 1 Hz
- Pin output function of 512 Hz, 16.384 kHz or 32 kHz

Figure 7-3. Block Diagram of Real-Time Counter



Remark f_{SUB}: Subclock frequency

The following registers control the real-time counter.

(1) Peripheral enable register 0 (PER0)

Bit 7 of this register is used to enable or stop operation of the real-time counter. The default value of this bit is set to stop the operation of the real-time counter.

(2) Real-time counter control register 0 (RTCC0)

The RTCC0 register is an 8-bit register that is used to start or stop the real-time counter operation, control the RTCCL and RTC1HZ pins, and set a 12- or 24-hour system and the constant-period interrupt function.

(3) Real-time counter control register 1 (RTCC1)

The RTCC1 register is an 8-bit register that is used to control the alarm interrupt function and the wait time of the counter.

(4) Real-time counter control register 2 (RTCC2)

The RTCC2 register is an 8-bit register that is used to control the interval interrupt function and the RTCDIV pin.

(5) Sub-count register (RSUBC)

The RSUBC register is a 16-bit register that counts the reference time of 1 second of the real-time counter. It takes a value of 0H to 7FFFH and counts 1 second with a clock of 32.768 kHz.

(6) Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds. It counts up when the sub-counter overflows.

(7) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes. It counts up when the second counter overflows.

(8) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 0 to 23 or 0 to 11 (decimal) and indicates the count value of hours. It counts up when the minute counter overflows.

(9) Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days. It counts up when the hour counter overflows.

(10) Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of dates. It counts up in synchronization with the day counter.

(11) Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months. It counts up when the day counter overflows.

(12) Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years. It counts up when the month counter overflows.

(13) Watch error correction register (SUBCUD)

This register is used to correct the count value of the sub-count register (RSUBC).

(14) Alarm minute register (ALARMWM)

This register is used to set minutes of alarm.

(15) Alarm hour register (ALARMWH)

This register is used to set hours of alarm.

(16) Alarm week register (ALARMWW)

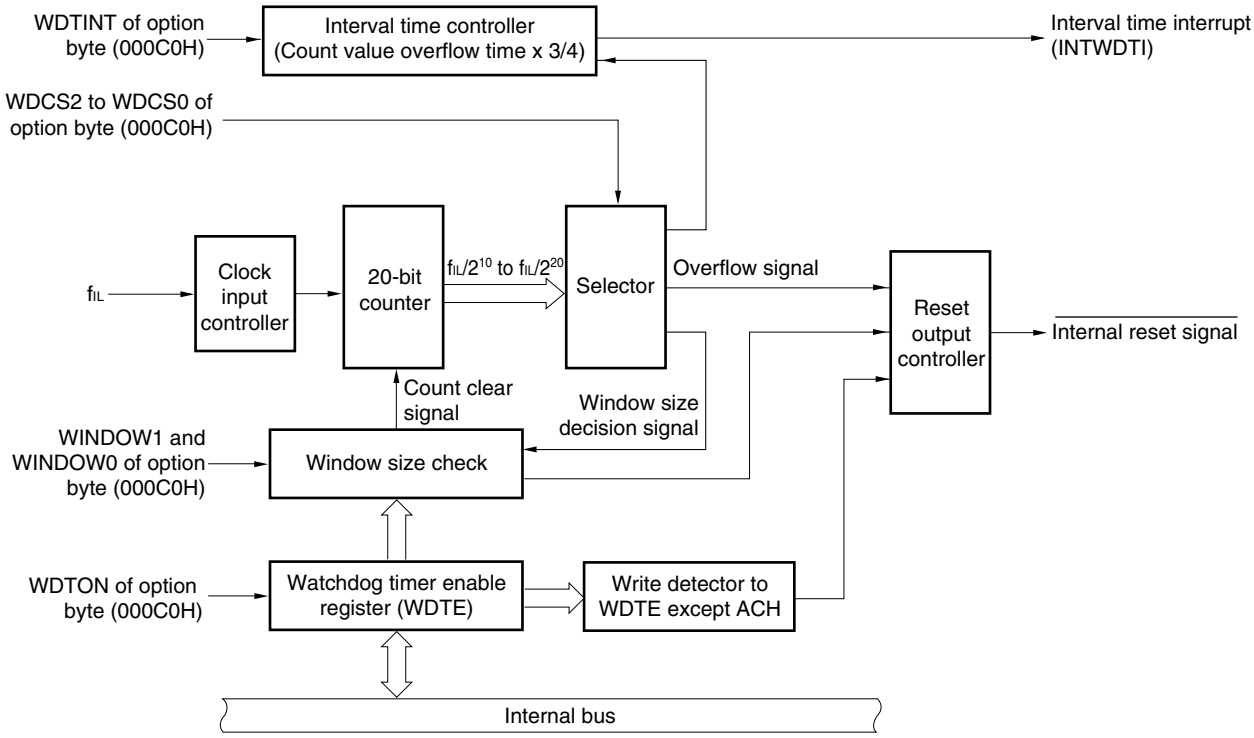
This register is used to set date of alarm.

7.5 Watchdog Timer

The watchdog timer operates on the internal low-speed oscillation clock.

The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

Figure 7-4. Block Diagram of Watchdog Timer



The watchdog timer uses the following register.

(1) Watchdog timer enable register (WDTE)

This register is used to control the operation of the watchdog timer/counter.

7.6 Clock Output/Buzzer Output Controller

The clock output controller is intended for carrier output during remote controlled transmission and clock output for supply to peripheral ICs.

Buzzer output is a function to output a square wave of buzzer frequency.

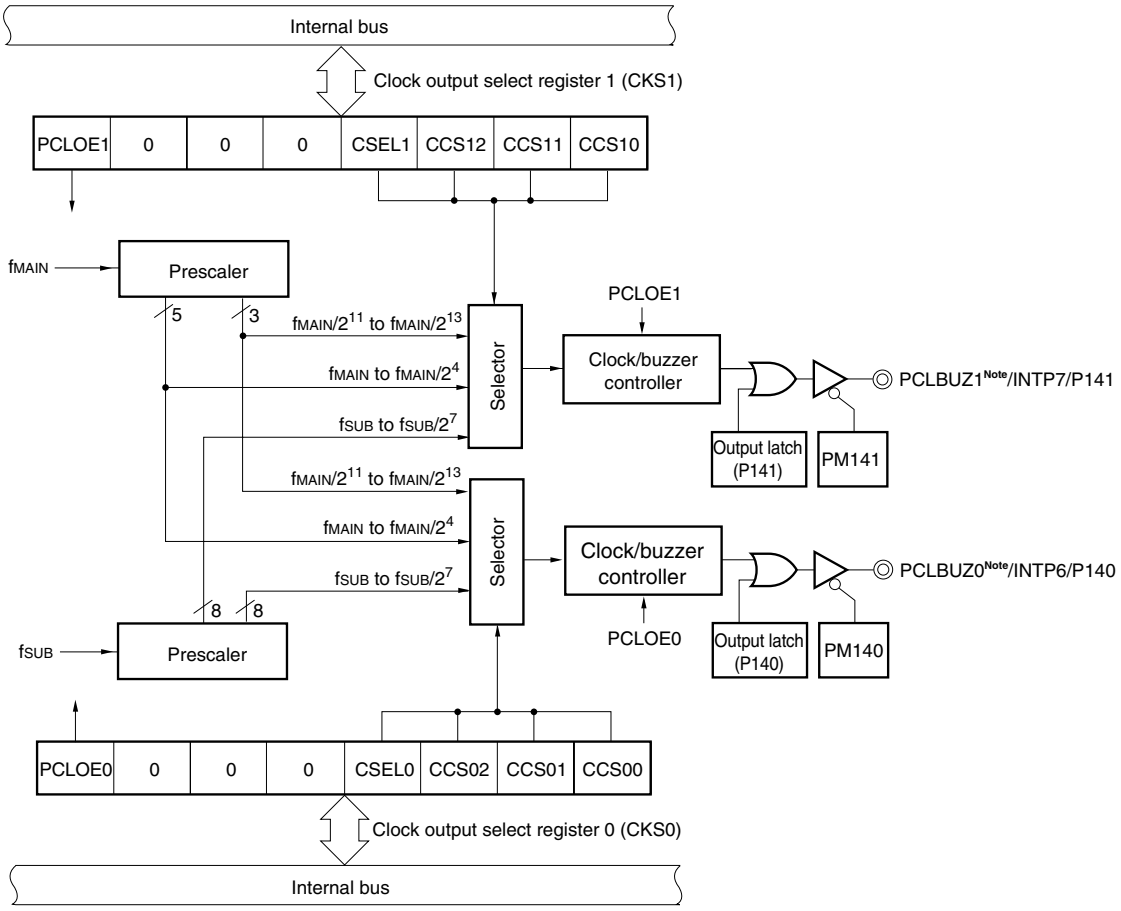
One pin can be used to output a clock or buzzer sound.

Two output pins, PCLBUZ0 and PCLBUZ1, are available.

PCLBUZ0 outputs a clock selected by clock output select register 0 (CKS0).

PCLBUZ1 outputs a clock selected by clock output select register 1 (CKS1).

Figure 7-5. Block Diagram of Clock Output/Buzzer Output Controller



Note The PCLBUZ0 and PCLBUZ1 pins can output a clock of up to 10 MHz at 2.7 V ≤ V_{DD}. Setting a clock exceeding 5 MHz at V_{DD} < 2.7 V is prohibited.

The clock output/buzzer output controller uses the following two types of registers.

(1) Clock output select register 0 (CKS0)

This register is used to enable or disable clock output or output of the pin that outputs a buzzer frequency (PCLBUZ0), and set an output clock.

(2) Clock output select register 1 (CKS1)

This register is used to enable or disable clock output or output of the pin that outputs a buzzer frequency (PCLBUZ1), and set an output clock.

7.7 A/D Converter

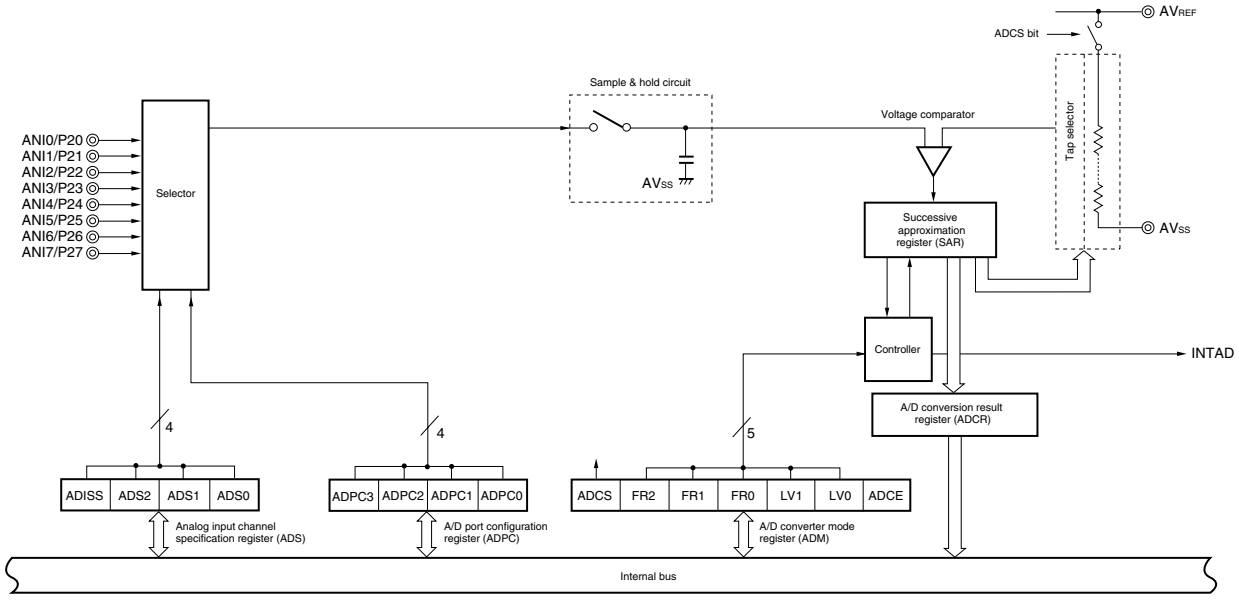
The A/D converter converts an analog input signal into a digital value, and consists of up to 8 channels (ANI0 to ANI7) with a resolution of 10 bits.

The A/D converter has the following function.

- 10-bit resolution A/D conversion

  10-bit resolution A/D conversion is carried out repeatedly for one analog input channel selected from ANI0 to ANI7. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated.

Figure 7-6. Block Diagram of A/D Converter



The A/D converter uses the following seven types of registers.

(1) Peripheral enable register 0 (PER0)
Bit 5 of this register is used to enable or stop operation of the A/D converter. The default value of this bit is set to stop operation of the A/D converter.

(2) A/D converter mode register (ADM)
This register is used to set conversion time of an input analog signal to be converted, and to start or stop the conversion operation.

(3) 10-bit A/D conversion result register (ADCR)
Each time A/D conversion has been completed, the conversion result is loaded from the successive approximation register to this register that holds the A/D conversion result at the higher 10 bits (the lower 6 bits are fixed to 0).

(4) 8-bit A/D conversion result register (ADCRH)
Each time A/D conversion has been completed, the conversion result is loaded from the successive approximation register to this register that stores the A/D conversion result in the higher 8 bits.

(5) Analog input channel specification register (ADS)
This register is used to specify a port that inputs an analog voltage to be converted.

(6) A/D port configuration register (ADPC)
This register is used to set the ANI0/P20 to ANI7/P27 pins in the analog input mode of the A/D converter or digital I/O mode of the ports.

(7) Port mode registers 2 (PM2)
These registers are used to set the ANI0/P20 to ANI7/P27 pins in the input or output mode.

7.8 Serial Array Unit (SAU)

The serial array unit has four serial channels per unit and can use two or more of various serial interfaces (three-wire serial (CSI), UART, and simplified IIC) in combination.

Function assignment of each channel supported by the 78K0R/KE3 is as shown below (channels 2 and 3 of unit 1 are dedicated to UART3 (supporting LIN-bus)).

Unit	Channel	Used as CSI	Used as UART	Used as Simplified IIC
0	0	CSI00	UART0	–
	1	–		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	–	–	–
	1	–	–	–
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–

(Example of combination) When “UART1” is used for channels 2 and 3 of unit 0, CSI10 and IIC10 cannot be used, but CSI00 or UART0 can be used.

7.8.1 Functional outline of serial array unit

Each serial interface supported by the 78K0R/KE3 has the following features.

(1) Three-wire serial (CSI)

This is a clocked communication function that uses three lines: serial clock (SCK) and serial data (SI and SO) lines.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

(2) UART

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. It transmits or receives data in asynchronization with the party of communication (by using an internal baud rate). Full-duplex UART communication can be realized by using two channels, one dedicated to transmission (even channel) and the other to reception (odd channel).

[Data transmission/reception]

-

7.8.2 Serial array unit configuration

Figure 7-7. Block Diagram of Serial Array Unit 0

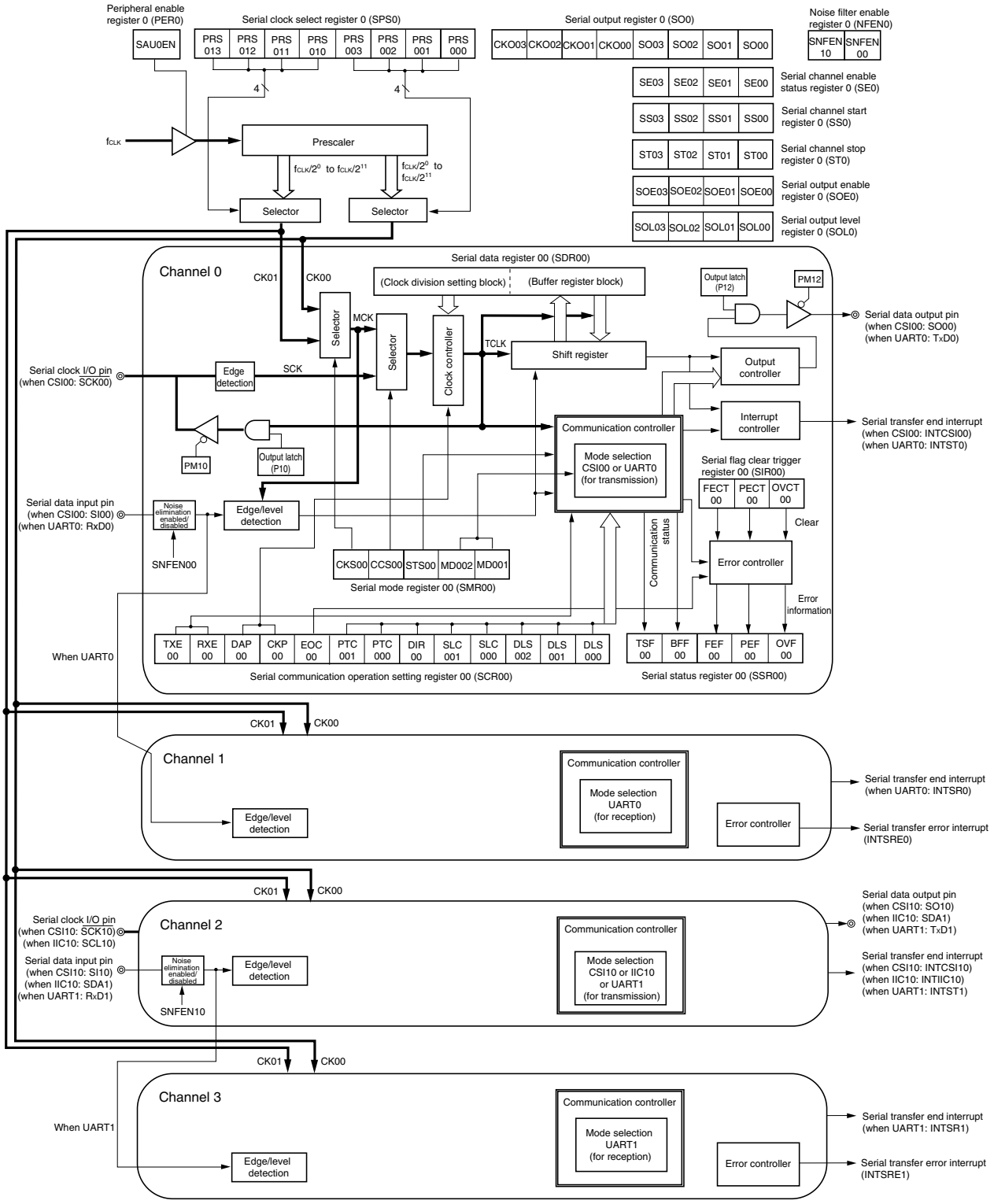
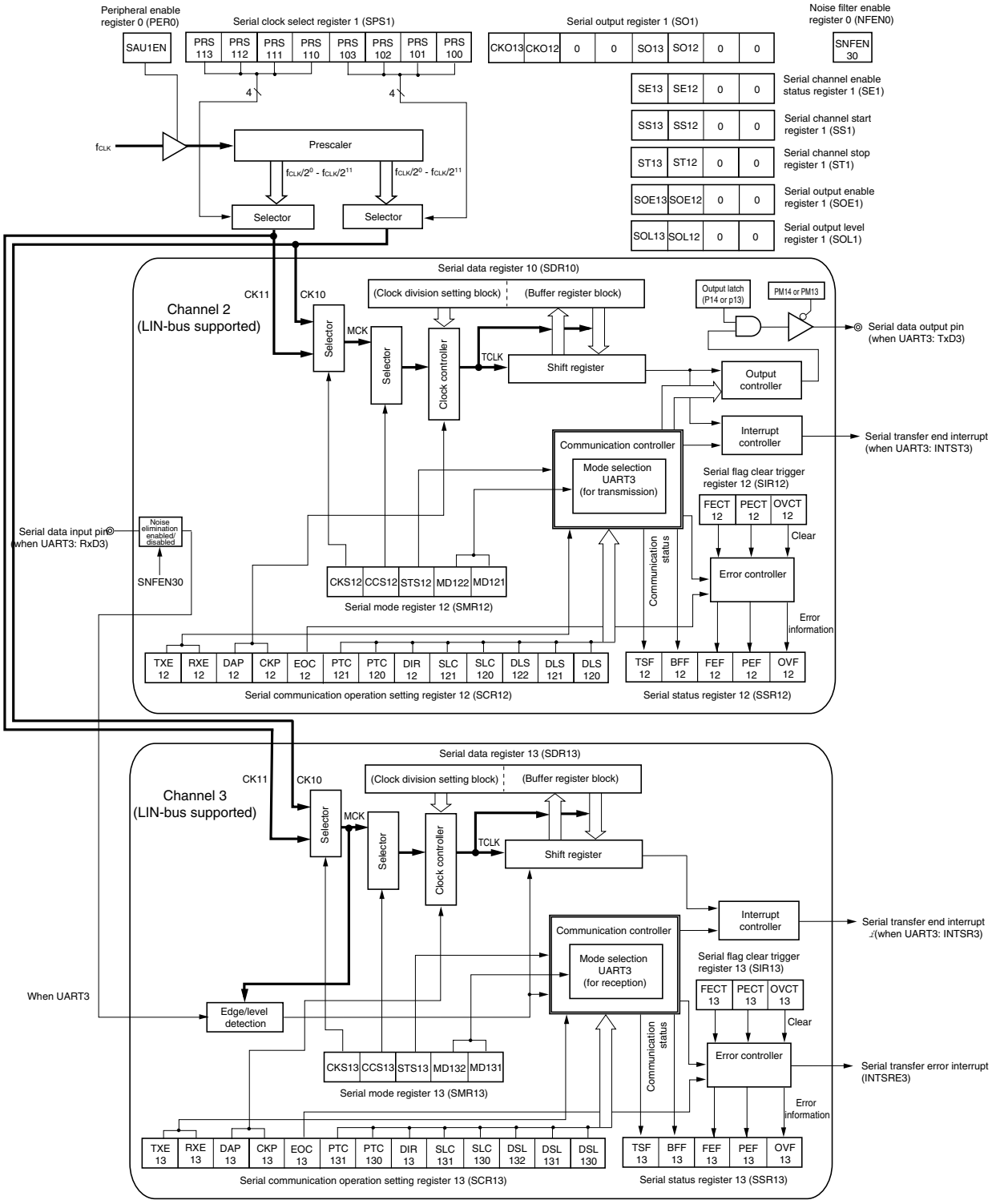


Figure 7-8. Block Diagram of Serial Array Unit 1



The serial array unit consists of the following registers.

<Registers of unit> m: Unit number (m = 0, 1)

(1) Peripheral enable register 0 (PER0)
Bit 2 of this register enables or stops the operation of serial array unit 0, and bit 3 enables or stops the operation of serial array unit 1. By default, both the units are stopped from operating.

(2) Serial clock select register m (SPSm)
This register is used to set the division ratio of CK0 clock and CK1 clock that are generated by dividing the peripheral hardware clock. The CK0 and CK1 clocks are supplied to all channels 0 to 3 of the unit.

(3) Serial channel enable status register m (SEm)
This register indicates whether data transmission/reception operation of each channel is enabled or stopped.

(4) Serial channel start register m (SSm)
This is a trigger register that is used to clear the shift register and start transmission/reception of data by each channel.

(5) Serial channel stop register m (STm)
This is a trigger register that is used to stop the shift register and stop data transmission/reception by each channel.

(6) Serial output enable register m (SOEm)
This register is used to enable or stop output of serial data by each channel.

(7) Serial output register m (SOm)
This is a buffer register of serial clock output and serial data output. The value of this register is output from the serial clock output pin and serial data output pin of each channel.

(8) Noise filter enable register 0 (NFEN0)
This register is used to set whether the noise filter can be used for the serial data input signal to each channel.

7.9 Serial Interface IIC0

Serial interface IIC0 has the following two modes.

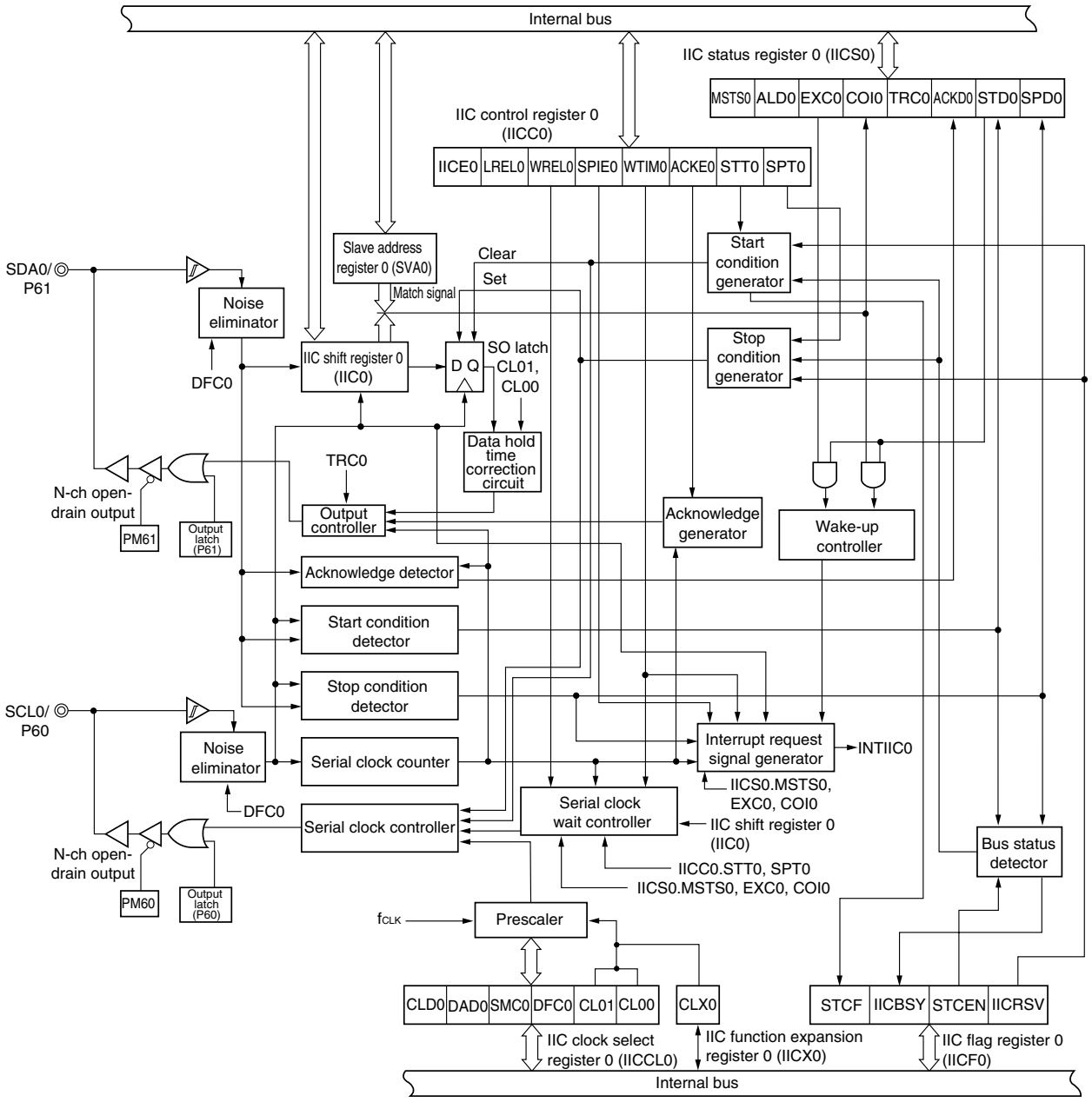
(1) Operation stop mode

This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

(2) I^2C bus mode (multimaster supported)

This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCL0) line and a serial data bus (SDA0) line.

Figure 7-9. Block Diagram of Serial Interface IIC0



Serial interface IIC0 consists of the following hardware units.

(1) Peripheral enable register 0 (PER0)
Bit 4 of this register is used to enable or stop operation of serial interface IIC0. The default value of this bit is set to stop the operation of serial interface IIC0.

(2) IIC shift register 0 (IIC0)
IIC0 is a register that converts 8-bit serial data into 8-bit parallel data or vice versa in synchronization with the serial clock. This register is used for both transmission and reception.

(3) Slave address register 0 (SVA0)
This register stores the source address when the microcontroller is used as a slave.

(4) IIC control register 0 (IICC0)
This register is used to enable or stop the operation of I^2C, set wait timing, and the other operations of I^2C.

(5) IIC status register 0 (IICS0)
This register indicates the status of I^2C.

(6) IIC flag register 0 (IICF0)
This register is used to set an operation mode of I^2C and indicate the status of the I^2C bus.

(7) IIC clock select register 0 (IICCL0)
This register is used to set the transfer clock of I^2C.

(8) IIC function expansion register 0 (IICX0)
This register is used to set the function expansion of I^2C.

(9) Port mode register 6 (PM6)
This register is used to set port 6 in the input or output mode in 1-bit units.

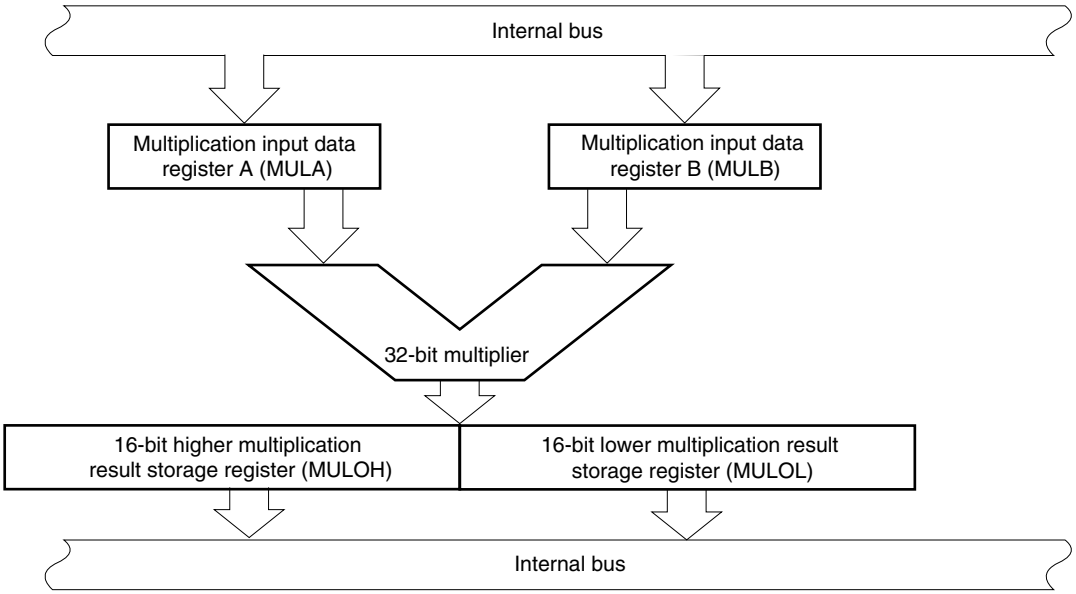
7.10 Multiplier

The multiplier executes an operation of 16 bits × 16 bits with one clock.

It has the following features.

- Can execute calculation of 16 bits × 16 bits = 32 bits.

Figure 7-10. Block Diagram of Multiplier



The multiplier uses the following four registers.

(1) 16-bit higher multiplication result storage register and 16-bit lower multiplication result storage register (MULOH and MULOL)

These two registers, MULOH and MULOL, are used to store a 32-bit multiplication result. The higher 16 bits of the multiplication result are stored in MULOH and the lower 16 bits, in MULOL, so that a total of 32 bits of the multiplication result can be stored.

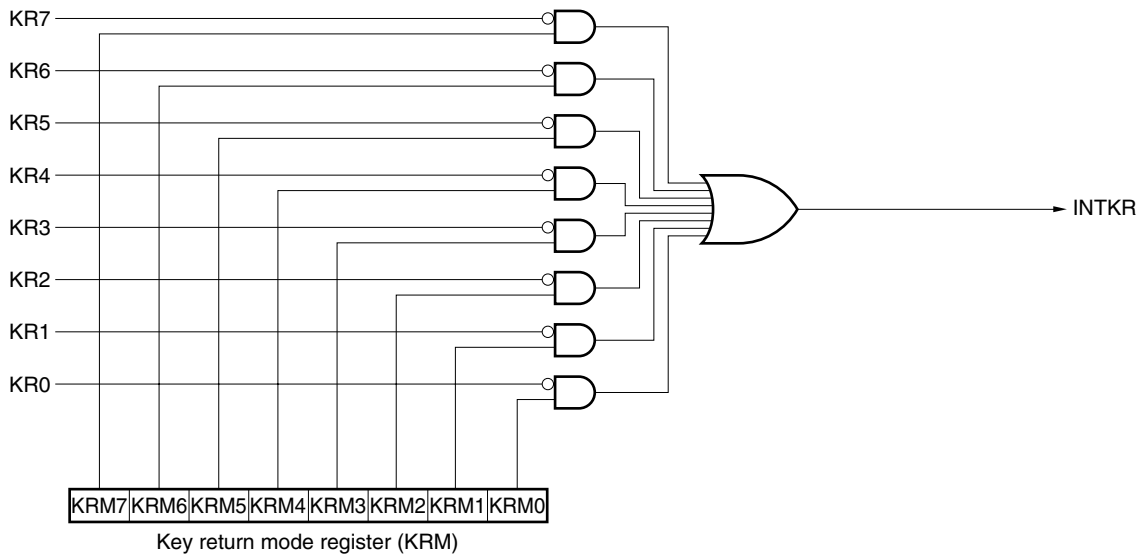
(2) Multiplication input data registers A and B (MULA and MULB)

These are 16-bit registers that store data for multiplication. The multiplier multiplies the values of MULA and MULB.

7.11 Key Return Signal Detector

A key interrupt (INTKR) can be generated by inputting the falling edge to key interrupt input pins (KR0 to KR7), depending on the setting of key return mode register (KRM).

Figure 7-11. Block Diagram of Key Return Signal Detector



The key interrupt function uses the following register.

(1) Key return mode register (KRM)

This register is used to enable or disable the key input signals of the KR0 to KR7 pins by the corresponding bits, KRM0 to KRM7.

7.12 Power-on-Clear (POC) Circuit

The power-on-clear circuit (POC) has the following functions.

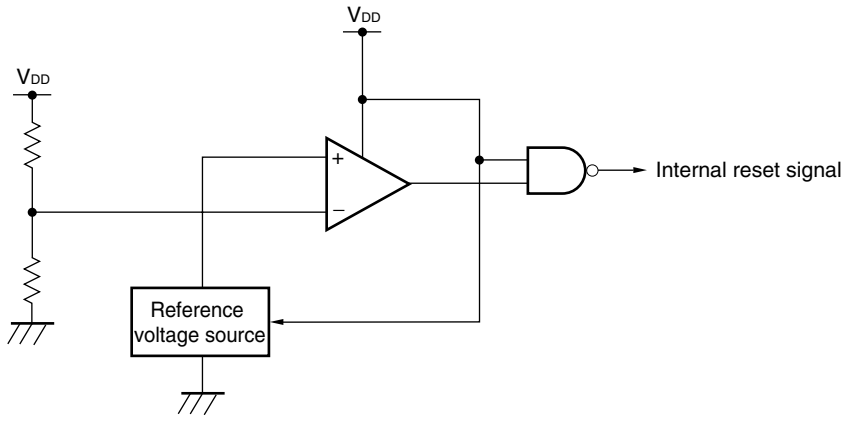
- Generates internal reset signal at power on.
  The reset signal is released if the supply voltage (V_{DD}) exceeds 1.59 V ±0.09 V[Note].

  Caution If the low-voltage detector (LVI) is set to ON by an option byte by default, the reset signal is not released until the supply voltage (V_{DD}) exceeds 2.07 V ±0.2 V[Note].

- Compares supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.09 V[Note]), generates internal reset signal when $V_{DD} < V_{POC}$.

  Note These are preliminary values and subject to change.

Figure 7-12. Block Diagram of Power-on-Clear Circuit



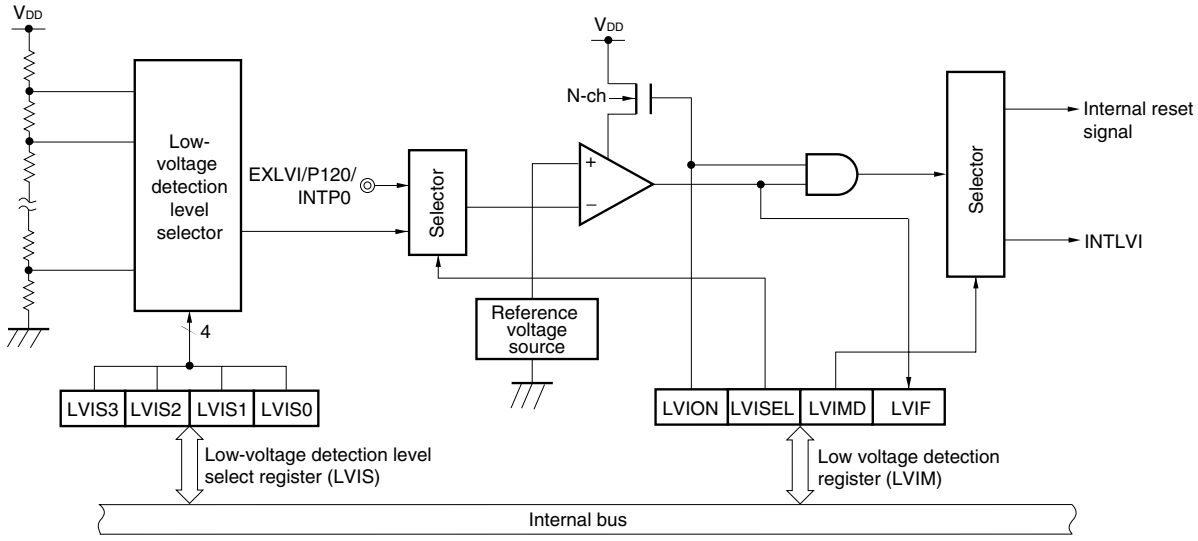
7.13 Low-Voltage Detector (LVI)

The low-voltage detector (LVI) has the following functions.

- The LVI circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVI}) or the input voltage from an external input pin (EXLVI) with the detection voltage (V_{EXLVI} = 1.21 V ±0.1 V[Note]), and generates an internal reset or internal interrupt signal.
- The low-voltage detector (LVI) can be set to ON by an option byte by default. If it is set to ON to raise the power supply from the POC detection voltage or lower, the internal reset signal is generated when the supply voltage (V_{DD}) < detection voltage (V_{LVI} = 2.07 V ±0.2 V[Note]). After that, the internal reset signal is generated when the supply voltage (V_{DD}) < detection voltage (V_{LVI} = 2.07 V ±0.1 V[Note]).
- The supply voltage (V_{DD}) or the input voltage from the external input pin (EXLVI) can be selected to be detected by software.
- A reset or an interrupt can be selected to be generated after detection by software.
- Detection levels (16 levels) of supply voltage can be changed by software.
- Operable in STOP mode.

Note These are preliminary values and subject to change.

Figure 7-13. Block Diagram of Low-Voltage Detector



The low-voltage detector is controlled by the following registers.

(1) Low-voltage detection register (LVIM)
This register sets low-voltage detection and the operation mode.

(2) Low-voltage detection level select register (LVIS)
This register selects the low-voltage detection level.

(3) Port mode register 12 (PM12)
When using the P120/EXLVI/INTP0 pin for external low-voltage detection potential input, set PM120 to 1. At this time, the output latch of P120 may be 0 or 1.

7.14 DMA Controller

The 78K0R/KE3 has an internal DMA (Direct Memory Access) controller.

Data can be automatically transferred between the peripheral hardware supporting DMA, SFRs, and internal RAM without via CPU.

As a result, the normal internal operation of the CPU and data transfer can be executed in parallel with transfer between the SFR and internal RAM, and therefore, a large capacity of data can be processed. In addition, real-time control using communication, timer, and A/D can also be realized.

- ○ Number of DMA channels: 2
- ○ Transfer unit: 8 or 16 bits
- ○ Maximum transfer unit: 1024 times
- ○ Transfer type: 2-cycle transfer (One transfer is processed in 2 clocks and the CPU stops during that processing.)
- ○ Transfer mode: Single-transfer mode
- ○ Transfer request: Selectable from the following peripheral hardware interrupts
  - A/D converter
  - Serial interface (CIS00, CSI10, UART0, UART1, UART3, or IIC10)
  - Timer (channel 0, 1, 4, or 5)
- ○ Subject to transfer: Between SFR and internal RAM

Here are examples of functions using DMA.

- Successive transfer of serial interface
- Batch transfer of analog data
- Capturing A/D conversion result at fixed interval
- Capturing port value at fixed interval

8. INTERRUPT FUNCTION

A total of 42 interrupt sources are provided, divided into the following two types.

- Maskable interrupt: 38
- Software interrupt: 1

Table 8-1. Interrupt Source List (1/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	0	INTWDTI	Watchdog timer interval[Note 3] (75% of overflow time)	Internal	0004H	(A)
	1	INTLVI	Low-voltage detection[Note 4]		0006H	
	2	INTP0	Pin input edge detection	External	0008H	(B)
	3	INTP1			000AH	
	4	INTP2			000CH	
	5	INTP3			000EH	
	6	INTP4			0010H	
	7	INTP5			0012H	
	8	INTST3	End of UART3 transmission	Internal	0014H	(A)
	9	INTSR3	End of UART3 reception		0016H	
	10	INTSRE3	UART3 communication error occurrence		0018H	
	11	INTDMA0	End of DMA0 transfer		001AH	
	12	INTDMA1	End of DMA1 transfer		001CH	
	13	INTST0 /INTCSI00	End of UART0 transmission/end of CSI00 communication		001EH	
	14	INTSR0	End of UART0 reception		0020H	
	15	INTSRE0	CSI00/UART0 communication error occurrence		0022H	
	16	INTST1 /INTCSI10 /INTIIC10	End of UART1 transmission/end of CSI10 communication/end of IIC10 communication		0024H	
	17	INTSR1	End of UART1 reception		0026H	
	18	INTSRE1	CSI10/UART1/IIC1 communication error occurrence		0028H	
	19	INTIIC0	End of IIC0 communication		002AH	

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 37 indicates the lowest priority.

2. Basic configuration types (A) to (C) correspond to (A) to (C) in Figure 8-1.

3. When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.

4. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is cleared to 0.

Table 8-1. Interrupt Source List (2/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	20	INTTM00	End of timer channel 0 count or capture	Internal	002CH	(A)
	21	INTTM01	End of timer channel 1 count or capture		002EH	
	22	INTTM02	End of timer channel 2 count or capture		0030H	
	23	INTTM03	End of timer channel 3 count or capture		0032H	
	24	INTAD	End of A/D conversion		0034H	
	25	INTRTC	Fixed-cycle signal of real-time counter/alarm match detection		0036H	
	26	INTRTCI	Interval signal detection of real-time counter		0038H	
	27	INTKR	Key return signal detection	External	003AH	(B)
	28	INTTM04	End of timer channel 4 count or capture		0042H	(A)
	29	INTTM05	End of timer channel 5 count or capture		0044H	
	30	INTTM06	End of timer channel 6 count or capture		0046H	
	31	INTTM07	End of timer channel 7 count or capture		0048H	
	32	INTP6	Pin input edge detection	External	004AH	(B)
	33	INTP7			004CH	
	34	INTP8			004EH	
	35	INTP9			0050H	
	36	INTP10			0052H	
	37	INTP11			0054H	
Software	–	BRK	Execution of BRK instruction	–	007EH	(C)
Reset	–	RESET	$\overline{\text{RESET}}$ pin input	–	0000H	–
		POC	Power-on-clear			
		LVI	Low-voltage detection[Note 3]			
		WDT	Overflow of watchdog timer			
		TRAP	Execution of illegal instruction[Note 4]			

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 37 indicates the lowest priority.

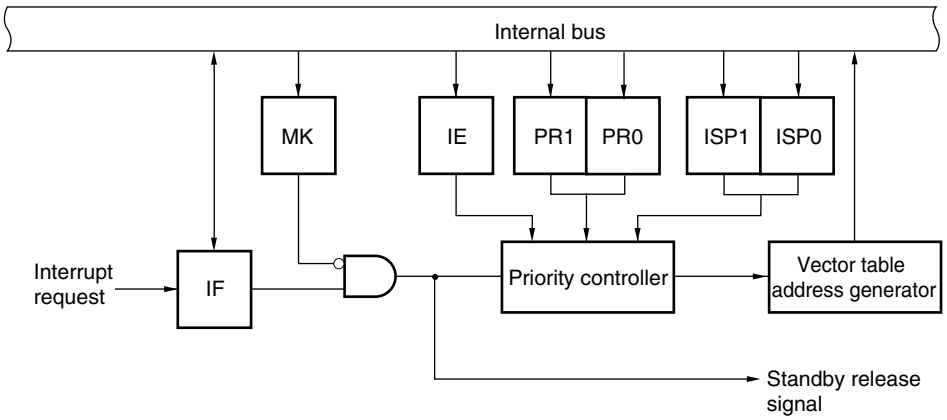
2. Basic configuration types (A) to (C) correspond to (A) to (C) in Figure 8-1.

3. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is set to 1.

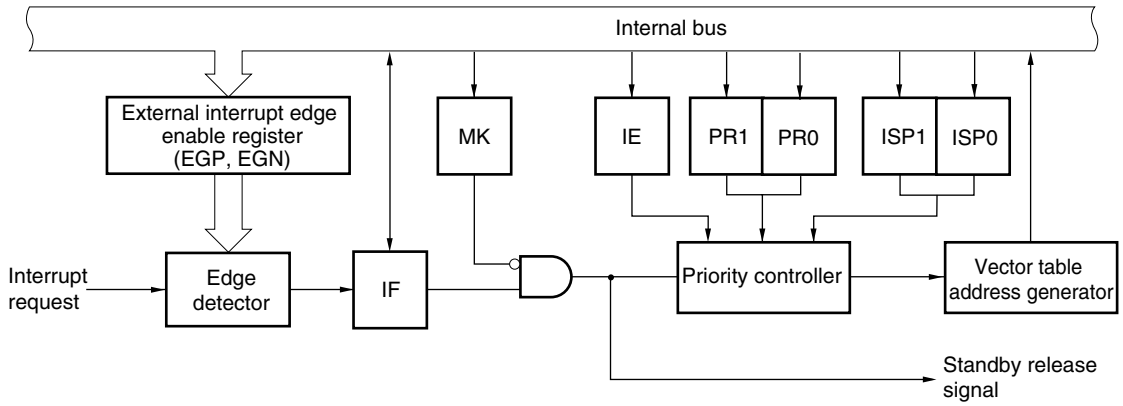
4. When the instruction code in FFH is executed.
Reset by the illegal instruction execution cannot be emulated by the in-circuit emulator or on-chip debug emulator.

Figure 8-1. Basic Configuration of Interrupt Function

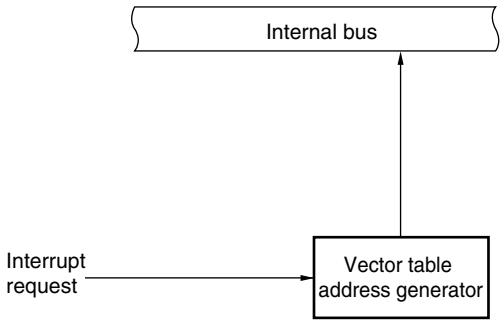
(A) Internal maskable interrupt



(B) External maskable interrupt



(C) Software interrupt



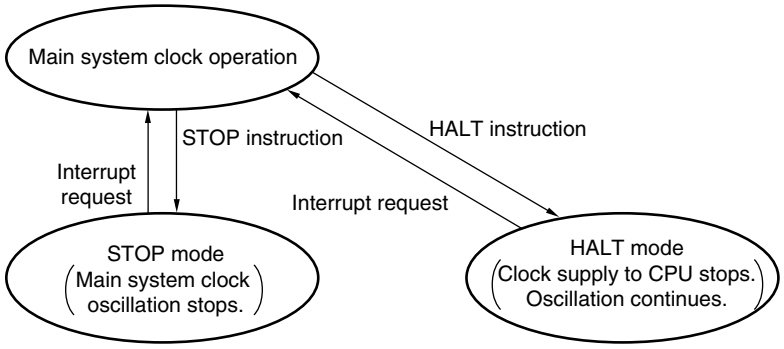
IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

9. STANDBY FUNCTION

The standby function is designed to reduce the operating current of the system. The following two modes are available.

- HALT mode: Stops the operating clock of the CPU. By using this mode in combination with the normal operation mode for intermittent operation, the average current consumption can be decreased.
- STOP mode: Stops oscillation of the main system clock. All operations using the main system clock are stopped, so that the power consumption can be reduced more than in the HALT mode.

Figure 9-1. Standby Function



The standby function uses the following two types of registers.

(1) Oscillation stabilization time counter status register (OSTC)

This register indicates the counting status of the oscillation stabilization time counter of the X1 clock.

The X1 clock oscillation stabilization time can be checked in the following case,

- If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating.

(2) Oscillation stabilization time select register (OSTS)

This register is used to select the oscillation stabilization time of the X1 clock when the STOP mode is released.

If the X1 clock is selected as the CPU clock, the CPU waits for the time set by OSTS after the STOP mode is released.

If the internal high-speed oscillation clock is selected as the CPU clock, confirm that the oscillation stabilization time has elapsed after the STOP mode was released, by using OSTC. OSTC can be used to check the time set in advance by OSTS.

10. RESET FUNCTION

The microcontroller is reset in the following five ways.

- External reset input via $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer program loop detection
- Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit
- Internal reset by comparison of supply voltage and detection voltage of low-power-supply detector (LVI)
- Internal reset by execution of illegal instruction[Note]

Note When instruction code FFH is executed
Reset by the illegal instruction execution cannot be emulated by the in-circuit emulator or on-chip debug emulator.

11. OPTION BYTES

Addresses 000C0H to 000C3H of the flash memory of the 78K0R/KE3 form an option byte area.

Option bytes consist of user option byte (000C0H to 000C2H) and on-chip debug option byte (000C3H).

Upon power application or resetting and starting, an option byte is automatically referenced and a specified function is set. When using the product, be sure to set the following functions by using the option bytes.

To use the boot swap operation during self programming, 000C0H to 000C3H are replaced by 010C0H to 010C3H. Therefore, set the same values as 000C0H to 000C3H to 010C0H to 010C3H.

Caution Be sure to set FFH to 000C2H (000C2H/010C2H when the boot swap operation is used).

11.1 User option byte (000C0H to 000C2H/010C0H to 010C2H)

(1) 000C0H/010C0H

- ○ Operation of watchdog timer
  - • Operation is stopped or enabled in the HALT or STOP mode.
- ○ Setting of interval time of watchdog timer
- ○ Operation of watchdog timer
  - • Operation is stopped or enabled.
- ○ Setting of window open period of watchdog timer
- ○ Setting of interval interrupt of watchdog timer
  - • Used or not used

Caution Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.

(2) 000C1H/010C1H

- ○ Setting of LVI on power application
  - • LVI is ON or OFF by default upon power application.

Caution Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

(3) 000C2H/010C2H

- ○ Be sure to set FFH, as these addresses are reserved areas.

Caution Set FFH to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

11.2 On-chip debug option byte (000C3H/ 010C3H)

- ○ Control of on-chip debug operation (software)
  - • On-chip debug operation is disabled or enabled.
- ○ Handling of data of flash memory in case of failure in on-chip debug security ID authentication
  - • Data of flash memory is erased or not erased in case of failure in on-chip debug security ID authentication.

Caution Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.

12. ELECTRICAL SPECIFICATIONS (TARGET)

Cautions 1. These specifications show target values, which may change after device evaluation.

2. The 78K0R/KE3 is provided with an on-chip debug function. After using the on-chip debug function, do not use the product for mass production because its reliability cannot be guaranteed from the viewpoint of the limit of the number of times the flash memory can be rewritten.

After the on-chip debug function is used, complaints will not be accepted.

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions		Ratings	Unit
Supply voltage	V_{DD}			−0.5 to +6.5	V
	EV_{DD}			−0.5 to +6.5	V
	V_{SS}			−0.5 to +0.3	V
	EV_{SS}			−0.5 to +0.3	V
	AV_{REF}			−0.5 to V_{DD} +0.3[Note]	V
	AV_{SS}			−0.5 to +0.3	V
Input voltage	V_{I1}	P00 to P06, P10 to P17, P20 to P27, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120 to P124, P130, P140, P141, EXCLK, $\overline{\text{RESET}}$		−0.3 to V_{DD} +0.3[Note]	V
	V_{I2}	P60-P63 (N-ch open-drain)		−0.3 to +6.5	V
Output voltage	V_O			−0.3 to V_{DD} +0.3[Note]	V
Analog input voltage	V_{AN}	ANI0 to ANI7		−0.3 to AV_{REF} +0.3[Note] and −0.3 to V_{DD} +0.3[Note]	V
Output current, high	I_{OH1}	Per pin		−10	mA
		Total of all pins −80 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	−25	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77	−55	mA
	I_{OH2}	Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	mA

Note Must be 6.5 V or lower.

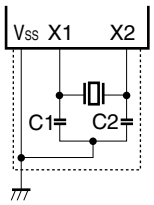
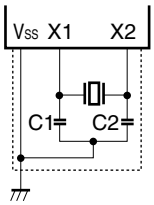
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute Maximum Ratings (T_A = 25°

X1 Oscillator Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		X1 clock oscillation frequency (f_X)[Note]	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	2.0		5.0	
Crystal resonator		X1 clock oscillation frequency (f_X)[Note]	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	2.0		5.0	

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Internal Oscillator Characteristics

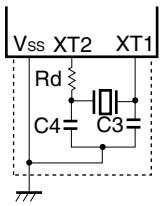
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
8 MHz internal oscillator	Internal high-speed oscillation clock frequency (f_{IH})[Note]	No temperature correction	2.7 V ≤ V_{DD} ≤ 5.5 V	7.6	8.0	8.4	MHz
			1.8 V ≤ V_{DD} < 2.7 V			8.0	MHz
		Temperature correction	2.7 V ≤ V_{DD} ≤ 5.5 V	7.8	8.0	8.2	MHz
			1.8 V ≤ V_{DD} < 2.7 V			8.0	MHz
240 kHz internal oscillator	Internal low-speed oscillation clock frequency (f_{IL})	2.7 V ≤ V_{DD} ≤ 5.5 V			240		kHz
		1.8 V ≤ V_{DD} < 2.7 V			TBD		kHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

XT1 Oscillator Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Items	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT})[Note]			32.768		kHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (1/4)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P120, P130, P131, P140, P141	4.0 V ≤ V_{DD} ≤ 5.5 V			–3.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–1.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–1.0	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141	4.0 V ≤ V_{DD} ≤ 5.5 V			–20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77	4.0 V ≤ V_{DD} ≤ 5.5 V			–30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–19.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–10.0	mA
		Total of all pins	4.0 V ≤ V_{DD} ≤ 5.5 V			–50.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–29.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			–15.0	mA
	I_{OH2}	Per pin for P20 to P27	AV_{REF} = V_{DD}			–0.1	mA
Output current, low[Note 2]	I_{OL1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P120, P130, P140, P141	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.5	mA
		Per pin for P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			3.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			15.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77	4.0 V ≤ V_{DD} ≤ 5.5 V			45.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins	4.0 V ≤ V_{DD} ≤ 5.5 V			65.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			40.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			35.0	mA
	I_{OL2}	Per pin for P20 to P27	AV_{REF} = V_{DD}			0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from V_{DD} to an output pin.

2. Value of current at which the device operation is guaranteed even if the current flows from an output pin to GND.

Caution P02 to P04 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (2/4)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P01, P02, P12, P13, P15, P41, P52 to P55, P121 to P124, P144		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00, P03 to P06, P10, P11, P14, P16, P17, P30, P31, P40, P42, P43, P50, P51, P70 to P77, P140, P141, P145, EXCLK, $\overline{\text{RESET}}$	Normal mode	0.8V_{DD}		V_{DD}	V
	V_{IH3}	P03, P04, P43	TTL mode 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
	V_{IH4}	P20 to P27	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH5}	P60 to P63		0.7V_{DD}		6.0	V
	V_{IH6}	FLMD0		0.9V_{DD} Note 1		V_{DD}	V
Input voltage, low	V_{IL1}	P01, P02, P12, P13, P15, P41, P52 to P55, P121 to P124		0		0.3V_{DD}	V
	V_{IL2}	P00, P03 to P06, P10, P11, P14, P16, P17, P30, P31, P40, P42, P43, P50, P51, P70 to P77, P140, P141, EXCLK, $\overline{\text{RESET}}$	Normal mode	0		0.2V_{DD}	V
	V_{IL3}	P03, P04, P43	TTL mode 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
	V_{IL4}	P20 to P27	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
	V_{IL5}	P60 to P63		0		0.3V_{DD}	V
	V_{IL6}	FLMD0		0		0.1V_{DD} Note 2	V

Notes 1. Must be 0.9V_{DD} or higher when used in the flash memory programming mode.

2. If a 0.1V_{DD} or lower voltage is set, the FLMD0 pin cannot be set to high level even when using an on-chip pull-up resistor.

Cautions 1. The maximum value of V_{IH} of pins P02 to P04 is V_{DD}, even in the N-ch open-drain mode.

2. For P122/EXCLK, V_{IH}/V_{IL} differs according to the input port mode or external clock mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (3/4)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = − 3.0 mA	V_{DD} − 0.7			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = −1.0 mA	V_{DD} − 0.5			V
	V_{OH2}	P20 to P27	AV_{REF} = V_{DD}, I_{OH2} = −100 μA	V_{DD} − 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P130, P140, P141	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.0 mA			0.5	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.5 mA			0.4	V
	V_{OL2}	P20 to P27	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA			0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 2.0 mA			0.4	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (4/4)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P140, P141, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P20 to P27	$V_I = V_{DD} = AV_{REF}$				1	μA
	I_{LIH4}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{DD}$	In Input port			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P140, P141, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{SS}$				−1	μA
	I_{LIL2}	P20 to P27	$V_I = V_{SS}$, $AV_{REF} = V_{DD}$				−1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{SS}$	In Input port			−1	μA
				In resonator connection			−10	μA
Pull-up resistance value	R_{U1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, $\overline{\text{RESET}}$	$V_I = V_{DD}$		10	20	100	kΩ
	R_{U2}	FLMD0	2.7 V ≤ V_{DD} ≤ 5.5 V, $V_I = V_{DD}$		10	20	40	kΩ
			1.8 V ≤ V_{DD} < 2.7 V, $V_I = V_{DD}$		10	20	60	kΩ
Pull-down resistance value	R_D	FLMD0	2.7 V ≤ V_{DD} ≤ 5.5 V, $V_I = V_{SS}$		10	20	40	kΩ
			1.8 V ≤ V_{DD} < 2.7 V, $V_I = V_{SS}$		10	20	60	kΩ
Protection resistance value	R_G	FLMD0			2	4.5	7	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

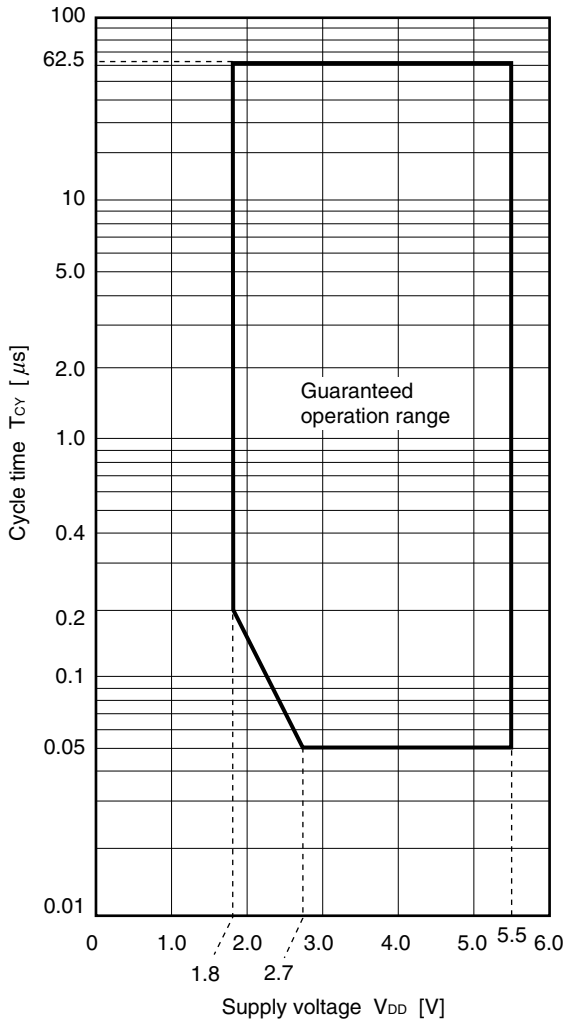
(1) Basic operation

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

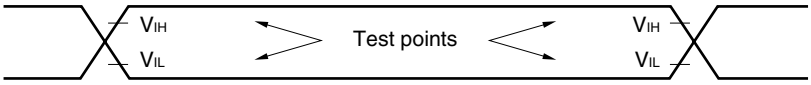
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{XP}) operation	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		8	μs
			1.8 V ≤ V_{DD} < 2.7 V	0.2		8	μs
		Subsystem clock (f_{SUB}) operation		28.5		62.5	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V		2.0		20.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V		2.0		5.0	MHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V		24		250	ns
		1.8 V ≤ V_{DD} < 2.7 V		96		250	ns
TI00 to TI07 input frequency	t_{TI}	2.7 V ≤ V_{DD} ≤ 5.5 V				f_{MCK}/2	MHz
		1.8 V ≤ V_{DD} < 2.7 V				f_{MCK}/2	MHz
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}			2/f_{MCK} -1			ns
TO00 to TO07 output frequency	t_{TO}	2.7 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		1.8 V ≤ V_{DD} < 2.7 V				5	MHz
PCLBUZ0/1 output frequency	t_{PCL}	2.7 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		1.8 V ≤ V_{DD} < 2.7 V				5	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}			1			μs
Key interrupt input low-level width	t_{KR}			250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Remark f_{MCK}: Macro operation clock frequency

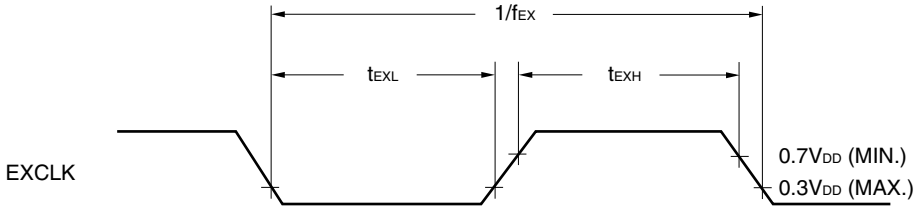
T_{CY} vs. V_{DD} (Main System Clock Operation)



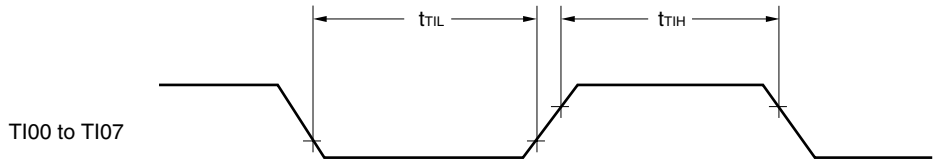
AC Timing Test Points (Excluding External Main System Clock)



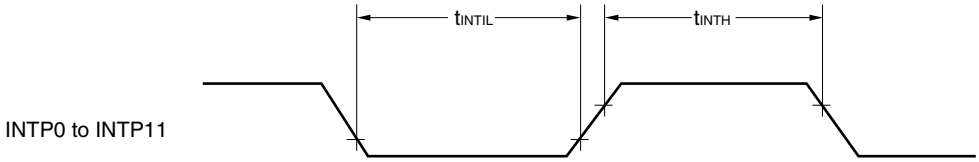
External Main System Clock Timing



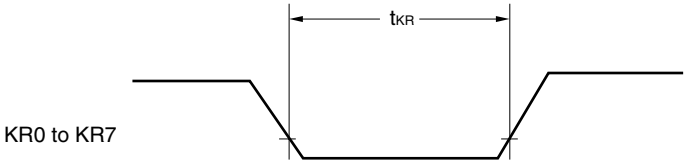
TI Timing



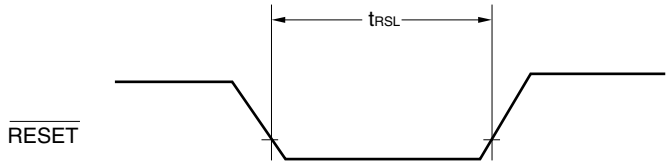
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



A/D Converter Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.3 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				10	bit
Overall error[Notes 1, 2]	AINL	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			TBD	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.1		36.7	μs
		2.7 V ≤ AV_{REF} < 4.0 V	6.1		36.7	μs
		2.3 V ≤ AV_{REF} < 2.7 V	27		TBD	μs
Zero-scale error[Notes 1, 2]	EZS	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			TBD	%FSR
Full-scale error[Notes 1, 2]	EFS	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			TBD	%FSR
Integral non-linearity error[Note 1]	ILE	4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
		2.3 V ≤ AV_{REF} < 2.7 V			TBD	LSB
Differential non-linearity error[Note 1]	DLE	4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}		AV_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} power supply current	I_{DD}			6		mA

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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For further information,
please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielski Strasse 166 B
30177 Hanover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52180
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Limburglaan 5
5616 HR Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
TEL: 010-8235-1155
http://www.cn.necel.com/

NEC Electronics Shanghai Ltd.
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai P.R. China P.C:200120
Tel: 021-5888-5400
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
12/F., Cityplaza 4,
12 Taikoo Wan Road, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

Seoul Branch
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-2719-2377

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/