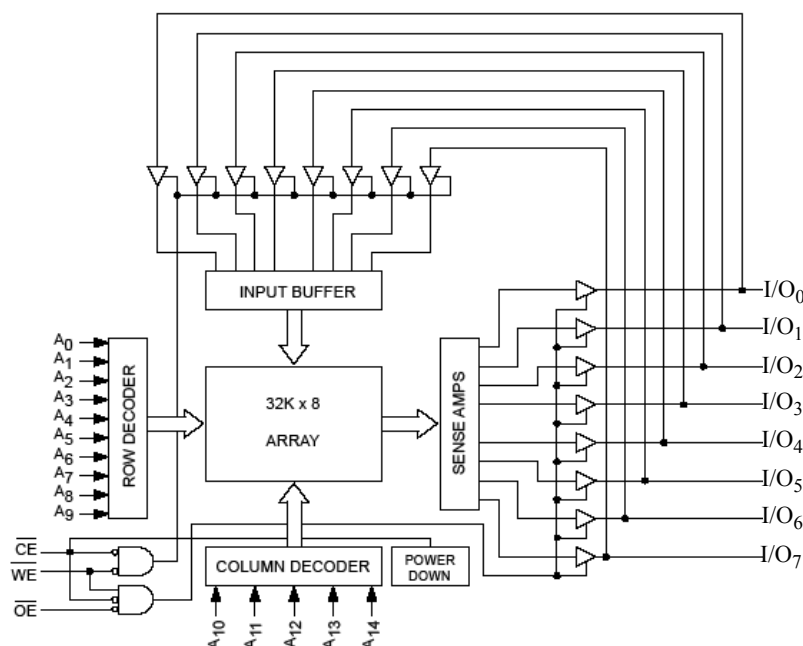


Features

- Temperature ranges
 - -40°C to 85°C
- Pin and function compatible with CY7C199C
- High speed
 - $t_{AA} = 10\text{ ns}$
- Low active power
 - $I_{CC} = 80\text{ mA}$ at 10 ns
- Low CMOS standby power
 - $I_{SB2} = 3\text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features
- Available in Pb-free 28-pin 300-Mil-wide molded small outline J-lead package (SOJ) and 28-pin thin small outline package (TSOP) I packages

Logic Block Diagram



Functional Description

The CY7C199D is a high performance CMOS static RAM organized as 32,768 words by 8-bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{\text{CE}}$), an active LOW output enable ($\overline{\text{OE}}$) and tri-state drivers. This device has an automatic power-down feature, reducing the power consumption when deselected. The input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

Write to the device by taking chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{14}).

Read from the device by taking chip enable ($\overline{\text{CE}}$) and output enable ($\overline{\text{OE}}$) LOW while forcing write enable ($\overline{\text{WE}}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the I/O pins.

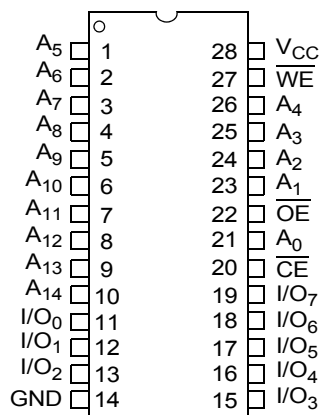
For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

Contents

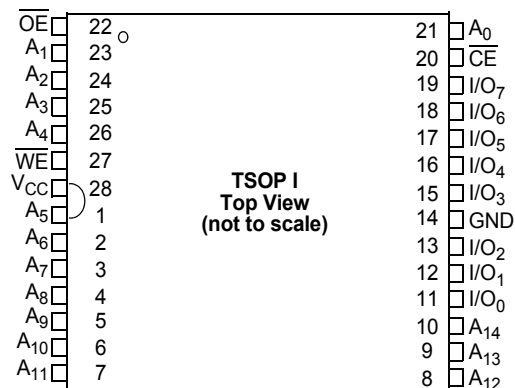
Pin Configuration	3	Truth Table	9
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Pin Configuration

**Figure 1. 28-pin SOJ
(Top View)**



**Figure 2. 28-pin TSOP I
(Top View)**



Selection Guide

Description	-10 (Industrial)	Unit
Maximum access time	10	ns
Maximum operating current	80	mA
Maximum CMOS standby current	3	mA

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with
power applied -55 °C to +125 °C

Supply voltage on V_{CC} to relative GND ^[1] -0.5 V to +6.0 V

DC voltage applied to outputs
in high Z State ^[1] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[1] -0.5 V to $V_{CC} + 0.5$ V

Output current into outputs (LOW) 20 mA

Static discharge voltage > 2,001 V
(per MIL-STD-883, method 3015)

Latch-up current > 140 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	-40 °C to +85 °C	5 V ± 0.5 V	10 ns

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		CY7C199D-10		Unit
				Min	Max	
V _{OH}	Output HIGH voltage	I _{OH} = −4.0 mA		2.4	–	V
V _{OL}	Output LOW voltage	I _{OL} = 8.0 mA		–	0.4	V
V _{IH}	Input HIGH voltage ^[1]			2.2	V _{CC} + 0.5	V
V _{IL}	Input LOW voltage ^[1]			−0.5	0.8	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}		−1	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , output disabled		−1	+1	μA
I _{CC}	V _{CC} operating supply current	V _{CC} = V _{CC(max)} , I _{OUT} = 0 mA, f = f _{max} = 1/t _{RC}	100 MHz	–	80	mA
			83 MHz	–	72	mA
			66 MHz	–	58	mA
			40 MHz	–	37	mA
I _{SB1}	Automatic CE power-down current— TTL Inputs	V _{CC} = V _{CC(max)} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{max}		–	10	mA
I _{SB2}	Automatic CE power-down current— CMOS Inputs	V _{CC} = V _{CC(max)} , $\overline{CE} \geq V_{CC} - 0.3$ V, V _{IN} ≥ V _{CC} − 0.3 V or V _{IN} ≤ 0.3 V, f = 0		–	3	mA

Note

1. $V_{IL(min)}$ = -2.0 V and $V_{IH(max)}$ = $V_{CC} + 1$ V for pulse durations of less than 5 ns.

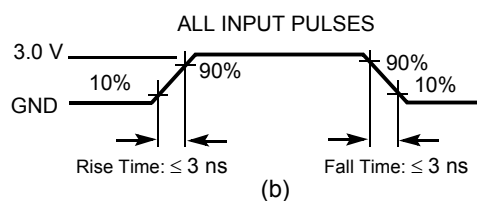
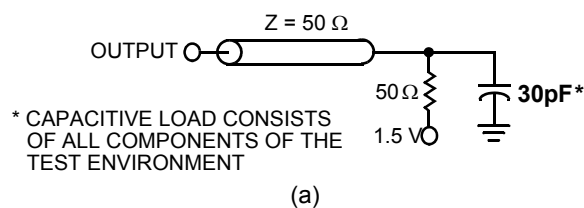
Capacitance [2]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{ V}$	8	pF
C_{OUT}	Output capacitance		8	pF

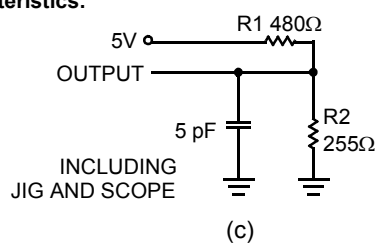
Thermal Resistance [2]

Parameter	Description	Test Conditions	SOJ	TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3×4.5 inch, four-layer printed circuit board	59.16	54.65	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		40.84	21.49	$^\circ\text{C/W}$

AC Test Loads and Waveforms [3]



High Z characteristics:



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except high Z) are tested using the load conditions shown in Figure (a). High Z characteristics are tested for all speeds using the test load shown in Figure (c).

Switching Characteristics

(Over the operating range) ^[4]

Parameter	Description	CY7C199D-10		Unit
		Min	Max	
Read Cycle				
t _{power} ^[5]	V _{CC(typical)} to the first access	100	–	μs
t _{RC}	Read cycle time	10	–	ns
t _{AA}	Address to data valid	–	10	ns
t _{OHA}	Data hold from address change	3	–	ns
t _{ACE}	$\overline{\text{CE}}$ LOW to data valid	–	10	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to data valid	–	5	ns
t _{LZOE} ^[6]	$\overline{\text{OE}}$ LOW to low Z	0	–	ns
t _{HZOE} ^[6, 7]	$\overline{\text{OE}}$ HIGH to high Z	–	5	ns
t _{LZCE} ^[6]	$\overline{\text{CE}}$ LOW to low Z	3	–	ns
t _{HZCE} ^[6, 7]	$\overline{\text{CE}}$ HIGH to high Z	–	5	ns
t _{PU} ^[8]	$\overline{\text{CE}}$ LOW to power-up	0	–	ns
t _{PD} ^[8]	$\overline{\text{CE}}$ HIGH to power-down	–	10	ns
Write Cycle ^[9, 10]				
t _{WC}	Write cycle time	10	–	ns
t _{SCE}	$\overline{\text{CE}}$ LOW to write end	7	–	ns
t _{AW}	Address setup to write end	7	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	$\overline{\text{WE}}$ pulse width	7	–	ns
t _{SD}	Data setup to write end	6	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{HZWE} ^[6]	$\overline{\text{WE}}$ LOW to high Z	–	5	ns
t _{LZWE} ^[6, 7]	$\overline{\text{WE}}$ HIGH to low Z	3	–	ns

Notes

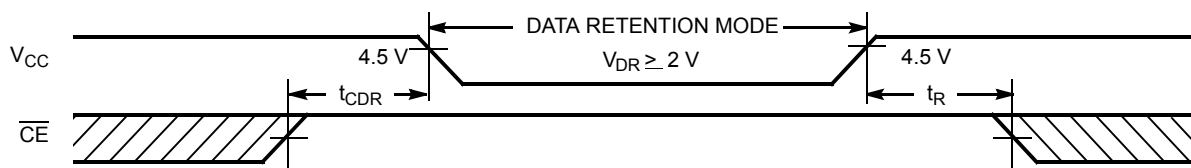
- Test conditions assume signal transition time of 3 ns or less for all speeds, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified $I_{\text{OL}}/I_{\text{OH}}$ and 30-pF load capacitance.
- t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_{\text{L}} = 5 \text{ pF}$ as in part (b) of “AC Test Loads and Waveforms [3]” on page 5. Transition is measured $\pm 200 \text{ mV}$ from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics

(Over the operating range)

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	3	mA
$t_{CDR}^{[11]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[12]}$	Operation recovery time		15	–	ns

Data Retention Waveform



Switching Waveforms

Figure 3. Read Cycle No. 1: Address Transition Controlled [13, 14]

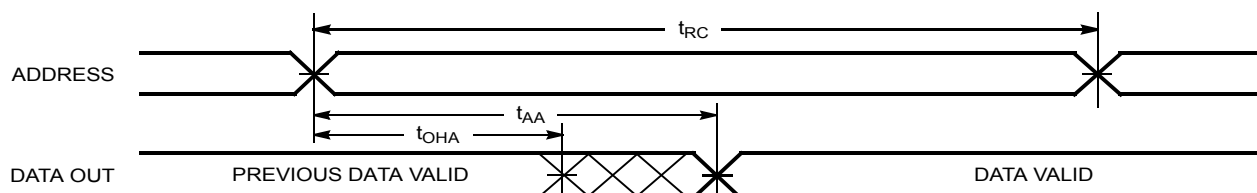
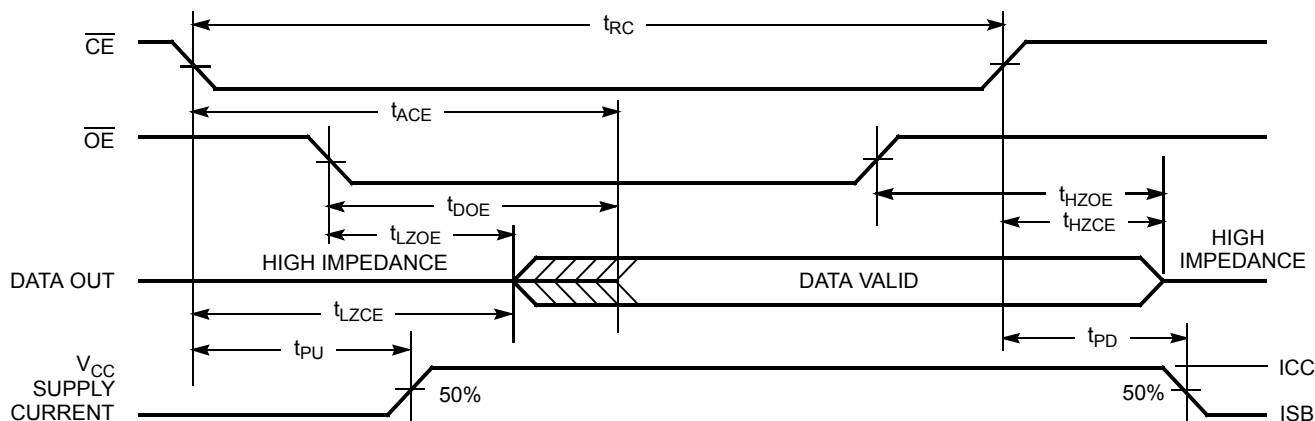


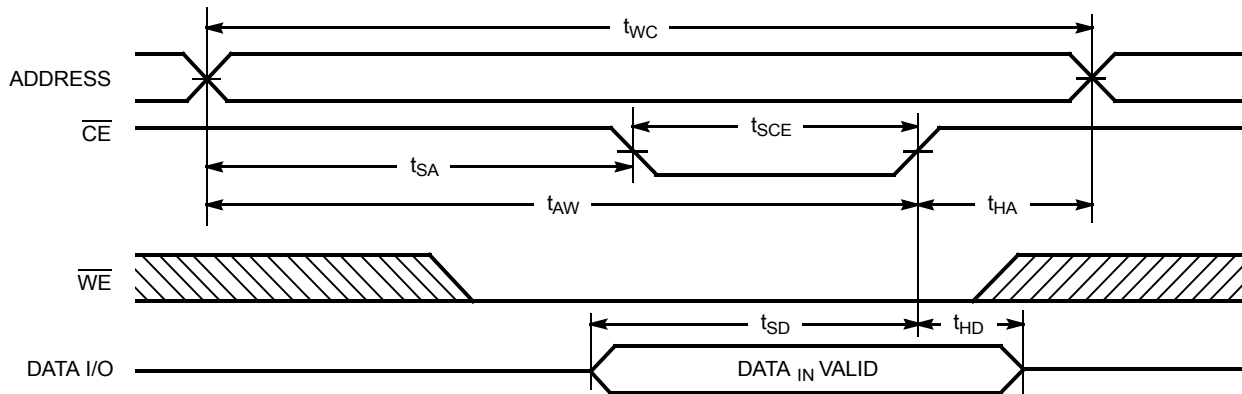
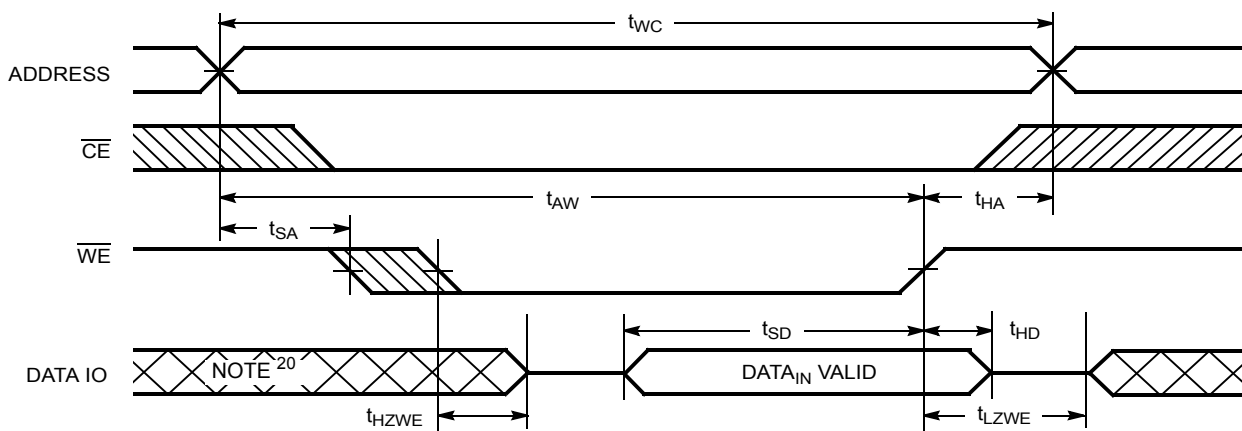
Figure 4. Read Cycle No. 2 \overline{OE} Controlled [14, 15]



Notes

11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 50\text{ }\mu\text{s}$.
13. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
14. \overline{WE} is HIGH for read cycle.
15. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1: $\overline{\text{CE}}$ Controlled [16, 18, 19]

Figure 6. Write Cycle No. 3 $\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW [17, 19]

Notes

16. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

17. The minimum write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .

18. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.

19. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

20. During this period the I/Os are in the output state and input signals should not be applied.



$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})
L	H	H	High Z	Deselect, output disabled	Active (I_{CC})

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at <http://www.cypress.com> and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

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Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C199D-10VXI	51-85031	28-pin (300-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C199D-10ZXI	51-85071	28-pin TSOP Type I (Pb-free)	

Please contact your local Cypress sales representative for availability of these parts.

CY 7 C 1 9 9 D - XX XXX X

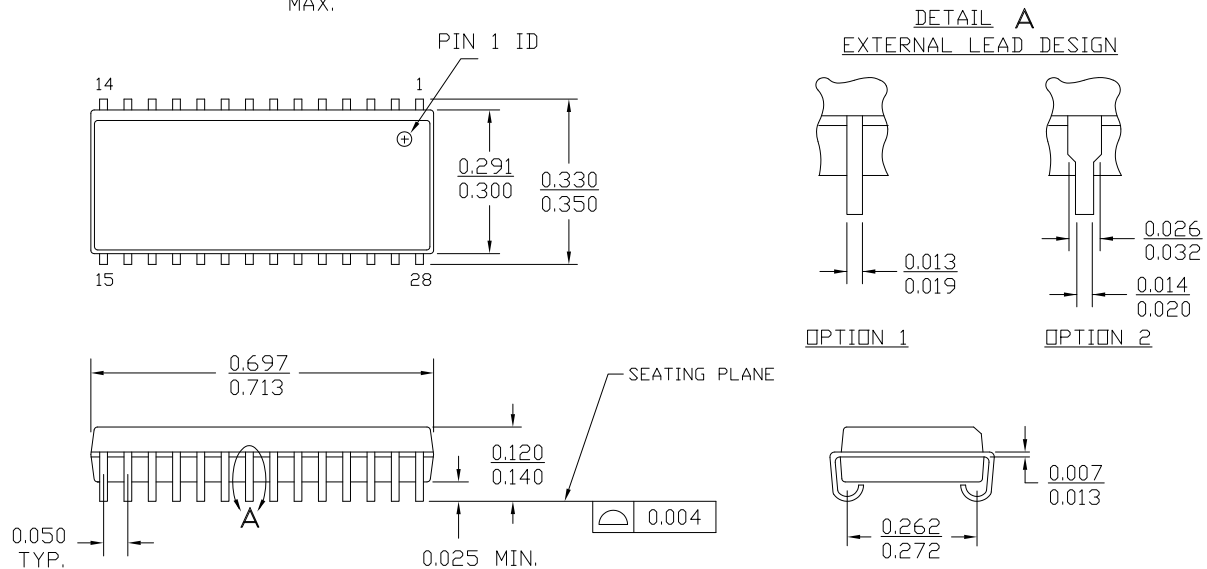
- Temperature Grade: I
I = Industrial
- Package Type: VX or ZX or SNX
VX = 28 pin (300-Mil) Molded SOJ (Pb-free)
ZX = 28 pin TSOP Type 1 (Pb-free)
- Speed Grade: 10 ns
- Process Technology: 90 nm
- Bus Width = ×8
- Density = 256 K
- Fast SRAM Family
- Technology Code: C = CMOS
- Marketing Code: 7 = SRAM
- Company ID: CY = Cypress

Package Diagrams

Figure 7. 28-pin (300-Mil) Molded SOJ

NOTE :

1. JEDEC STD REF M0088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.
MAX.

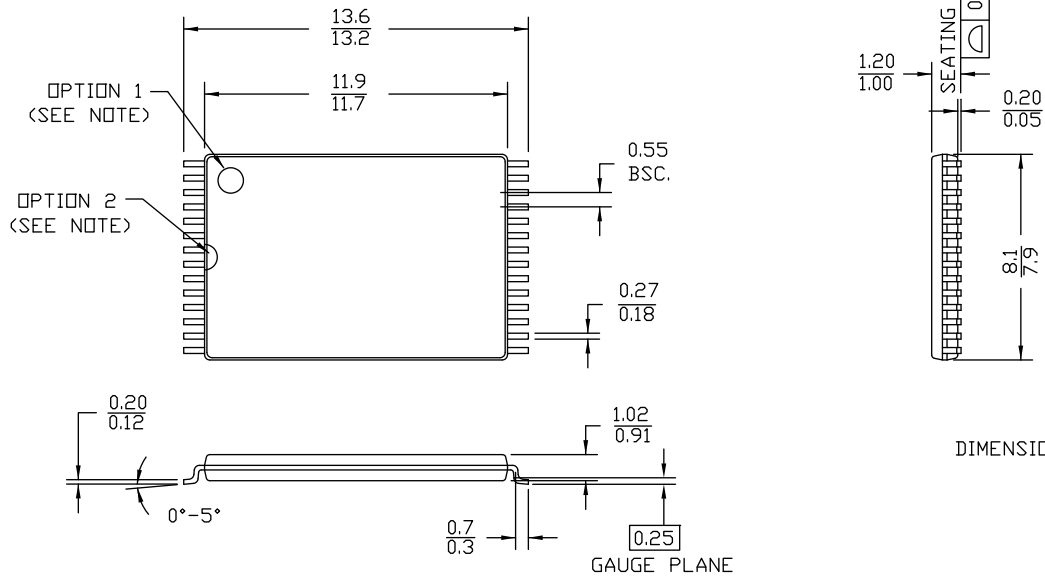


51-85031 *D

Package Diagrams (continued)

Figure 8. 28-pin Thin Small Outline Package Type 1 (8x13.4 mm)

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

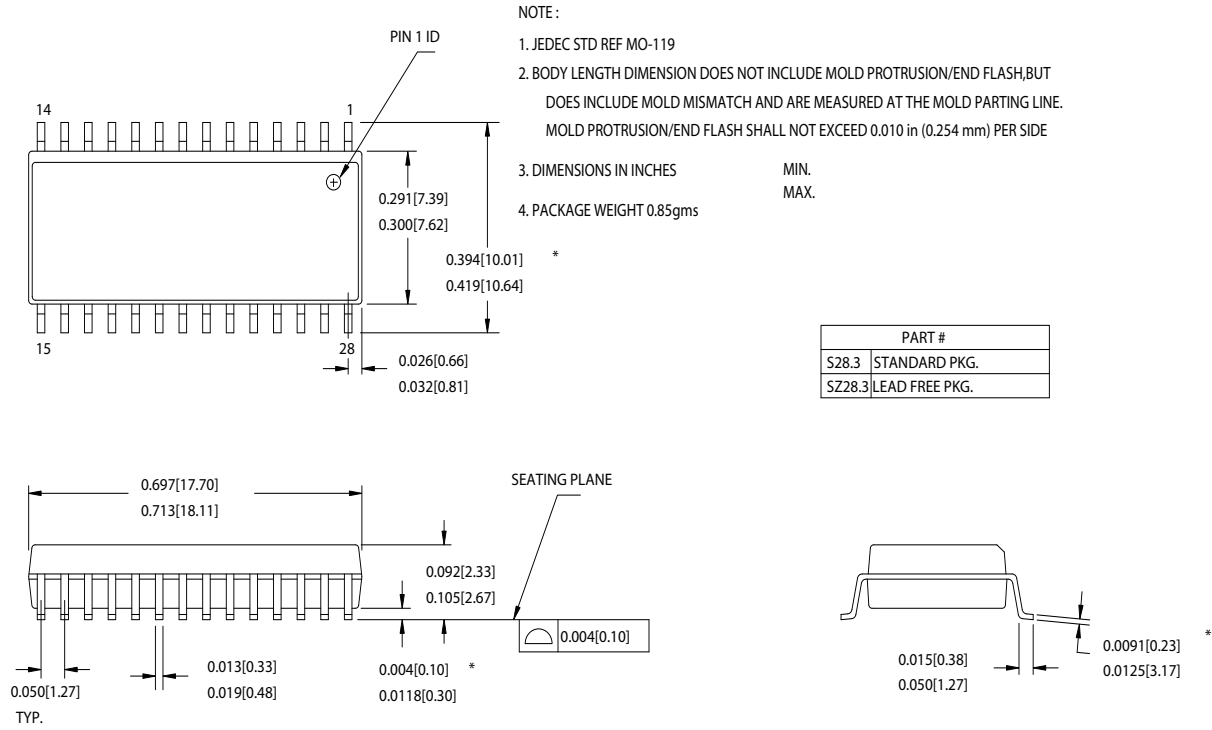


DIMENSION IN MM
MAX.
MIN.

51-85071 *H

Package Diagrams (continued)

Figure 9. 28-pin (300-Mil) SOIC



51-85026 *E

Acronyms

Acronym	Description
\overline{CE}	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
\overline{OE}	output enable
SOIC	small-outline integrated circuit
SOJ	small outline J-lead package
SRAM	static random access memory
TSOP	thin small outline package
TTL	Transistor-transistor logic
\overline{WE}	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	volts
μA	micro amperes
mA	milli amperes
pF	pico Farad
°C	degree Celsius
W	watts

Document History Page

Document Title: CY7C199D 256 K (32 K × 8) Static RAM Document Number: 38-05471				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	201560	SWI	See ECN	Advance Information datasheet for C9 IPP
*A	233728	RKF	See ECN	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in Ordering Information
*B	262950	RKF	See ECN	Removed 28-LCC Pinout and Package Diagrams Added Data Retention Characteristics table Added T _{power} Spec in Switching Characteristics table Shaded Ordering Information
*C	307594	RKF	See ECN	Reduced Speed bins to -10, -12 and -15 ns
*D	820660	VKN	See ECN	Converted from Preliminary to Final Removed 12 ns and 15 ns speed bin Removed Commercial Operating range Removed "L" part Removed 28-pin PDIP and 28-pin SOIC package Changed Overshoot spec from V _{CC} +2V to V _{CC} +1V in footnote #2 Changed I _{CC} spec from 60 mA to 80 mA for 100 MHz speed bin Added I _{CC} specs for 83 MHz, 66 MHz and 40 MHz speed bins Updated Thermal Resistance table Updated Ordering Information Table
*E	2745093	VKN	See ECN	Included 28-Pin SOIC package Changed V _{IH} level from 2.0V to 2.2V For Industrial grade, changed t _{SD} from 5 ns to 6 ns, and t _{HZWE} from 6 ns to 5 ns Included Automotive-E information
*F	2897087	AJU	03/22/10	Removed obsolete parts from ordering information table Updated package diagrams
*G	3023234	RAME	09/06/2010	Added Auto-E SOIC package related info Changed TDOE spec from 10 ns to 11 ns in CY7C199D-25. Added Ordering Code Definitions . Added Acronyms and Document Conventions .
*H	3130763	PRAS	01/07/11	Dislodged Automotive information to a new datasheet (001-65530)

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