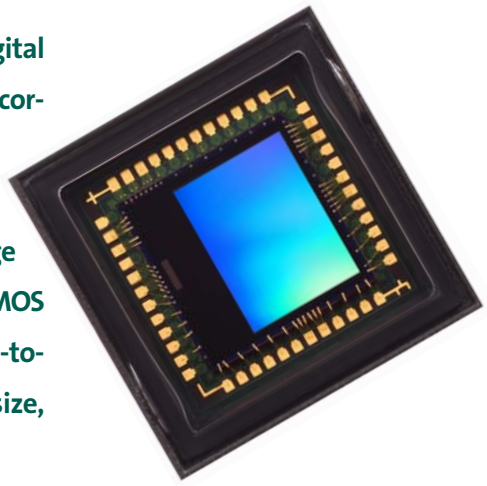
MT9T031 Image Sensor

Product Brief

Aptina's MT9T031 is a QXGA-format 1/2-inch CMOS active-pixel digital image sensor with an active imaging pixel array of 2048H x 1536V. It incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface. The 3-megapixel CMOS image sensor features DigitalClarity™—Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.



Applications

- High-resolution network cameras
- Wide field of view cameras
- Dome cameras with electronic pan, tilt, and zoom
- Security video cameras with high resolution stills
- Detailed feature extraction for smart cameras

Features

- DigitalClarity® imaging technology
- High frame rate
- Global reset release
- Horizontal and vertical binning
- Column and row skip modes
- Superior low-light performance
- Low dark current
- Simple two-wire serial interface
- Programmable controls: Gain, frame rate, frame size, exposure
- Pin-for-pin compatible with Aptina's 1.3-megapixel MT9M001

Ordering Information

Part Number	Description
MT9T031C12STC	48-pin CLCC
MT9T031C12STCD ES	48-pin CLCC Demo
MT9T031C12STCH ES	48-pin CLCC Demo headboard

Parameter	
Optical format	1/2-inch (4:3)
Active imager size	6.55mm(H) x 4.92mm(V) 8.19 (diagonal)
Active pixels	2048H x 1536V
Pixel size	3.2µm x 3.2µm
Color filter array	RGB Bayer pattern
Shutter type	Global reset release (GRR), electronic rolling shutter (ERS)
Maximum data rate/ master clock	48 Mp/s/48 MHz
Frame rate	
QXGA (2048 x 1536)	Programmable up to 12 fps
UXGA (1600 x 1200)	Programmable up to 20 fps
HDTV (1280 x 720)	Programmable up to 39 fps
XGA (1024 x 768)	Programmable up to 43 fps
VGA (640 x 480)	Programmable up to 93 fps
ADC resolution	10-bit, on-chip
Responsivity	>1.0 V/lux-s (550nm)
Dynamic range	61dB
SNR_{MAX}	43dB
Supply voltage	3.0V—3.6V (3.3V nominal)
Power consumption	228mW (nominal); 1.65µW (standby)
Operating temp	0°C to 60°C
Packaging	48-pin CLCC
Output gain	25 e-/LSB
Read noise	6 e-RMS at 16X
Dark current	100 e-/pixel/s at 55°C

General Description

The MT9T031 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of consumer and industrial applications, including high-resolution network cameras, electronic PTZ cameras, and security video cameras that can also produce high-resolution still images.

The sensor can be operated in its default mode or programmed for frame size, exposure, gain setting, and other parameters. The default mode outputs a QXGA image at 12 frames per second (fps). An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

Figure 1: Block Diagram

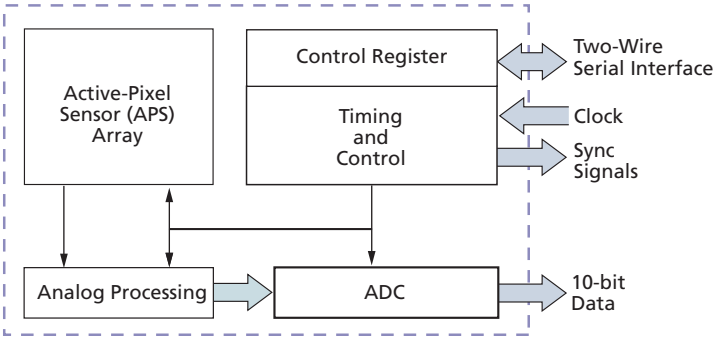


Figure 2 illustrates the MT9T031's quantum efficiency in relation to wavelength.

Figure 2: MT9T031 Quantum Efficiency

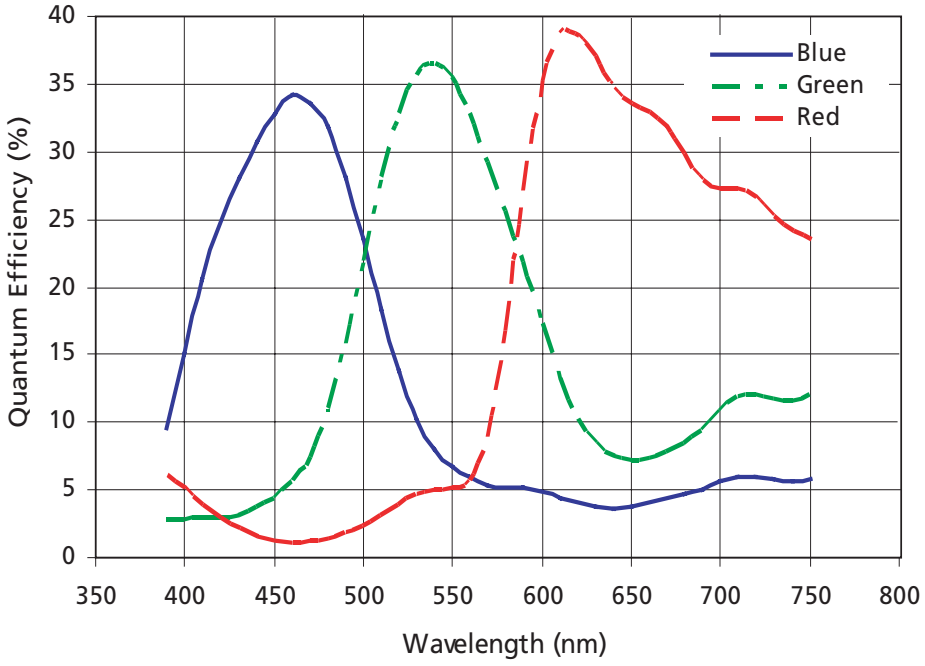
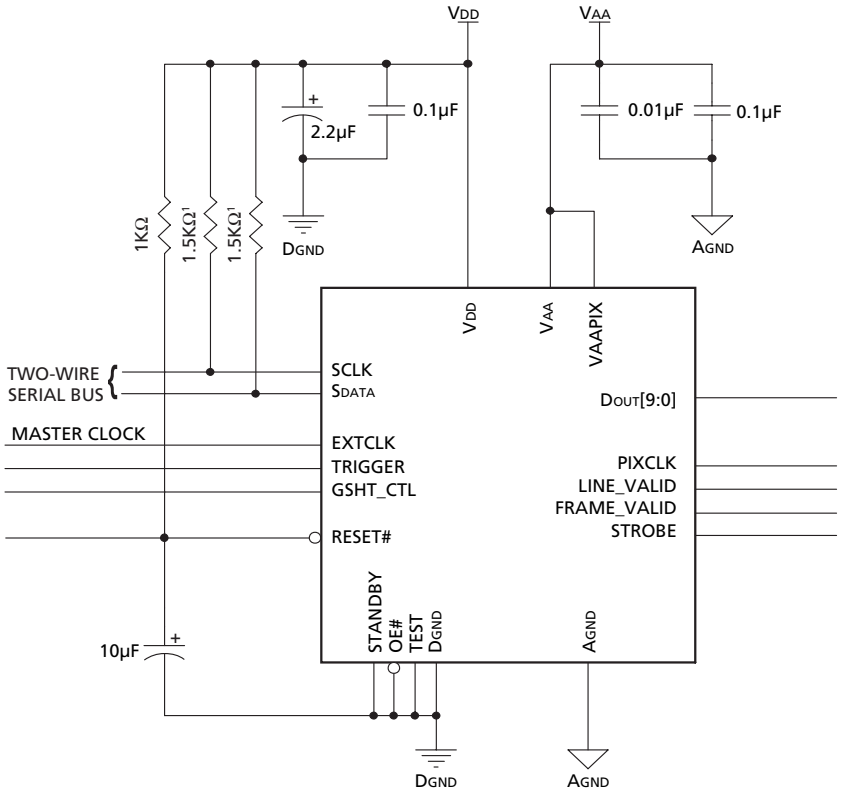


Figure 3: Typical Configuration (connection)



Notes: 1. Resistor value 1.5KΩ is recommended, but resistance may be greater for slower two-wire speed.

Figure 4: 48-Pin CLCC

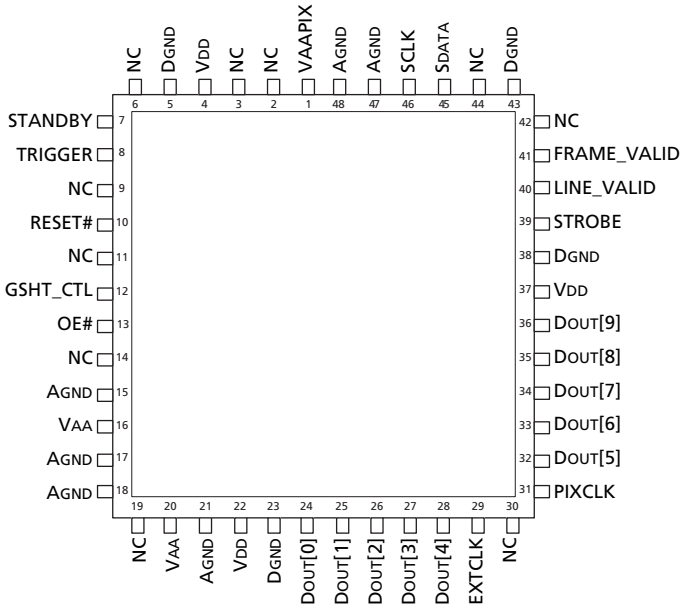


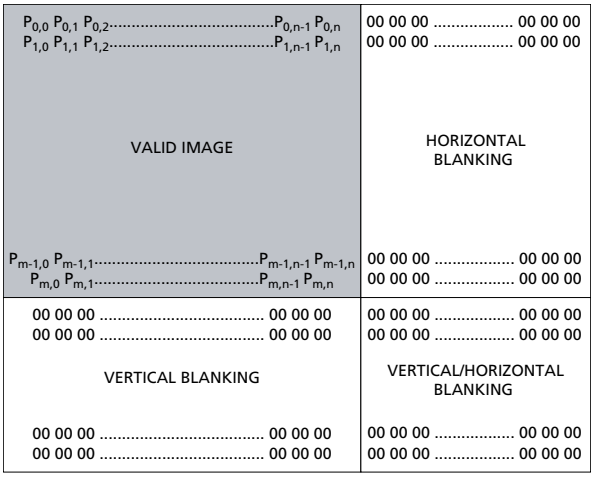
Table 1: Pin Descriptions

Pin Numbers	Symbol	Type	Description
7	STANDBY	Input	Standby: Activates (HIGH) standby mode, disables analog bias circuitry for power saving mode.
8	TRIGGER	Input	Trigger: Activates (HIGH) snapshot sequence.
10	RESET#	Input	Reset: Activates (LOW) asynchronous reset of sensor. All registers assume factory defaults.
13	OE#	Input	Output enable: OE# when HIGH, places outputs DOUT[9:0], FRAME_VALID, LINE_VALID, PIXCLK, and STROBE into a tri-state configuration.
29	EXTCLK	Input	Clock in: Master clock into sensor (48 MHz maximum).
46	SCLK	Input	Serial clock: Clock for serial interface.
12	GSHT_CTL	Input	Global shutter control.
45	SDATA	I/O	Serial data: Serial data bus, requires 1.5KΩ resistor to 3.3V for pull-up.
24, 25, 26, 27, 28, 32, 33, 34, 35, 36	DOUT[9:0]	Output	Data out: Pixel data output bit 0, DOUT[9] (MSB), DOUT[0] (LSB).
31	PIXCLK	Output	Pixel clock: Pixel data outputs are valid during falling edge of this clock. Frequency = master clock.
39	STROBE	Output	Strobe: Output is pulsed HIGH to indicate sensor reset operation of pixel array has completed.
40	LINE_VALID	Output	Line valid: Output is pulsed HIGH during line of selectable valid pixel data (see R0x20 for options).
41	FRAME_VALID	Output	Frame valid: Output is pulsed HIGH during frame of valid pixel data.
1	VAAPIX	Supply	Analog pixel power: Provides power supply for pixel array, 3.3V ±0.3V.
4, 22, 37	VDD	Supply	Digital power: Provides power supply for digital block, 3.3V ±0.3V.
5, 23, 38, 43	DGND	Supply	Digital ground: Provides isolated ground for digital block.
16, 20	VAA	Supply	Analog power: Provides power supply for analog block, 3.3V ±0.3V.
15, 17, 18, 21, 47, 48	AGND	Supply	Analog ground: Provides isolated ground for analog block and pixel array.
2, 3, 6, 9, 11,14,19, 30 42, 44	NC	–	No connect: These pins must be left unconnected.

Output Data Format

The MT9T031 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 5.

Figure 5: Spatial Illustration of Image Readout



Feature Description

Window Size

The default programmed window size is 2,048 columns by 1,536 rows (2048H x 1536V), though the window size can be changed through the control logic. Table 2 shows examples of register settings that may be used to achieve various resolutions and frame rates.

Table 2: Standard Resolutions

Resolution	Frame Rate	Column_Size	Row_Size	Shutter Width
2048 x 1536 QXGA	12 fps	2047	1535	<1552
1600 x 1200 UXGA	20 fps	1599	1199	<1216
1280 x 1024 SXGA	27 fps	1279	1023	<1040
1024 x 768 XGA	43 fps	1023	767	<784
800 x 600 SVGA	65 fps	799	599	<616
640 x 480 VGA	93 fps	639	479	<496

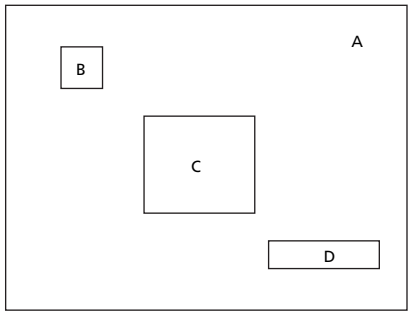
Table 3: Wide-Screen (16:9) Resolutions

Resolution	Frame Rate	Column_Size	Row_Size	Shutter Width
1920 x 1080 HDTV	18 fps	1919	1079	<1096
1280 x 720 HDTV	39 fps	1279	719	<736

Electronic Panning

The location of the readout window can be changed. This enables a zooming function, since only a segment of the imager array is read out. Figure 6 on page 6 shows some examples of the electronic pan/zoom and windowing capabilities of the sensor.

Figure 6: Windowing Capabilities



Window	Size
Window A	2048 x 1536
Window B	128 x 128
Window C	512 x 512
Window D	400 x 96

Blanking Control

Registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). Horizontal blanking is specified in terms of pixel clocks. Vertical blanking is specified in terms of row readout times.

Frame Time

The user can change the number of columns and rows read out as well as the horizontal and vertical blanking times to obtain different frame rates.

High Frame Rate Readout Modes

In addition to having the flexibility to read out smaller standard formats, the sensor can also read out nonstandard formats. This is particularly useful for zooming in on a particular segment of the image to perform high-speed mathematical calculations (for example, a high-speed viewfinder or autofocus applications).

Applications with an autofocus mode may require more horizontal than vertical resolution. That way, the imager can window to the midsection of the array by changing the row start address and the window height.

The MT9T031change registers can obtain the different frame rates. The imager can also perform row skip modes to obtain a larger field of view when high-frequency vertical resolution is not critical.

Pixel Integration Time Control

Sensor integration time can be changed by adjusting the amount of time the pixels are set to collect charge generated from light. The sensor also supports sub-row integration time for fine control of pixel integration time.

Note that not all integration times may be desired under certain lighting conditions. If the light source has a flicker component, then the integration time needs to be set properly to avoid banding in the image.

Snapshot Mode and Flash Control

Setting Up for Snapshot Mode

There are two important signals used for snapshot mode: TRIGGER and STROBE. The TRIGGER signal initiates the start of a single-frame capture, and STROBE is an output pulse that may be used to turn on a flash and/or activate a mechanical shutter.

Triggering a Snapshot

An external trigger signal input allows the snapshot operation to begin after the TRIGGER pulse moves from a HIGH to LOW state. Alternately, an internal register can be set through the serial inteface.

Strobe Pulse Output

After the TRIGGER pulse has signaled a snapshot operation, each row of the imager array is reset in sequence to clear out any accumulated signal. Once each row of the imager is reset, the STROBE pulse is output from the imager

Global Shutter Release Snapshot Mode

In addition to the standard snapshot mode, the MT9T031 has a global shutter release mode which may be combined with a mechanical shutter to achieve simultaneous exposure of all rows in the image. Two global shutter modes are available: programmed exposure and bulb mode.

Skip and Bin Modes

Row and column skip modes use subsampling to reduce the output resolution without reducing the field of view. The MT9T031 also has row and column binning modes, which can reduce the impact of aliasing introduced by the use of skip modes. Both 2X and 3X binning modes are supported. Rows and columns can be binned independently.

Smaller Format Resolution

With the flexible windowing capability of the sensor, the user is able to read out different resolution formats from default of QXGA to UXGA, SXGA, XGA, SVGA, VGA, CIF, QVGA, QCIF, and so on.

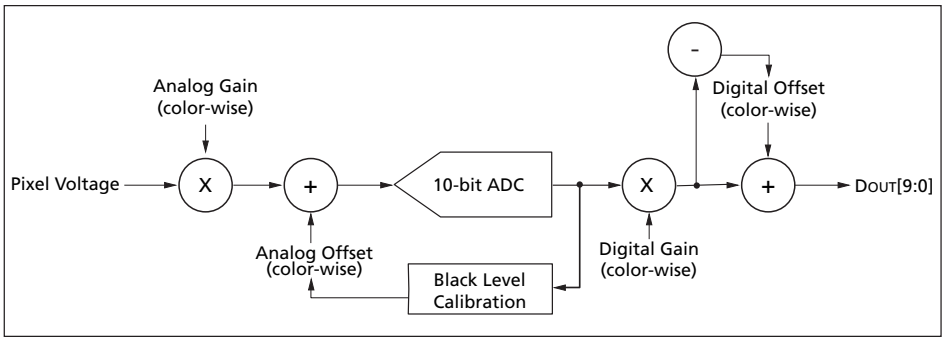
Signal Path

The MT9T031 sensor analog signal path consists of the pixel array, the column sample and hold (S/H) circuitry, the programmable gain stage, the analog offset correction, and the analog-to-digital converter (ADC).

The reset and signal voltages from the pixel are sampled onto the column sample and hold circuitry by row. After signal sampling is complete, the differential signal (reset - signal) is transferred to the programmable gain stage.

After the gain stage, the differential signal goes through the analog offset correction circuitry. The user can decide if a positive or negative offset or no offset needs to be added to the differential signal. The signal is then sampled onto the sample and hold circuitry of the ADC before being converted to a digital signal.

Figure 7: Signal Path



Gain Settings

The analog programmable gain stage consists of two stages of gain that operate in a pipelined manner. The first stage has programmable gain of 1 or 2 while the second stage has programmable gain of 1 to 4 with steps of 0.125, for a maximum analog gain of 8. The gain settings can be adjusted independently for the colors of green1, blue, red, and green2.

Black Level Calibration

The digital black level of the MT9T031 sensor potentially varies with temperature or gain setting changes. The MT9T031 sensor enables the flexibility of automatic black level calibration or manual black level control.

Manual Black Level Calibration

The programmable analog offset stage corrects for analog offset that might be present in the analog signal. The analog offset settings can be independently adjusted for the colors of green1, green2, red, and blue.

Black Level

Digital offset is applied such that the average black level of a frame in a resulting image equals the value of this register. This adjustment happens after black-level calibration.

Serial Bus Description

Registers are written to and read from the MT9T031 through the two-wire serial interface bus. The MT9T031 is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9T031 through the serial data (SDATA) line. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Sequence

A typical read or write sequence begins with the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request is a read or a write (“0” indicates a write and a “1” indicates a read). The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits.

The MT9T031 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows:

1. The master sends the write-node slave address and 8-bit address, just as in the write request.
2. The master sends a start bit and the read-mode slave address.
3. The master clocks out the register data 8 bits at a time.
4. The master sends an acknowledge bit after each 8-bit transfer.
5. The register address is auto-incremented after every 16 bits transferred.
6. The data transfer is stopped when the master sends a no-acknowledge bit.

Electrical Specifications

Table 4: DC Electrical Characteristics

^{f}EXTCLK = 48 MHz, V_{DD} = 3.3V, V_{AA} = 3.3V, VAAPIX = 3.3V, T_A = 25°C

Symbol	Definition	Condition	Min	Typ	Max	Units
V_{DD}	Core digital voltage		3	3.3	3.6	V
V_{AA}	Analog voltage		3	3.3	3.6	V
VAAPIX	Pixel supply voltage		3	3.3	3.6	V
V_{IH}	Input high voltage		–	1.84	–	V
V_{IL}	Input low voltage		–	1.54	–	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DD} or D_{GND}	–5	–	+5	µA
V_{OH}	Output high voltage	At specified I_{OH} = 0mA	2.54	2.72	2.82	V
V_{OL}	Output low voltage	At specified I_{OL}	0.13	0.19	0.3	V
I_{OH}	Output high current	At specified V_{OH}	–		11.5	mA
I_{OL}	Output low current	At specified V_{OL}	–		12.5	mA
I_{OZ}	Tri-state output leakage current		–		5	µA
I_{DD}	Digital operating current	0 lux, 48 MHz	–	20	23.0	mA
I_{AA}	Analog operating current	0 lux, 48 MHz	–	45.0	54.0	mA
I_{AAPIX}	Pixel supply current	0 lux, 48 MHz	–	4.0	5.0	mA
I_{STDBYD}	Digital standby current	Input clock disabled, 0 lux	–	0.2	2.0	µA
I_{STDBYA}	Analog standby current	Input clock disabled, 0 lux	–	0.2	2.0	µA
$I_{STDBYDA}$	Pixel standby current	Input clock disabled, 0 lux	–	0.1	1.0	µA

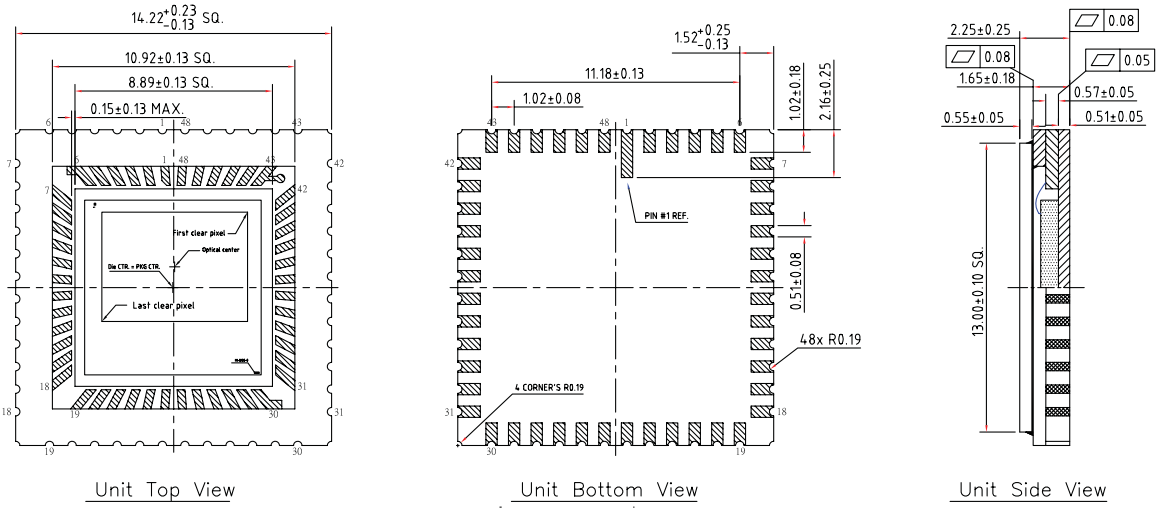
Table 5: Absolute Maximum Ratings

Symbol	Definition	Conditions	Min	Max	Units
V_{DD}_MAX	Core digital voltage		–0.3	+3.6	V
V_{AA}_MAX	Analog voltage		–0.3	+3.6	V
V_{AA}PIX_MAX	Pixel supply voltage		–0.3	+3.6	V
V_{IN}_MAX	Input voltage		–	1.9	V
I_{DD}_MAX	Digital operating current		–	29.5	µA
I_{AA}_MAX	Analog operating current		–	56.3	µA
I_{AA}PIX_MAX	Pixel supply current		–	6.4	µA
T_{OP}[2]	Operating temperature	Measured at junction	0	60	°C
T_{ST}	Storage temperature		–40	+125	°C

Notes:
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. To keep dark current and shot noise artifacts from impacting image quality, keep operating temperature at a minimum.

Package Dimensions

Figure 8: 48-Pin CLCC



NOTE:

1. ALL EXPOSED METALLIZED AREA SHALL BE GOLD PLATED 60 MICRO INCHES MIN. THK. OVER NICKEL PLATED UNLESS OTHERWISE SPECIFIED IN PURCHASE ORDE
2. SEAL AREA AND DIE ATTACH AREA SHALL BE WITHOUT METALLIZATION.
3. DIE PLACEMRNT ACCARUCY = ±0.125mm
4. WAFER THICKNESS = 0.675mm (26.57 mil) .
5. EPOXY THICKNESS FOR DIE ATTACHMENT IS 0.025~0.050mm
6. GLASS TRANSMITTANCE >=90%.
7. GLASS TILT = 0.10mm MAX.
8. DIE LOCATION : DIE CENTER AIMS AT PACKAGE CENTER.

Notes: 1. All dimensions in millimeters.

Revision History

Rev. B 11/16/09

- Updated to Aptina template
- Updated to CLCC package

Rev. A 8/06

- Initial release

10 Eunos Road 8 13-40, Singapore Post Center, Singapore 408600 prodmktg@aptina.com www.aptina.com