Structure　Silicon monolithic integrated circuit

Product Name　ADPCM Decoder LSI for Voice production

Product No.　**BU8844FV**

Features　4Bit ADPCM / 16Bit PCM
Sampling Frequencies 4KHz to 32KHz
I2C Interface
Built-in FIFO
Built-in 11Bit DA converter

○Absolute Maximum Ratings(unless otherwise noted, Ta = 25℃)

Parameter	Symbol	Rating	Unit	Remarks
Analog supply voltage	DACVDD	-0.3 ～ 4.5	V	
Digital I/O supply voltage	DVDDIO	-0.3 ～ 4.5	V	
Digital CORE supply voltage	VDDCORE	-0.3 ～ 2.5	V	
Voltage applied to pins	VIN	DVSS-0.3 ～ DVDDIO+0.3	V	
Allowable dissipation	Pd	200 (*1)	mW	
Storage temperature range	Tstg	-50 ～ 125	℃	
Operating temperature range	Topr	-25 ～ 85	℃	

(*1) Note: Reduce to 2.0mW/℃ when Ta = 25℃ or above

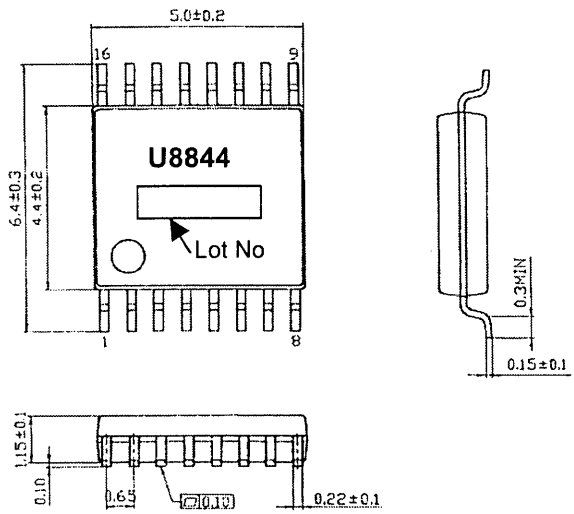
○Operating Power Supply Voltage Range(Unless otherwise noted, Ta = 25℃)

○Electrical Characteristics

(Unless otherwise noted, Ta = 25℃, DVDDIO=3.0V, VDDCORE=1.8V, DACVDD=3.0V)

Parameter	Symbol	Rating			Unit	Measurement Conditions
		MIN	TYP	MAX		
Digital block DC Characteristics						
H Level Input Voltage	VIH	DVDDIO-0.5	-	-	V	
L Level Input Voltage	VIL	-	-	DVDDIO+0.5	V	
H Level Input Current	IIH	-	-	1	uA	VIH=DVDDIO
L Level Input Current	IIL	-1	-	-	uA	VIL=DVSS
H Level Output Voltage	VOH	DVDDIO-0.3	-	-	V	IOH=-4mA type
L Level Output Voltage	VOL	-	-	DVDDIO+0.3	V	IOL=4mA type
Analog PIN Characteristics						
Full-scale amplitude	VMAX	-	1.80	-	Vp-p	0.6xDACVDD
VREF Rise time	TRVR	-	35	45	msec	CVREF= 1uF NRST=L→H
		-	20	30	msec	CVREF= 0.47uF NRST=L→H
Power consumption						
Analog Idd1 (DACVDD)	AIDD1	-	0.7	2.5	mA	Playing (8KHz Sampling case)
Digital Idd11 (VDDCORE)	DIDD11	-	0.5	3	mA	Playing (8KHz Sampling case)
Digital Idd12 (DVDDIO)	DIDD12	-	0.1	0.5	mA	Playing (8KHz Sampling case)
Analog Idd2 (DACVDD)	AIDD2	-	-	2	uA	Standby
Digital Idd20 (VDDCORE)	DIDD20	-	-	20	uA	Standby
Digital Idd21 (DVDDIO)	DIDD21	-	-	10	uA	Standby

○ External measure and View



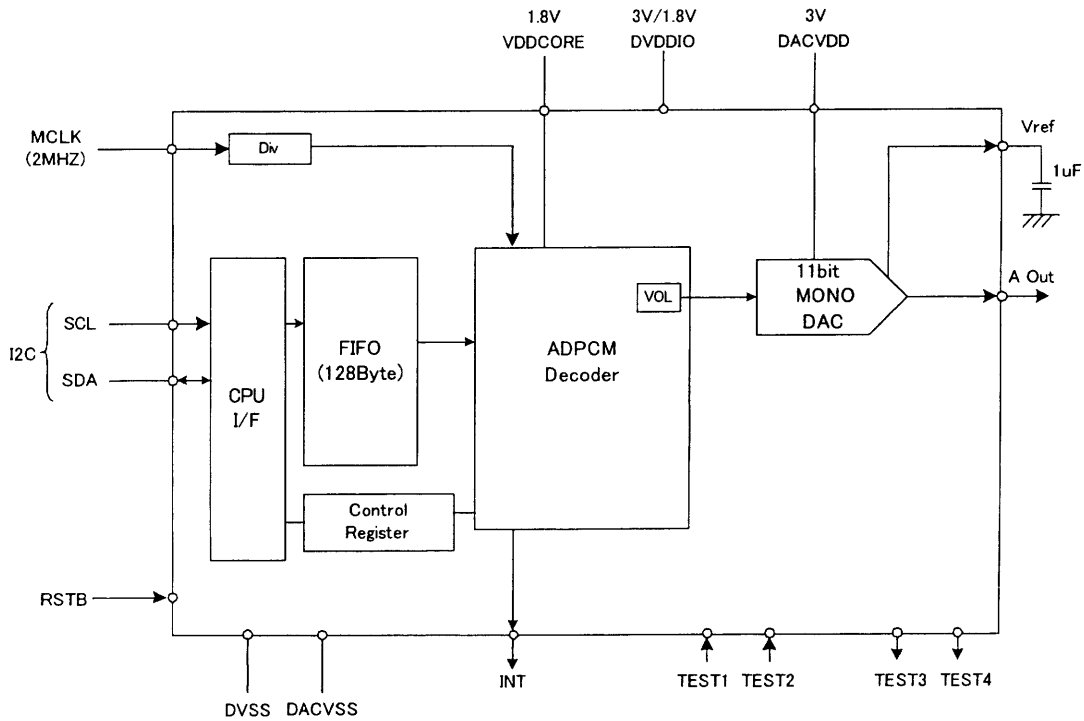
(UNIT : mm)

○Pin layout diagram

No.	PIN Name	Function
1	TEST1	TEST Input
2	TEST2	TEST Input
3	DACVDD	Analog Supply
4	DACVSS	Analog VSS
5	VREF	Analog Reference output
6	AOUT	Analog output
7	RSTB	Reset Input
8	TEST3	TEST OUT
9	VDDCORE	CORE Supply
10	TEST4	TEST OUT
11	INT	INT Signal
12	SCL	I2C Clock
13	SDA	I2C Data
14	DVDDIO	I/O Supply
15	DVSS	CORE GND
16	MCLK	Main clock Input (2MHz)

* TEST1 and TEST2 are DVSS fixations.
* TEST3 and TEST4 are OPEN.

○Block diagram



○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9)Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of