

Features

The MAX[®] II development board, included with the MAX II Development Kit, is a full-featured platform for evaluating MAX II device features and prototyping CPLD designs. Circuits are provided to allow users to measure MAX II power consumption and MAX II power-up timing. Memory, displays, and interfaces enable designers to begin the development or testing of custom CPLD designs.

Circuits

The MAX II development board contains the following circuits:

- *Active I/O sense circuit*—Allows users to load V_{CCINT} and observe the effect on MAX II user I/O ramp times
- *Power measuring circuit*—Allows users to measure the stand-by and nominal power consumed by the MAX II device
- *Schmitt trigger circuit*—Allows users to generate a custom clock using the internal Schmitt trigger

Components

The MAX II development board contains the following components:

- MAX II EPM1270F256C5 device
- 66-MHz oscillator
- Temperature sensor
- Four user-definable push-button switches
- Four user-definable LEDs
- 16×2 character LCD
- SRAM

Interfaces

The MAX II development board contains the following interfaces:

- USB Interface
 - V1.1 or V2.0
 - Type B connector
- 32-bit PCI edge connector
- Altera[®] expansion prototype header
- Prototyping area

General Description

The MAX II development board provides a hardware platform designers can use to evaluate MAX II device features and to prototype CPLD designs.

Components & Interfaces

Figure 1 shows a top view of the board components and interfaces.

Figure 1. MAX II Development Board Top View

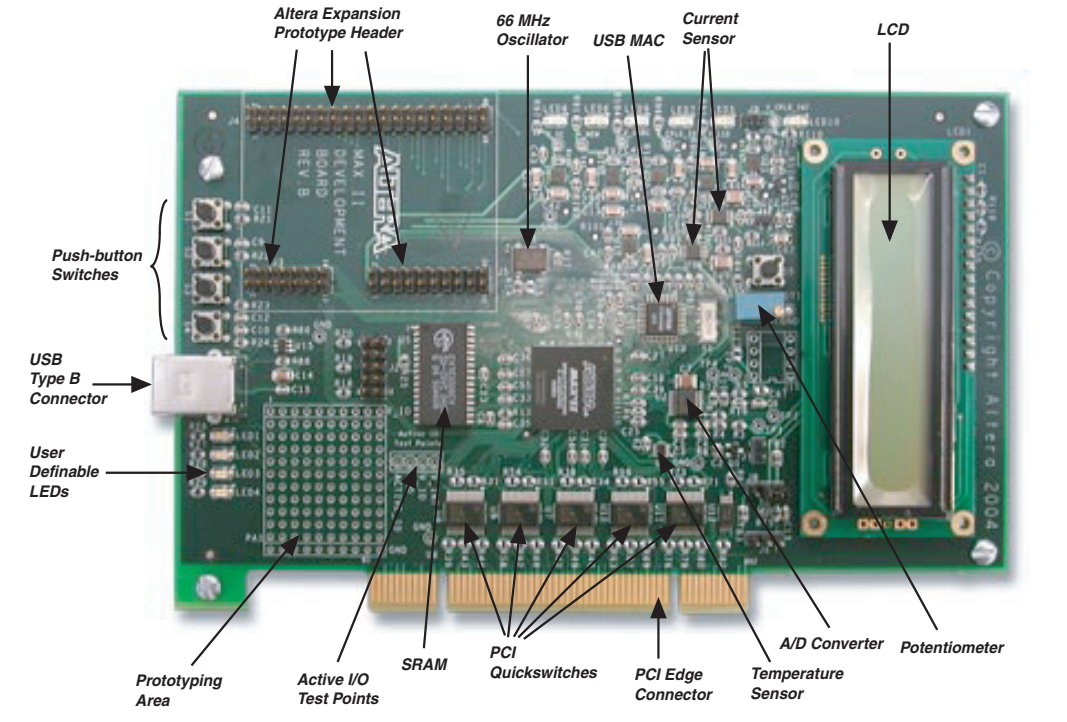


Table 1 describes the components on the board and the interfaces it supports.

Table 1. MAX II Development Board Components & Interfaces			
Component/Interface	Type	Board Designation	Description
Circuits			
Active I/O sensor	Circuit	Active I/O test points	Circuit for investigating MAX II power optimization
Current sensor	Circuit	U2, U19, U23	Power measuring circuit
Schmitt trigger	Circuit	R13, C8	RC circuit for investigating the internal Schmitt trigger in MAX II devices
Components			
66-MHz oscillator	Clock	U3	Main clock for MAX II board
Temperature sensor	I/O	U1	Allows designer to measure board temperature
User push-button switches	Input	S1, S2, S3, S4	User-definable push-button switches
User LEDs	Output	LED1, LED2, LED3, LED4	User-definable LEDs
Status LEDs	Status	LED5, LED6, LED7, LED8, LED9, LED10	Indicate which components are receiving power
LCD	I/O	LCD1	On-board LCD
SRAM	Memory	U5	1 Mbit of SRAM
PCI quickswitches	I/O	U7, U8, U9, U10, U11	Convert 5.0-V PCI signals into 3.3-V signals
Potentiometer	I/O	POT1	Adjusts the load on the V_{CCINT} plane
Interfaces			
USB	I/O	U13	Universal serial bus media access controller
PCI	I/O	B1, B62, A1, A62	PCI edge connector
Altera Expansion Prototype Header	I/O	J3, J4, J5	Daughter card header
Prototyping area	I/O	PA1	Allows designer to add custom components to the MAX II development board

Environmental Requirements

The MAX II development board must be stored between -40°C and 100°C . The recommended operating temperature is between 0°C and 55°C .



The MAX II development board can be damaged without proper anti-static handling.

Using the Board

This section provides information on using the MAX II development board.

Apply Power

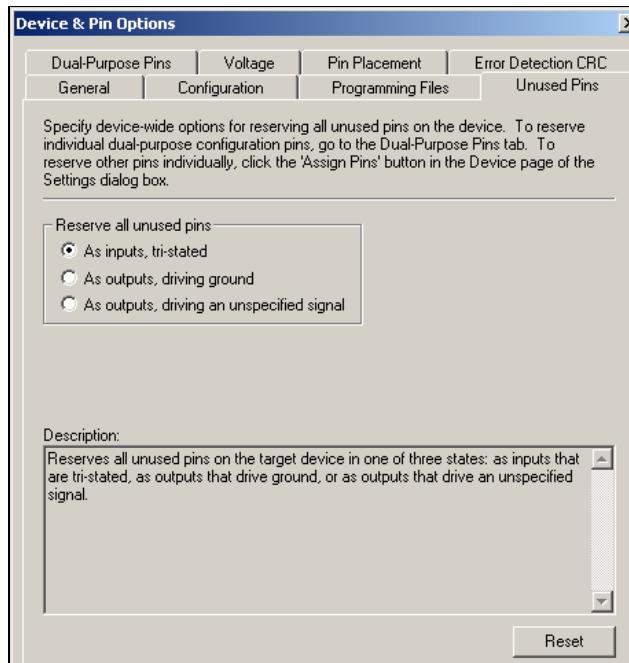
Power can be applied to the board from the USB or PCI bus. Jumper J8 controls which source supplies power. If the shunt is on pins 1 and 2, the board will be powered via the USB bus. If the shunt is on pins 2 and 3, the board will be powered via the PCI bus. Pin 1 of J8 is the pin closest to the LCD. When the board is powered up, the LED power indicators (LEDs 5, 6, 7, 8, 9, and 10) will illuminate.

Program the MAX II Device

The MAX II device on the MAX II development board can be programmed using the Quartus® II software. To program the board, the designer must supply power as indicated above and then connect the ByteBlaster™ cable to the 10-pin JTAG header on the board (J2). More detail on programming MAX II devices is available in the *MAX II Development Kit Getting Started User Guide* and Quartus II Help.



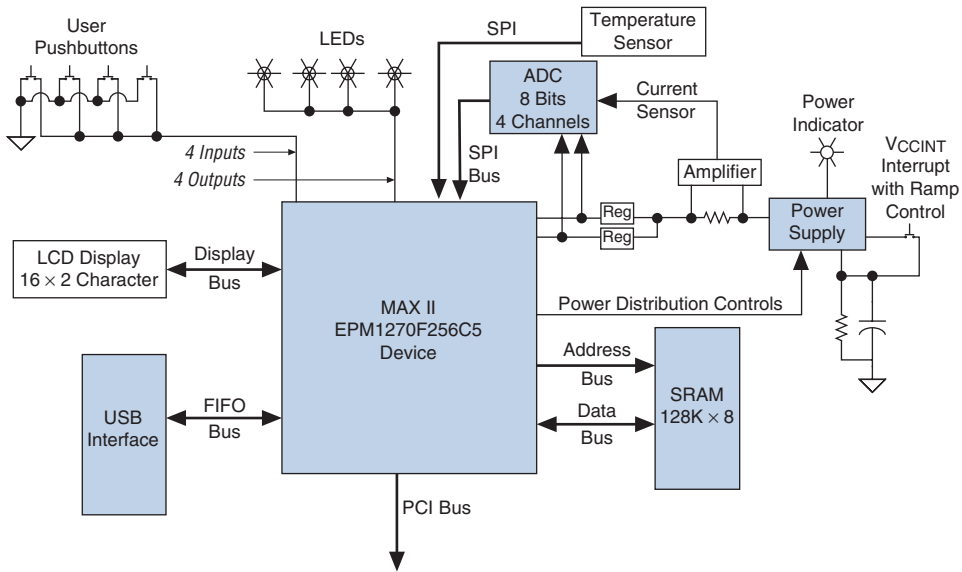
The Quartus II software default setting in the **Unused Pins** tab leaves unused pins as outputs, driving ground. When compiling designs that target Altera development boards, change this setting so that unused pins act as inputs and are tri-stated. The reason for this change is that components on the board may be damaged by having GND signals driven onto pins that drive V_{CC} . However, if you set these unused pins to behave as inputs and they are tri-stated, then they will not damage the board. To change this option in the Quartus II software, select **Settings** (Assignments menu). In the menu on the right, click **Device**, then click **Device and Pin Options**. In the **Device & Pin Options** dialog box, click the **Unused Pins** tab. Ensure this option is set to **As inputs, tri-stated**. See [Figure 2](#).

Figure 2. Quartus II Device & Pin Options Dialog Box

Functional Description

This section describes the components of the MAX II development board. [Figure 3](#) shows a block diagram of the board. See [Figure 1 on page 2](#) for a photograph of the board, which shows the names and locations of all board features.

Figure 3. MAX II Development Board Block Diagram



Power

You can power the MAX II development board from either the PCI bus or the USB bus. If you are not using the board in the PCI slot of a PC, then you must power the board from the USB bus. Jumper J8 is used to select which bus powers the board. If the shunt is on pins 1 and 2, the board will be powered via the USB bus. If the shunt is on pins 2 and 3, the board will be powered via the PCI bus. Pin 1 of J8 is the pin closest to the LCD.

The PCI bus or the USB bus routes the power to six different regulators, which power individual board components. The MAX II device is powered from either a 2.5-V or a 3.3-V power supply. You select which supply voltage to use (for V_{CCINT}) by using jumper J9. The slew rate (or load) of V_{CCINT} can be adjusted by the potentiometer (POT1).

Power-Up Sequence

When you apply power to the MAX II development board, the 5.0-V power supply powers up first, because it is the source for the 3.3-V/2.5-V power supply. The 3.3-V/2.5-V V_{CCINT} supply powers up second. You can increase or decrease the rate at which the V_{CCINT} supply comes up by

increasing or decreasing the value of the potentiometer (POT1). The MAX II device enables the regulators, which supply power to the LCD, Altera Expansion Prototype Header, and memory device.

The outputs from the MAX II device power the ADC and the temperature sensor because they require very little current. Those components power up last (and at roughly the same time) because they depend upon outputs of the MAX II device to get power. [Figure 4](#) shows a block diagram of power distribution on the board.

Figure 4. Power Supply Distribution Block Diagram

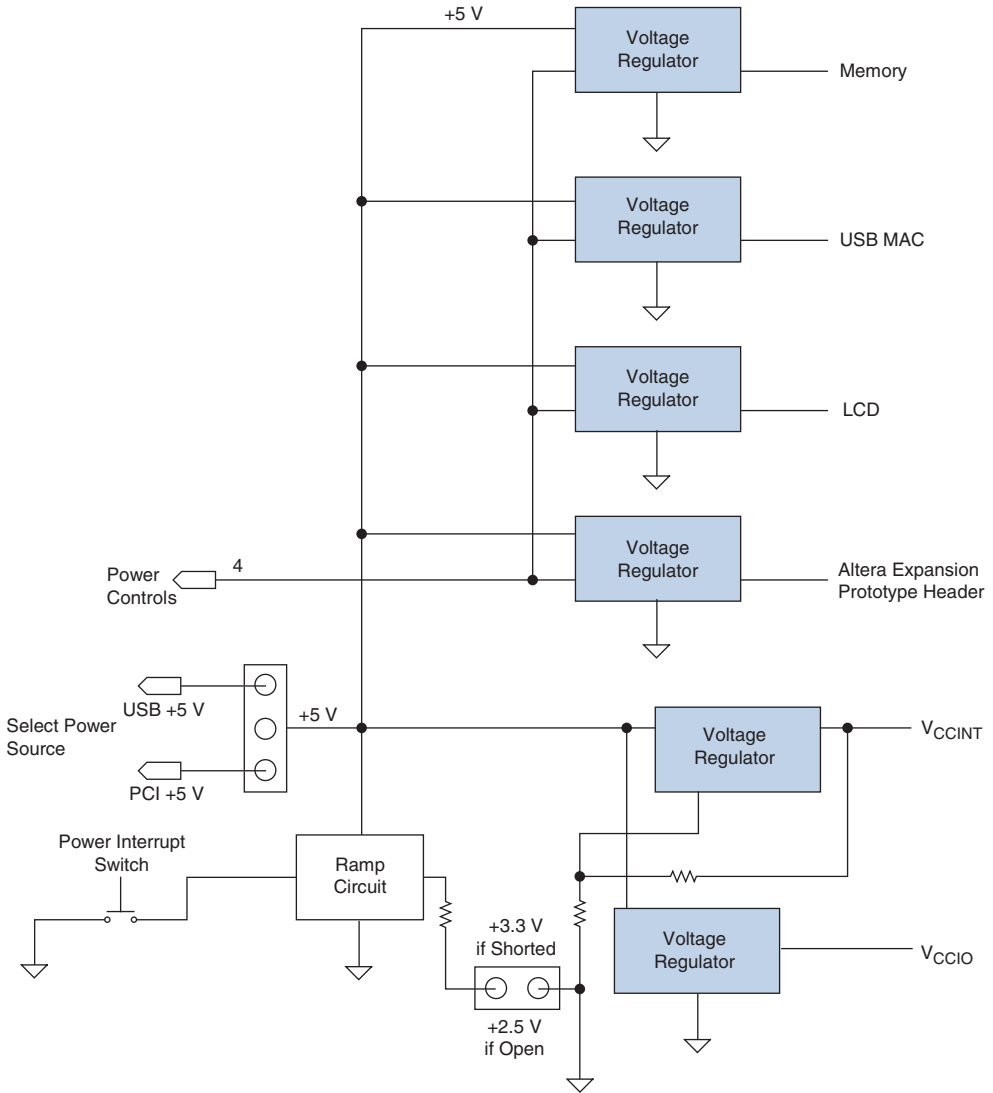


Table 2 provides information on the MAX II development board voltage regulator.

Parameter	Definition
Board References	U14, U16, U17, U18, U20, U21
Part Number	LP3982ILD-ADJ
Device Description	Adjustable linear voltage regulator
Manufacturer	National Semiconductor
Manufacturer Web Site	www.national.com

Power Budget

Table 3 shows the typical and maximum power requirements of the main components on the MAX II development board.

Description	MFG	MFG Part Number	Quantity	+3.3 V	
				Typical Current (mA)	Maximum Current (mA)
MAX II device	Altera	EPM1270F256C5	1	N/A	225
SRAM	Cypress	CY7009B	1	5	70
LCD	Crystalfontz	CFAH1602B-NYA-JP	1	2	2
Oscillator	ECS	ECS-3953C-666-TR	1	25	25
ADC	Maxim	MAX1111	1	0.1	0.25
Current sensor	Maxim	MAX4072	2	0.1	0.25
Temperature sensor	Maxim	MAX6642	1	0.5	1
USB	FTDI	FT245BM	1	25	–
Regulator	National Semiconductor	LM38982	6	0.1	0.27
TOTAL [A]				0.376	
TOTAL [W]				1.241	
Total +5 V power [W]				1.880	
Total watts (entire board)				1.88	

Table 4 shows the pin-outs for the power supply enable signals for each of the components on the board.

Signal	MAX II Pin
V_LCD_ENA	B3
V_MEM_ENA	A2
V_SC_ENA	B1

MAX II Device

The MAX II device (EPM1270) on the board features 1270 logic elements (LEs) and 8 Kbit of user flash memory in a 256-pin FBGA package.



For more information on MAX II device features, see the *MAX II Device Family Data Sheet* section in the *MAX II Device Handbook*.

Table 5 describes the features of the MAX II device.

Item	Description
Logic Elements (LEs)	1,270
User Flash Memory	8 Kbit
User I/O Pins	206
Board Reference	U4
Internal Voltage	Variable (2.5 V or 3.3 V)

Clocks & Clock Distribution

The main user clock on the board is the 66 MHz oscillator. [Table 6](#) describes this component.

Table 6. 66 MHz On-Board Oscillator Reference	
Item	Description
Board Reference	U3
Part Number	ECS-3953C-666
Device Description	66 MHz Crystal Oscillator
Manufacturer	ECS Inc.
Manufacturer Web Site	www.ecsxtal.com

[Table 7](#) lists the clocks available on the MAX II development board. There are four different clocks on the board.

Table 7. Clock Signal Distribution		
Clock	Source	Destination
66 MHz Oscillator	On-board oscillator (U3)	MAX II device, pin H5
6 MHz Resonator	On-board resonator (Y1)	USB MAC (U13, pins 26 and 27)
PCI Clock	PCI edge connector	MAX II device, pin H12
Altera Expansion Prototype Header	Altera expansion header (J3, J4, J5)	MAX II device, pin J5

Reset

The MAX II device handles the reset for the board internally. The S1 push-button switch connects to the `DEV_CLRn` pin of the MAX II device, which may be a user-defined I/O or a reset input.

Board Components

The following sections describe the development board components.

Push-Button Switches

The board has five user push-button switches (S1, S2, S3, S4, and S5). S1 connects to the DEV_CLRn pin of the MAX II device. S5 interrupts the MAX II V_{CCINT} power supply. [Table 8](#) describes the push-button switches.

<i>Table 8. Push-Button Switches Reference</i>	
Item	Description
Board References	S1, S2, S3, S4, S5
Part Number	EVQPAC07K
Device Description	Push-button switches
Manufacturer	Panasonic
Manufacturer Web Site	www.panasonic.com

[Table 9](#) shows the pin-outs for the push-button switches.

<i>Table 9. Push-Button Switch Pin-Outs</i>		
Signal Name	Description	MAX II Pin
S1	Reset, DEV_CLRn	M9
S2	User defined	R14
S3	User defined	T15
S4	User defined	R16
S5	Power interrupt	None

LEDs

The MAX II development board has the following LEDs:

- Four user-definable LEDs that connect to outputs from the MAX II device
- Six power indicator LEDs, one for each main component on the board

Table 10 describes the LEDs.

Table 10. LED Reference	
Item	Description
Board References	LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10
Part Number	LTST-C150CKT
Device Description	LED
Manufacturer	Lite-on Industry
Manufacturer Web Site	www.liteon.com

Table 11 shows the pin-outs for the LEDs.

Table 11. LED Pin-Outs		
Signal Name	Description	MAX II Pin
LED1	User-defined	T13
LED2	User-defined	R13
LED3	User-defined	P13
LED4	User-defined	T12
LED5	LCD power indicator	N/A
LED6	SRAM power indicator	N/A
LED7	V _{CCIO} power indicator	N/A
LED8	Altera Expansion Prototype Header power indicator	N/A
LED9	USB power indicator	N/A
LED10	V _{CCINT} power indicator	N/A

LCD

The liquid crystal display (LCD) is a 16 × 2 character display from either Crystalfontz (CFAH1602B-NYA-JP) or AZD.

Table 12 describes the Crystalfontz LCD.

Table 12. Crystalfontz LCD Reference	
Item	Description
Board Reference	LCD1
Part Number	CFAH1602B-NYA-JP
Device Description	LCD
Manufacturer	Crystalfontz
Manufacturer's Web Site	www.crystalfontz.com

Table 13 describes the AZD LCD.

Table 13. AZD LCD Reference	
Item	Description
Board Reference	LCD1
Part Number	ACM1602-RN-GBS
Device Description	LCD
Manufacturer	AZD
Manufacturer's Web Site	www.az.azdisplays.com

Table 14 shows the pin-outs for the LCD.

Table 14. LCD Pin-Outs (Part 1 of 2)		
Signal Name	Description	MAX II Pin
LCD_DB0	Data Bus	B10
LCD_DB1	Data Bus	C10
LCD_DB2	Data Bus	D10
LCD_DB3	Data Bus	A9
LCD_DB4	Data Bus	B9
LCD_DB5	Data Bus	C9
LCD_DB6	Data Bus	D9

Table 14. LCD Pin-Outs (Part 2 of 2)

Signal Name	Description	MAX II Pin
LCD_DB7	Data Bus	A8
LCD_E	Enable	A10
LCD_RS	Data/Instruction Select	C11
LCD_RW	Read/Write Select	D11

Current Sensor Amplifier

You measure current to the MAX II development board by using an on-board Maxim MAX4072 high-side current sense amplifier with a pair of 0.33- Ω resistors in parallel as the sensing element. This has a maximum voltage drop of 41 mV at 250 mA. At high current levels, the resolution with an 8-bit converter is roughly 1 mA.

The current sensor is located upstream from the regulators for the V_{CCINT} and V_{CCIO} voltages so that only one of the voltages is required to measure all of the current of the MAX II development board. The output of the Maxim MAX4072 amplifier feeds the analog-to-digital converter (ADC). See “[Analog/Digital Converter](#)” on page 16. The output of the ADC feeds the MAX II device.

The current drawn by the MAX II device can also be determined by measuring the voltage across R109 or R113 (for V_{CCINT}) and R95 or R99 (for V_{CCIO}). The resistance value from the two 0.33- Ω resistors in parallel is 0.165 Ω .

$$I_{VCCINT} = (V_{R109}/0.165) = (V_{R113}/0.165)$$

$$I_{VCCIO} = (V_{R95}/0.165) = (V_{R99}/0.165)$$

Table 15 describes the current sensor.

Table 15. Current Sensor Reference

Item	Description
Board References	U19, U23
Part Number	MAX4072AUA
Device Description	Current Sense Amplifier
Manufacturer	Maxim
Manufacturer Web Site	www.maxim-ic.com

Table 16 shows the pin-outs for the current sensor.

Table 16. Current Sensor Pin-Outs		
Signal Name	Description	MAX II Pin
GSEL_Int	Gain Select for V_{CCINT} (U23)	A4
GSEL_IO	Gain Select for V_{CCIO} (U19)	D4
IO_V_ADC	Enables power supply to the ADC and Current Sensors	A13

Analog/Digital Converter

The analog-to-digital converter (ADC) is a Maxim MAX1111 device. It has a Serial Peripheral Interface (SPI) that provides eight bits of resolution on four channels. It also provides the reference voltage for the current sensor amplifier. Table 17 describes the ADC.

Table 17. 8-Bit, 4-Channel ADC Reference	
Item	Description
Board Reference	U2
Part Number	MAX1111
Device Description	Analog-to-digital converter
Manufacturer	Maxim
Manufacturer Web Site	www.maxim-ic.com

Table 18 shows the pin-outs for the ADC.

Table 18. 8-Bit, 4-Channel ADC Pin-Outs		
Signal Name	Description	MAX II Pin
ADC_CLK	Clock	D12
ADC_CSN	Chip Select	C12
ADC_DIN	Data Input	B12
ADC_DOUT	Data Output	A11
ADC_SHDN	Three-level Shutdown Input	B11
ADC_SSTRB	Serial Strobe Output	A12
IO_V_ADC	Allows power to the ADC and Current Sensors	A13

Temperature Sensor

The temperature sensor is a Maxim MAX6627 device. It uses an SPI interface to provide the temperature reading on the board or from a remote sensor diode. Remove the Q1 component from the board to use a remote sensor so the diode can be connected across J1. [Table 19](#) describes the temperature sensor.

Table 19. Temperature Sensor Reference	
Item	Description
Board Reference	U1
Part Number	MAX6627MKA-T
Device Description	Temperature Sensor
Manufacturer	Maxim
Manufacturer Web Site	www.maxim-ic.com

[Table 20](#) shows the pin-outs for the temperature sensor.

Table 20. Temperature Sensor Pin-Outs		
Signal Name	Description	MAX II Pin
TEMP_CSN	Chip Select	B14
TEMP_SCK	Clock	C13
TEMP_SDO	Data Output	A15

SRAM

The board features 1 Mbit of SRAM. [Table 21](#) describes the SRAM.

Table 21. SRAM Reference	
Item	Description
Board Reference	U5
Part Number	CY7C1019CV
Device Description	128K × 8 SRAM
Manufacturer	Cypress
Manufacturer Web Site	www.cypress.com

Table 22 shows the pin-outs for the SRAM.

Table 22. SRAM Pin-Outs		
Signal Name	Description	MAX II Pin
A0	Address input to SRAM	T2
A1	Address input to SRAM	T4
A2	Address input to SRAM	P4
A3	Address input to SRAM	R5
A4	Address input to SRAM	N8
A5	Address input to SRAM	R9
A6	Address input to SRAM	T10
A7	Address input to SRAM	P10
A8	Address input to SRAM	R10
A9	Address input to SRAM	P9
A10	Address input to SRAM	T9
A11	Address input to SRAM	P8
A12	Address input to SRAM	T8
A13	Address input to SRAM	T5
A14	Address input to SRAM	R4
A15	Address input to SRAM	R3
A16	Address input to SRAM	R1
D0	Data to/from SRAM	R6
D1	Data to/from SRAM	N6
D2	Data to/from SRAM	R7
D3	Data to/from SRAM	N7
D4	Data to/from SRAM	P7
D5	Data to/from SRAM	T7
D6	Data to/from SRAM	P6
D7	Data to/from SRAM	T6
CEN	Chip enable to SRAM	N5
OEN	Output enable to SRAM	P5
WEN	Write enable to SRAM	R8

USB MAC/PHY

The USB MAC solution is from FTDI. This MAC supports USB versions 1.1 and 2.0 (High-speed only). If you want to use USB version 2.0, the EEPROM socket (J10) must be added to the board and populated with an EEPROM. The EEPROM should then be programmed using the utilities provided by FTDI. See the FTDI Chip web site at www.ftdichip.com for detailed instructions and for the required software and drivers. The footprint on the board is for the SAMTEC EEPROM socket, part number ICA-308-STT.

The default configuration works for USB version 1.1. FTDI's VCOM drivers provide a simple method to interface the MAX II development board to a PC. The MAX II Development Kit provides an open-source reference design using these drivers.



For more information on this reference design, refer to the *MAX II Development Kit Getting Started User Guide*.

Table 23 describes the USB MAC.

Table 23. USB MAC Reference	
Item	Description
Board Reference	U13
Part Number	FT245BM
Device Description	USB MAC
Manufacturer	FTDI
Manufacturer Web Site	www.ftdichip.com

Table 24 shows the pin-outs for the USB MAC.

Table 24. USB MAC Pin-Outs (Part 1 of 2)		
Signal Name	Description	MAX II Pin
USB_D0	Data input	A7
USB_D1	Data input	B7
USB_D2	Data input	C7
USB_D3	Data input	D7
USB_D4	Data input	A6
USB_D5	Data input	B6
USB_D6	Data input	C6

Table 24. USB MAC Pin-Outs (Part 2 of 2)

Signal Name	Description	MAX II Pin
USB_D7	Data input	D6
USB_RDN	Read FIFO	A5
USB_RXFN	Data available in FIFO	D5
USB_TXEN	USB FIFO ready to receive data from MAX II device	C5
USB_WR	Write FIFO	B5
USB_PWREN	Power enable	B4
USB_WU	Send Immediate/Wake Up	C4
USB_SK	Clock Signal to EEPROM (1)	C8
USB_CS	EEPROM Chip Select (1)	D8
USB_EEDATA	EEPROM Data (1)	B8

Note for **Table 24**:

- (1) This signal is routed directly to the MAX II device and to the (unpopulated) EEPROM at J10

PCI Edge Connector

The MAX II development board features a PCI edge connector. The board can be used in either 3.3- or 5.0-V PCI slots. This functionality is possible because the quickswitches limit the voltage in 5.0-V systems. The board is also equipped with unpopulated resistors. You can populate these resistors and remove the quickswitches if the desired voltage is 3.3 V and the quickswitches are unwanted.

The recommended method of operation in either 3.3- or 5.0-V systems is with the quickswitches in place. The MAX II Development Kit includes a reference design that implements Altera's `pci_t32` MegaCore® function on the MAX II development board. See the *MAX II Development Kit Getting Started User Guide* for more details.

Table 25 shows the pin-outs for the PCI edge connector.

Table 25. PCI Edge Connector Pin-Outs (Part 1 of 3)

Signal Name	MAX II Pin
PCI_AD[0]	C14
PCI_AD[1]	C15
PCI_AD[10]	F12
PCI_AD[11]	F13
PCI_AD[12]	F15

Table 25. PCI Edge Connector Pin-Outs (Part 2 of 3)

Signal Name	MAX II Pin
PCI_AD[13]	F16
PCI_AD[14]	G12
PCI_AD[15]	G13
PCI_AD[16]	J16
PCI_AD[17]	K12
PCI_AD[18]	K13
PCI_AD[19]	K14
PCI_AD[2]	D13
PCI_AD[20]	K15
PCI_AD[21]	K16
PCI_AD[22]	L11
PCI_AD[23]	L12
PCI_AD[24]	L16
PCI_AD[25]	M13
PCI_AD[26]	M14
PCI_AD[27]	M15
PCI_AD[28]	M16
PCI_AD[29]	N13
PCI_AD[3]	D14
PCI_AD[30]	N14
PCI_AD[9]	F11
PCI_CBEN[0]	E15
PCI_CBEN[1]	G14
PCI_CBEN[2]	J15
PCI_CBEN[3]	L15
PCI_CLK	H12
PCI_DEVSELN	H15
PCI_ENABLEN	B16
PCI_FRAMEN	J14
PCI_GNTN	P15
PCI_IDSEL	L13
PCI_INTAN	N16
PCI_IRDYN	J13
PCI_LOCKN	K11

Table 25. PCI Edge Connector Pin-Outs (Part 3 of 3)

Signal Name	MAX II Pin
PCI_PAR	G15
PCI_PERRN	H13
PCI_REQN	P14
PCI_RSTN	J12
PCI_SERRN	G16
PCI_STOPN	H14
PCI_TRDYN	H16
PCI_AD[31]	N15
PCI_AD[4]	D15
PCI_AD[5]	D16
PCI_AD[6]	E12
PCI_AD[7]	E13
PCI_AD[8]	E16

Altera Expansion Prototype Header

The Altera expansion prototype header consists of three 0.1-inch headers: one 40-pin connector (J4), one 14-pin connector (J3), and one 20-pin connector (J5). These pins are arranged as shown in [Figure 5](#). The only difference between a male and a female connector is the sex of the 0.1-inch headers.

In [Figure 5](#), NC signifies no connection. SC_40 to SC_0 are user I/O pins routed to the MAX II device. The SC_CLK2 pin is routed to GCLK1, one of two global clocks, in the MAX II device.

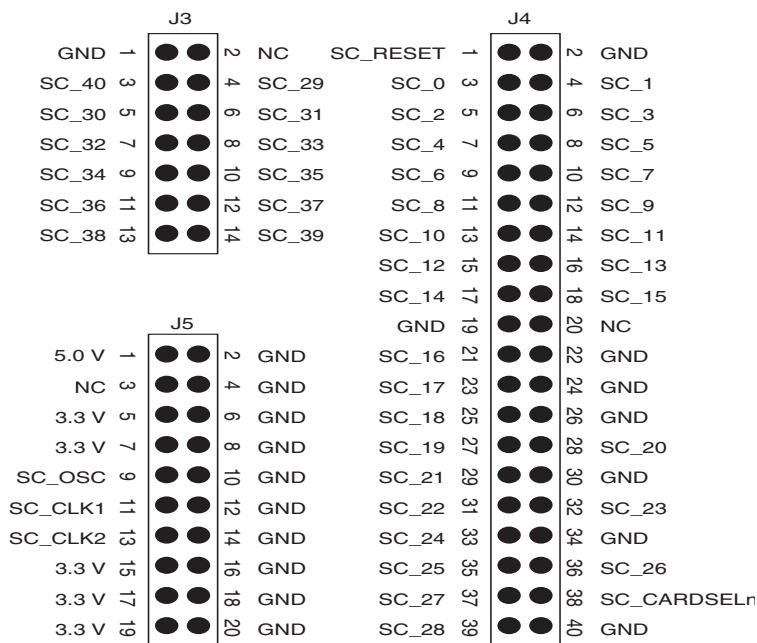
Figure 5. Altera Expansion Prototype Header Pins

Table 26 shows the pin-outs for Altera expansion prototype header pins.

Signal Name	Location	MAX II Pin
SC_CARDSELn	J4p38	H4
SC_CLK1	J5p11	L4
SC_CLK2	J5P13	J5
SC_OSC	J5p9	L3
SC_RESETn	J4p1	E5
SC_0	J4p3	C2
SC_1	J4p4	C3
SC_2	J4p5	D1
SC_3	J4p6	D2
SC_4	J4p7	D3
SC_5	J4p8	E1
SC_6	J4p9	E2

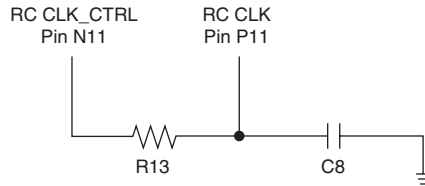
Table 26. Altera Expansion Prototype Header Pin-Outs (Part 2 of 2)

Signal Name	Location	MAX II Pin
SC_7	J4p10	E3
SC_8	J4p11	E4
SC_9	J4p12	F1
SC_10	J4p13	F2
SC_11	J4p14	F3
SC_12	J4p15	F4
SC_13	J4p16	G1
SC_14	J4p17	G2
SC_15	J4p18	G3
SC_16	J4p21	G4
SC_17	J4p23	H1
SC_18	J4p25	H2
SC_19	J4p27	H3
SC_20	J4p28	J1
SC_21	J4p29	J2
SC_22	J4p31	J3
SC_23	J4p32	K1
SC_24	J4p33	K2
SC_25	J4p35	K3
SC_26	J4p36	K4
SC_27	J4p37	L1
SC_28	J4p39	L2
SC_29	J3p4	M1
SC_30	J3p5	M2
SC_31	J3p6	M3
SC_32	J3p7	M4
SC_33	J3p8	N1
SC_34	J3p9	N2
SC_35	J3p10	N3
SC_36	J3p11	P2
SC_37	J3p12	T11
SC_38	J3p13	N10
SC_39	J3p14	R11
SC_40	J3p3	J4

Schmitt Trigger Circuit

The MAX II development board has an R-C circuit to allow designers to investigate the internal Schmitt trigger on MAX II I/O pins. [Figure 6](#) shows the circuit.

Figure 6. R-C Circuit



Active I/O Test Points



The MAX II development board provides four test points to allow the designer to analyze the timing of the MAX II device power-up and configuration.

For more information on using the test points to analyze the MAX II device power up and configuration, see the *MAX II Development Kit Getting Started User Guide*.

[Table 27](#) shows the pin-outs for the signals in this circuit.

ID	Signal	Description
V_int	3.3 or 2.5 V	+3.3-V/2.5-V power for the MAX II internal logic
V_io	3.3 V	3.3-V supply for MAX II V _{CCIO}
GND	GND	Ground plane of MAX II development board
Active IO	MAX II pin P12	MAX II user I/O pin

Prototype Section

A prototype area consisting of an array of 120 0.1-inch holes is provided. This area can be used to add custom components to the MAX II development board. Connections to both the 3.3 V plane and ground plane of the MAX II board are included. The silk-screen text on the board indicates which holes are connected to which planes. All of the other holes are not connected to anything on the board.

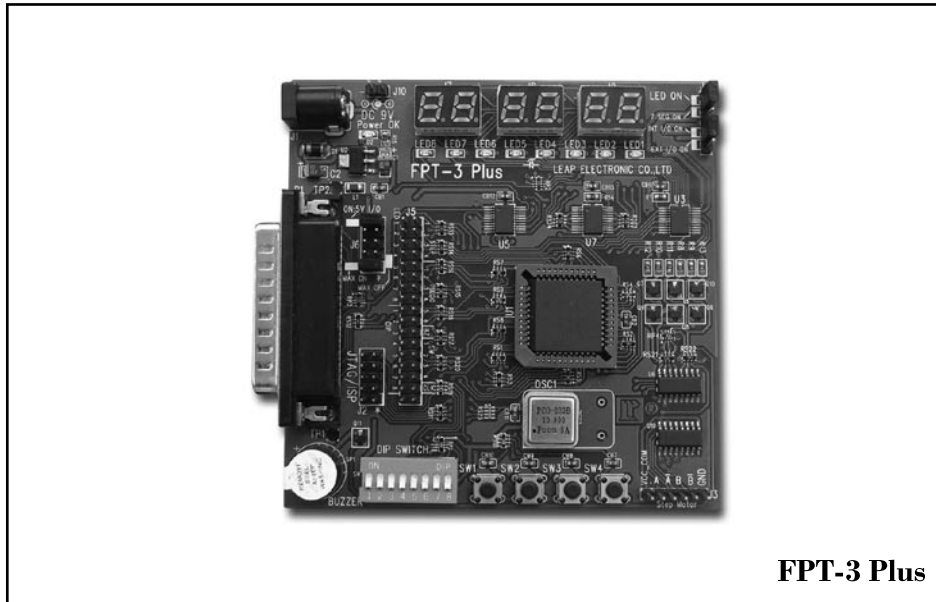


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CPLD/FPGA SIMPLE LOGIC CIRCUIT DESIGN BOARD



FPT-3 Plus

Specifications

- Support Altera CPLD MAX7000S devices series
 1. EPM7064SLC44-10
 2. PLD on EEPROM structure
 3. 5V working voltage
 4. Support 1250 logic gates and 64 LCs
 5. 32 I/O available
- System clock: 4.000MHz
- JTAG/ISP programming interface
- Dimension: 100 x 115 x 21.8 mm
- Weight: 500 g
- Input: 9V DC Adaptor

Optional Accessories

- DC 9V/500mA Adaptor
- Print-Cable (25 pin)

FPT-3 Plus offers complete interface about CPLD/FPGA circuit and design. The user is able to integrate the logical circuit design into his product easily. With utilizing the simulation and design of the products, it is easily to examine out the problems of the circuit designs. There are several learning units on the product. Through this product, the user not only can experience how to establish the technique of the circuit by the basic component, but also can utilize the auxiliary design and simulation to achieve the result in studying.

Features

- Exploit CPLD / FPGA hardware / software development system to learn the newest design of logical IC to instead of the complex hardware design of TTL/CMOS.
- Capable to use Circuit Graphic and VHDL to develop hardware circuit. Directly download the designed program from the development system to CPLD via printer port to operate independently.

Input Unit

1. 8 logic DIP switch
2. 4 sets of negative pulse press button

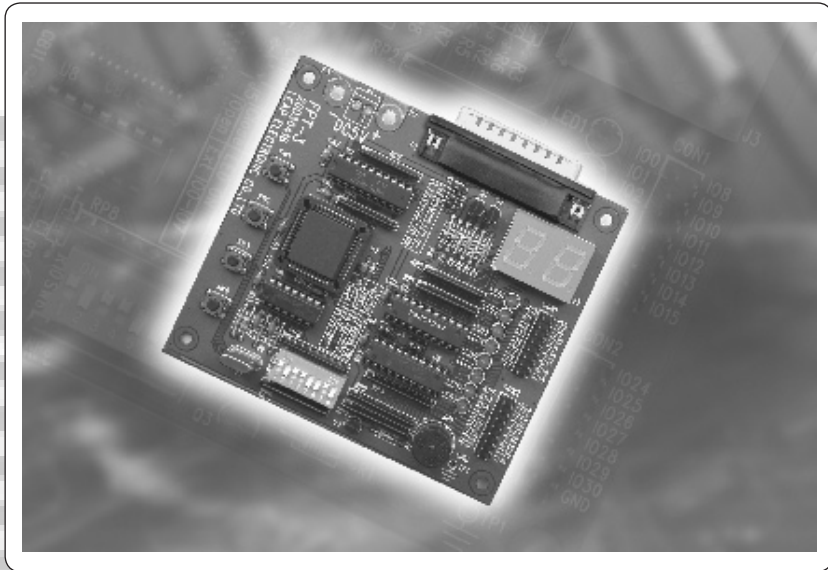
Output Unit

1. 8 SMD LED (low voltage drove)
2. 6 digits 7 segment display (Common anode: low voltage drove)
3. Buzzer x 1

Experiment Content

- Basic logic
 1. Logic experiment (DIP SW + LED)
 2. Relationship experiment (DIP SW + LED)
 3. Compiler/Decoder
- Arithmetic logic circuit
 1. Adder
 2. Subtractor
 3. Multiplexer
- Frequency divide and count
 1. 6 digits 7 segment display (Binary to Decimalism)
 2. 8 LED (Binary to Decimalism)
 3. Frequency divide test (LED)
 4. All I/O test
 5. Upward counter
 6. Traffic light display
 7. Simple electric piano
 8. Hour-Minute-Second (H-M-S) timepiece
 9. Motor Driver Controller





Features

- Exploit CPLD/FPGA hardware/software development system to learn the newest design of logical IC instead of the complex hardware design of TTL/CMOS.
- Capable to use Circuit Graphic and VHDL to develop hardware circuit.
- Directly download the designed program from the development system to CPLD via printer port to operate independently.

Specifications

- Support Altera CPLD MAX7000S devices series
- 1. EPM7064/32SLC44-10(alternative)
- 2. PLD on EEPROM structure
- 3. 5V working voltage
- 4. Support 1250 logic gates and 64 LCs
- 5. 32 I/O availably
- System clock: 1.8432MHz
- ISP programming interface
- Dimension:100 x 115 x 21.8 mm
- Weight: 500 g
- Input: 5V DC

Input Unit

- 8 logic DIP switch
- 4 sets of negative pulse press button

Output Unit

- 8 LED (low voltage drove)
- Buzzer x 1
- 2 digits 7 segment display
(Common cathode: low voltage drove)

Experiment Content

- Basic logic
 1. Logic experiment (DIP SW + LED)
 2. Relationship experiment (DIP SW + LED)
 3. Compiler/Decoder
- Arithmetic logic circuit
 1. Adder
 2. Subtractor
 3. Multiplexer
- Frequency divide and count
 1. 7 segment display
(Binary to Decimalism)
 2. 8 LED
(Binary to Decimalism)
 3. Frequency divide test (LED)
 4. All I/O test
 5. Upward counter
 6. Traffic light display
 7. Simple electric piano

Optional Accessories

- ALTERA EPM7064SLC44-10
- ALTERA EPM7032SLC44-10