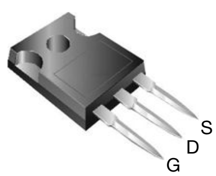
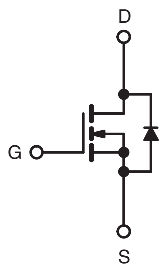
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.21
Q_g (Max.) (nC)	180	
Q_{gs} (nC)	61	
Q_{gd} (nC)	85	
Configuration	Single	

TO-247AC





N-Channel MOSFET

FEATURES

- Superfast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhanced dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Compliant to RoHS Directive 2002/95/EC

Pb Available

RoHS* COMPLIANT

APPLICATIONS

- Zero Voltage Switching (SMPS)
- Telecom and Server Power Supplies
- Uninterruptible Power Suplies
- Motor Control Applications

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFP26N60LPbF
	SiHFP26N60L-E3
SnPb	IRFP26N60L
	SiHFP26N60L

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

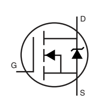
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	600	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	26	A
		T_C = 100 °C		17	
Pulsed Drain Current[a]			I_{DM}	100	
Linear Derating Factor				3.8	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	570	mJ
Repetitive Avalanche Current[a]			I_{AR}	26	A
Repetitive Avalanche Energy[a]			E_{AR}	47	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	470	W
Peak Diode Recovery dV/dt[c]			dV/dt	21	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting T_J = 25 °C, L = 1.7 mH, R_g = 25 Ω, I_{AS} = 26 A, dV/dt = 21 V/ns (see fig. 12).
c. $I_{SD} \leq$ 26 A, dI/dt $\leq$ 480 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.27	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.33	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	-	-	50	μA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125 °C	-	-	2.0	mA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 16 A[b]	-	0.21	0.25	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 16 A	13	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	5020	-	pF
Output Capacitance	C_{oss}		-	450	-	
Reverse Transfer Capacitance	C_{rss}		-	34	-	
Effective Output Capacitance	C_{oss} eff.	V_{GS} = 0 V; V_{DS} = 0 V to 480 V[c]	-	230	-	
Effective Output Capacitance (Energy Related)	C_{oss} eff. (ER)		-	170	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 26 A, V_{DS} = 480 V, see fig. 7 and 15[b]	-	-	180	nC
Gate-Source Charge	Q_{gs}		-	-	61	
Gate-Drain Charge	Q_{gd}		-	-	85	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 300 V, I_D = 26 A, R_g = 4.3 Ω, V_{GS} = 10 V see fig. 11a and 11b[b]	-	31	-	ns
Rise Time	t_r		-	110	-	
Turn-Off Delay Time	$t_{d(off)}$		-	47	-	
Fall Time	t_f		-	42	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	26	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	100	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 26 A, V_{GS} = 0 V[b]	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 26 A	-	170	250	ns
		T_J = 125 °C, dI/dt = 100 A/μs[b]	-	210	320	
Body Diode Reverse Recovery Charge	Q_{rr}	T_J = 25 °C, I_F = 26 A, V_{GS} = 0 V[b]	-	670	1000	nC
		T_J = 125 °C, dI/dt = 100 A/μs[b]	-	1050	1570	
Reverse Recovery Current	I_{RRM}	T_J = 25 °C	-	7.3	11	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.
C_{oss} eff. (ER) is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

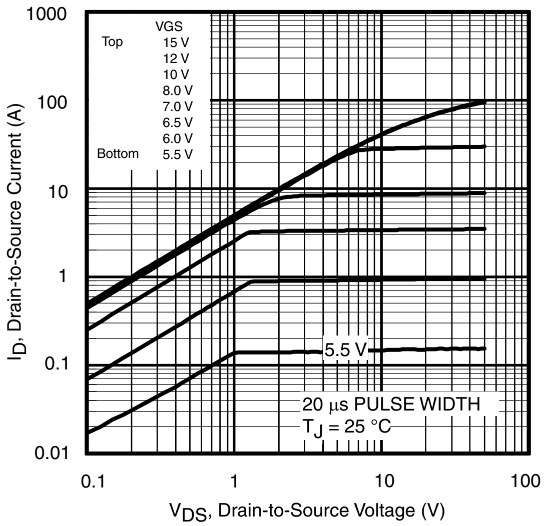


Fig. 1 - Typical Output Characteristics

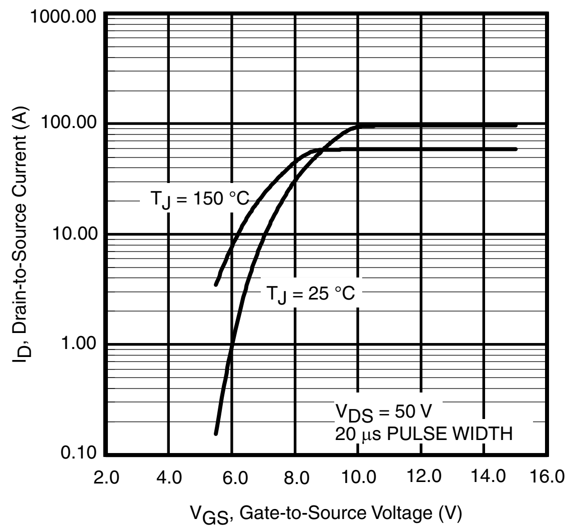


Fig. 3 - Typical Transfer Characteristics

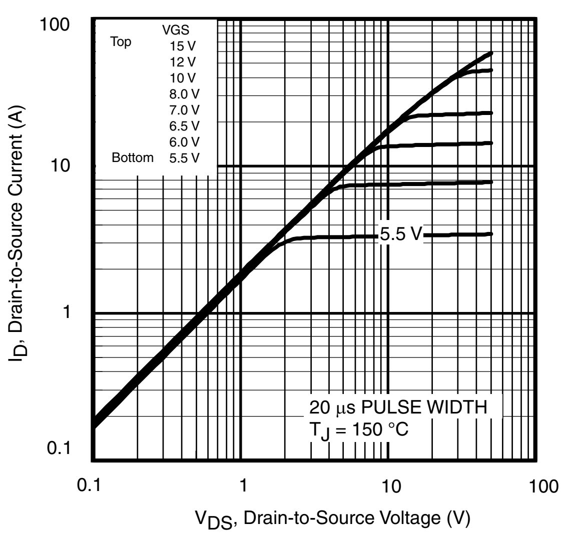


Fig. 2 - Typical Output Characteristics

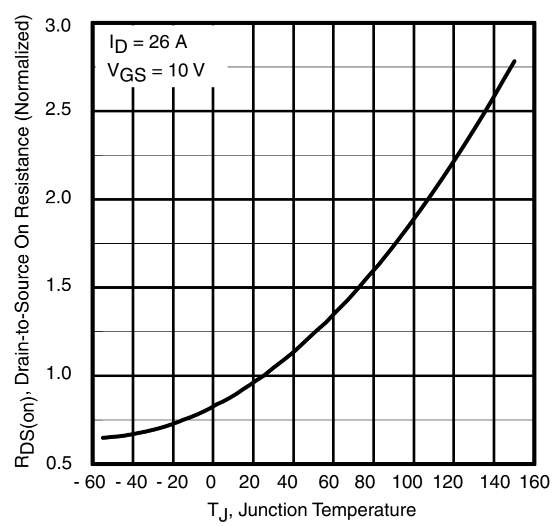


Fig. 4 - Normalized On-Resistance vs. Temperature

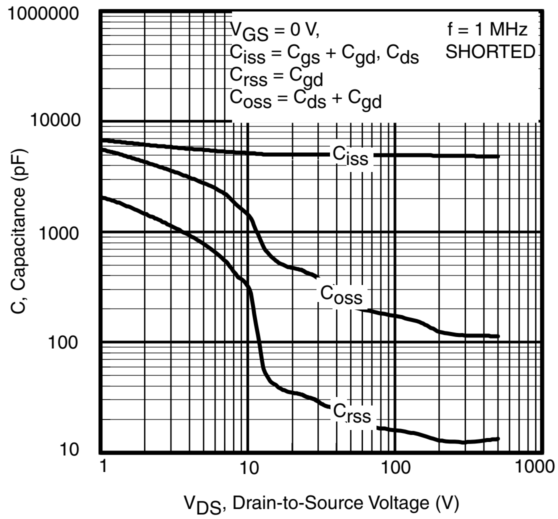


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

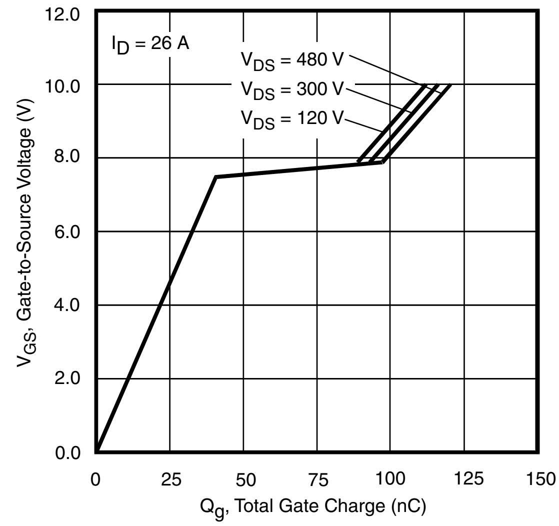


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

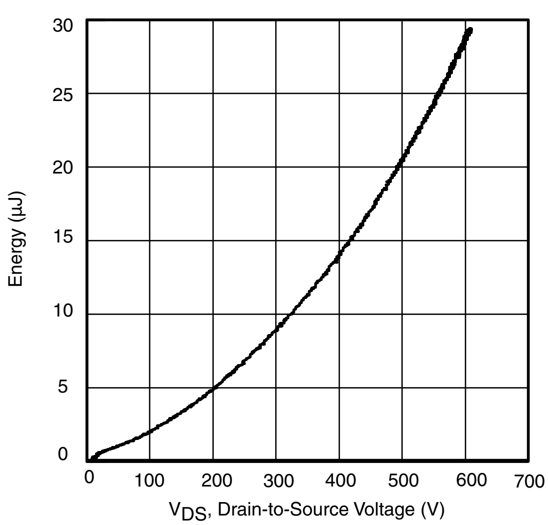


Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

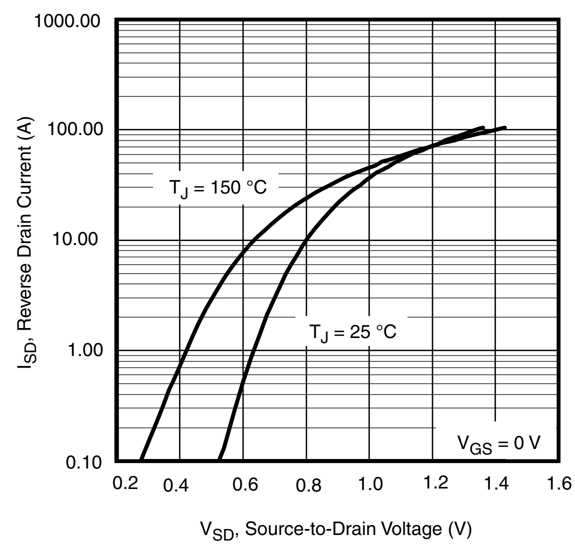


Fig. 8 - Typical Source-Drain Diode Forward Voltage

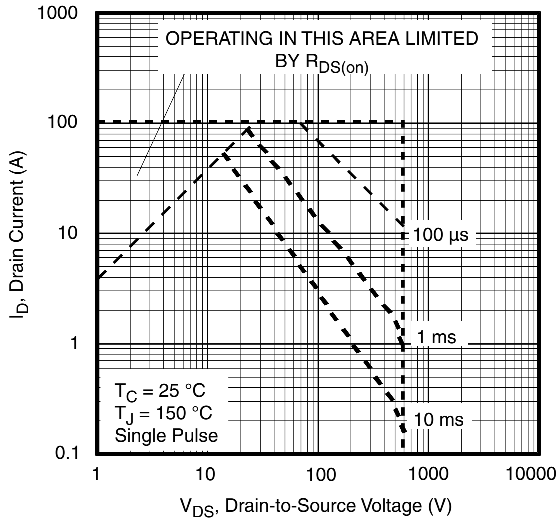


Fig. 9a - Maximum Safe Operating Area

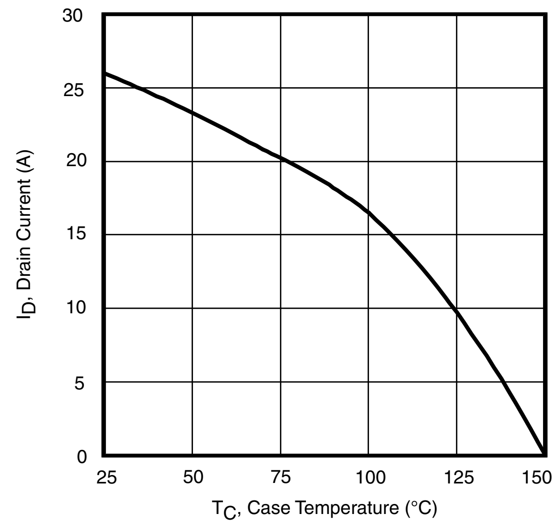


Fig. 10 - Maximum Drain Current vs. Case Temperature

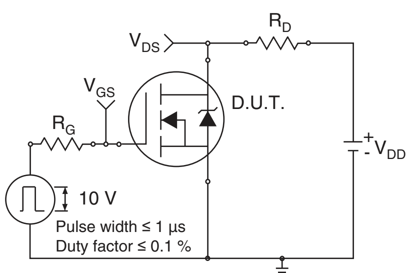


Fig. 11a - Switching Time Test Circuit

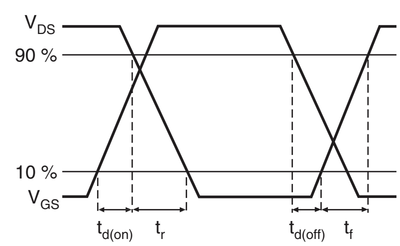


Fig. 11b - Switching Time Waveforms

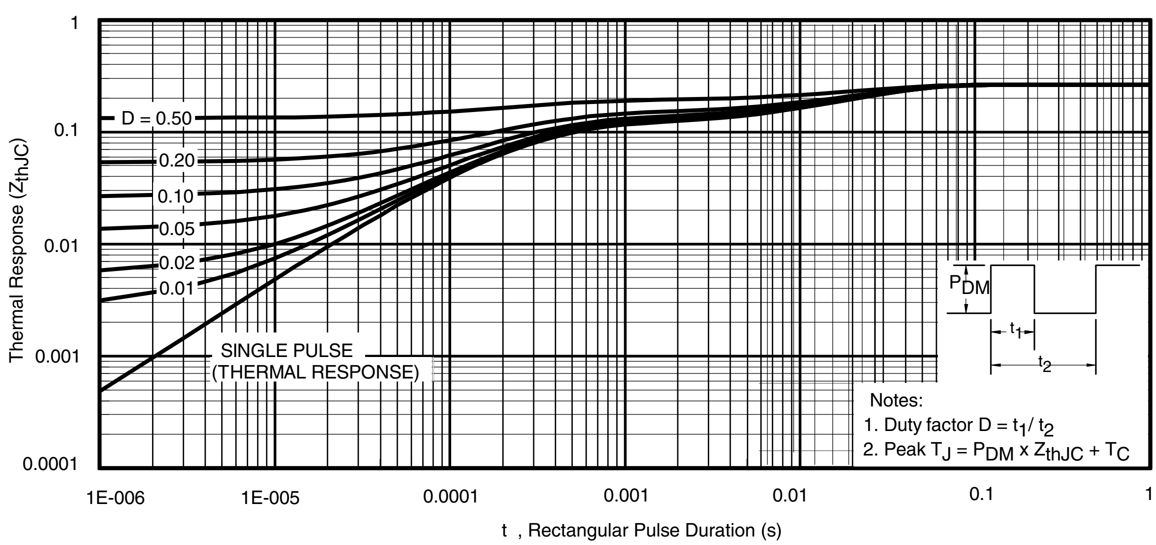


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

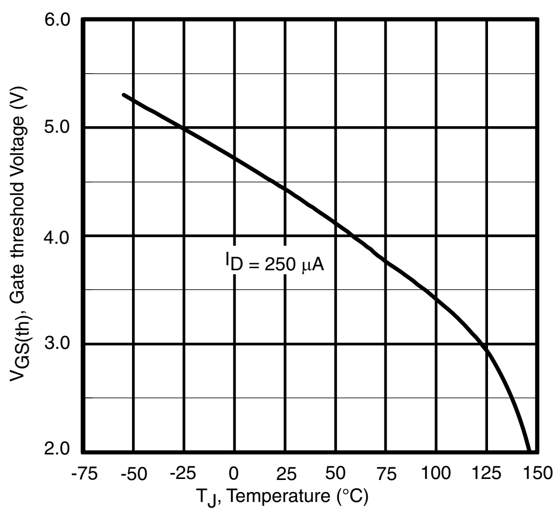


Fig. 13 - Threshold Voltage vs. Temperature

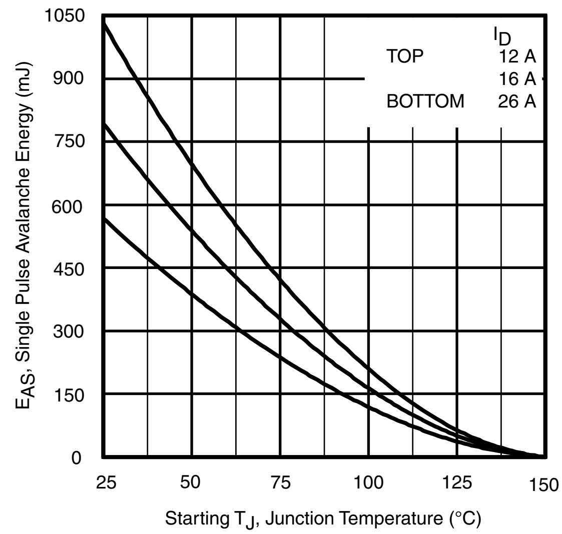


Fig. 14c - Maximum Avalanche Energy vs. Drain Current

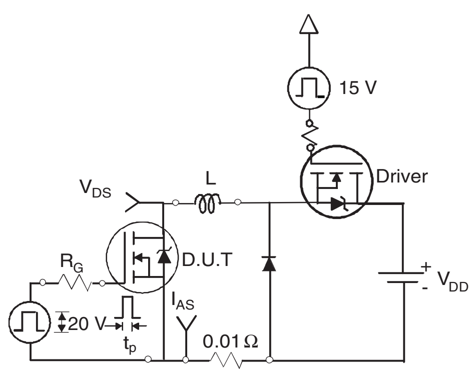


Fig. 14a - Unclamped Inductive Test Circuit

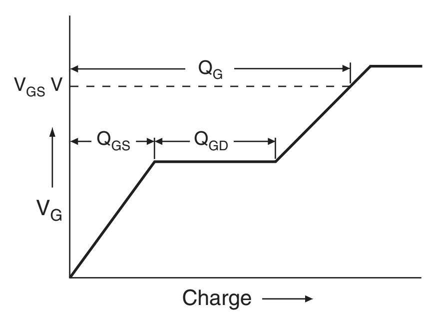


Fig. 15a - Basic Gate Charge Waveform

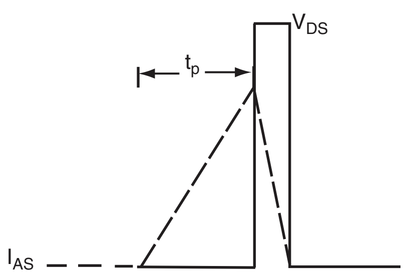


Fig. 14b - Unclamped Inductive Waveforms

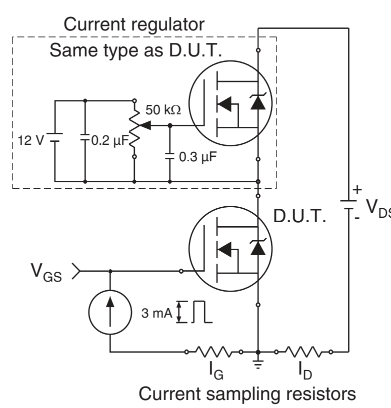
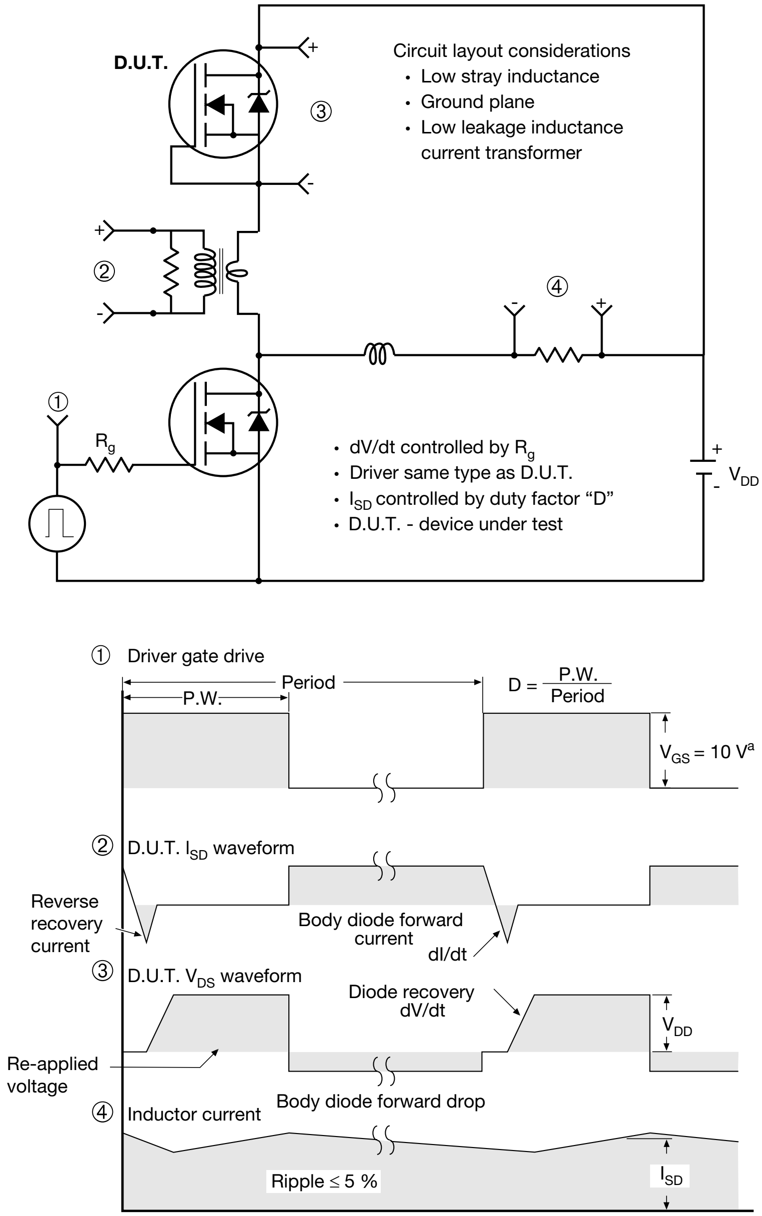


Fig. 15b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. V_{GS} = 5 V for logic level devices

Fig. 16 - For N-Channel

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