TPS84620EVM-692 6-A, Integrated Power Solution Evaluation Module

This user's guide contains background information for the TPS84620 and support documentation for the TPS84620EVM-692 evaluation module (HPA692). Also included are the performance specifications, the schematic, and the bill of materials for the TPS84620EVM-692.

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1 Introduction

1.1 Background

The TPS84620 integrated power solution is designed to provide up to a 6-A output. The TPS84620 contains dual-voltage inputs for the power stage and control circuitry. The power stage input (PVIN) is rated for 1.6 V to 14.5 V whereas the control input (VIN) is rated for 4.5 V to 14.5 V. The TPS84620EVM-692 provides both inputs but is designed and tested with PVIN connected to VIN. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS84620 regulator. The TPS84620EVM-692 default output voltage is 3.3 V at a 630-kHz switching frequency. The high-side and low-side MOSFETs are incorporated inside the TPS84620 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS84620 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are internal to the TPS84620, and external resistors and jumpers allow for adjustable output voltage and frequency adjustment. Additionally, the TPS84620 provides adjustable slow start, tracking, and undervoltage lockout inputs. The absolute maximum input voltage is 15 V for the TPS84620EVM-692.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS84620EVM-692	PVIN = VIN = 8 V to 14.5 V (Start voltage = 8 V)	0 A to 6 A

1.2 Performance Specification Summary

A summary of the TPS84620EVM-692 performance specifications is provided in Table 2. Specifications are given for an input voltage of 12 V and an output voltage of 3.3 V, unless otherwise specified. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS84620EVM Electrical and Performance Specification

Parameter	Condition		Min	Typ	Max	Units
Output Voltage	8 V ≤ PVIN = VIN ≤ 14.5 V, ILOAD ≤ ILOAD (max)	5 V 3.3 V 2.5 V 1.8 V 1.5 V 1.2 V	4.925 3.250 2.462 1.773 1.477 1.182	5.00 3.30 2.50 1.80 1.50 1.20	5.075 3.350 2.538 1.827 1.523 1.218	Volts
Output Current	8 V ≤ PVIN = VIN ≤ 14.5 V		–	–	6.0	Amps
Output ripple voltage, peak-to-peak	PVIN = VIN = 12 V, ILOAD = 6 A	5 V 3.3 V 2.5 V 1.8 V 1.5 V 1.2 V	–	12	–	mV
Switching frequency	PVIN = VIN = 12 V, ILOAD = 6 A	5 V 3.3 V 3.3 V 2.5 V 2.5 V 1.8 V 1.8 V 1.5 V 1.5 V 1.2 V 1.2 V		780 780 630 630 530 630 480 630 480 580 480		kHz

Table 2. TPS84620EVM Electrical and Performance Specification (continued)

Parameter	Condition		Min	Typ	Max	Units
Efficiency, end-to-end	ILOAD = 6 A PVIN = VIN = 12 V PVIN = VIN = 5 V PVIN = VIN = 12 V PVIN = VIN = 5 V PVIN = VIN = 12 V PVIN = VIN = 5 V PVIN = VIN = 12 V PVIN = VIN = 5 V PVIN = VIN = 12 V PVIN = VIN = 5 V PVIN = VIN = 12 V	5 V, 780 kHz 3.3 V, 780 kHz 3.3 V, 630 kHz 2.5 V, 630 kHz 2.5 V, 480 kHz 1.8 V, 630 kHz 1.8 V, 480 kHz 1.5 V, 630 kHz 1.5 V, 480 kHz 1.2 V, 580 kHz 1.2 V, 480 kHz		91% 89% 88% 87% 86% 83% 82% 81% 80% 79% 78%		
Line Regulation				±0.1%		
Load Regulation				±0.1%		
Load Transient Deviation	1 A/µs load step 50% to 100% ILOAD			60		mV
Load Transient Recovery Time	1 A/µs load step 50% to 100% ILOAD			80		µs
Operating Temperature			–40		85	°C
Slow Start				4		ms
Tracking			0 to 1.2	0 to 1.8	0 to 5	V
Synchronization			480		780	kHz

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS84620. Some modifications can be made to this module.

1.3.1 Output Voltage Setpoint

The output voltage is set using J4. The EVM default voltage is 3.3 V. To change the output voltage of the EVM, move the shunt on J4 to another position. To derive other unique output voltages, change the Rset resistor value (R2, R3, R4, R5, R6, R7, or R8) per the Rset equation in the TPS84620 data sheet (SLVSA43).

1.3.2 Slow Start Time

The slow start time can be adjusted by changing the value of C8. See the slow start table in the TPS84620 data sheet (SLVSA43) for more information. The EVM is set for a slow start time of 2.8 ms (C8 = 4700 pF and J10 installed).

1.3.3 Track In

The TPS84620 can track an external voltage during start-up. The J6 connector is provided to allow connection to an external voltage. Ratio-metric or simultaneous tracking can be implemented using the provided resistor dividers with J5. See the TPS84620 data sheet (SLVSA43) for details.

1.3.4 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted as described in the TPS84620 data sheet (SLVSA43). The EVM provides two selectable UVLO setpoints using the provided resistor dividers and J8. J9 provides an inhibit input.

1.3.5 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the PVIN and VIN inputs are connected using a jumper across J3 pins 2 and 3 (VIN=PVIN position). The single input voltage is supplied at J1. If desired, input voltage may be separated by moving the J3 jumper to pins 1 and 2 (VIN = VBIAS position). Dual input voltages must then be provided at both J1 and J2.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS84620EVM-692 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS84620EVM-692 is provided with input/output connectors and test points as shown in Table 3. A power supply capable of supplying 4 A must be connected to J1 through a pair of 20 AWG wires. The jumper across J3 must be in place. See Section 1.3.5 for split input voltage rail operation. The load must be connected to J7 through a pair of 20 AWG wires. The maximum load current capability must be 6 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP4 is used to monitor the output voltage with TP12 as the ground reference.

Table 3. EVM Connectors and Test Points

Reference Designator	Label	Description
J1	PVIN	Primary VIN connector
J2	VBIAS	VBIAS input voltage input connector
J3	VIN	Jumper used to connect VIN to PVIN. EVM default setting connects VIN to PVIN.
J7	VOUT	VOUT connector
J4	VADJ	VOUT selection. Default VOUT is 3.3 V.
J11	FREQ	Switching frequency selection. Default frequency is 630 kHz.
J6	TR_IN	TRACK IN connector. J5 provides two divider settings.
J5	SS_TR	Track voltage select jumper. Used with J6.
J9	INH_UVLO	Enable jumper. Install shunt to inhibit the power supply.
J8	INH_UVLO	Selects UVLO for power supply turn on. Default setting is for 8-V UVLO.
J10	STSEL	Internal slow start select jumper. Install shunt for internal slow start.
TP1	PVIN	PVIN circuit point
TP3	VBIAS	VBIAS circuit point
TP6	VIN	VIN circuit point
TP4	VOUT	VOUT circuit point
TP2, TP12	GND	Power grounds
TP15	AGND	Analog ground
TP7	TR_IN	Track input
TP8	SS_TR	Tracking input after divider
TP9	PWRGD	Power good status
TP14	RT/CLK	SYNC input
TP10	COMP	Error amplifier output
TP13	PH	Switch node
TP11	INH_UVLO	Inhibit and UVLO input
TP5	SENSE+	VOUT remote sense node connected to J7 pin 2. TP5 can be used for measuring the loop response along with changing R1 to 49.9 Ω.

2.2 Efficiency vs Input Voltage

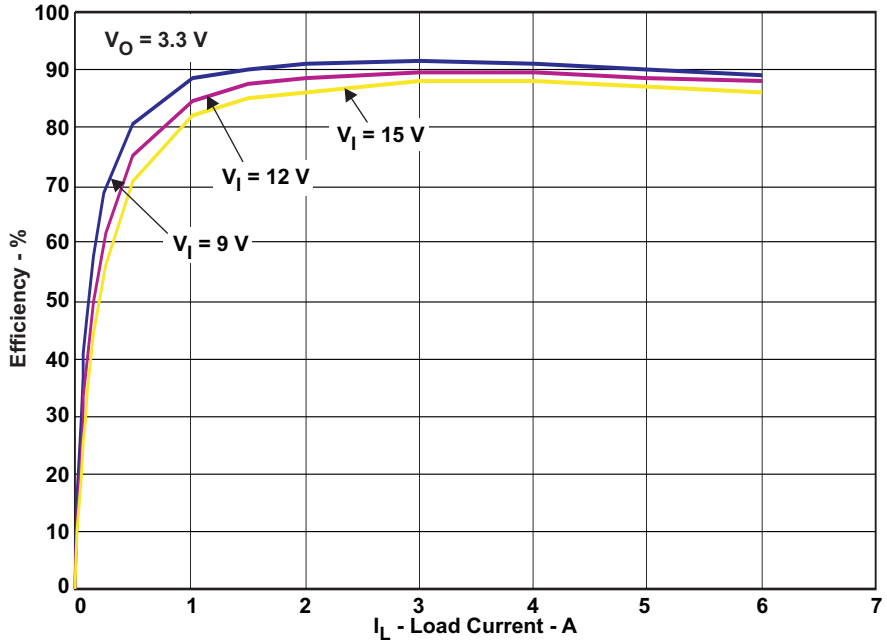

Figure 1. Efficiency vs Voltage at 25°C

2.3 Light-Load Efficiency vs Input Voltage

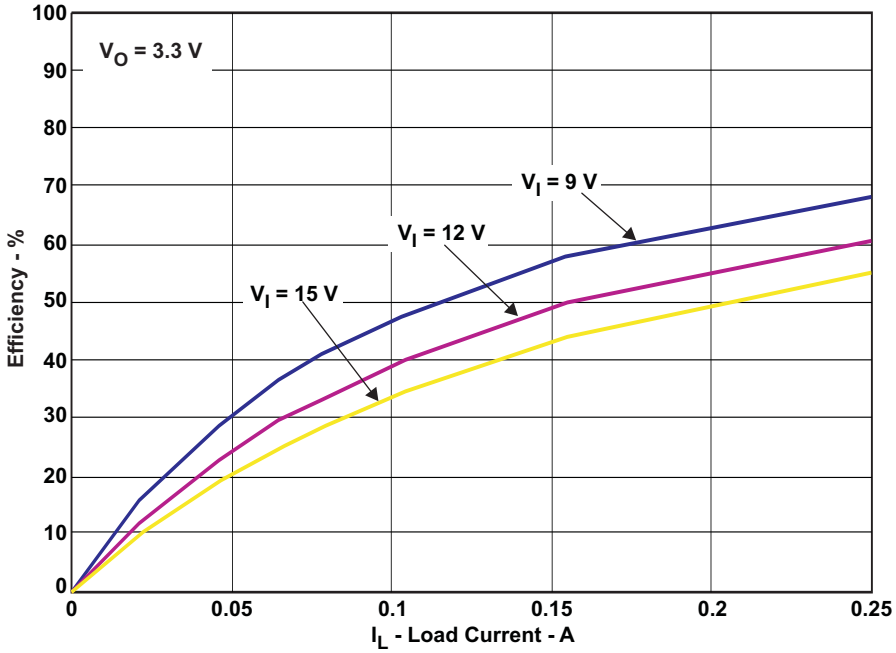

Figure 2. Light-Load Efficiency vs Input Voltage at 25°C

2.4 Efficiency vs Output Voltage/Frequency, PVIN = 12 V

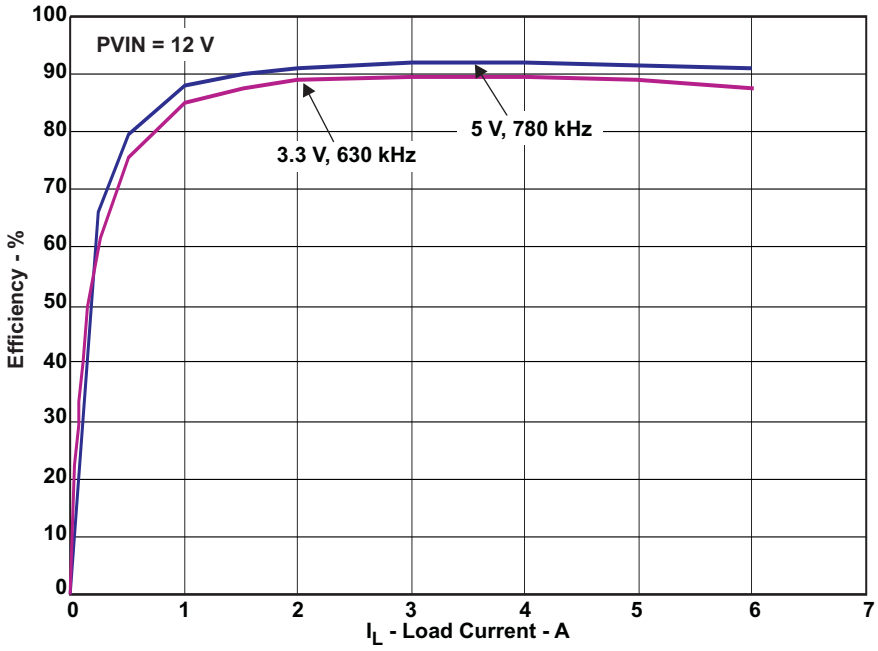

Figure 3. Efficiency vs Output Voltage at 25°C

2.5 Efficiency vs Output Voltage/Frequency, PVIN = 5 V

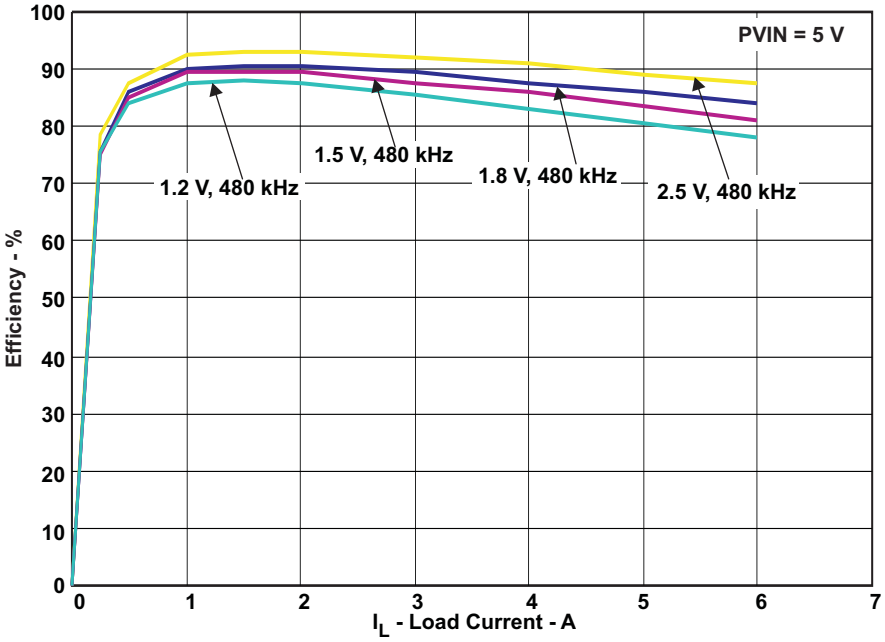

Figure 4. Efficiency vs Output Voltage/Frequency at 25°C

2.6 Output Voltage Load Regulation

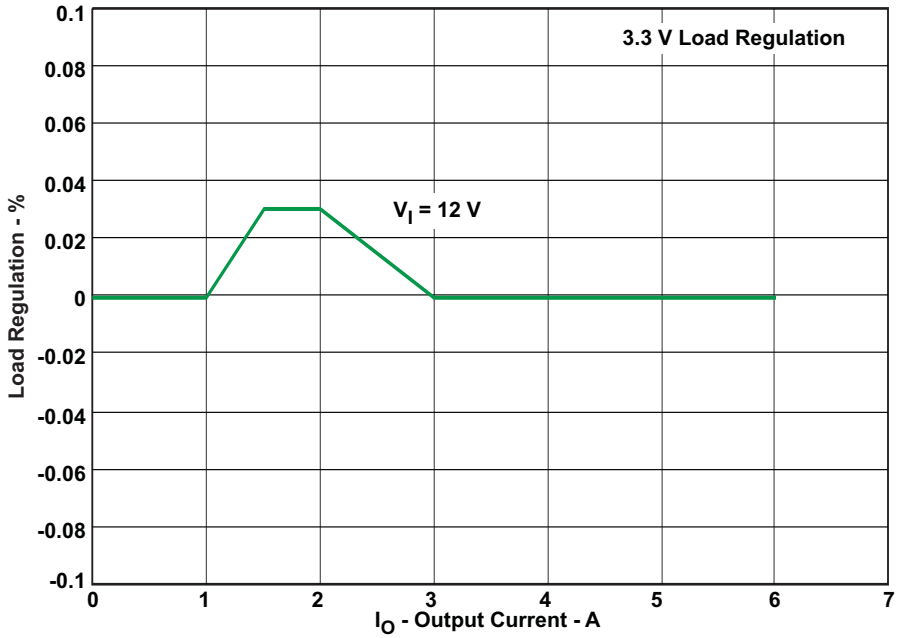

Figure 5. Load Regulation at 25°C

2.7 Output Voltage Line Regulation

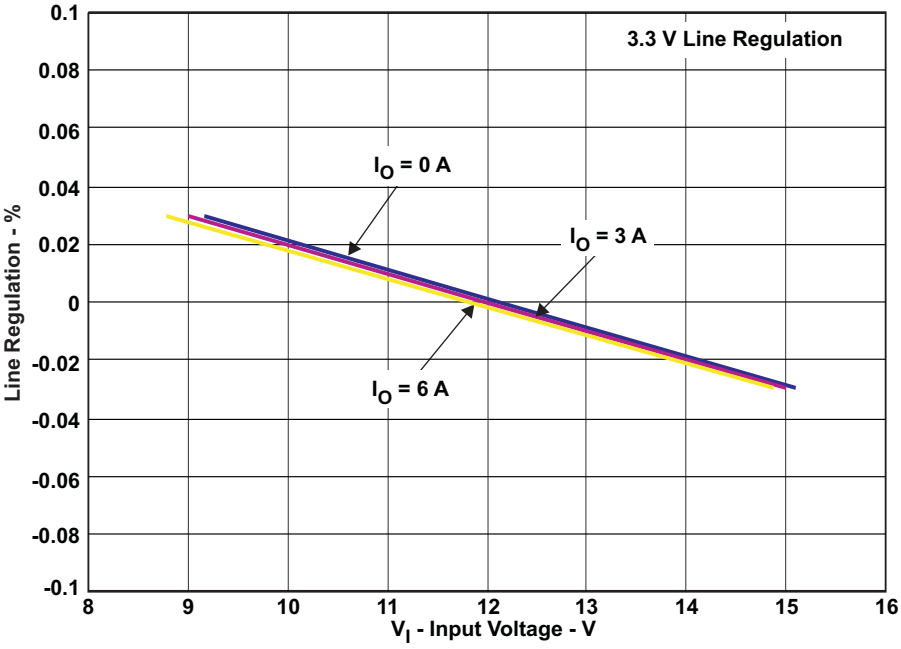

Figure 6. Line Regulation at 25°C

2.8 3.3-V TPS84620EVM-692 Response to Load Transients

Figure 7 shows the TPS84620EVM-692 response to load transients. The current step is from 1.5 A to 4.5 A at 12-V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

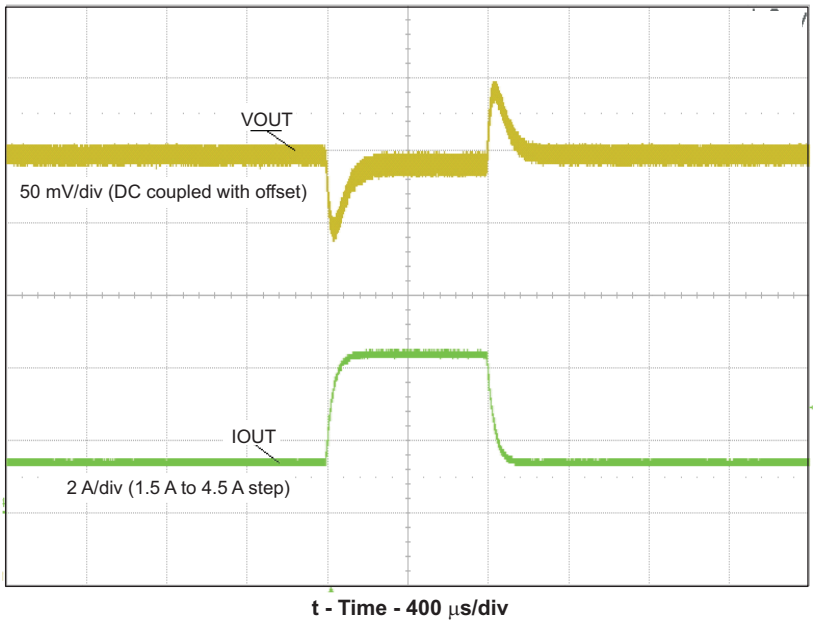

Figure 7. 3.3-V TPS84620EVM-692 Transient Response at 25°C

2.9 TPS84620EVM-692 Loop Response

Figure 8 shows the TPS84620EVM-692 loop response. The unity gain bandwidth is 50 kHz, phase margin is 70 degrees, gain margin is 19 dB and the gain slope is –1.

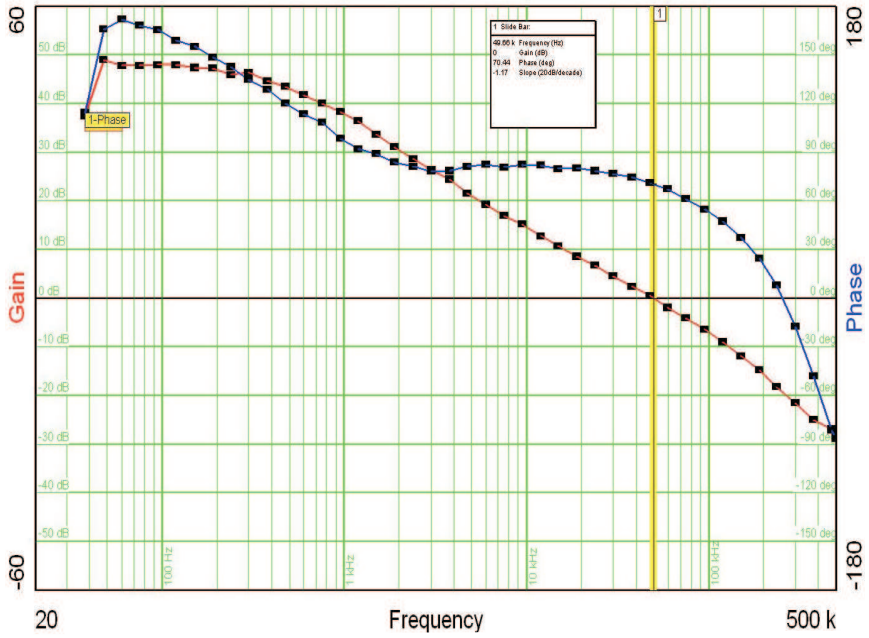

Figure 8. TPS84620EVM-692 Loop Response at 25°C

2.10 TPS84620EVM-692 Voltage Ripple

Figure 9 shows the TPS84620EVM-692 output voltage ripple when operating from 12 V with an output load of 6 A.

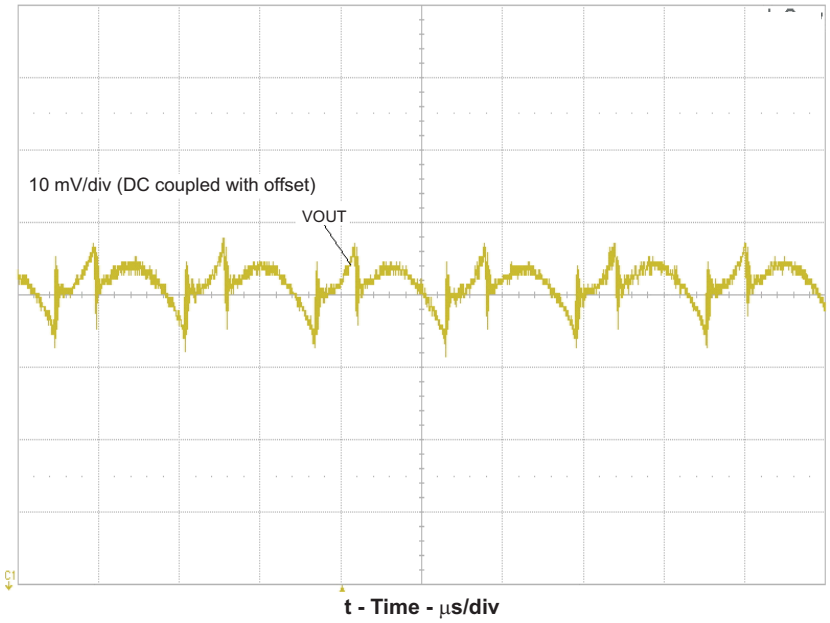

Figure 9. TPS84620EVM-692 Output Voltage Ripple

Figure 10 shows the TPS84620EVM-692 input voltage ripple when operating from 12 V with an output load of 6 A.

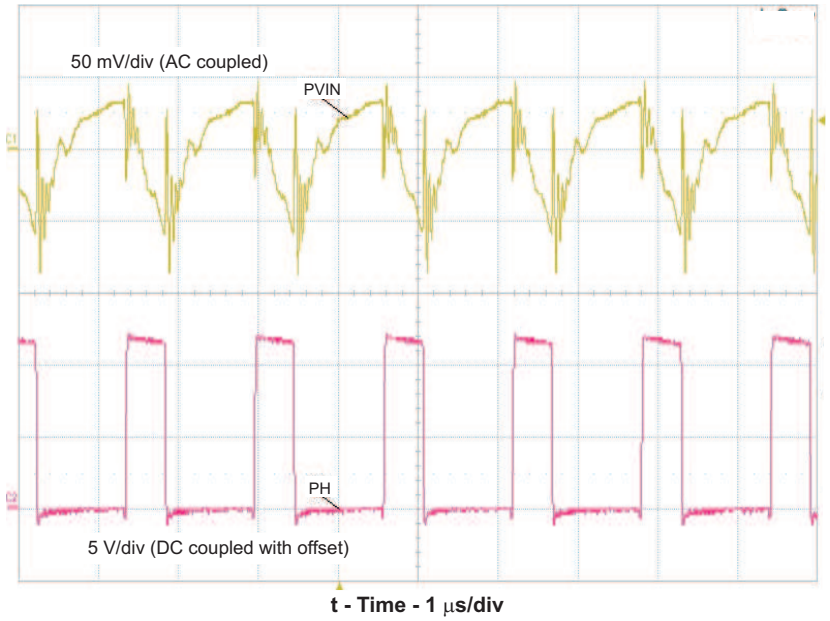

Figure 10. TPS84620EVM-692 Input Voltage Ripple

2.11 Power Up

Figure 11 shows the TPS84620EVM-692 start-up waveforms with rising PVIN. In Figure 11, the output starts to rise when PVIN reaches the rising UVLO of 8 V. J9 can also be used to inhibit VOUT when PVIN is present.

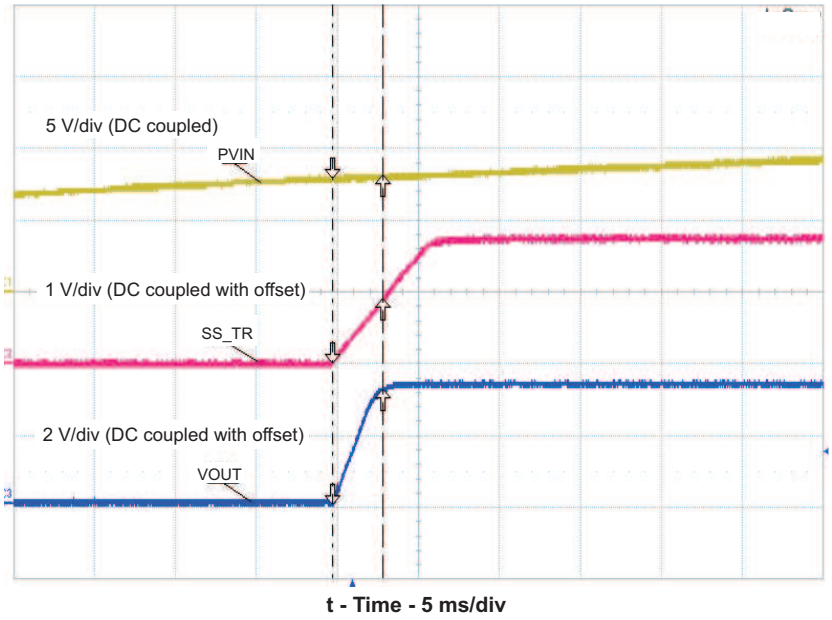

Figure 11. TPS84620EVM-692 Start-Up Waveforms With Rising PVIN

3 Board Layout

This section provides a description of the TPS84620EVM-692, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS84620EVM-692 is shown in Figure 13 through Figure 12. The topside layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper. A basic set of layout guidelines include:

- Place the input capacitors close to the PVIN and PGND terminals.
- Place the output capacitors close to the VO and PGND terminals.
- AGND is a 0-Vdc reference for the analog control circuitry. Connect AGND to PGND at a single point. AGND terminal 45 provides a means to remove heat from the device and must be connected to an AGND plane with multiple vias as shown in the TPS84620 data sheet, (SLVSA43).
- The SENSE+ pin (pin 44) provides a remote sense function for the device. Connect the SENSE+ pin to VO near the load.
- Analog control pins: Connect the analog control pins (VADJ, RT/CLK, INH/UVLO, STSEL, and SS/TR) to AGND using the recommended circuit components.

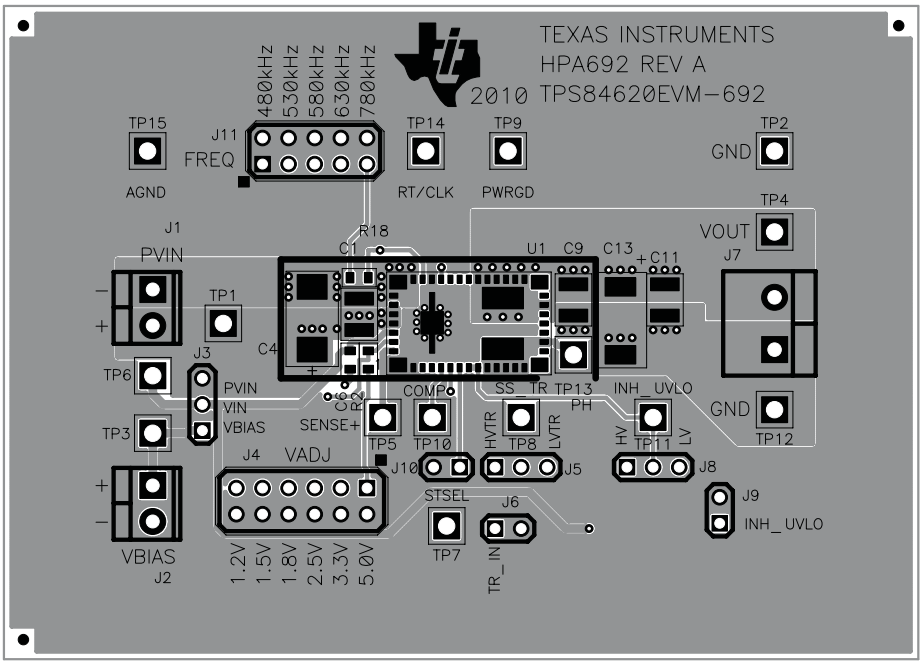

Figure 12. TPS84620EVM-692 Top-Side Layer and Assembly

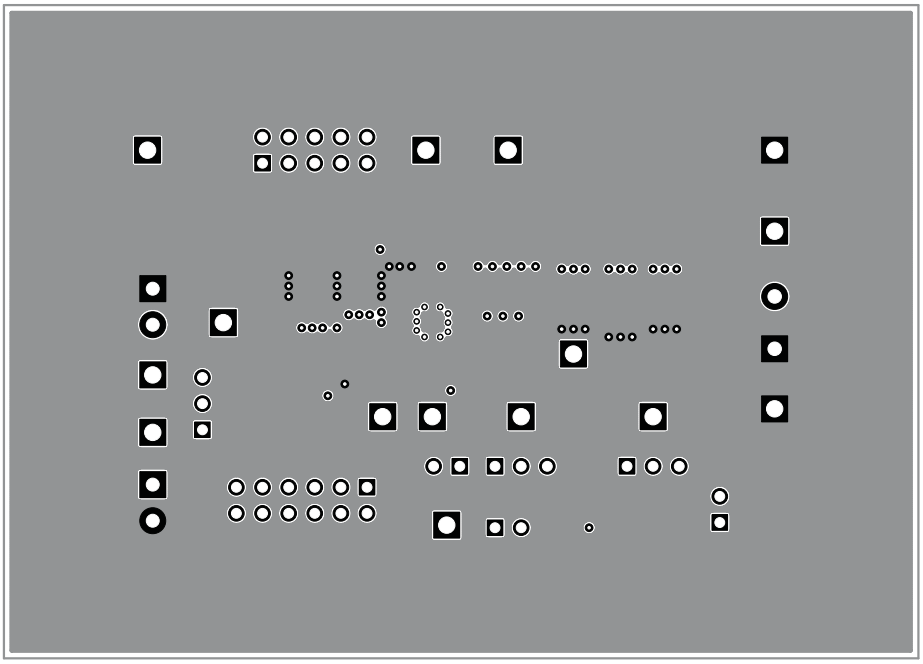

Figure 13. TPS84620EVM-692 Layer 2

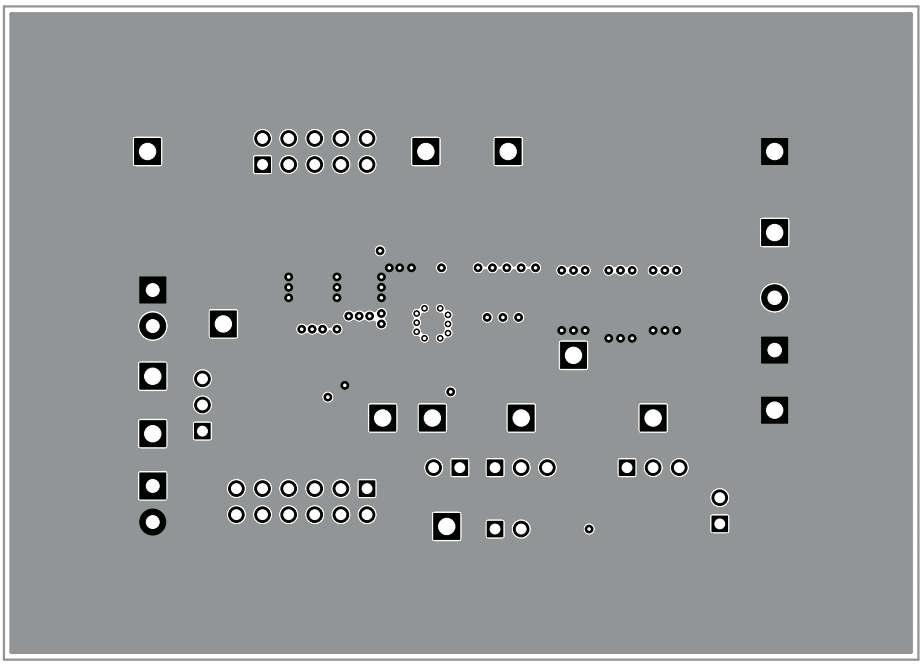

Figure 14. TPS84620EVM-692 Layer 3

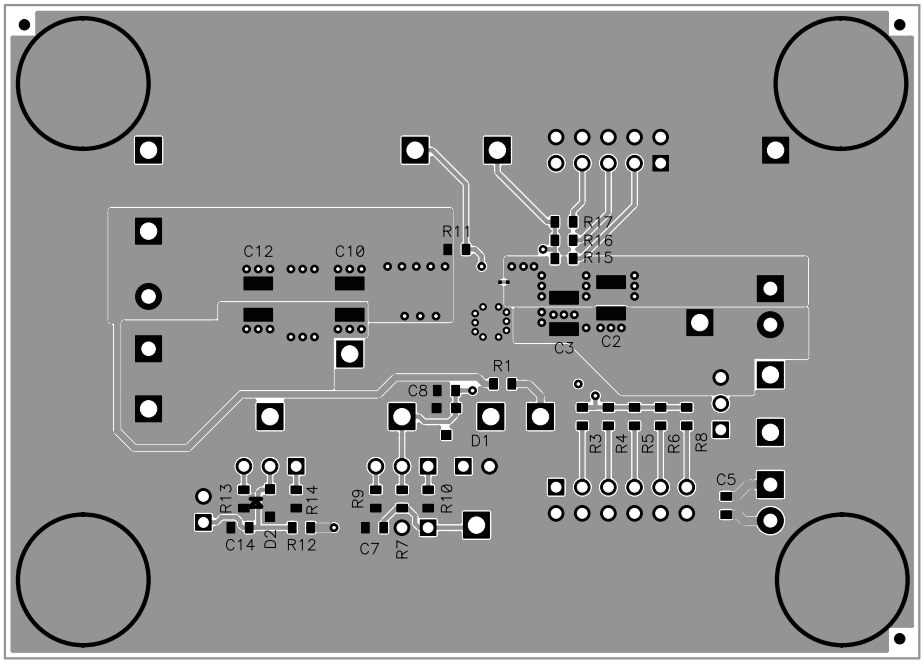

Figure 15. TPS84620EVM-692 Bottom-Side Layer and Assembly

3.2 Estimated Circuit Area

The estimated printed-circuit board area for the components used in this design is 0.55 in^2 (354 mm^2). This area does not include test point or connectors.

4 Schematic and Bill of Materials

This section presents the TPS84620EVM-692 schematic and bill of materials.

4.1 Schematic

Figure 16 is the schematic for the TPS84620EVM-692.

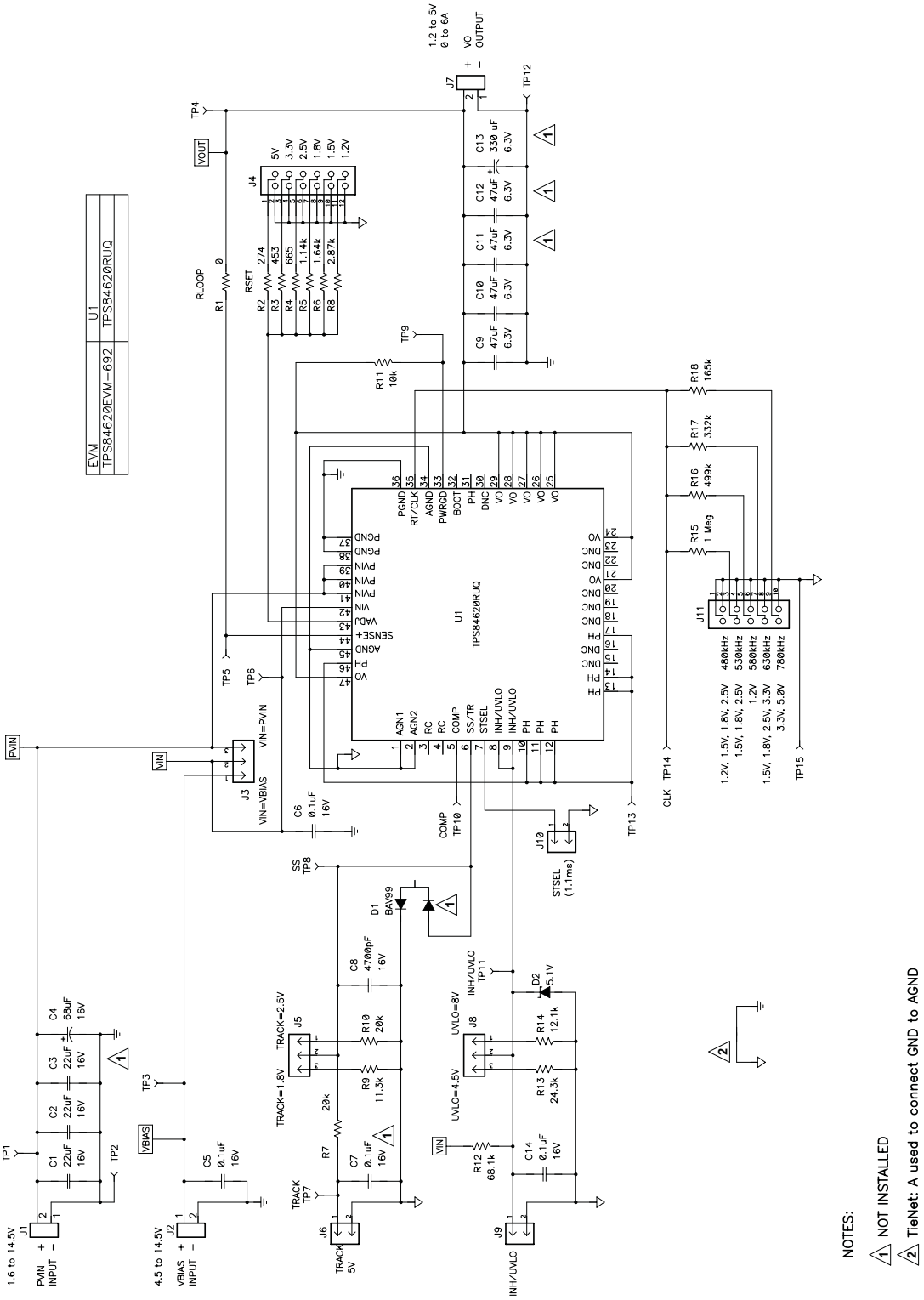

Figure 16. TPS84620EVM-692 Schematic

4.2 Bill of Materials

Table 4 presents the bill of materials for the TPS84620EVM-692.

Table 4. TPS84620EVM-692 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	Mfr
2	C1, C2	22 µF	Capacitor, Ceramic, 16V, X5R, 10%	1210	GRM32ER61E226K	Murata
0	C3	22 µF	Capacitor, Ceramic, 16V, X5R, 10%	1210	GRM32ER61E226K	Murata
0	C13	330 µF	Capacitor, Polymer SMT, 6.3V, –25 to +105°C, ±20%	7343(D)	T530D337M006ATE006	Kemet
1	C4	68 µF	Capacitor, Polymer Tantalum, 16V, 20%	7343(D)	16TQC68M	Sanyo
3	C5, C6, C14	0.1 µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
0	C7	0.1 µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C8	4700 pF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
2	C9, C10	47 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	1210	GRM32ER60J476M	Murata
0	C11, C12	47 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	1210	GRM32ER60J476M	Murata
0	D1	BAV99	Diode, Dual Ultra Fast, Series, 200-mA, 70-V	SOT23	BAV99	Fairchild
1	D2	5.1V	Diode, Zener, 200mW, 5.1V	SOD-323	BZT52C5V1S	Diodes Inc.
2	J1, J2	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
1	J11	PEC05DAAN	Header, Male 2x5-pin, 100mil spacing	0.100 inch x 5 X 2	PEC05DAAN	Sullins
3	J3, J5, J8	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
1	J4	PEC06DAAN	Header, Male 2x6 pin, 100mil spacing	0.100 inch x 2X6	PEC06DAAN	Sullins
3	J6, J9, J10	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
1	J7	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
1	R1	0	Resistor, Chip, 1/10W, –100/+600ppm/C	0603	Std	Std
1	R11	10k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R12	68.1k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R13	24.3k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R14	12.1k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R15	1 Meg	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R16	499k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R17	332k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R18	165k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	274	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	453	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	665	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	1.14k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	1.64k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R7, R10	20k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	2.87k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	11.3k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	TP1, TP3, TP4, TP6	5010	Test Point, Red, Thru Hole	0.125 x 0.125 inch	5010	Keystone
3	TP2, TP12, TP15	5011	Test Point, Black, Thru Hole	0.125 x 0.125 inch	5011	Keystone
3	TP5, TP10, TP13	5013	Test Point, Orange, Thru Hole	0.125 x 0.125 inch	5013	Keystone
5	TP7, TP8, TP9, TP11, TP14	5012	Test Point, White, Thru Hole	0.125 x 0.125 inch	5012	Keystone
1	U1	TPS84620RUQ	IC, 4.5-14.5V Input, 6A Sync. Buck, SWIFT Module	QFN	TPS84620RUQ	TI
4		SJ-5003	BUMPON HEMISPHERE .44X.20 BLACK		SJ-5003	3M
5			Shunt, Black	100-mil	929950-00	3M
1	--		PCB, 3.5 In x 2.5 In x 0.062 In		HPA692	Any

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 4.5 V to 14.5 V and the output voltage range of 1.2 V to 5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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