FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

ADG451/ADG452/ADG453-SPECIFICATIONS¹

Dual Supply (V_{DD} = +15 V, V_{SS} = -15 V, V_L = +5 V, GND = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

	B Version			
		T _{MIN} to		
Parameter	+25°C	T _{MAX}	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V _{SS} to V _{DD}	V	
On-Resistance (R _{ON})	4.0		Ω typ	$V_{\rm D} = -10$ V to +10 V, $I_{\rm S} = -10$ mA
	5	7	Ω max	
On-Resistance Match Between	0.1		Ω typ	$V_{\rm D} = \pm 10$ V, $I_{\rm S} = -10$ mA
Channels (ΔR_{ON})	0.5	0.5	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.2	0.5	Ω typ	$V_{\rm D} = -5$ V, 0 V, $+5$ V, $I_{\rm S} = -10$ mA
	0.5	0.5	12 max	
LEAKAGE CURRENTS ²				
Source OFF Leakage I _S (OFF)	±0.02		nA typ	$V_{\rm D} = \pm 10 \text{ V}, V_{\rm S} = \pm 10 \text{ V};$
	± 0.5	± 2.5	nA max	Test Circuit 2
Drain OFF Leakage I _D (OFF)	±0.02	105	nA typ	$V_{\rm D} = \pm 10$ V, $V_{\rm S} = \pm 10$ V;
Channel ON Leekage L. L. (ON)	± 0.5	± 2.5	nA max	Test Circuit 2 $V = V + 10 V_{\odot}$
Channel ON Leakage I_D , I_S (ON)	± 0.04 + 1	+5	nA typ	$V_D = V_S = \pm 10 V;$ Tost Circuit 3
	<u> </u>	± 0	ПА Шах	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.4	V min	
Input Low Voltage, V _{INL}		0.8	V max	
Input Current	0.005		u A trun	V V on V All Others 24 V
I _{INL} OF I _{INH}	0.005	+0.5	$\mu A typ$	$v_{\rm IN} = v_{\rm INL}$ or $v_{\rm INH}$, All Others = 2.4 v or 0.8 V Respectively
		±0.5	μΑ ΠΙάχ	01 0.8 V Respectively
DYNAMIC CHARACTERISTICS ³				
t _{ON}	70	000	ns typ	$R_{L} = 300 \Omega, C_{L} = 35 pF;$
	180	220	ns max	$V_{\rm S} = \pm 10$ V; Test Circuit 4
t _{OFF}	60	100	ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$;
Brook-Before-Make Time Delay t-	140	160	ns typ	$V_{\rm S} = \pm 10$ V, Test Clicuit 4 R ₂ = 300 O, C ₂ = 35 pF:
(ADG453 Only)	5	5	ns min	$V_{L} = 300.32$, $C_{L} = 35$ pr , $V_{c1} = V_{c2} = +10$ V·
(12 0 100 0 11)		Ū		Test Circuit 5
Charge Injection	20		pC typ	$V_{S} = 0 V, R_{S} = 0 \Omega, C_{L} = 1.0 nF;$
	30		pC max	Test Circuit 6
OFF Isolation	65		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$;
			15	Test Circuit 7
Channel-to-Channel Crosstalk	-90		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$;
C. (OFF)	15		nF typ	f = 1 MHz
$C_{\rm S}$ (OFF)	15		nF typ	f = 1 MHz
$C_{\rm D}$ (ON)	100		pF typ	f = 1 MHz
			F- JF	
POWER REQUIREMENTS				$V_{DD} = +16.5 \text{ V}, V_{SS} = -16.5 \text{ V}$
L -	0.0001		uA two	Digital inputs = $0 v$ or $5 v$
IDD	0.0001	5	μA typ μA max	
Iss	0.0001	0	uA typ	
55	0.5	5	μA max	
IL	0.0001		μA typ	
	0.5	5	μA max	
$I_{GND}{}^3$	0.0001		μA typ	
	0.5	5	μA max	

NOTES

¹Temperature range is as follows: B Version: -40 °C to +85 °C. ²T_{MAX} = +70 °C

³Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply $(V_{DD} = +12 V, V_{SS} = 0 V, V_L = +5 V, GND = 0 V. All specifications T_{MIN}$ to T_MAX unless otherwise noted.)

	B Version			
		T _{MIN} to		
Parameter	+25°C	T _{MAX}	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to Vpp	V	
On-Resistance (R_{ON})	6		Ω typ	$V_{\rm D} = 0$ V to 10 V. $I_{\rm S} = -10$ mA
	8	10	0 max	
On-Resistance Match Between	01	10	Q typ	$V_{\rm D} = 10 \text{ V}$ $I_{\rm S} = -10 \text{ mA}$
Channels (ΛR_{oN})	0.5	0.5	0 max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	1.0	1.0	Ω typ	$V_{D} = 0 V_{c} + 5 V_{c} I_{s} = -10 \text{ mA}$
			- J I	
LEAKAGE CURRENTS ^{2, 3}				
Source OFF Leakage I _S (OFF)	± 0.02		nA typ	$V_{\rm D} = 0$ V, 10 V, $V_{\rm S} = 0$ V, 10 V;
	± 0.5	± 2.5	nA max	Test Circuit 2
Drain OFF Leakage I _D (OFF)	± 0.02		nA typ	$V_{\rm D} = 0$ V, 10 V, $V_{\rm S} = 0$ V, 10 V;
	± 0.5	± 2.5	nA max	Test Circuit 2
Channel ON Leakage I _D , I _S (ON)	± 0.04		nA typ	$V_{\rm D} = V_{\rm S} = 0$ V, 10 V;
	±1	± 5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, VINH		2.4	V min	
Input Low Voltage, VINI		0.8	V max	
Input Current				
	0.005		uA typ	$V_{IN} = V_{INII}$ or V_{INIII}
	01000	± 0.5	μA max	
DVNAMIC CHADACTEDISTICS ⁴				
	100		ne typ	$P_{-} = 300 \ O_{-} C_{-} = 35 \ nE_{-}$
LON	220	260	ns typ	$M_{L} = 500.22, C_{L} = 55 \text{ pr},$ $M_{L} = 48 \text{ W: Test Circuit 4}$
+	220	200	ns tup	$V_{\rm S} = +6$ V, rest Circuit 4 $P_{\rm s} = 200 \ O_{\rm s} C_{\rm s} = 25 \ {\rm nE}$
LOFF	00 160	200	ns typ	$K_L = 500 \Omega_2, C_L = 55 \mu \Gamma$, $V_{-} = + 9 V_2$ Test Circuit 4
Prook Potoro Mako Timo Dolay, t	100	200	ns tup	$V_{\rm S} = +6 V$, rest Circuit 4 $P_{\rm s} = 200 O_{\rm s} C_{\rm s} = 25 \text{ pE}$
(ADC452 Only)	10	10	ns typ	$R_{\rm L} = 500 \Omega_2, C_{\rm L} = 55 \mu {\rm F},$
(ADG455 Olly)	10	10	IIS IIIII	$\mathbf{v}_{S1} = \mathbf{v}_{S2} = +\mathbf{o} \mathbf{v};$ Test Circuit 5
Charge Injection	10		nC turn	V = 0 V P = 0 O C = 10 nE
Charge injection	10		pc typ	$V_{\rm S} = 0$ V, $R_{\rm S} = 0$ 22, $C_{\rm L} = 1.0$ HF, Tost Circuit 6
Channel to Channel Crosstalk	00		dB twp	$P_{\rm c} = 50 \ O_{\rm c} = 5 \ pE_{\rm c} = 1 \ MHz$
Channel-to-Channel Closstalk	-30		ub typ	$R_{L} = 50.52, C_{L} = 5 \text{ pr}, 1 = 1 \text{ WHZ},$ Tost Circuit 8
$C_{\rm c}$ (OFF)	15		nE typ	$f = 1 MH_7$
$C_{\rm S}$ (OFF)	15		pr typ	$f = 1 MH_{7}$
$C_{\rm D}$ (OII)	100		pr typ	$f = 1 MH_{7}$
$C_{\rm D}, C_{\rm S}(\rm ON)$	100		pr typ	
POWER REQUIREMENTS				$V_{\rm DD} = +13.2 \ { m V}$
				Digital Inputs = 0 V or 5 V
I _{DD}	0.0001		μA typ	
	0.5	5	μA max	
IL	0.0001		μA typ	
	0.5	5	μA max	$V_{\rm L} = +5.5 \text{ V}$
I_{GND}^{4}	0.0001		μA typ	
	0.5	5	μA max	$V_{L} = +5.5 V$

NOTES

¹Temperature range is as follows: B Version: $-40 \,^{\circ}\text{C}$ to $+85 \,^{\circ}\text{C}$. ²T_{MAX} = $+70 \,^{\circ}\text{C}$. ³Tested with dual supplies. ⁴Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG451/ADG452/ADG453-SPECIFICATIONS¹

Dual Supply

Parameter $\frac{T_{MAX}}{T_{MAX}}$ Units Test Conditions/Comments ANALOG SWITCH Analog Signal Range Vss to VpD V 0 0 On-Resistance Match Between Channels (AB _{CN}) 7 0 typ Vp = 3.5 V to + 3.5 V, Is = -10 mA Dr.Resistance Match Between Channels (AB _{CN}) 0.5 0.5 Ω max Vp Vp = 3.5 V, Is = -10 mA LEAKAGE CURRENTS ^{2,3} 0.5 0.5 Ω max Vp Vp = 4.5, Vs = ±4.5; Source OFF Leakage Ip (OFF) ±0.02 nA typ Vp = 0.7, 5 V; Vs = 0 V, 5 V; Channel ON Leakage Ip, Is (ON) ±0.04 nA max Test Circuit 2 To V, 5 V; Tes = 0 V, 5 V; DIGITAL INPUTS 1 ±5 nA max Test Circuit 3 Test Circuit 3 DIGITAL INPUTS 1 ±0.5 μ typ Vp Vp Vp Vp Vp Univ 0.005 μ typ Kp Vp Vp SV Test Circuit 4 Input High Voltage, Vrait 0.005 μ typ Kp SV Test Circuit 4	B Version				
Parameter +25°C T_{MAX} Units Test Conditions/Comments NALOG SWITCH Analog Signal Range 7 Ω typ $V_D = -3.5$ V to $+3.5$ V. $I_S = -10$ mA On-Resistance Match Between 0.3 Ω typ $V_D = -3.5$ V to $+3.5$ V. $I_S = -10$ mA Channels (Max) 0.5 0.5 Ω typ $V_D = -3.5$ V to $+3.5$ V. $I_S = -10$ mA Channels (Max) 0.5 0.5 Ω typ $V_D = -3.5$ V to $+3.5$ V. $I_S = -10$ mA Channel (Max) 0.5 0.5 Ω max Test Circuit 2 Drain OFF Leakage I _D (OFF) ± 0.02 nA typ $V_D = \pm 4.5$, V_S V $\in = 0$ V, 5 V; Channel ON Leakage I _D , I _S (ON) ± 0.04 nA typ $V_D = -0$, 5 V; Input Lev Voltage, V _{PNL} 0.8 V max Input Lev Voltage, V _{PNL} 0.20 ms max V_F = 300 \Omega, C_L = -35 pF;	_		T _{MIN} to		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Parameter	+25°C	T _{MAX}	Units	Test Conditions/Comments
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	ANALOG SWITCH				
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Analog Signal Range		V_{SS} to V_{DD}	V	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	On-Resistance (R _{ON})	7		Ω typ	$V_{\rm D} = -3.5 \text{ V}$ to $+3.5 \text{ V}$, $I_{\rm S} = -10 \text{ mA}$
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		12	15	Ω max	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	On-Resistance Match Between	0.3		Ω typ	$V_{\rm D} = 3.5$ V, $I_{\rm S} = -10$ mA
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Channels (ΔR_{ON})	0.5	0.5	Ω max	
Source OFF Leakage Ig (OFF) ± 0.02 nA typ $V_D = \pm 4.5$, $V_S = \pm 4.5$; Drain OFF Leakage Ig (OFF) ± 0.02 nA typ $V_D = 0$, V_S , $V_S = 0$,	LEAKAGE CURRENTS ^{2, 3}				
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Source OFF Leakage $I_{\rm s}$ (OFF)	+0.02		nA tvn	$V_{\rm D} = \pm 4.5$ $V_{\rm S} = \pm 4.5$
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Source off Leanage 13 (off)	$\pm 0.5^{2}$	+2.5	nA max	Test Circuit 2
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Drain OFF Leakage Ip (OFF)	± 0.02	_2.0	nA typ	$V_{\rm D} = 0 \text{ V} 5 \text{ V} V_{\rm S} = 0 \text{ V} 5 \text{ V}$
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Drum off Loundgo ID (off)	$\pm 0.5^{2}$	+2.5	nA max	Test Circuit 2
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Channel ON Leakage In Is (ON)	± 0.0 ± 0.04	± 2.0	nA typ	$V_{\rm D} = V_{\rm c} = 0 V 5 V^{\circ}$
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		±1	± 5	nA max	Test Circuit 3
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$					
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	DIGITAL INPUTS		0.4	• •	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input High Voltage, V _{INH}		2.4	V min	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Input Low Voltage, V _{INL}		0.8	v max	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input Current	0.005		A .	X 7 X 7 X 7
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	I _{INL} or I _{INH}	0.005	105	μA typ	$\mathbf{V}_{\mathrm{IN}} = \mathbf{V}_{\mathrm{INL}}$ or $\mathbf{V}_{\mathrm{INH}}$
$\begin{array}{c c c c c c c c c c c c c c c c c c c $			±0.5	μA max	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	DYNAMIC CHARACTERISTICS ⁴				
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	t _{ON}	160		ns typ	$R_{L} = 300 \Omega, C_{L} = 35 pF;$
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		220	300	ns max	$V_{\rm S} = 3$ V; Test Circuit 4
140 180 ns max $V_s = 3 V$; Test Circuit 4 Break-Before-Make Time Delay, t_D 50 ns typ $R_L = 300 \Omega$, $C_L = 35 pF$; (ADG453 Only) 5 5 ns min $V_{S1} = V_{S2} = 3 V$; Charge Injection 10 pC typ $V_s = 0 \Omega$, $C_L = 1.0 nF$; OFF Isolation 65 dB typ $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Channel-to-Channel Crosstalk -76 dB typ $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Cs (OFF) 15 pF typ $f = 1 MHz$ Test Circuit 7 Channel-to-Channel Crosstalk -76 dB typ $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Cs (OFF) 15 pF typ $f = 1 MHz$ C_D (OFF) 15 pF typ $f = 1 MHz$ C_D, C_S (ON) 100 pF typ $f = 1 MHz$ POWER REQUIREMENTS 0.5 5 $\mu A \max$ Iss 0.5 5 $\mu A \max$ Iss 0.5 5 $\mu A \max$ I_{GND}^4 0.0001 $\mu A typ$ $\nu_L = +5.5 V$ 0.5 5 $\mu A \max$ $V_L = +5.5 V$	t _{OFF}	60		ns typ	$R_{L} = 300 \Omega, C_{L} = 35 pF;$
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		140	180	ns max	$V_{\rm S} = 3$ V; Test Circuit 4
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Break-Before-Make Time Delay, t _D	50		ns typ	$R_{L} = 300 \Omega, C_{L} = 35 pF;$
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	(ADG453 Only)	5	5	ns min	$V_{S1} = V_{S2} = 3 \overline{V};$
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Ū				Test Circuit 5
$\begin{array}{cccc} \text{OFF Isolation} & 65 & & \text{Test Circuit 6} \\ \text{OFF Isolation} & 65 & & \text{dB typ} & & \text{R}_{L} = 50 \ \Omega, \ C_{L} = 5 \ \text{pF}, \ f = 1 \ \text{MHz}; \\ \text{Test Circuit 7} \\ \text{Test Circuit 7} \\ \text{Channel-to-Channel Crosstalk} & -76 & & \text{dB typ} & & \text{R}_{L} = 50 \ \Omega, \ C_{L} = 5 \ \text{pF}, \ f = 1 \ \text{MHz}; \\ \text{Test Circuit 8} \\ \text{C}_{S} (\text{OFF}) & & 15 & & \text{pF typ} & f = 1 \ \text{MHz} \\ \text{C}_{D} (\text{OFF}) & & 15 & & \text{pF typ} & f = 1 \ \text{MHz} \\ \text{C}_{D}, \ C_{S} (\text{ON}) & & 100 & & \text{pF typ} & f = 1 \ \text{MHz} \\ \end{array} \\ \hline \begin{array}{c} \text{POWER REQUIREMENTS} & & & V_{\text{DD}} = +5.5 \ \text{V} \\ \text{I}_{\text{DD}} & & & 0.0001 & & & \mu \text{A typ} \\ \text{I}_{\text{SS}} & & & 0.0001 & & & & \mu \text{A max} \\ \text{I}_{L} & & & 0.0001 & & & & & \mu \text{A max} \\ \text{I}_{C} & & & 0.5 & 5 & & & & \mu \text{A max} \\ \text{I}_{GND}^{4} & & & 0.0001 & & & & & & \mu \text{A typ} \\ \end{array} $	Charge Injection	10		pC typ	$V_{S} = 0 V, R_{S} = 0 \Omega, C_{L} = 1.0 nF;$
$\begin{array}{cccccccccccccccccccccccccccccccccccc$					Test Circuit 6
$\begin{array}{cccc} Test Circuit 7 \\ Test Circuit 7 \\ Channel-to-Channel Crosstalk & -76 \\ C_{S} (OFF) & 15 \\ C_{D} (OFF) & 15 \\ C_{D} C_{S} (ON) & 100 \\ \end{array} \qquad \begin{array}{ccccc} pF typ & f = 1 & MHz \\ Test Circuit 8 \\ F typ & f = 1 & MHz \\ F typ & f = 1 & MHz \\ Test Circuit 8 \\ Test Circuit 8 \\ Test Circuit 8 \\ Test Circuit 7 \\ Test Circuit 8 \\ Tes$	OFF Isolation	65		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$;
$ \begin{array}{cccc} Channel-to-Channel Crosstalk & -76 & dB typ & R_L = 50 \ \Omega, \ C_L = 5 \ pF, \ f = 1 \ MHz; \\ Test Circuit 8 & Test Circuit 8 \\ C_S (OFF) & 15 & pF typ & f = 1 \ MHz & f = 1 $					Test Circuit 7
$\begin{array}{cccc} & Test Circuit 8 \\ C_{S} (OFF) & 15 & pF typ & f = 1 \ MHz \\ C_{D} (OFF) & 15 & pF typ & f = 1 \ MHz \\ C_{D}, C_{S} (ON) & 100 & pF typ & f = 1 \ MHz \\ \hline POWER REQUIREMENTS & V_{DD} = +5.5 \ V \\ I_{DD} & 0.0001 & \mu A typ \\ 0.5 & 5 & \mu A \ max \\ I_{SS} & 0.0001 & \mu A typ \\ 0.5 & 5 & \mu A \ max \\ I_{L} & 0.0001 & \mu A typ \\ 0.5 & 5 & \mu A \ max \\ I_{GND}^{4} & 0.0001 & \mu A typ \\ 0.5 & 5 & \mu A \ max \\ V_{L} = +5.5 \ V \\ I_{GND}^{4} & 0.0001 & \mu A typ \\ 0.5 & 5 & \mu A \ max \\ V_{L} = +5.5 \ V \\ \hline \end{array}$	Channel-to-Channel Crosstalk	-76		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$;
$\begin{array}{cccc} C_{S}\left(OFF\right) & 15 & pF typ & f = 1 \ MHz \\ C_{D}\left(OFF\right) & 15 & pF typ & f = 1 \ MHz \\ C_{D}, C_{S}\left(ON\right) & 100 & pF typ & f = 1 \ MHz \\ \hline \\ POWER REQUIREMENTS & & V_{DD} = +5.5 \ V \\ Digital \ Inputs = 0 \ V \ or 5 \ V \\ I_{DD} & 0.5 & 5 & \muA \ max \\ I_{SS} & 0.0001 & \muA \ typ \\ 0.5 & 5 & pA \ max \\ I_{L} & 0.0001 & \muA \ typ \\ 0.5 & 5 & \muA \ max \\ I_{GND}^{4} & 0.0001 & \muA \ typ \\ 0.5 & 5 & \muA \ max \\ V_{L} = +5.5 \ V \\ O.5 & 5 & \muA \ max \\ V_{L} = +5.5 \ V \\ V_{L} = +5.$					Test Circuit 8
$\begin{array}{ccccc} C_{D} \ (OFF) & 15 & pF \ typ & f = 1 \ MHz \\ C_{D}, \ C_{S} \ (ON) & 100 & pF \ typ & f = 1 \ MHz \\ \hline POWER \ REQUIREMENTS & V_{DD} = +5.5 \ V \\ Digital \ Inputs = 0 \ V \ or \ 5 \ V \\ I_{DD} & 0.5 & 5 & \muA \ max \\ I_{SS} & 0.0001 & \muA \ typ \\ 0.5 & 5 & \muA \ max \\ I_{L} & 0.0001 & \muA \ typ \\ 0.5 & 5 & \muA \ max \\ I_{GND}^{4} & 0.0001 & \muA \ typ \\ 0.5 & 5 & \muA \ max & V_{L} = +5.5 \ V \\ O.5 & 5 & \muA \ max & V_{L} = +5.5 \ V \\ I_{GND}^{4} & 0.0001 & \muA \ typ \\ 0.5 & 5 & \muA \ max & V_{L} = +5.5 \ V \\ \end{array}$	C _S (OFF)	15		pF typ	f = 1 MHz
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	C _D (OFF)	15		pF typ	f = 1 MHz
POWER REQUIREMENTS $V_{DD} = +5.5 V$ Digital Inputs = 0 V or 5 V I_{DD} 0.0001 $\mu A \text{ typ}$ I_{SS} 0.0001 $\mu A \text{ typ}$ I_{SS} 0.0001 $\mu A \text{ typ}$ I_L 0.0001 $\mu A \text{ typ}$ I_L 0.0001 $\mu A \text{ typ}$ I_{GND}^4 0.0001 $\mu A \text{ typ}$ I_{GND}^4 0.0001 $\mu A \text{ typ}$ 0.5 5 $\mu A \text{ max}$ $V_L = +5.5 V$ $V_L = +5.5 V$	$C_D, C_S(ON)$	100		pF typ	f = 1 MHz
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	POWER REOLUREMENTS				$V_{22} = \pm 5.5 V$
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	I OWER RECORDINE VIS				$V_{DD} = +3.5$ V Digital Inputs = 0 V or 5 V
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Inn	0.0001		uA tvn	
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	-00-	0.5	5	uA max	
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Icc	0.0001	Ū	uA typ	
$I_{L} = \begin{pmatrix} 0.0001 & \mu A \text{ typ} \\ 0.5 & 5 & \mu A \text{ max} & V_{L} = +5.5 \text{ V} \\ I_{GND}^{4} & 0.0001 & \mu A \text{ typ} \\ 0.5 & 5 & \mu A \text{ max} & V_{L} = +5.5 \text{ V} \end{pmatrix}$	-33	0.5	5	uA max	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	It	0.0001	Ť	uA typ	
I_{GND}^4 0.0001 $\mu A typ$ 0.5 5 $\mu A max$ $V_L = +5.5 V$	L	0.5	5	uA max	$V_{I} = +5.5 V$
0.5 5 $\mu A \max V_L = +5.5 V$	I_{GND}^4	0.0001	-	uA tvp	L
		0.5	5	µA max	$V_{L} = +5.5 V$

NOTES ¹Temperature range is as follows: B Version: -40° C to $+85^{\circ}$ C. ²T_{MAX} = $+70^{\circ}$ C. ³Tested with dual supplies. ⁴Guaranteed by design, not subject to production test. Nc0.0 Vm(D)

ORDERING GUIDE

V _{DD}	Most positive power supply potential.	V _D (V _S)	Analog voltage on terminals D, S.
V _{SS} Most negati supplies. In connected to	Most negative power supply potential in dual	C _S (OFF)	"OFF" switch source capacitance.
	supplies. In single supply applications, it may be	C _D (OFF)	"OFF" switch drain capacitance.
	Le rie a serve servele (c. 7 V)	C _D , C _S (ON)	"ON" switch capacitance.
vL	Logic power supply (+5 v).	t _{ON}	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
GND	Ground (0 V) reference.		
S	Source terminal. May be an input or output.	t _{OFF}	Delay between applying the digital control input and the output switching off.
D	Drain terminal. May be an input or output.		
IN	Logic control input.	t _D	"OFF" time or "ON" time measured between
R _{ON}	Ohmic resistance between D and S.		the 90% points of both switches, when switching from one address state to another. See Test Circuit 5.
ΔR_{ON}	On resistance match between any two channels		
	i.e., R _{ON} max – R _{ON} min.	Crosstalk	A measure of unwanted signal coupled through from one channel to another as a result of para- sitic capacitance.
R _{FLAT(ON)}	Flatness is defined as the difference between the	Crosstan	
max mea	maximum and minimum value of on-resistance as		
	measured over the specified analog signal range.	Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
I _S (OFF)	Source leakage current with the switch "OFF."		
I _D (OFF)	Drain leakage current with the switch "OFF."	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output dur- ing switching.
I_D, I_S (ON)	Channel leakage current with the switch "ON."		





Figure 1. On Resistance as a Function of V_D (V_S) for Various Dual Supplies



Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures with Dual Supplies

Typical Performance Characteristics-ADG451/ADG452/ADG453



Figure 3. On Resistance as a Function of V_D (V_S) for Various Single Supplies



Figure 4. Leakage Currents as a Function of Temperature



Figure 5. Supply Current vs. Input Switching Frequency



Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures with Single Supplies



Figure 7. Leakage Currents as a Function of V_D (V_S)



Figure 8. Off Isolation vs. Frequency







Figure 10. Frequency Response with Switch On

APPLICATION

Figure 11 illustrates a precise, fast, sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output $V_{\rm OUT}$ follows the input signal $V_{\rm IN}$. In the hold mode, SW1 is opened and the signal is held by the hold capacitor $C_{\rm H}$.



Figure 11. Fast, Accurate Sample-and-Hold Circuit

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG451/ ADG452/ADG453 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 30 μ V/ μ s.

A second switch, SW2, that operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp AD711, which will minimize charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C . This compensation network reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ± 10 V input range. Both the acquisition and settling times are 850 ns.

Test Circuits







Test Circuit 1. On Resistance

Test Circuit 2. Off Leakage

Test Circuit 3. On Leakage



Test Circuit 4. Switching Times



Test Circuit 5. Break-Before-Make Time Delay



Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation



Test Circuit 8. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



16-Lead SOIC (R-16A)



C3119a-0-2/98