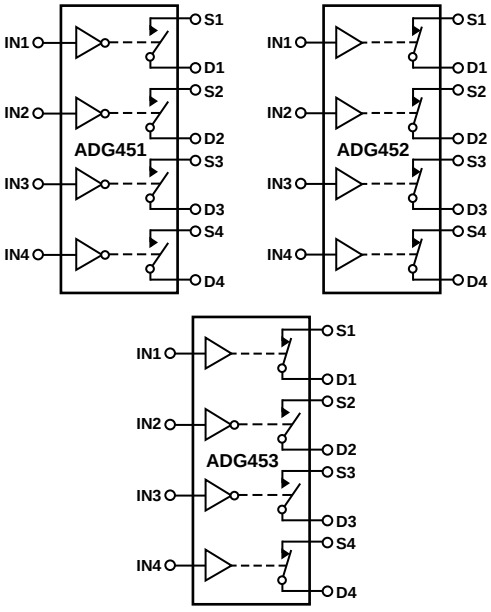
FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

ADG451/ADG452/ADG453–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V, V_{SS} = –15 V, V_L = +5 V, GND = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version +25°C	B Version T_{MIN} to T_{MAX}	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On-Resistance (R_{ON})	4.0		Ω typ	V_D = –10 V to +10 V, I_S = –10 mA
	5	7	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	V_D = ±10 V, I_S = –10 mA
	0.5	0.5	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.2		Ω typ	V_D = –5 V, 0 V, +5 V, I_S = –10 mA
	0.5	0.5	Ω max	
LEAKAGE CURRENTS[2]				
Source OFF Leakage I_S (OFF)	±0.02		nA typ	V_D = ±10 V, V_S = ±10 V;
	±0.5	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.02		nA typ	V_D = ±10 V, V_S = ±10 V;
	±0.5	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.04		nA typ	V_D = V_S = ±10 V;
	±1	±5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}, All Others = 2.4 V
		±0.5	µA max	or 0.8 V Respectively
DYNAMIC CHARACTERISTICS[3]				
t_{ON}	70		ns typ	R_L = 300 Ω, C_L = 35 pF;
	180	220	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	60		ns typ	R_L = 300 Ω, C_L = 35 pF;
	140	180	ns max	V_S = ±10 V; Test Circuit 4
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF;
(ADG453 Only)	5	5	ns min	V_{S1} = V_{S2} = +10 V; Test Circuit 5
Charge Injection	20		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1.0 nF;
	30		pC max	Test Circuit 6
OFF Isolation	65		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	–90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	15		pF typ	f = 1 MHz
C_D (OFF)	15		pF typ	f = 1 MHz
C_D, C_S (ON)	100		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +16.5 V, V_{SS} = –16.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		µA typ	
	0.5	5	µA max	
I_{SS}	0.0001		µA typ	
	0.5	5	µA max	
I_L	0.0001		µA typ	
	0.5	5	µA max	
I_{GND}[3]	0.0001		µA typ	
	0.5	5	µA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]T_{MAX} = +70°C.
[3]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Single Supply (V_{DD} = +12 V, V_{SS} = 0 V, V_L = +5 V, GND = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version +25°C	B Version T_{MIN} to T_{MAX}	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	6		Ω typ	V_D = 0 V to 10 V, I_S = –10 mA
	8	10	Ω max	
On-Resistance Match Between	0.1		Ω typ	V_D = 10 V, I_S = –10 mA
Channels (ΔR_{ON})	0.5	0.5	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	1.0	1.0	Ω typ	V_D = 0 V, +5 V, I_S = –10 mA
LEAKAGE CURRENTS[2, 3]				
Source OFF Leakage I_S (OFF)	±0.02		nA typ	V_D = 0 V, 10 V, V_S = 0 V, 10 V;
	±0.5	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.02		nA typ	V_D = 0 V, 10 V, V_S = 0 V, 10 V;
	±0.5	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.04		nA typ	V_D = V_S = 0 V, 10 V;
	±1	±5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	µA max	
DYNAMIC CHARACTERISTICS[4]				
t_{ON}	100		ns typ	R_L = 300 Ω, C_L = 35 pF;
	220	260	ns max	V_S = +8 V; Test Circuit 4
t_{OFF}	80		ns typ	R_L = 300 Ω, C_L = 35 pF;
	160	200	ns max	V_S = +8 V; Test Circuit 4
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF;
(ADG453 Only)	10	10	ns min	V_{S1} = V_{S2} = +8 V; Test Circuit 5
Charge Injection	10		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1.0 nF; Test Circuit 6
Channel-to-Channel Crosstalk	–90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	15		pF typ	f = 1 MHz
C_D (OFF)	15		pF typ	f = 1 MHz
C_D, C_S (ON)	100		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +13.2 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		µA typ	
	0.5	5	µA max	
I_L	0.0001		µA typ	
	0.5	5	µA max	V_L = +5.5 V
I_{GND}[4]	0.0001		µA typ	
	0.5	5	µA max	V_L = +5.5 V

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]T_{MAX} = +70°C.
[3]Tested with dual supplies.
[4]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ADG451/ADG452/ADG453–SPECIFICATIONS[1]

Dual Supply

Parameter	B Version +25°C	B Version T_{MIN} to T_{MAX}	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On-Resistance (R_{ON})	7		Ω typ	V_D = –3.5 V to +3.5 V, I_S = –10 mA
	12	15	Ω max	
On-Resistance Match Between	0.3		Ω typ	V_D = 3.5 V, I_S = –10 mA
Channels (ΔR_{ON})	0.5	0.5	Ω max	
LEAKAGE CURRENTS[2, 3]				
Source OFF Leakage I_S (OFF)	±0.02		nA typ	V_D = ±4.5, V_S = ±4.5;
	±0.5	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.02		nA typ	V_D = 0 V, 5 V, V_S = 0 V, 5 V;
	±0.5	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.04		nA typ	V_D = V_S = 0 V, 5 V;
	±1	±5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	µA max	
DYNAMIC CHARACTERISTICS[4]				
t_{ON}	160		ns typ	R_L = 300 Ω, C_L = 35 pF;
	220	300	ns max	V_S = 3 V; Test Circuit 4
t_{OFF}	60		ns typ	R_L = 300 Ω, C_L = 35 pF;
	140	180	ns max	V_S = 3 V; Test Circuit 4
Break-Before-Make Time Delay, t_D	50		ns typ	R_L = 300 Ω, C_L = 35 pF;
(ADG453 Only)	5	5	ns min	V_{S1} = V_{S2} = 3 V; Test Circuit 5
Charge Injection	10		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1.0 nF; Test Circuit 6
OFF Isolation	65		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	–76		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	15		pF typ	f = 1 MHz
C_D (OFF)	15		pF typ	f = 1 MHz
C_D, C_S (ON)	100		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +5.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		µA typ	
	0.5	5	µA max	
I_{SS}	0.0001		µA typ	
	0.5	5	µA max	
I_L	0.0001		µA typ	
	0.5	5	µA max	V_L = +5.5 V
I_{GND}[4]	0.0001		µA typ	
	0.5	5	µA max	V_L = +5.5 V

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]T_{MAX} = +70°C.
[3]Tested with dual supplies.
[4]Guaranteed by design, not subject to production test.
Nc0.0 Vm(D)

ORDERING GUIDE

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
V_L	Logic power supply (+5 V).
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	On resistance match between any two channels i.e., R_{ON}max – R_{ON}min.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."

V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance.
C_D (OFF)	"OFF" switch drain capacitance.
C_D, C_S (ON)	"ON" switch capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another. See Test Circuit 5.
Crosstalk	A measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

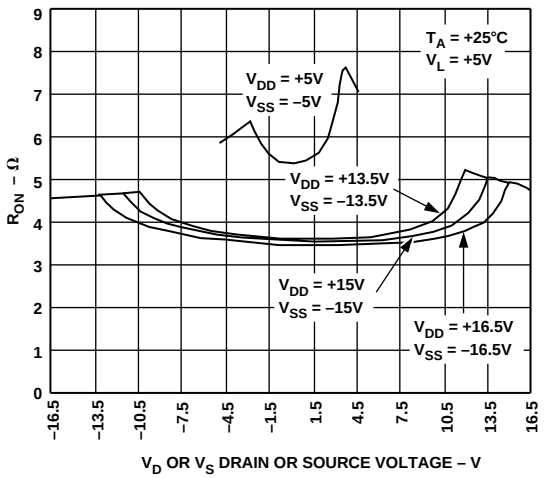


Figure 1. On Resistance as a Function of V_D (V_S) for Various Dual Supplies

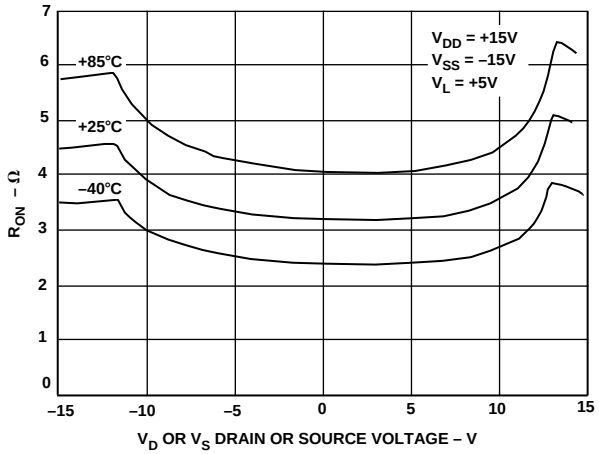


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures with Dual Supplies

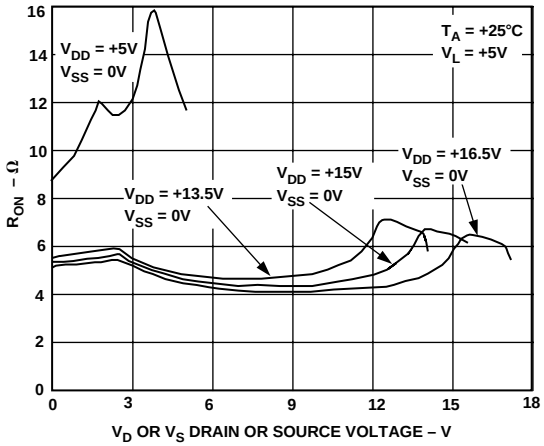


Figure 3. On Resistance as a Function of V_D (V_S) for Various Single Supplies

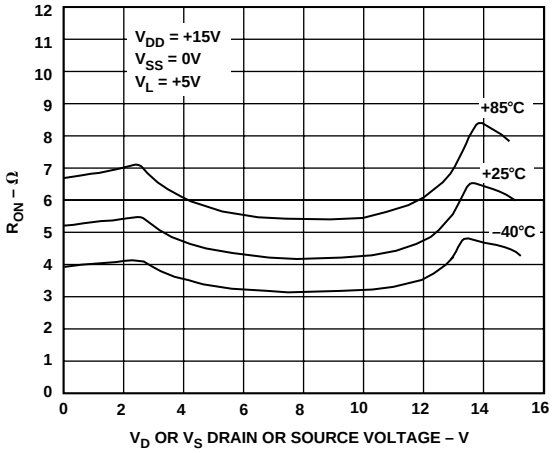


Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures with Single Supplies

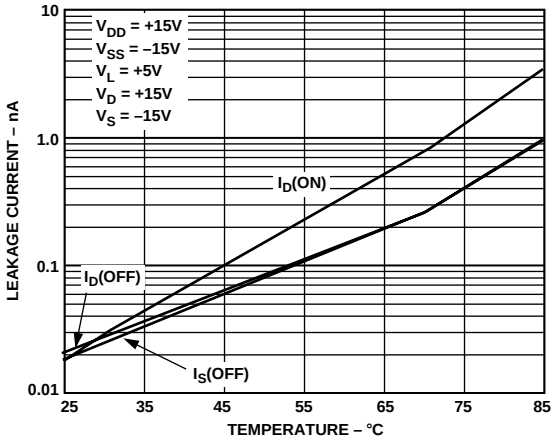


Figure 4. Leakage Currents as a Function of Temperature

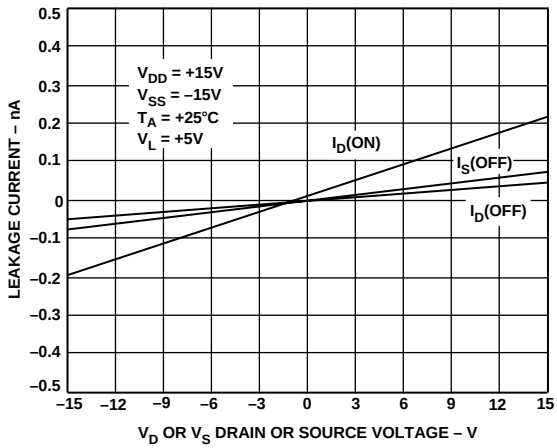


Figure 7. Leakage Currents as a Function of V_D (V_S)

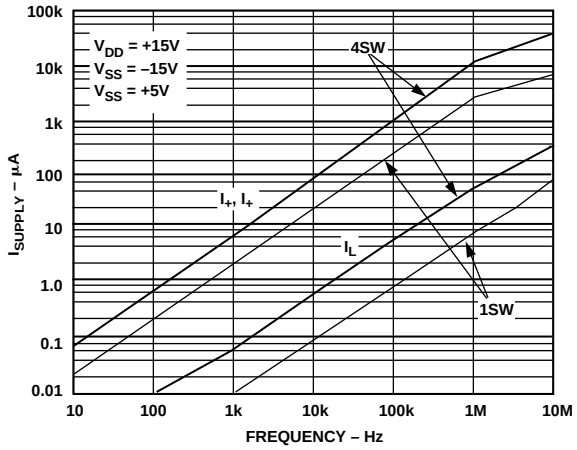


Figure 5. Supply Current vs. Input Switching Frequency

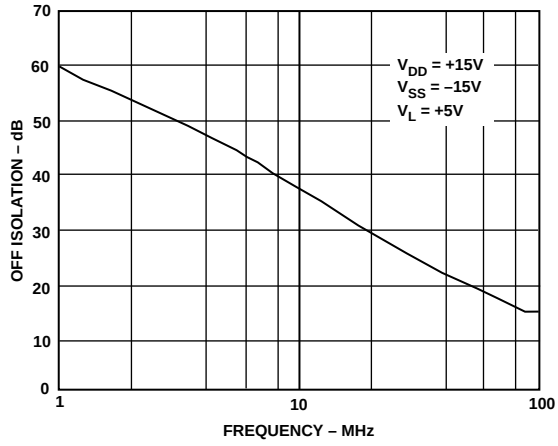


Figure 8. Off Isolation vs. Frequency

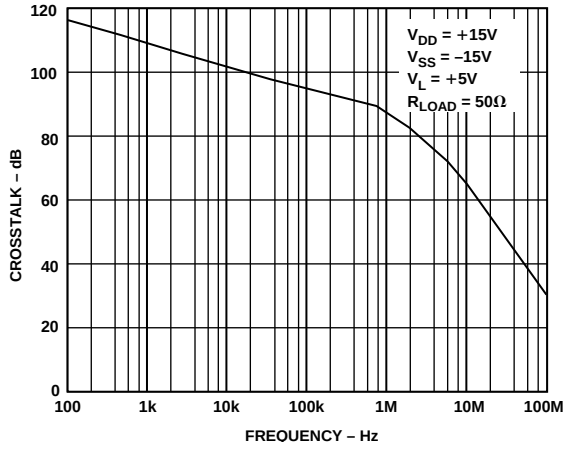


Figure 9. Crosstalk vs. Frequency

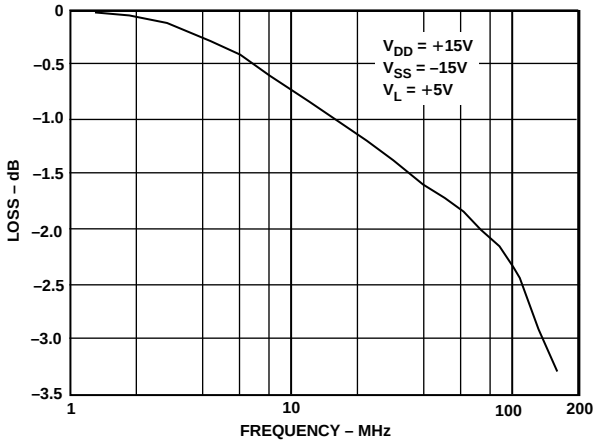


Figure 10. Frequency Response with Switch On

APPLICATION

Figure 11 illustrates a precise, fast, sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN}. In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H.

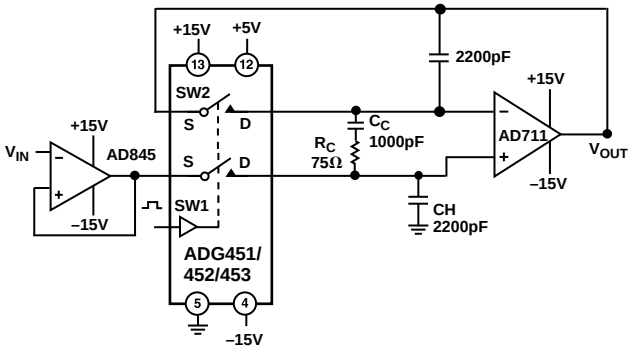
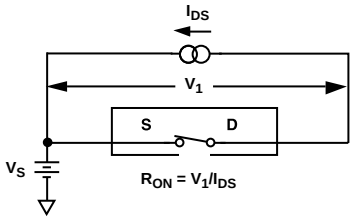


Figure 11. Fast, Accurate Sample-and-Hold Circuit

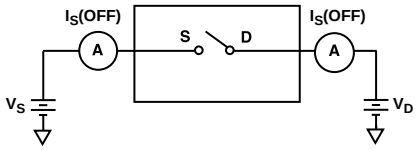
Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG451/ ADG452/ADG453 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 30 µV/µs.

A second switch, SW2, that operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp AD711, which will minimize charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C. This compensation network reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ±10 V input range. Both the acquisition and settling times are 850 ns.

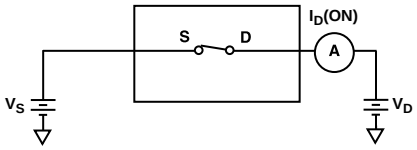
Test Circuits



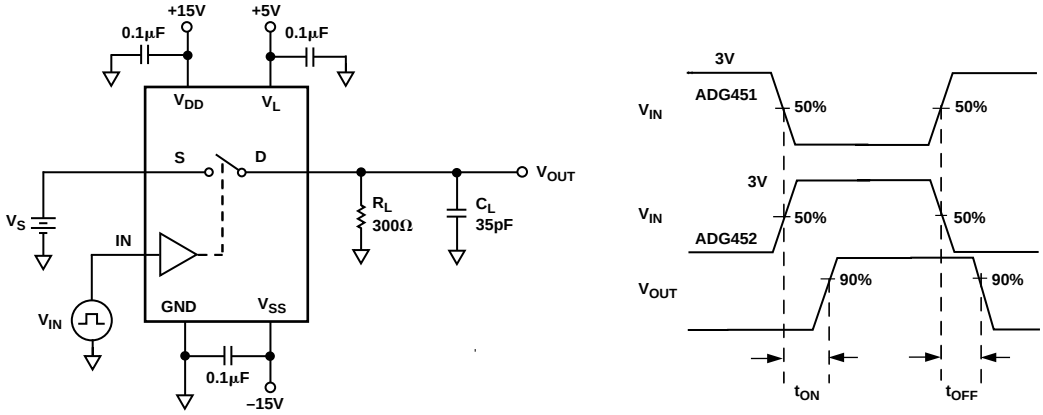
Test Circuit 1. On Resistance



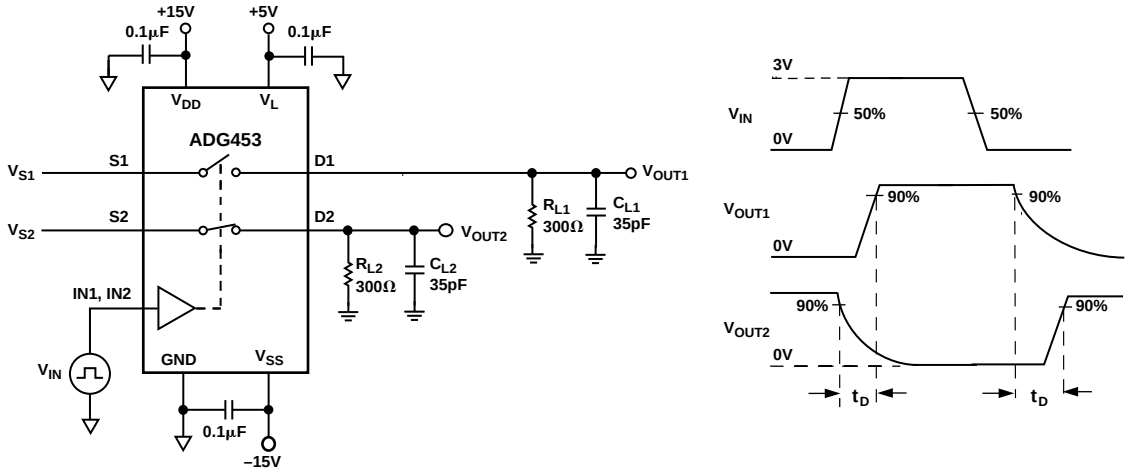
Test Circuit 2. Off Leakage



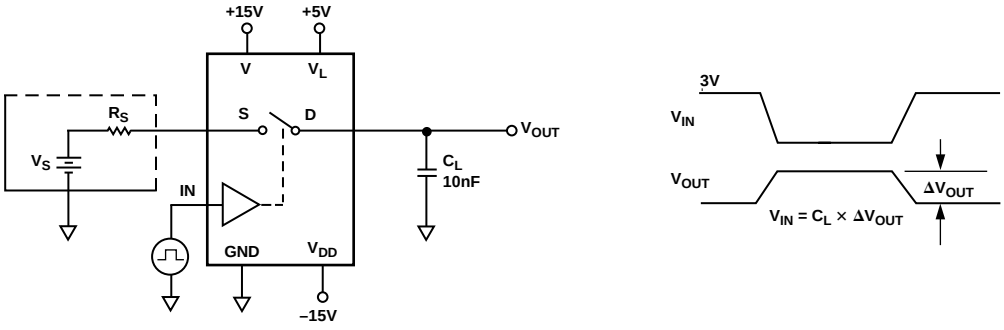
Test Circuit 3. On Leakage



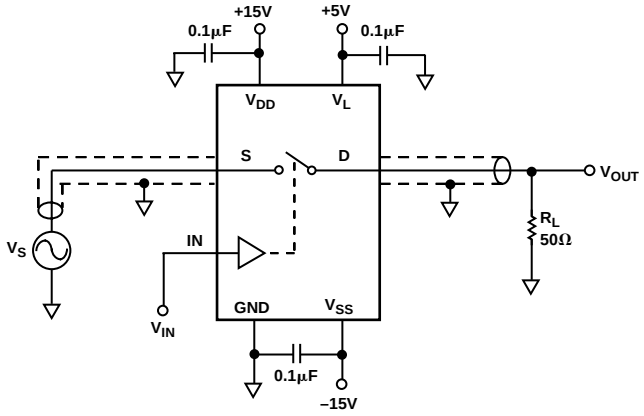
Test Circuit 4. Switching Times



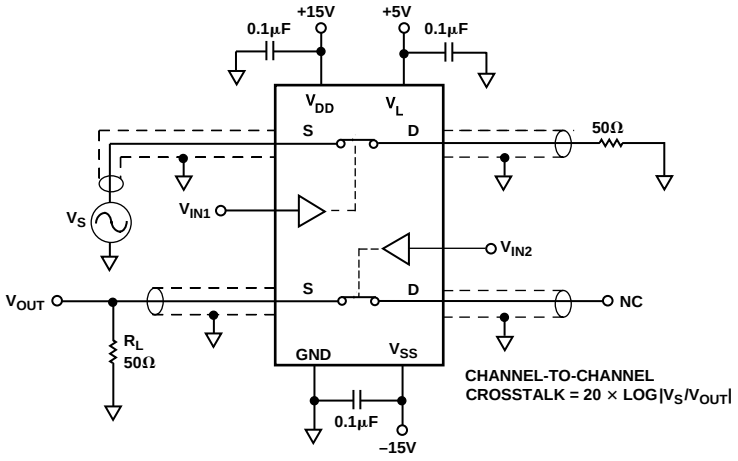
Test Circuit 5. Break-Before-Make Time Delay



Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation

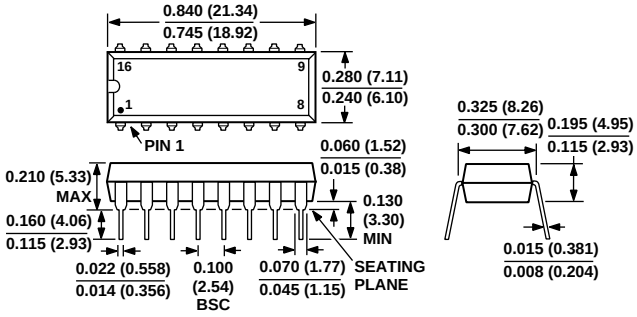


Test Circuit 8. Channel-to-Channel Crosstalk

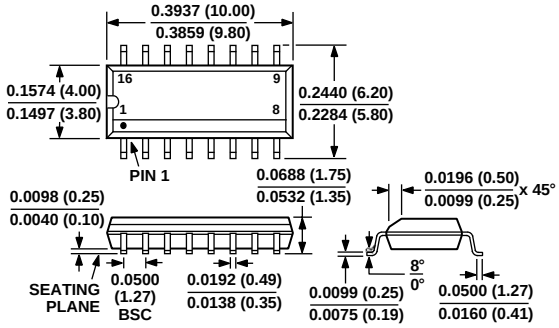
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Plastic DIP
(N-16)



16-Lead SOIC
(R-16A)



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