

1. TYPE	QS6J3				
2. STRUCTURE	SILICON P-CHANNEL MOS FET				
3. APPLICATIONS	SWITCHING				
4. ABSOLUTE MAXIMUM RATINGS [Ta=25°C]	《 MOSFET 》				
DRAIN-SOURCE VOLTAGE		V <sub>DSS</sub>	· · ·	-20V	
GATE-SOURCE VOLTAGE		V <sub>GSS</sub>	· · ·	±12V	
DRAIN CURRENT	CONTINUOUS	I <sub>D</sub>	· · ·	±1.5A	
	PULSED	I <sub>DP</sub>	· · ·	±6.0A PW ≤ 10μs DUTY CYCLE ≤ 1%	
SOURCE CURRENT	CONTINUOUS	I <sub>S</sub>	· · ·	-0.75A	
(BODY DIODE)	PULSED	I <sub>SP</sub>	· · ·	-6.0A PW ≤ 10μs DUTY CYCLE ≤ 1%	
TOTAL POWER DISSIPATION		P <sub>D</sub>	· · ·	1.25W/TOTAL 0.9W/ELEMENT MOUNTED ON A CERAMIC BOARD	
CHANNEL TEMPERATURE		T <sub>ch</sub>	· · ·	150°C	
RANGE OF STORAGE TEMPERATURE		T <sub>stg</sub>	· · ·	-55~150°C	
5. THERMAL RESISTANCE					
CHANNEL TO AMBIENT		R <sub>th(ch-a)</sub>	· · ·	100°C/W/TOTAL 139°C/W/ELEMENT MOUNTED ON A CERAMIC BOARD	

DESIGN	CHECK	APPROVAL	DATE : 28/JUL/2008	SPECIFICATION No. TSQ03122-QS6J3
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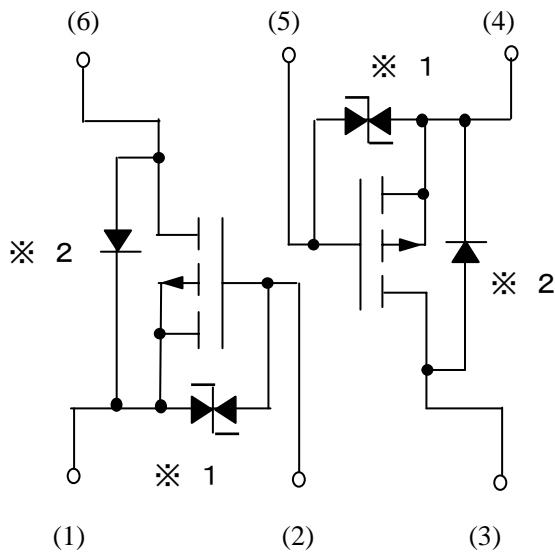
6.ELECTRICAL CHARACTERISTICS [Ta=25°C]  
 《 MOSFET 》

PARAMETER	ITEM	CONDITION	MIN.	TYP.	MAX.
GATE-SOURCE LEAKAGE	$I_{GSS}$	$V_{GS} = \pm 12V / V_{DS} = 0V$	-	-	$\pm 10\mu A$
DRAIN-SOURCE BREAKDOWN VOLTAGE	$V_{(BR)DSS}$	$I_D = -1mA / V_{GS} = 0V$	-20V	-	-
ZERO GATE VOLTAGE DRAIN CURRENT	$I_{DSS}$	$V_{DS} = -20V / V_{GS} = 0V$	-	-	-1 $\mu A$
GATE THRESHOLD VOLTAGE	$V_{GS(th)}$	$V_{DS} = -10V / I_D = -1mA$	-0.7V	-	-2.0V
STATIC DRAIN-SOURCE ON-STATE RESISTANCE	$R_{DS(on)}$ * PULSED	$I_D = -1.5A / V_{GS} = -4.5V$	-	155m $\Omega$	215m $\Omega$
		$I_D = -1.5A / V_{GS} = -4V$	-	170m $\Omega$	235m $\Omega$
		$I_D = -0.75A / V_{GS} = -2.5V$	-	310m $\Omega$	430m $\Omega$
FORWARD TRANSFER ADMITTANCE	$ Y_{fs} $ * PULSED	$V_{DS} = -10V / I_D = -0.75A$	1.0S	-	-
INPUT CAPACITANCE	$C_{iss}$	$V_{DS} = -10V$ $V_{GS} = 0V$ $f = 1MHz$	-	270pF	-
OUTPUT CAPACITANCE	$C_{oss}$		-	40pF	-
REVERSE TRANSFER CAPACITANCE	$C_{rss}$		-	35pF	-
TURN-ON DELAY TIME	$t_{d(on)}$ * PULSED	$I_D = -0.75A$ $V_{DD} \doteq -15V$ $V_{GS} = -4.5V$ $R_L = 20\Omega / R_G = 10\Omega$ see Fig.1-1,1-2	-	10ns	-
RISE TIME	$t_r$ * PULSED		-	12ns	-
TURN-OFF DELAY TIME	$t_{d(off)}$ * PULSED		-	45ns	-
FALL TIME	$t_f$ * PULSED		-	20ns	-
TOTAL GATE CHARGE	$Q_g$ * PULSED	$V_{DD} \doteq -15V$ $V_{GS} = -4.5V$ $I_D = -1.5A$ $R_L = 10\Omega / R_G = 10\Omega$ see Fig.2-1,2-2	-	3.0nC	-
GATE-SOURCE CHARGE	$Q_{gs}$ * PULSED		-	0.8nC	-
GATE-DRAIN CHARGE	$Q_{gd}$ * PULSED		-	0.85nC	-

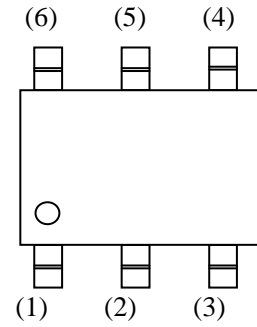
## 《 MOSFET 》 BODY DIODE (SOURCE-DRAIN)

PARAMETER	ITEM	CONDITION	MIN.	TYP.	MAX.
FORWARD VOLTAGE	$V_{SD}$	$I_S = -0.75A / V_{GS} = 0V$	-	-	-1.2V

### 7. INNER CIRCUIT

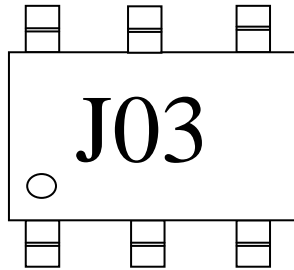


- (1) Tr1 SOURCE
- (2) Tr1 GATE
- (3) Tr2 DRAIN
- (4) Tr2 SOURCE
- (5) Tr2 GATE
- (6) Tr1 DRAIN



- ※ 1 ESD PROTECTION DIODE
- ※ 2 BODY DIODE

### 8. MARKING



“ J03 ” MEANS QS6J3.

9.MEASUREMENT CIRCUIT

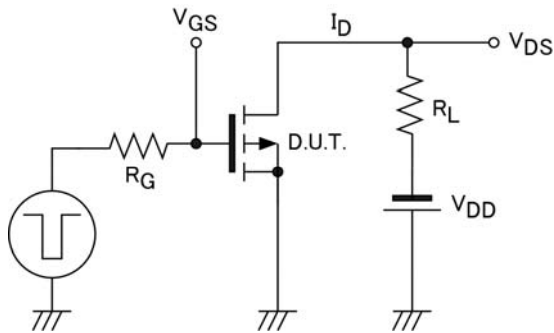


Fig.1-1 SWITCHING TIME MEASUREMENT CIRCUIT

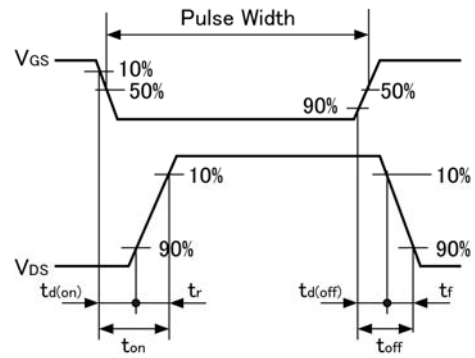


Fig.1-2 SWITCHING WAVEFORMS

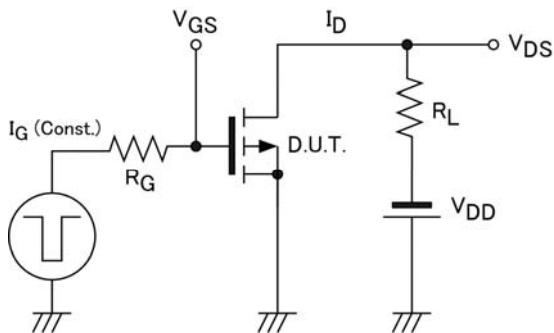


Fig.2-1 GATE CHARGE MASUREMENT CIRCUIT

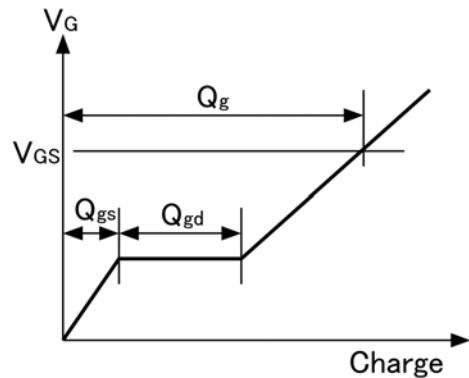


Fig.2-2 GATE CHARGE WAVEFORM

10.Notice

This product might cause chip aging and breakdown under the large electrified environment.  
Please consider to design ESD protection circuit.