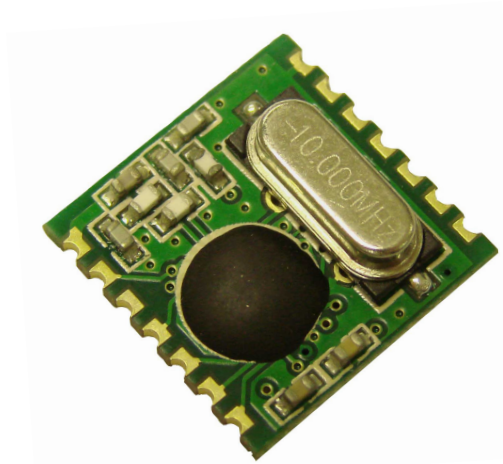


- FM Transceiver Module
- Low cost, high performance
- Fast PLL lock time
- Wakeup timer
- 2.2V – 3.8V power supply
- Low power consumption
- 10MHz crystal for PLL timing
- Clock and reset signal output for external MCU use
- 16 bit RX Data FIFO
- SPI interface
- Internal data filtering and clock recover
- Analog and digital signal strength indicator (ARSSI/DRSSI)
- Programmable TX frequency deviation (from 15 to 240 KHz)
- Programmable receiver bandwidth (from 67 to 400 kHz)
- Standby current less than 0.3uA
- Two 8 bit TX data registers
- High data rate (up to 115.2 kbps with internal demodulator □ with external RC filter highest data rate is 256 kbps)
- Operates from -45 to +85°C



## Applications

- Wireless Security Systems
- Car Alarms
- Remote Gate Controls
- Remote Sensing
- Data Capture
- Sensor Reporting

## Introduction

The Alpha Modules are extremely cost effective but high performance radio modules. Supplied in a miniature Surface mount package this Transceiver module can Transmit/Receive at upto 115Kbps at a maximum of 300m.

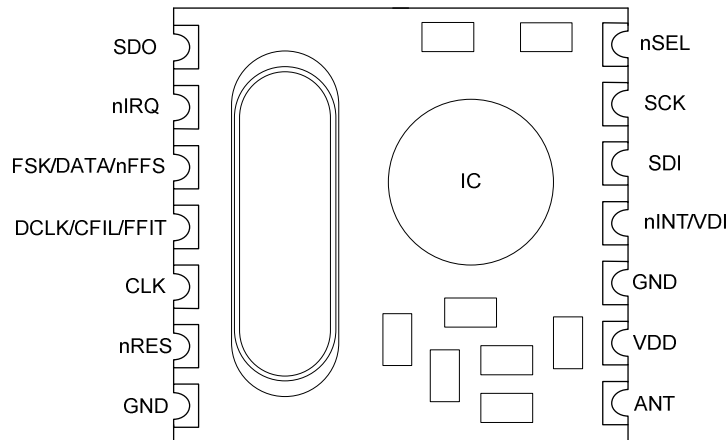
Operating at 2-5V, the module monitors its battery voltage and can sleep with very low standby current. The module can wake intermittently and provide direct control outputs to a microcontroller making it ideally suited to battery applications.

These Modules will suit one to one multi-node wireless links in applications including car and building security, POS and inventory tracking, remote process monitoring.

## Part Numbers

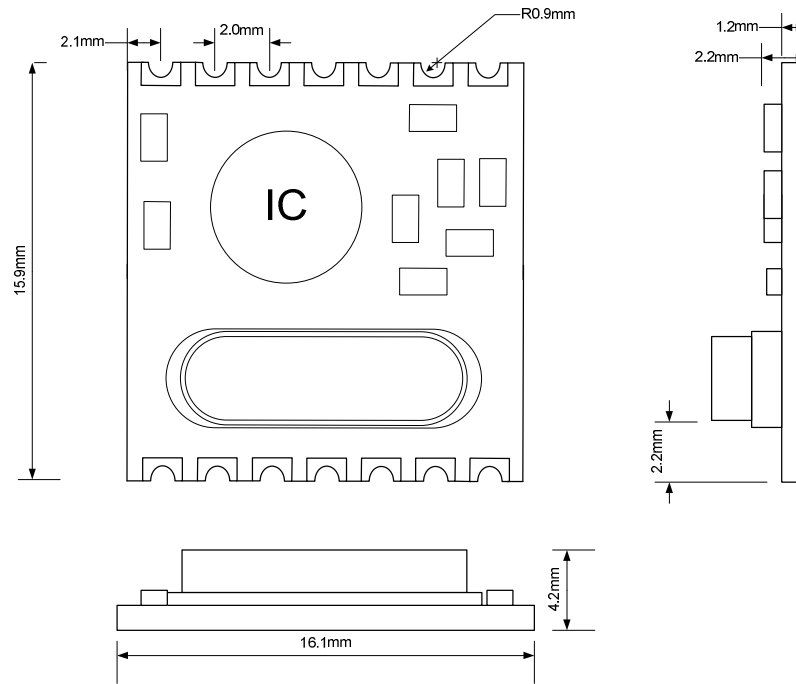
Part Number	Description
ALPHA-TRX433S	FM Transceiver Module, preset to 433MHz
ALPHA-TRX868S	FM Transceiver Module, preset to 868MHz
ALPHA-TRX915S	FM Transceiver Module, preset to 915MHz

## Pin Description



Pin	definition	Type	Function
11	nINT/VDI	DI/ DO	Interrupt input (active low)/Valid data indicator
9	VDD	S	Positive power supply
12	SDI	DI	SPI data input
13	SCK	DI	SPI clock input
8	ANT	IN	Antenna Connection
1	SDO	DO	Serial data output with bus hold
2	nIRQ	DO	Interrupts request output ( active low )
3	FSK/DATA/nFFS	DI/DO/DI	Transmit FSK data input/ Received data output (FIFO not used)/ FIFO select
4	DCLK/CFIL/FFIT	DO/AIO/DO	Clock output (no FIFO )/ external filter capacitor(analog mode)/ FIFO interrupts(active high)when FIFO level set to 1, FIFO empty interruption can be achieved
5	CLK	DO	Clock output for external microcontroller
6	nRES	DIO	Reset Input (active low )
7, 10	GND	S	Power ground
14	nSEL	DI	Chip select (active low)

## Mechanical Dimensions



## Electrical Parameters

### Maximum (not in working mode) □

symbol	parameter	minimum	maximum	Unit
$V_{dd}$	Positive power supply	-0.5	6.0	V
$V_{in}$	All pin input level	-0.5	$V_{dd}+0.5$	V
$I_{in}$	Input current except power	-25	25	mA
ESD	Human body model		1000	V
$T_{st}$	Storage temperature	-55	125	°C
$T_{ld}$	Soldering temperature(10s)		260	°C

### Recommended working range

symbol	parameter	minimum	maximum	Unit
$V_{dd}$	Positive power supply	2.2	3.8	V
$T_{op}$	Working temperature	-40	85	°C



# ALPHA RF TRANSCEIVER

ALPHA-TRX433S  
ALPHA-TRX915S

## DC characteristic

symbol	parameter	Remark	minimum	typical	maximum	Unit
I <sub>dd_TX_0</sub>	Supply current (TX mode, P <sub>out</sub> = 0dBm)	433MHz band 915MHz band		13 17		mA
I <sub>dd_TX_PMAX</sub>	Supply current (TX mode, P <sub>out</sub> = P <sub>max</sub> )	433MHz band 915MHz band		21 25		mA
I <sub>dd_RX</sub>	Supply current (RX mode)	433MHz band 915MHz band		10 13		mA
I <sub>x</sub>	Stand by current	Crystal and base band on		3□0	3□5	mA
I <sub>pd</sub>	Sleep mode current	All blocks off		0.3		uA
I <sub>lb</sub>	Low battery detection			0.5		uA
V <sub>lb</sub>	Low battery step	0.1V per step	2.2		5.3	V
V <sub>lba</sub>	Low battery detection accuracy			75		mV
V <sub>il</sub>	Low level input				0.3*V <sub>dd</sub>	V
V <sub>ih</sub>	High level input		0.7*V <sub>dd</sub>			V
I <sub>il</sub>	Leakage current	V <sub>il</sub> =0V	-1		1	uA
I <sub>ih</sub>	Leakage current	V <sub>ih</sub> =V <sub>dd</sub> , V <sub>dd</sub> =5.4V	-1		1	uA
V <sub>ol</sub>	Low level output	I <sub>ol</sub> =2mA			0.4	V
V <sub>oh</sub>	High level output	I <sub>oh</sub> =-2mA	V <sub>dd</sub> -0.4			V

## AC characteristic

symbol	parameter	remark	min	typical	max	Unit
f <sub>ref</sub>	PLL frequency		8	10	12	MHz
f <sub>LO</sub>	frequency (10MHz crystal used)	433 MHz band, 2.5KHz step 915 MHz band, 7.5KHz step	430.24 900.72		439.75 929.27	MHz
f <sub>LO</sub>	frequency (8MHz crystal used)	433 MHz band, 2.5KHz step 915 MHz band, 7.5KHz step	344.19 720.57		351.80 743.41	MHz
f <sub>LO</sub>	frequency (12MHz crystal used)	433 MHz band, 2.5KHz step 915 MHz band, 7.5KHz step	3516.28 1080.8		527.71 1115.1	MHz
BW	Receiver bandwidth	1 2 3 4 5 6	60 120 180 240 300 360	67 134 200 270 350 400	75 150 225 300 375 450	KHz
t <sub>lock</sub>	PLL lock time	After 10MHz step hopping, frequency error <10 kHz		20		us
BR	Data rate	With internal digital demodulator	0.6		115.2	kbps
BR <sub>A</sub>	Data rate	With external RC filter			256	kbps
		BW=134KHz, BR=1.2kbps, 433MHz band		-106	-100	
		BW=134KHz, BR=1.2kbps, 915MHz band		-102	-95	
AFC <sub>range</sub>	AFC working range	df <sub>FSK</sub> FSK deviation in the received signal		0.8* df <sub>FSK</sub>		
RS <sub>A</sub>	RSSI accuracy			±5		dB
RS <sub>R</sub>	RSSI range			46		dB
C <sub>ARSSI</sub>	ARSSI filter			1		nF
RS <sub>STEP</sub>	RSSI programmable step			6		dB
RS <sub>RESP</sub>	DRSSI response time	RSSI output high after valid, CARRSI=5nF		500		us





### AC characteristic(Transmitter)

symbol	parameter	remark	min	typical	max	Unit
		433MHz band	<b>3</b>	<b>5</b>		
		915MHz band	<b>-2</b>	<b>0</b>		
P <sub>out</sub>	Typical output power	Selectable in 3 dB steps	P <sub>max</sub> -21		P <sub>max</sub>	dbm
C <sub>o</sub>	Output capacitance (set by the automatic antenna tuning circuit)	In low bands In high bands	2 2.1	2.6 2.7	3.2 3.3	pf
Q <sub>o</sub>	Quality factor of the output capacitance	In low bands In high bands	13 8	15 10	17 12	
L <sub>out</sub>	Output phase noise	100 kHz from carrier 1 MHz from carrier			-75 -85	dbc/HZ
BR	FSK bit rate				256	kbps
df <sub>fsk</sub>	FSK frequency deviation	Programmable in 15 kHz steps	15		240	kHZ

### AC characteristic(Turn-on/Turnaround timings)

symbol	parameter	remark	min	typical	max	Unit
T <sub>st</sub>	Crystal oscillator startup time	Crystal ESR < 100			5	ms
T <sub>tx_rx_XTAL_ON</sub>	Transmitter - Receiver turnover time	Synthesizer off, crystal oscillator on		450		us
T <sub>rx_tx_XTAL_ON</sub>	Receiver - Transmitter turnover time	Synthesizer off, crystal oscillator on		350		us
T <sub>tx_rx_SYNT_ON</sub>	Transmitter - Receiver turnover time	Synthesizer on, crystal oscillator on		425		us
T <sub>rx_tx_SYNT_ON</sub>	Receiver - Transmitter turnover time	Synthesizer on, crystal oscillator on		300		us
C <sub>xl</sub>	Crystal load capacitance	Programmable in 0.5 pF steps, tolerance+/- 10%	8.5		16	pf
t <sub>POR</sub>	Internal POR timeout	After V <sub>dd</sub> has reached 90% of final value			100	ms
t <sub>PBt</sub>	Wake-up timer clock period	Calibrated every 30 seconds	0.96		1.05	ms
C <sub>in,D</sub>	Digital input apacitance				2	pf
t <sub>r, f</sub>	Digital output rise/fall time	15pF pure capacitive load			10	ns

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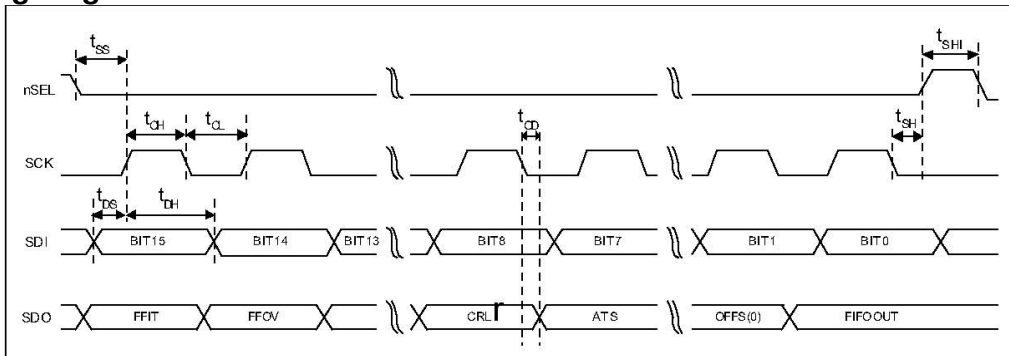
## Programming guide

### Brief description

ALPHA-TRX supports a command interface to setup frequency, deviation, output power and also data rate. There is no need to change any hardware when using frequency-hopping applications

### Commands

#### Timing diagram



### Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	0	0	el	ef	b1	b0	x3	x2	x1	x0	8008h

e l: Enable TX register  
e f: Enable RX FIFO buffer

b1..b0: select band

b1	b0	band[MHz]
0	0	Reserved
0	1	433
1	0	868
1	1	915

x3..x0: select crystal load capacitor

x3	x2	x1	x0	load capacitor [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
1	1	1	0	15.5
1	1	1	1	16.0



## Power Management Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	1	0	er	ebb	et	es	ex	eb	ew	dc	8208h

- er  Enable receiver
- ebb  Enable base band block
- et  Enable transmitter
- es  Enable synthesizer
- ex  Enable crystal oscillator
- eb  Enable low battery detector
- ew  Enable wake-up timer
- dc  Disable clock output of CLK pin

## Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A680h

- f11..f0: Set operation frequency:  
 433band:  $F_c = 430 + F * 0.0025$  MHz  
 868band:  $F_c = 860 + F * 0.0050$  MHz  
 915band:  $F_c = 900 + F * 0.0075$  MHz  
 Fc is carrier frequency and F is the frequency parameter.  $36 \leq F \leq 3903$

## Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	cs	r6	r5	r4	r3	r2	r1	r0	C623h

- r6..r0: Set data rate:  
 $BR = 10000000 / 29 / (R + 1) / (1 + cs * 7)$

## Receiver Control Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	0	P16	d1	d0	i2	i1	i0	g1	g0	r2	r1	r0	9080h

P16: select function of pin16

P16	
0	Interrupt input
1	VDI output

i2..i0: select baseband bandwidth

i2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	67
1	1	1	reserved



d1..d0: select VDI response time

d1	d0	Response
0	0	Fast
0	1	Medium
1	0	Slow
1	1	Always on

g1..g0: select LNA gain

g1	g0	LNA gain (dBm)
0	0	0
0	1	-6
1	0	-14
1	1	-20

r2..r0: select DRSSI threshold

r2	r1	r0	RSSIsetth [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85
1	0	0	-79
1	0	1	-73
1	1	0	Reserved
1	0	1	Reserved

The actual DRSSI threshold is related to LNA setup:  $SSI_{th} = RSSI_{setth} + G_{LNA}$ .

### Data Filter Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	al	ml	1	s	1	f2	f1	f0	C22Ch

al: Enable clock recovery auto-lock

ml: Enable clock recovery fast mode

s: select data filter type

s	Filter type
0	Digital filter
1	Analog RC filter

f1..f0: Set DQD threshold





## FIFO and Reset Mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	1	0	f3	f2	f1	f0	sp	al	ff	dr	CA80h

f3..f0: Set FIFO interrupt level

sp: Select the length of the synchron pattern:

sp	Byte1	Byte0 (POR)	Synchron Pattern (Byte1+Byte0)
0	2Dh	D4h	2DD4h
1	Not used	D4h	D4h

al: select FIFO fill start condition

al	condition
0	Sync-word
1	Always

ff: Enable FIFO fill

dr  Disable hi sensitivity reset mode

## Synchron pattern Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	b7	b6	b5	b4	b3	b2	b1	b0	CED4h

This command is used to reprogram the synchronic pattern;

## Receiver FIFO Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	B00h

This command is used to read FIFO data when FFIT interrupt generated. FIFO data output starts at 8th SCK period.

## AFC Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	a1	a0	r1	r0	st	fi	oe	en	C4F7h

a1..a0: select AFC auto-mode

a1	a0	
0	0	Controlled by MCU
0	1	Run once at power on
1	0	Keep offset when VDI hi
1	1	Keeps independently from VDI

r1..r0: select range limit

r1	r0	Range (fres)
0	0	No restriction
0	1	+15/-16
1	0	+7/-8
1	1	+3-4

freq

315  433band: 2.5kHz  
868band: 5kHz  
915band: 7.5kHz

st: st goes hi will store offset into output register

fi: Enable AFC hi accuracy mode

oe: Enable AFC output register

en: Enable AFC function

## TX Configuration Control Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	1	0	0	mp	m3	m2	m1	m0	0	p2	p1	p0	9800h

m: select modulation polarity

m2..m0: select frequency deviation:

m3	m2	m1	m0	frequency deviation [kHz]
0	0	0	0	15
0	0	0	1	30
0	0	1	0	45
0	0	1	1	60
0	1	0	0	75
0	1	0	1	90
0	1	1	0	105
0	1	1	1	120
1	0	0	0	135
1	0	0	1	150
1	0	1	0	165
1	0	1	1	180
1	1	0	0	195
1	1	0	1	210
1	1	1	0	225
1	1	1	1	240

p2..p0: select output power

p2	p1	p0	Output power[dBm]
0	0	0	0
0	0	1	-3
0	1	0	-6
0	1	1	-9
1	0	0	-12
1	0	1	-15
1	1	0	-18
1	0	1	-21

## PLL Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	0	ob1	ob0	lpx	ddy	ddi	1	bw0	CC67h

ob1-ob0: Microcontroller output clock buffer rise and fall time control.

ob1	ob0	Selected uC CLK frequency
0	0	5 or 10 MHz (recommended)
0	1	3.3 MHz
1	X	2.5 MHz or less

lpx: select low power mode of the crystal oscillator.

lpx	Crystal start-up time (typ)	Power consumption (typ)
0	1 ms	620 uA
1	2 ms	460 uA

ddy: phase detector delay enable.

ddi: disables the dithering in the PLL loop.

bw1-bw0: select PLL bandwidth

bw0	Max bit rate [kbps]	Phase noise at 1MHz offset [dBc/Hz]
0	86.2	-107
1	256	-102



### Transmitter Register Write Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	1	0	0	0	t7	t6	t5	t4	t3	t2	t1	t0	B8AAh

This command is use to write a data byte to RF12 and then RF12 transmit it

### Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up period is determined by:

$$T_{\text{wake-up}} = M * 2^R \text{ [ms]}$$

For continual operation, bit 'et' must be cleared and set

### Low Duty-Cycle Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	d6	d5	d4	d3	d2	d1	d0	en	C80Eh

d6..d0: Set duty cycle  
D.C.= (D \* 2 +1) / M \*100%

En: Enable low duty cycle mode

### Low Battery Detector and Microcontroller Clock Divider Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d2	d1	d0	0	v3	v2	v1	v0	C000h

d2..d0: select frequency of CLK pin

d2	d1	d0	Clock frequency[MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

CLK signal is derive form crystal oscillator and it can be applied to MCU clock in to save a second crystal.

If not used, please set bit "dc" to disable CLK output

To integrate the load capacitor internal can not only save cost, but also adjust reference frequency by software

v3..v0: Set threshold voltage of Low battery detector  $V_{lb}=2.2+V*0.1$  [V]





### Status Read Command

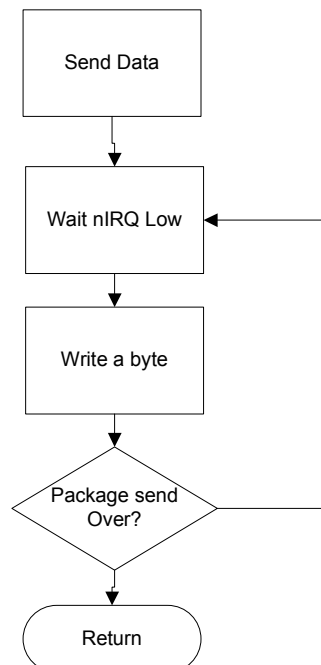
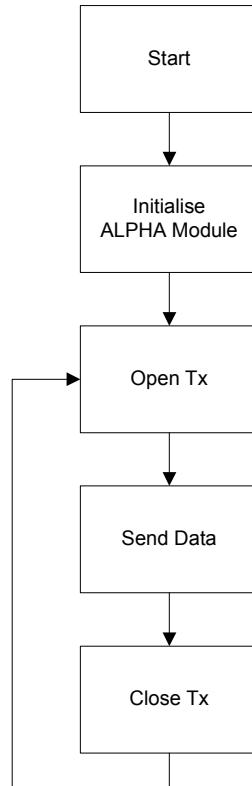
bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-

Bit	
15	TX ready for next byte or FIFO received data status
14	Power on reset status
13	TX Register under run or RX FIFO Overflow status
12	Wakeup timer overflow status
11	Interrupt on external source status
10	Low battery detect status
9	FIFO empty status
8	Antenna tuning signal strength
7	Received signal strength indicator
6	Data Quality Detector status
5	Clock Recovery Locked status
4	Toggling in each AFC cycle
3	Measured Offset Frequency Sign Value 1='+', 0='-'
2	Measured offset Frequency value (3 bits)
1	Measured offset Frequency value (3 bits)
0	Measured offset Frequency value (3 bits)

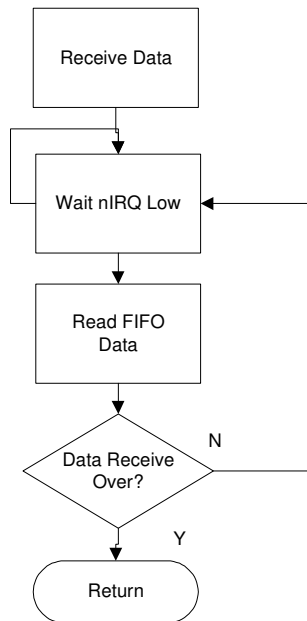
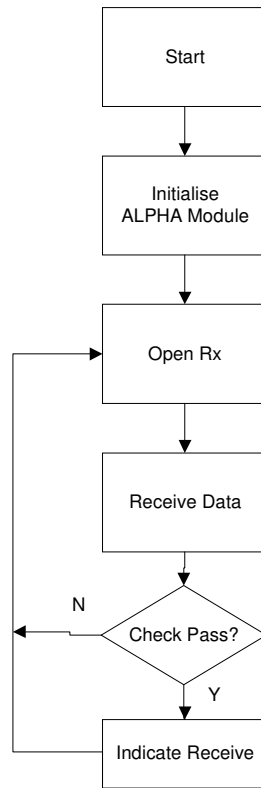
This command starts with a 0 and be used to read internal status register. Data output starts at 8<sup>th</sup> SCK period.



## Transmitter Operation Flow



## Receiver Operation Flow



After Initialisation, open FIFO receive mode and wait for nIRQ low, only then can the MCU read received and stored data in FIFO.  
For the next received package please reset FIFO