

Features

- Temperature ranges:
 - Commercial: 0 °C to 70 °C
 - Industrial: -40 °C to 85 °C
 - Automotive-A: -40 °C to 85 °C
- High speed
 - 55 ns
- CMOS for optimum speed/power
- Easy memory expansion with \overline{CE}_1 , CE_2 and \overline{OE} features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- Available in Pb-free 28-pin SNC package

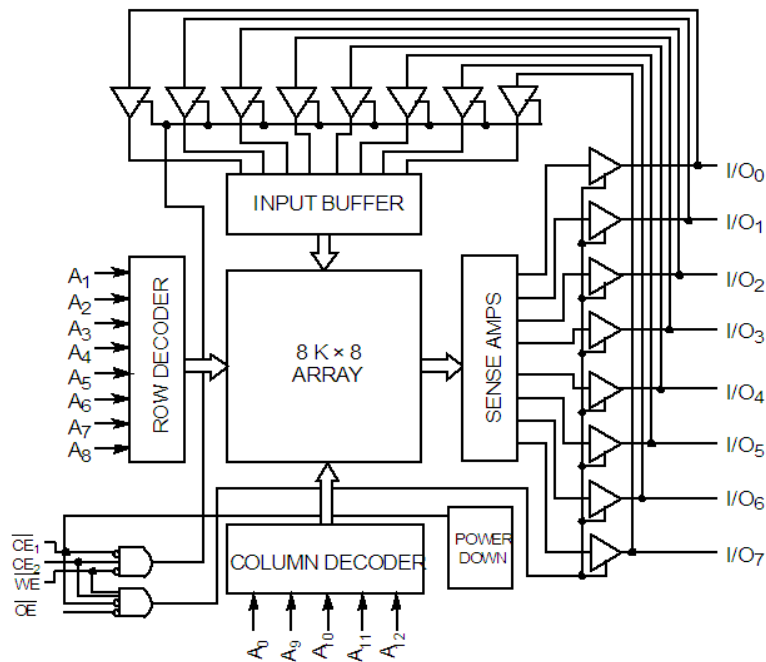
Functional Description

The CY6264 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), and active LOW output enable (\overline{OE}) and three-state drivers. Both devices have an automatic power-down feature (\overline{CE}_1), reducing the power consumption by over 70% when deselected. The CY6264 is packaged in a 450-mil (300-mil body) SOIC.

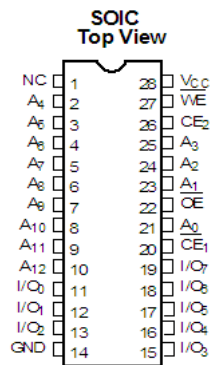
An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE}_1 and \overline{WE} inputs are both LOW and CE_2 is HIGH, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE}_1 and \overline{OE} active LOW, CE_2 active HIGH, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH. A die coat is used to ensure alpha immunity.

Logic Block Diagram



Pin Configuration



Selection Guide

Description	Range	-55	-70	Unit
Maximum access time		55	70	ns
Maximum operating current	Commercial	100	100	mA
	Industrial	260	200	mA
	Automotive-A	–	200	mA
Maximum CMOS standby current	Commercial	15	15	mA
	Industrial	30	30	mA
	Automotive-A	–	30	mA

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

- Storage temperature -65 °C to +150°C
- Ambient temperature with power applied -55 °C to +125 °C
- Supply voltage to ground potential -0.5 V to +7.0 V
- DC voltage applied to outputs in high Z state^[1] -0.5 V to +7.0 V
- DC input voltage^[1] -0.5 V to +7.0 V
- Output current into outputs (LOW) 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, Method 3015)

Latch-up current > 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	-40 °C to +85 °C	
Automotive-A	-40 °C to +85 °C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-55		-70		Unit	
			Min	Max	Min	Max		
V _{OH}	Output HIGH voltage	V _{CC} = Min, I _{OH} = -4.0 mA	2.4		2.4		V	
V _{OL}	Output LOW voltage	V _{CC} = Min, I _{OL} = 8.0 mA		0.4		0.4	V	
V _{IH}	Input HIGH voltage		2.2	V _{CC}	2.2	V _{CC}	V	
V _{IL}	Input LOW voltage ^[1]		-0.5	0.8	-0.5	0.8	V	
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	μA	
I _{OZ}	Output leakage current	GND ≤ V _I ≤ V _{CC} , output disabled	-5	+5	-5	+5	μA	
I _{CC}	V _{CC} operating supply current	V _{CC} = Max, I _{OUT} = 0 mA	Commercial	-	100	-	100	mA
			Industrial	-	260	-	200	
			Automotive-A	-		-	200	
I _{SB1}	Automatic \overline{CE}_1 power-down current	Max V _{CC} , $\overline{CE}_1 \geq V_{IH}$, Min duty cycle=100%	Commercial	-	20	-	20	mA
			Industrial	-	50	-	40	
			Automotive-A	-		-	40	
I _{SB2}	Automatic \overline{CE}_1 power-down current	Max V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3 V$, $V_{IN} \geq V_{CC} - 0.3 V$ or $V_{IN} \leq 0.3 V$	Commercial	-	15	-	15	mA
			Industrial	-	30	-	30	
			Automotive-A	-		-	30	

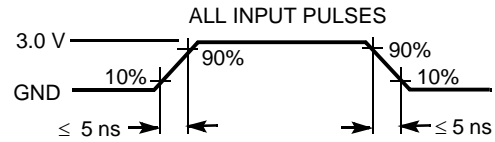
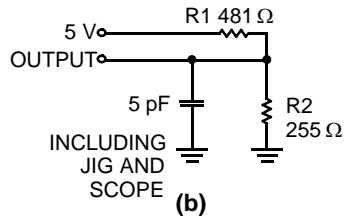
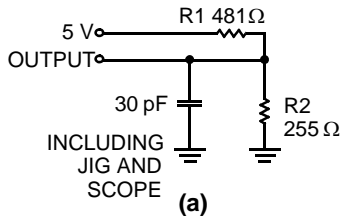
Capacitance

Parameter ^[2]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V	7	pF
C _{OUT}	Output capacitance		7	pF

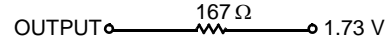
Notes

1. Minimum voltage is equal to -3.0 V for pulse durations less than 30 ns.
2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics

Over the Operating Range

Parameter ^[3]	Description	-55		-70		Unit
		Min	Max	Min	Max	
READ CYCLE						
t _{RC}	Read cycle time	55	–	70	–	ns
t _{AA}	Address to data valid	–	55	–	70	ns
t _{OHA}	Data hold from address change	5	–	5	–	ns
t _{ACE1}	CE ₁ LOW to data valid	–	55	–	70	ns
t _{ACE2}	CE ₂ HIGH to data valid	–	40	–	70	ns
t _{DOE}	OE LOW to data valid	–	25	–	35	ns
t _{LZOE}	OE LOW to low Z	3	–	5	–	ns
t _{HZOE}	OE HIGH to high Z ^[4]	–	20	–	30	ns
t _{LZCE1}	CE ₁ LOW to low Z ^[5]	5	–	5	–	ns
t _{LZCE2}	CE ₂ HIGH to low Z	3	–	5	–	ns
t _{HZCE}	CE ₁ HIGH to high Z ^[4, 6] CE ₂ LOW to high Z	–	20	–	30	ns
t _{PU}	CE ₁ LOW to power-up	0	–	0	–	ns
t _{PD}	CE ₁ HIGH to power-down	–	25	–	30	ns
WRITE CYCLE^[6]						
t _{WC}	Write cycle time	50	–	70	–	ns
t _{SCE1}	CE ₁ LOW to write end	40	–	60	–	ns
t _{SCE2}	CE ₂ HIGH to write end	30	–	50	–	ns
t _{AW}	Address setup to write end	40	–	55	–	ns
t _{HA}	Address hold from write end	0	–	0	–	ns
t _{SA}	Address setup to write start	0	–	0	–	ns
t _{PWE}	WE pulse width	25	–	40	–	ns
t _{SD}	Data setup to write end	25	–	35	–	ns
t _{HD}	Data hold from write end	0	–	0	–	ns
t _{HZWE}	WE LOW to high Z ^[4]	–	20	–	30	ns
t _{LZWE}	WE HIGH to low Z	5	–	5	–	ns

Notes

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any device.
- The internal write time of the memory is defined by the overlap of CE₁ LOW, CE₂ HIGH, and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

Figure 1. Read Cycle No. 1^[7, 8]

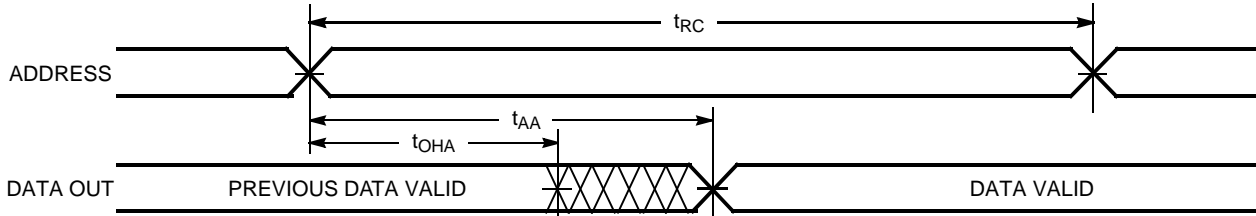
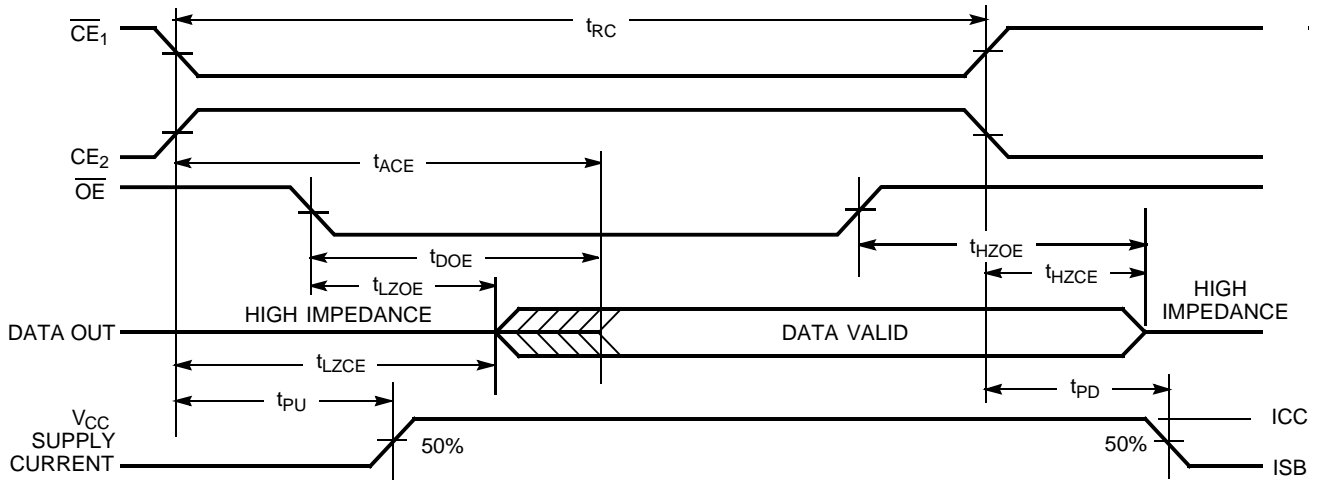


Figure 2. Read Cycle No. 2^[9, 10]



Notes

7. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}, CE_2 = V_{IH}$.
8. Address valid prior to or coincident with CE transition LOW.
9. \overline{WE} is HIGH for read cycle.
10. Data I/O is High Z if $\overline{OE} = V_{IH}, \overline{CE}_1 = V_{IH}$, or $\overline{WE} = V_{IL}$.

Switching Waveforms (continued)

Figure 3. Write Cycle No. 1 (\overline{WE} Controlled)^[11, 12]

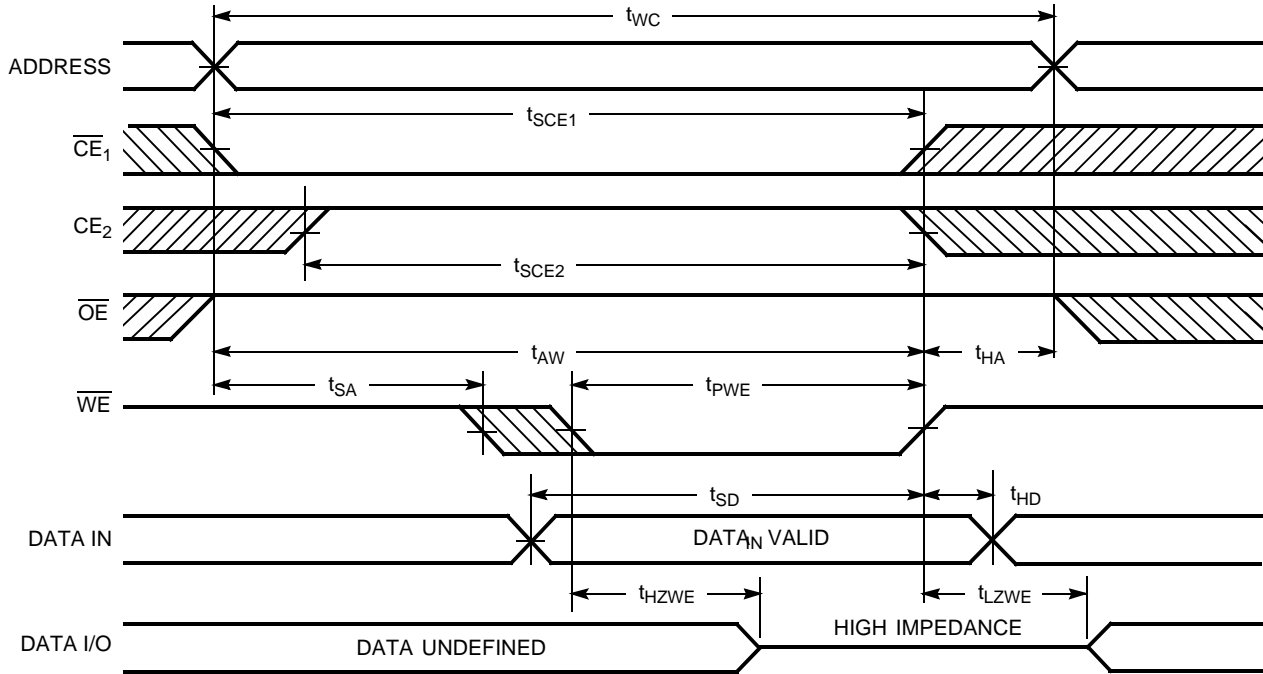
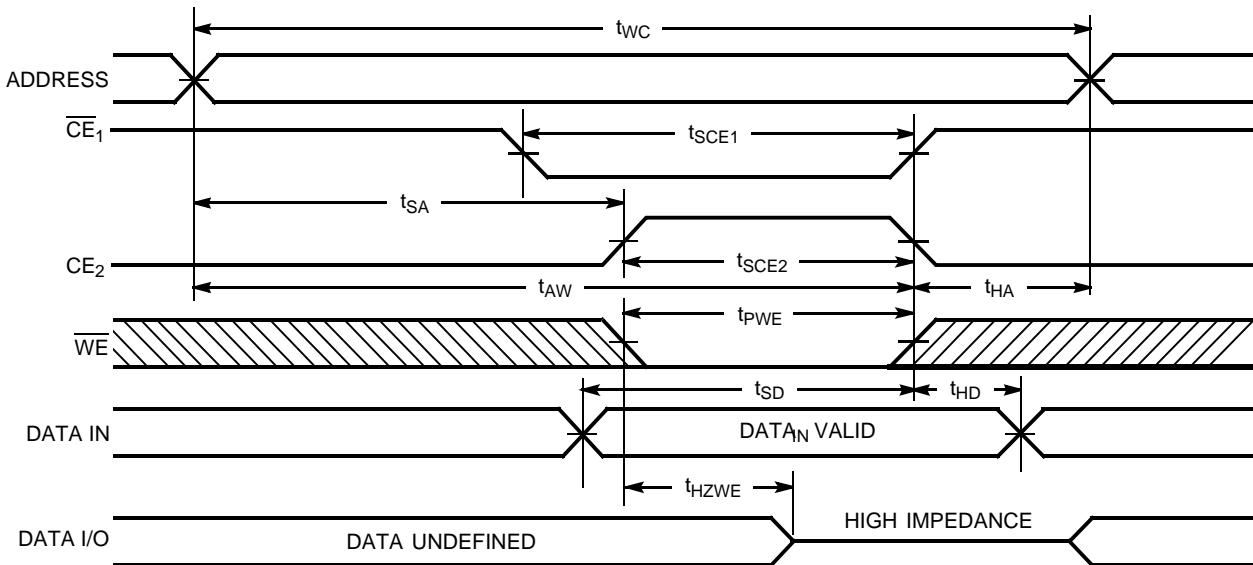


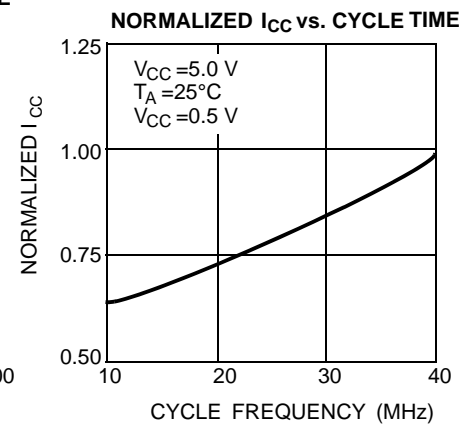
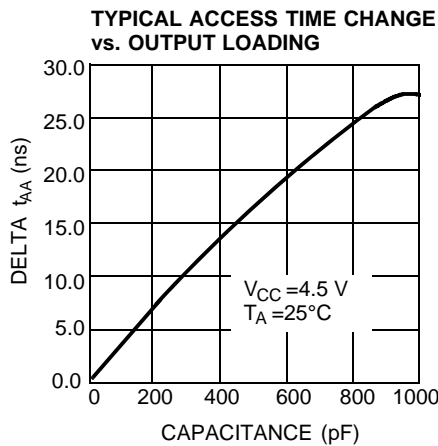
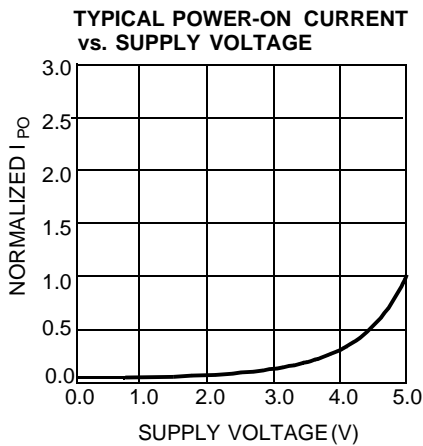
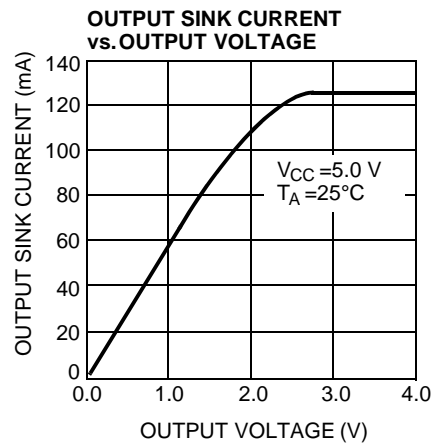
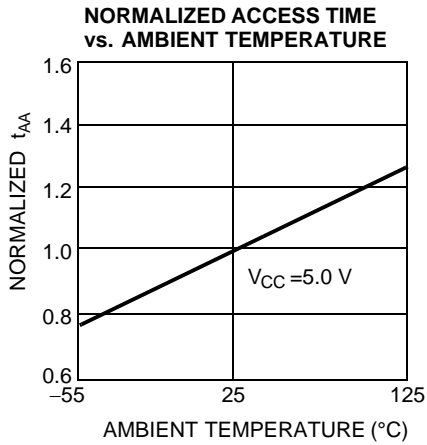
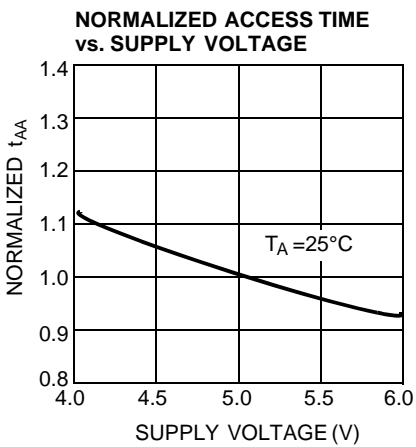
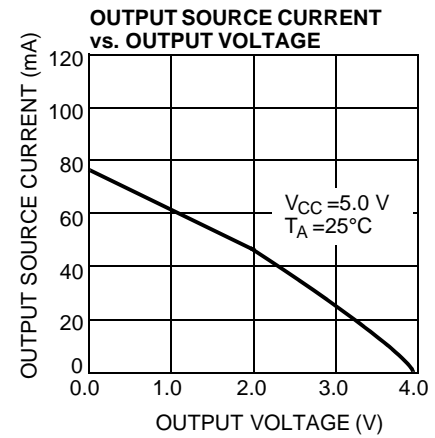
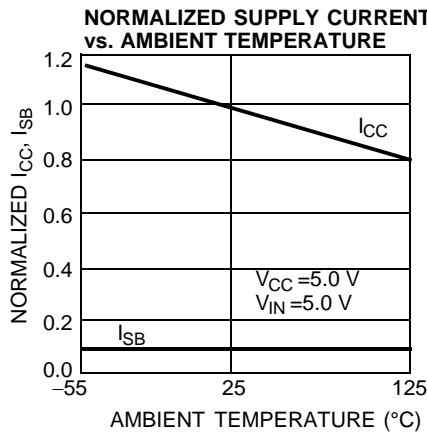
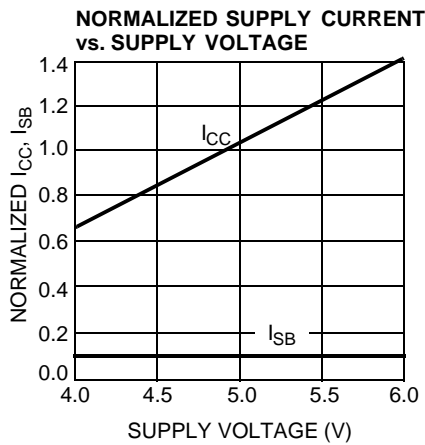
Figure 4. Write Cycle No. 2 (\overline{CE} Controlled)^[11, 12, 13]



Notes

- 11. Address valid prior to or coincident with \overline{CE} transition LOW.
- 12. Data I/O is High Z if $OE = V_{IH}$, $\overline{CE}_1 = V_{IH}$, or $WE = V_{IL}$.
- 13. If \overline{CE} goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



Truth Table

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

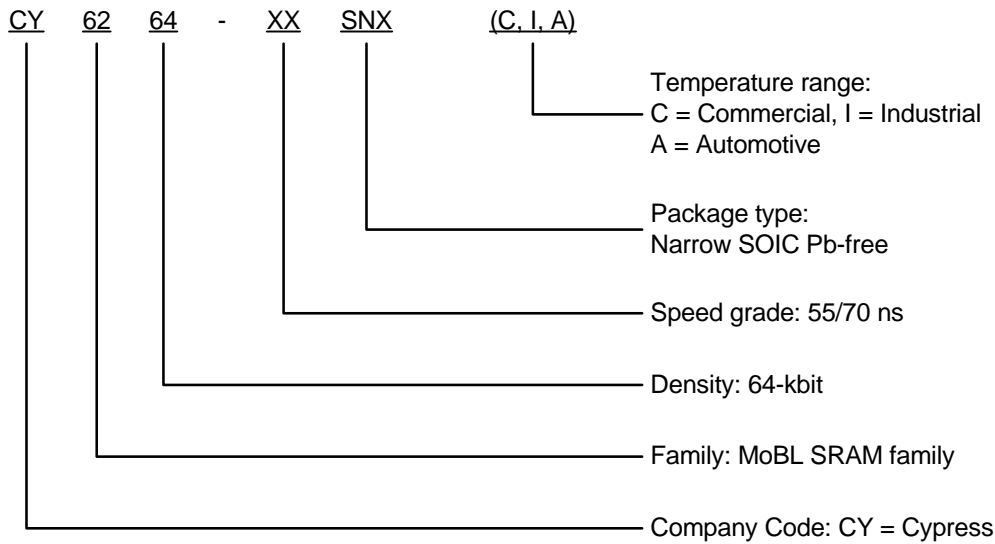
Ordering Information

Table 1 lists the CY6264 key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and see the product summary page at <http://www.cypress.com/products>.

Table 1. Static RAM Key Features and Ordering Information

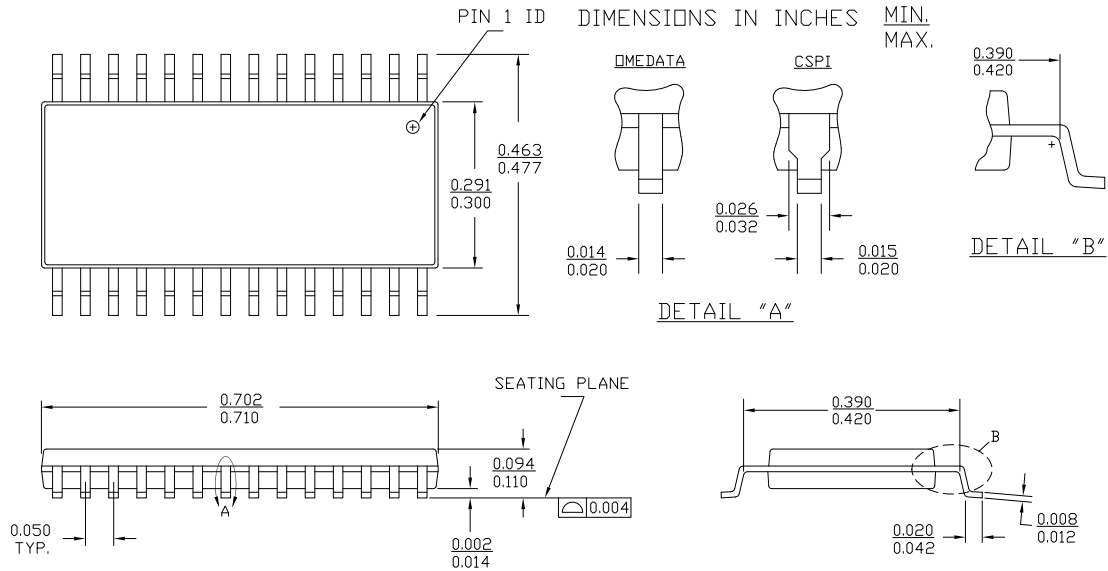
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY6264-55SNXI	51-85092	28-pin (300-mil narrow body) SNC (Pb-free)	Industrial
70	CY6264-70SNXC	51-85092	28-pin (300-mil narrow body) SNC (Pb-free)	Commercial
	CY6264-70SNXA		28-pin (300-mil narrow body) SNC (Pb-free)	Automotive-A

Ordering Code Definitions



Package Diagram

Figure 5. 28-pin (300-mil) SNC Package Outline (Narrow Body) (51-85092)



51-85092 *C

Reference Information

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
VFBGA	very fine ball grid array
TSOP	thin small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microampere
mA	milliampere
MHz	megahertz
ns	nanosecond
pF	picofarad
V	volt
Ω	ohm
W	watt

Document History Page

Document Title: CY6264 8 K x 8 Static RAM Document Number: 001-02367				
Revision	ECN	Orig. of Change	Submission date	Description of Change
**	384870	PCI	06/28/05	Spec # change from 38-00425 to 001-02367
*A	488954	VKN	See ECN	Added Automotive product Added 55 ns Industrial spec Removed SOIC package from the product offering Changed the description of I _{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I _{OS} parameter from DC Electrical Characteristics table Updated ordering Information table
*B	2892510	VKN	See ECN	Updated Ordering Information table Updated Package Diagram Added Sales, Solutions, and Legal Information
*C	3329873	RAME	07/27/11	Updated template and styles according to current Cypress standards. Added acronyms, units, and ordering code definitions. Removed reference to AN1064 SRAM system guidelines.

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