User's Guide

SLVU185–September 2006

TPS5410EVM-203 1-A, SWIFT™ Regulator Evaluation Module

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1 Introduction

This user's guide contains background information for the TPS5410 as well as support documentation for the TPS5410EVM-203 evaluation module (HPA203) . Also included are the performance specifications, the schematic, and the bill of materials for the TPS5410EVM-203.

1.1 Background

The TPS5410 dc/dc converter is designed to provide up to a 1-A output from an input voltage source of 5.5 V to 36 V. The TPS5410EVM-203 is designed using 2 independent circuits providing output voltages of 12 V and 5 V. Rated input voltage and output current range for the evaluation module is given in Table 1. This evaluation module is configured to demonstrate the flexibility of the TPS5410 regulators. The switching frequency is internally set at a nominal 500 kHz. The high-side MOSFET is incorporated inside the TPS5410 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS5410 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are provided internal to the integrated circuit (IC), whereas an external divider allows for an adjustable output voltage. Additionally, the TPS5430/31 provides an enable input. The absolute maximum input voltage is 40 V for the TPS5410EVM-203.

Table 1. Input Voltage and Output Current Summary

OUTPUT VOLTAGE	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
12 V	VIN = 14.5 V to 36 V	0 A to 1 A
5 V	VIN = 7 V to 36 V	0 A to 1 A

1.2 Performance Specification Summary

A summary of the TPS5410EVM-203 performance specifications is provided in Table 2. Specifications are given for an input voltage of VIN = 25 V and an output voltage of 12 V or 5 V, unless otherwise specified. The TPS5410EVM-203 is designed and tested for VIN = 14.5 V to 36 V for the 12 V circuit and VIN = 7 V to 36 V for the 5 V circuit. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS5410EVM-203 Performance Specification Summary

SPECIFICATION		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VIN voltage range	12 V output			14.5		36	V
	5 V output			7		36	
Output voltage set point	12 V output				12.0		V
	5 V output				5.0		
Output current range (both circuits)				0		1	A
Line regulation	12 V output	I_O = 0.5 A, VIN = 14.5 V – 36 V			±0.05%		
	5 V output	I_O = 0.5 A, VIN = 3 V – 36 V			±0.09%		
Load regulation	12 V output	VIN = 25 V, I_O = 0 A to 1 A			±0.03%		
	5 V output				±0.03%		
Load transient response	12 V output	I_O = 0.25 A to 0.75 A	Voltage change		–110		mV
			Recovery time		150		µs
	5 V output		Voltage change		–70		mV
			Recovery time		200		µs
	12 V output	I_O = 0.25 A to 0.75 A	Voltage change		110		mV
			Recovery time		150		µs
	5 V output		Voltage change		70		mV
			Recovery time		200		µs
Loop bandwidth	12 V output	VIN = 25 V, I_O = 0.5 A			10		kHz
	5 V output	VIN = 25 V, I_O = 0.5 A			17		

Table 2. TPS5410EVM-203 Performance Specification Summary (continued)

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase margin	12 V output	VIN = 25 V , I_O = 0.5 A		60		°
	5 V output	VIN = 25 V, I_O = 0.5 A		71		
Input ripple voltage	12 V output	I_O = 1 A		180		mVpp
	5 V output			50		
Output ripple voltage	12 V output	I_O = 1 A		15		mVpp
	5 V output			8		
Output rise time				8		ms
Operating frequency				500		kHz
Max efficiency	12 V output	VIN = 14.5 V, V_O = 12 V, I_O = 0.8 A		96.3%		
	5 V output	VIN = 7 V, V_O = 5 V, I_O = 0.4 A		94.3%		

1.3 Modifications

These evaluation modules are designed to demonstrate the small size that can be attained when designing with the TPS5410. A few changes can be made to this module.

1.3.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R3 (12 V circuit) or R4 (5 V circuit). Changing the value of these resistors can change the output voltage above 1.25 V. The value of R for a specific output voltage can be calculated using Equation 1.

$$R2 = 10\ k\Omega \times \frac{1.221\ V}{V_O - 1.221\ V} \quad (1)$$

Table 3 lists the R values for some common output voltages. Note that VIN must be in a range so that the minimum on-time is greater than 200 ns, and the maximum duty cycle is less than 87%. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Table 3. Output Voltages Available

Output Voltage (V)	R_2 Value (kΩ)
1.8	21.5
2.5	9.53
3.3	5.90
5	3.24

1.3.2 External Compensation

The TPS5410 utilizes an internally synthesized type 3 compensation network. As this compensation network is fixed, it is ideally suited for a limited range of output filter components. Both the 12 V and 5 V circuits contain additional component locations that allow the overall loop characteristics of the circuits to be modified so that output filter capacitors that would normally not be useable can be accommodated. These components are C6, C9, C12 and R1 for the 12 V circuit and C5, C10, C13 and R2 for the 5 V circuit. These components can be used to place two additional pole / zero pairs into the feedback loop. Also present are 0 Ω resistors, R5 and R7, in the feedback path of each circuit. These maybe removed to break the loop to verify the loop response if modifications are made.

The 12 V circuit on the EVM is designed using as standard type of output filter that works well with the internal compensation. The external compensation components C6, C9, C12 and R1 are left open. The 5 V circuit is designed to use ceramic output capacitors. The external compensation components are required for this design and are populated as shown in the schematic of Figure 20. For additional information on designing with ceramic or aluminum electrolytic capacitors using the TPS5410 or other

wide voltage range SWIFT devices, see SLVA237 *Using TPS5410/20/30/31 With Aluminum/Ceramic Output Capacitors.* It should be noted that for this design the value of the output capacitors was derated by 70 percent to account for the reduced capacitance of ceramic capacitors that have a bias voltage applied. Also, C5 is added to the circuit to improve load regulation performance. If the circuit is modified for different pole / zero locations, C5 should be chosen to be less than 1/10 the value of C13.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS5410EVM-203 evaluation module. The section also includes test results typical for the evaluation modules and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and startup.

2.1 Input / Output Connections

The TPS5410EVM-203 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 1 A should be connected to J1 and J2 for the 12 V circuit or J3 and J4 for the 5 V circuit. If both circuits are powered from the same supply, make sure that the supply is capable of supplying the full current for both circuits. The load should be connected to J5 and J6 for the 12 V output, and J7 and J8 for the 5 V output. Connections should be made using short lengths of 20 AWG wires or better to avoid losses. The maximum load current capability should be 1 A for each circuit. Each of the input and output connectors provides two pins, one for the intended connection and one provides Kelvin connection point to monitor the input and output voltages.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	VIN for 12 V circuit (see Table 1 for Vin range)
J2	GND return for 12 V circuit VIN
J3	VIN for 5 V circuit (see Table 1 for Vin range)
J4	GND return for 5 V circuit VIN
J5	12 V output
J6	GND return for 12 V output
J7	5 V output
J8	GND return for 5 V output
JP1	2-pin header for enable of 5 V output. Connect EN to ground to disable, open to enable.
JP2	2-pin header for enable of 12 V output. Connect EN to ground to disable, open to enable.
TP1	PH node of 5 V circuit
TP2	PH node of 12 V circuit
TP3	VSENSE node of 12 V output
TP4	VSENSE node of 5 V output
TP5	Test point between voltage divider network and R5. Used for loop response measurements of 12 V circuit.
TP6	Test point between voltage divider network and R7. Used for loop response measurements of 5 V circuit.

2.2 Efficiency

The efficiency for both EVM output voltages peak at a load current of about 0.75 A, and then decrease as the load current increases towards full load. Figure 1 shows the efficiency for the 12 V output at an ambient temperature of 25°C.

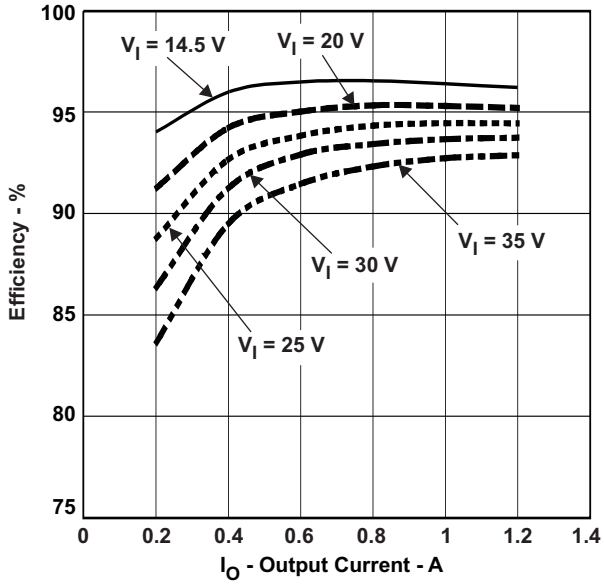


Figure 1. TPS5410 12 V Output Efficiency

Figure 2 shows the efficiency for the 5 V output at an ambient temperature of 25°C.

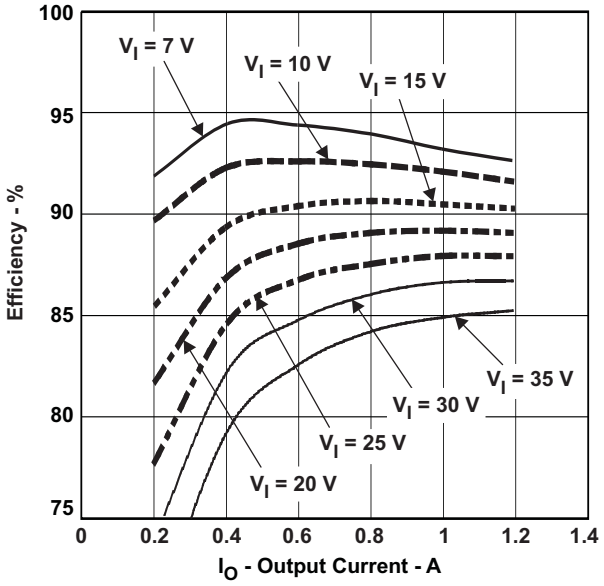


Figure 2. TPS5410 5 V Output Efficiency

The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs.

2.3 Output Voltage Load Regulation

The load regulation for the 12 V and 5 V outputs are shown in Figure 3 and Figure 4.

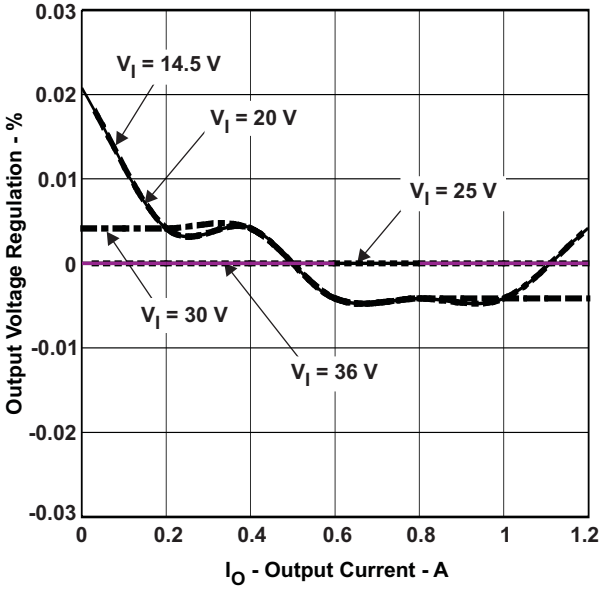


Figure 3. TPS5410 12 V Output Load Regulation

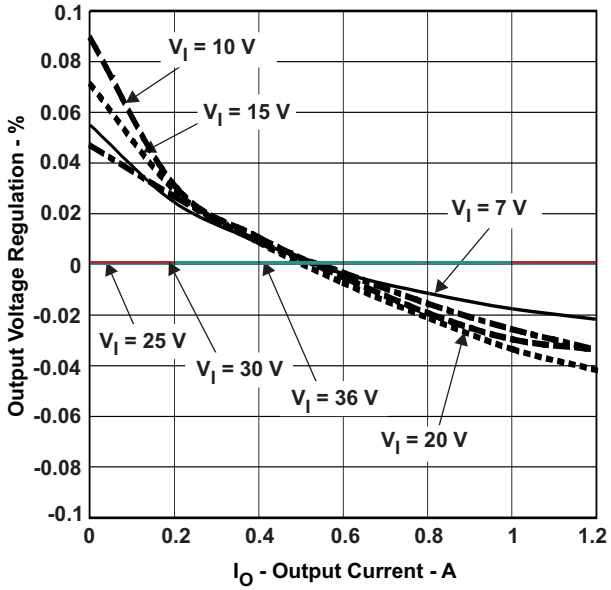


Figure 4. TPS5410 5 V Output Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output voltage Line Regulation

The line regulation for the 12 V and 5 V outputs are shown in Figure 5 and Figure 6.

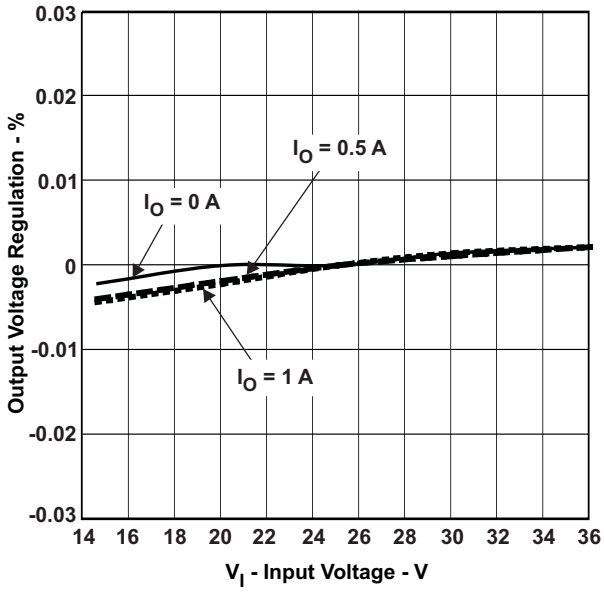


Figure 5. TPS5410 12 V Output Line Regulation

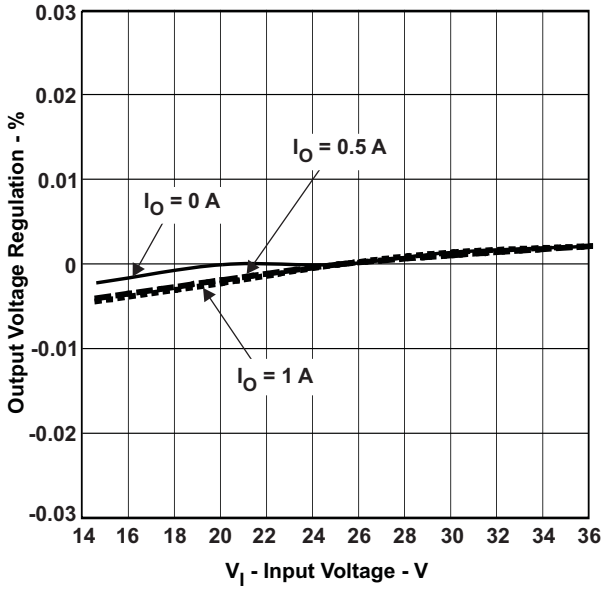


Figure 6. TPS5410 5 V Output Line Regulation

2.5 Load Transients

The 12 V and 5 V circuit response to load transients is shown in Figure 7 and Figure 8. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

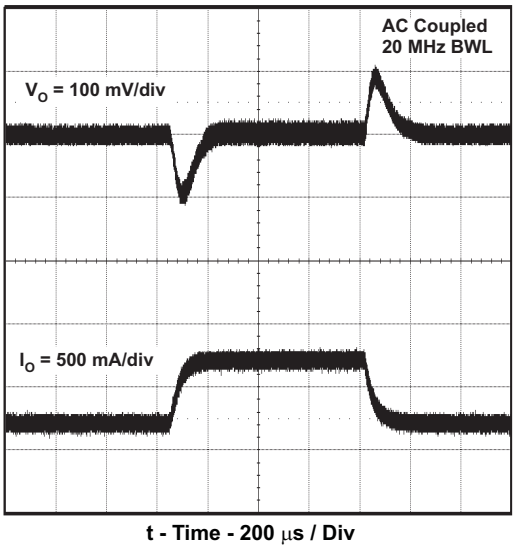


Figure 7. TPS5410 12 V Output Transient Response

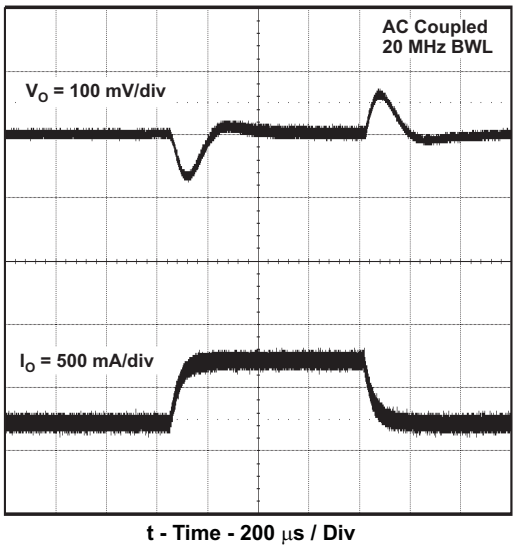


Figure 8. TPS5410 5 V Output Transient Response

2.6 Loop Characteristics

The 12 V and 5 V output loop-response characteristics are shown in Figure 9 and Figure 10. Gain and phase plots are shown for VIN voltage of 25 V. Load current for both measurements is 0.5 A.

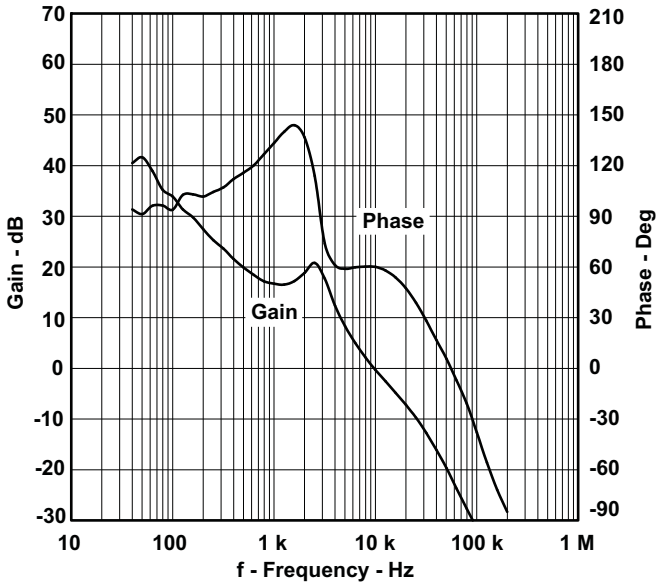


Figure 9. TPS5410 12 V Output Loop Response

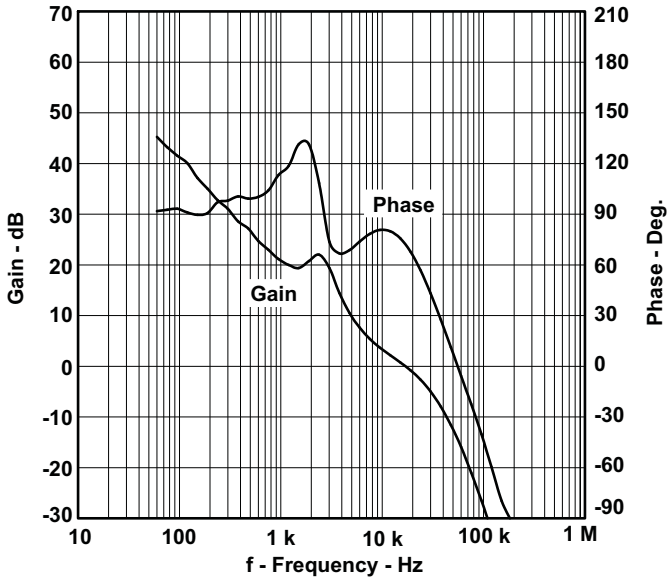


Figure 10. TPS5410 5 V Output Loop Response

2.7 Output Voltage Ripple

The 12 V and 5 V output voltage ripple is shown in Figure 11 and Figure 12 . The output current is the rated full load of 1 A. Voltage is measured directly across output capacitors.

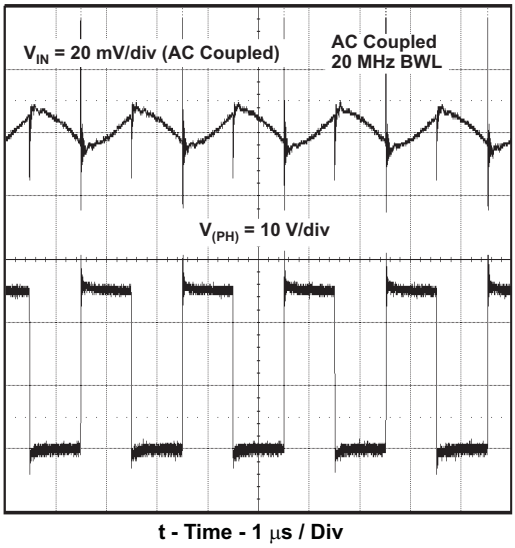


Figure 11. TPS5410 12 V Output Ripple

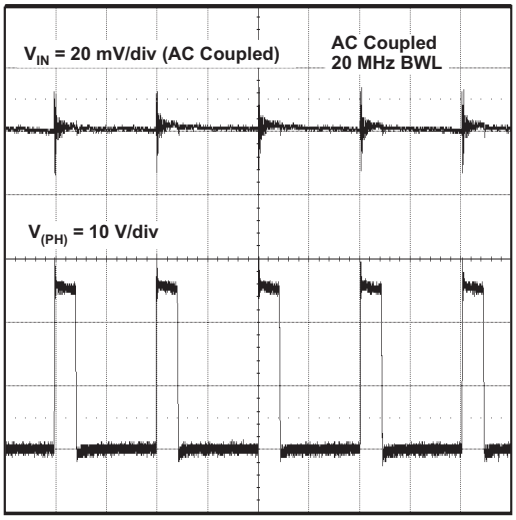


Figure 12. TPS5410 5 V Output Ripple

2.8 Input Voltage Ripple

The 12 V and 5 V input voltage ripple is shown in Figure 13 and Figure 14. The output current for each device is at full rated load of 1 A.

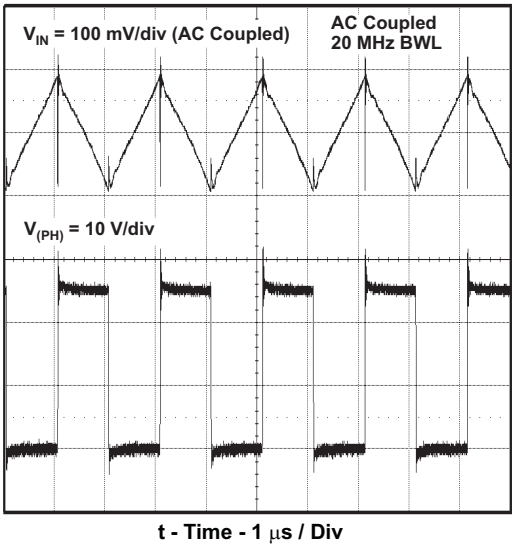


Figure 13. TPS5410 12 V Input Ripple

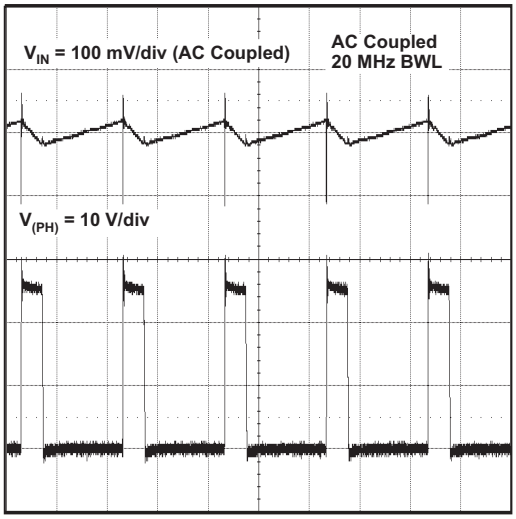


Figure 14. TPS5410 5 V Input Ripple

2.9 Powering Up

The start-up waveforms are shown in Figure 15 and Figure 16. In Figure 15, the top trace shows ENA, and the bottom trace shows Vout for the 12 V circuit. Initially, the output is inhibited by using a jumper at JP2 to tie ENA to GND. When the jumper is removed, ENA is released. When the ENA voltage reaches the enable-threshold voltage of 1.06 V, the start-up sequence begins and the internal reference voltage begins to ramp up at the internally set rate towards 1.221 V and the output voltage ramps up to the externally set value of 12 V. Figure 16 shows the start-up waveform relative to the input voltage. With the ENA pin open, the input voltage is applied to the circuit. When the UVLO threshold is reached, the start up sequence begins and the internal reference voltage begins to ramp up at the internally set rate towards 1.221 V and the output voltage ramps up to the externally set value of 12 V. The start up waveforms are similar for the 5 V circuit.

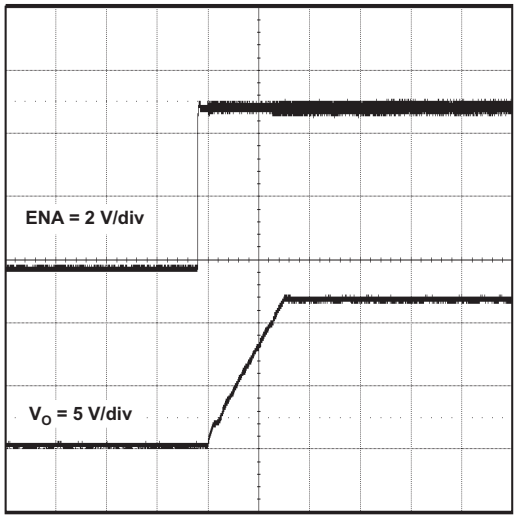


Figure 15. TPS5410 Start-Up, ENA and V_O

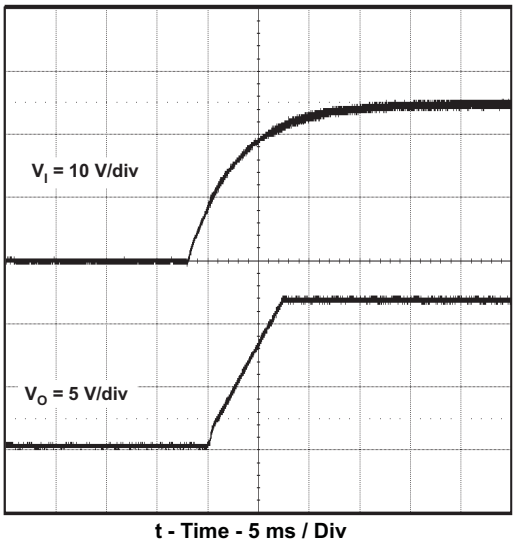


Figure 16. Startup Waveform, V_I and V_O

3 Board Layout

This section provides a description of the TPS5410EVM-203 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS5410EVM-203 is shown in Figure 17 through Figure 19. The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for VOUT, and VPH for both circuits. Also on the top layer are connections for the remaining pins of each TPS5410 and a large ground traces. The bottom layer contains the input voltage traces, routes for the ENA feature and VSENSE traces for both circuits. Although the two circuits are independent, the ground traces are connected together with a trace on the top side.

The input decoupling capacitors (C1 and C2) and bootstrap capacitors (C3 and C4) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper Vout trace at the output connector.

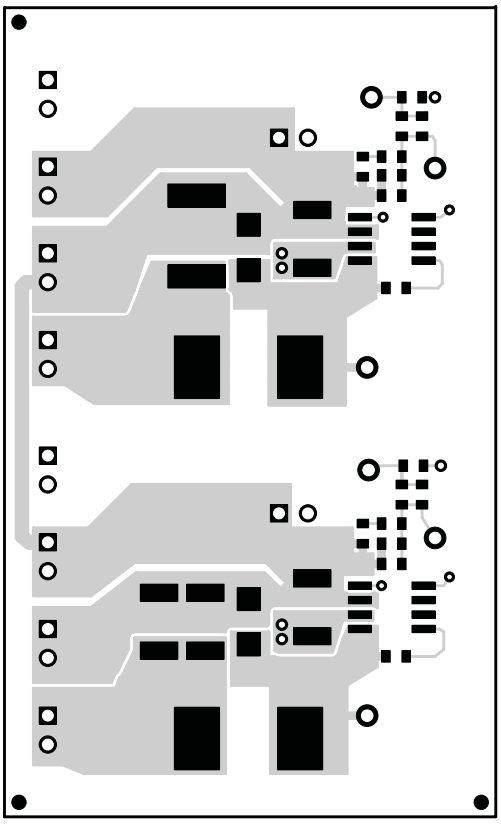


Figure 17. Top-Side Layout

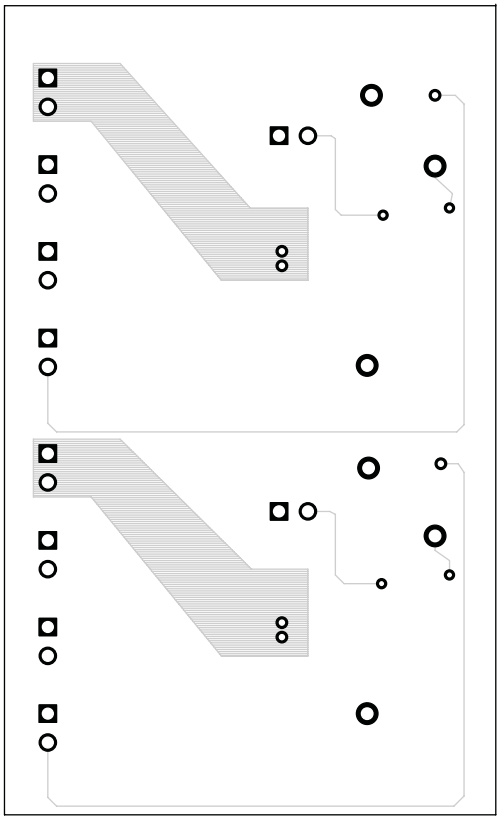


Figure 18. Bottom-Side Layout (Looking From Top Side)

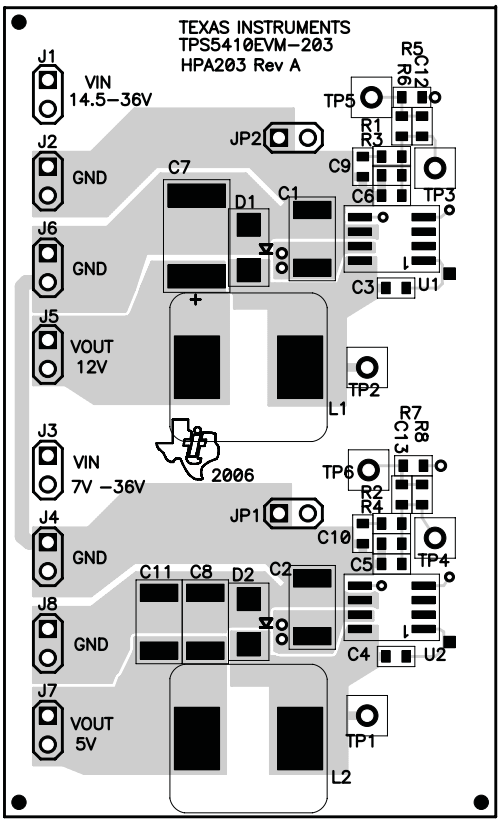


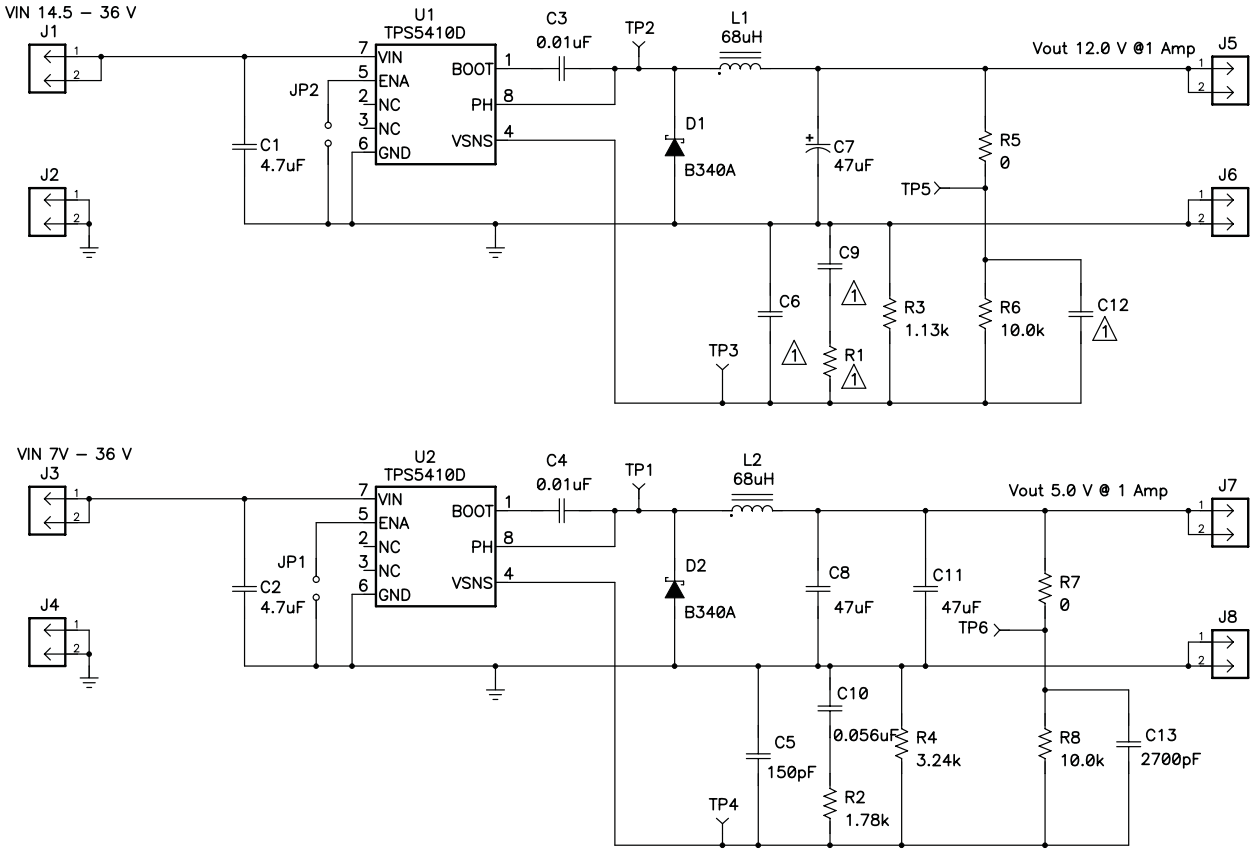
Figure 19. Top-Side Assembly

4 Schematic and Bill of Materials

The TPS5410EVM-203 and TPS5431EVM-173 schematic and bill of materials are presented in this section.

4.1 Schematic

The schematic for the TPS5410EVM-203 is shown in Figure 20.



(1) Not used.

Figure 20. TPS5410EVM-203 Schematic

4.2 Bill of Materials

The bill of materials for the TPS5410EVM-203 is given by Table 5.

Table 5. Bill of Materials

			HPA203A BOM			
COUNT	**RefDes**	**Value**	**DESCRIPTION**	**SIZE**	**Part Number**	**MFR**
2	C1, C2	4.7uF	Capacitor, Ceramic, 50V, X5R, 20%	1812	C4532X5R1H475MT	TDK
1	C10	0.056uF	Capacitor, Ceramic, 25V, X7R, 10%	0603	ECJ-1VB1E563K	Panasonic
1	C13	2700pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H272J	TDK
2	C3, C4	0.01uF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H103K	TDK
1	C5	150pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H151J	TDK
0	C6, C9, C12	Open	Capacitor, Ceramic, xxV	0603		
1	C7	47uF	Capacitor, Tantalum, 20V,	7343 (D)	TPSE476M020R0150	AVX
2	C8, C11	47uF	Capacitor, Ceramic, 10V, X5R, 20%	1812	C4532X5R1A476MT	TDK
2	D1, D2		Diode, Schottky, 3A, 40V	SMA	B340A	Diodes Inc
8	J1- J8		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	
2	JP1, JP2		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
2	L1, L2	68uH	Inductor, SMT, 2.3A, 130milliohm	0.484 x 0.484	MSS1260-683MLB	Coilcraft
0	R1	Open	Resistor, Chip, 1/16W, yy%	0603		
1	R2	1.78k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	1.13k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	3.24k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R5, R7	0	Resistor, Chip, 1/16W, 5%	0603	Std	Std
2	R6, R8	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
6	TP1 - TP6		Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100	5000	Keystone
2	U1, U2		IC, Switching Step-Down Regulator, 5.5V-36V, 1A	SO8	TPS5410D	TI
1	--		PCB, 2.8 In x 1.7 In x 0.062 In		HPA203	Any
2	--		Shunt, 100mil, Black	0.100	929950-00	3M

Table 5. Bill of Materials (continued)

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range and the output current range specified in Table 1.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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