DMOS Dual Full-Bridge PWM Motor Driver With Overcurrent Protection

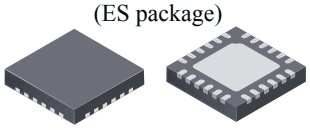
Features and Benefits

- Low $R_{DS(ON)}$ outputs
- Internal mixed current decay mode
- Synchronous rectification for low power dissipation
- Internal UVLO
- Crossover-current protection
- 3.3 and 5 V compatible logic supply
- Thin profile QFN and TSSOP packages
- Thermal shutdown circuitry
- Short-to-ground protection
- Shorted load protection
- Low current Sleep mode, < 10 µA

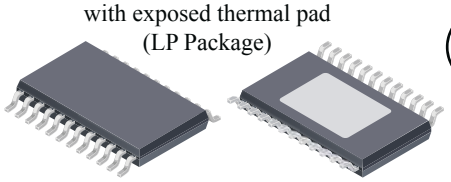
Packages:

24-contact QFN
4 mm × 4 mm × 0.75 mm
(ES package)

Approximate size



24-pin TSSOP
with exposed thermal pad
(LP Package)



Description

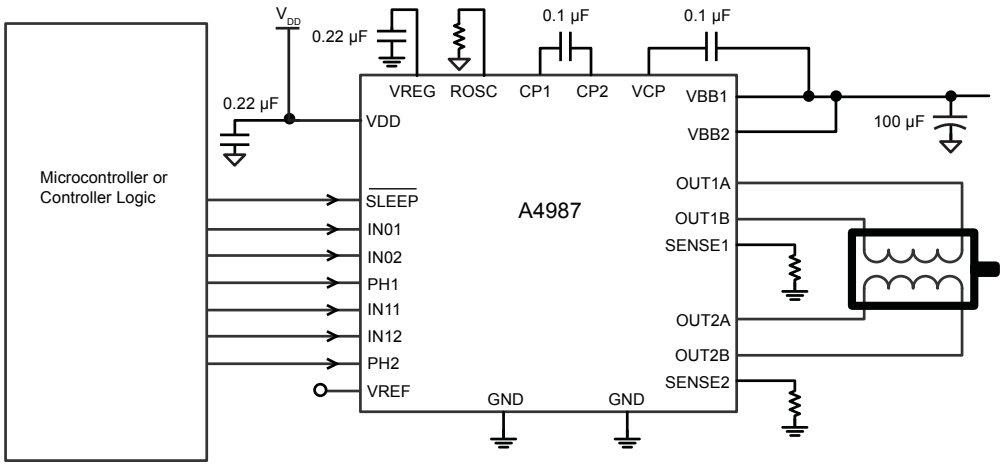
The A4987 is a dual DMOS full-bridge stepper motor driver with parallel input communication and overcurrent protection. Each full-bridge output is rated up to 35 V and ±1 A. The A4987 includes fixed off-time pulse width modulation (PWM) current regulators, along with 2- bit nonlinear DACs (digital-to-analog converters) that allow stepper motors to be controlled in full, half, and quarter steps. The PWM current regulator uses the Allegro® patented mixed decay mode for reduced audible motor noise, increased step accuracy, and reduced power dissipation.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation.

The outputs are protected from shorted load and short-to-ground events, which protect the driver and associated circuitry from thermal damage or flare-ups. Other protection features include thermal shutdown with hysteresis, undervoltage lockout (UVLO) and crossover current protection. Special power-up sequencing is not required.

The A4987 is supplied in two packages, a 24-contact QFN (ES) and a 24-pin TSSOP (LP). Both packages have exposed thermal pads for enhanced thermal performance. The 24-contact ES is 4 mm × 4 mm, with a nominal overall package height of 0.75 mm. The 24-pin LP is a TSSOP with 0.65 pitch and an overall package height of ≤1.2 mm. Both packages are lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application Diagram



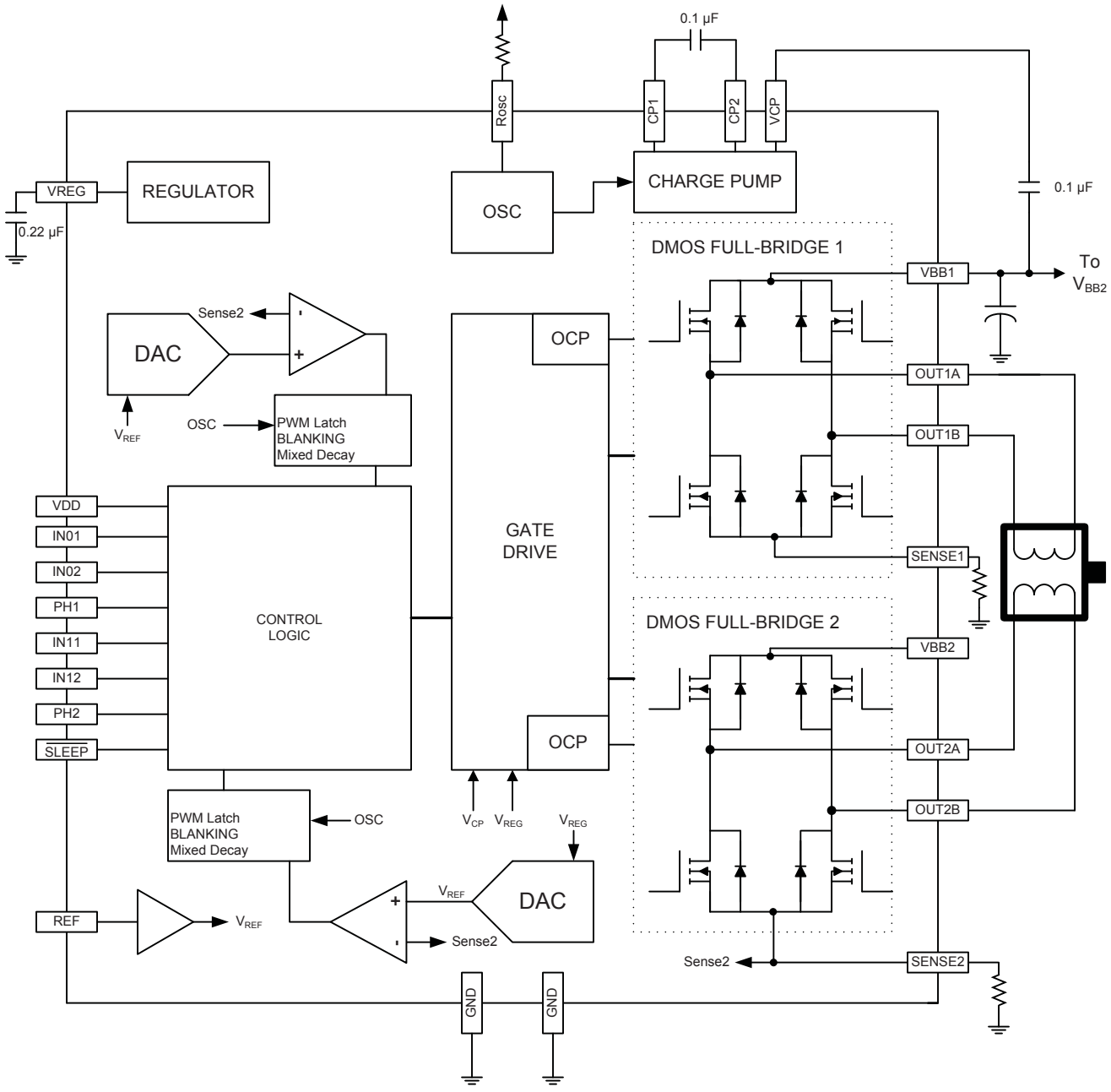
Selection Guide

Part Number	Package	Packing
A4987SESTR-T	24-pin QFN with exposed thermal pad	1500 pieces per 7-in. reel
A4987SLPTR-T	24-pin TSSOP with exposed thermal pad	4000 pieces per 13-in. reel

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		35	V
Output Current	I_{OUT}		±1	A
Logic Input Voltage	V_{IN}		–0.3 to 5.5	V
Logic Supply Voltage	V_{DD}		–0.3 to 5.5	V
VBBx to OUTx			35	V
Sense Voltage	V_{SENSE}		0.5	V
Reference Voltage	V_{REF}		5.5	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	ºC
Maximum Junction	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Functional Block Diagram



ELECTRICAL CHARACTERISTICS[1] at T_A = 25°C, V_{BB} = 35 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	8	–	35	V
		During Sleep Mode	0	–	35	V
Logic Supply Voltage Range	V_{DD}	Operating	3.0	–	5.5	V
Output On Resistance	$R_{DS(ON)}$	Source Driver, I_{OUT} = –800 mA	–	700	900	mΩ
		Sink Driver, I_{OUT} = 800 mA	–	700	900	mΩ
Body Diode Forward Voltage	V_F	Source Diode, I_F = –800 mA	–	–	1.3	V
		Sink Diode, I_F = 800 mA	–	–	1.3	V
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	–	4	mA
		Operating, outputs disabled	–	–	2	mA
		Sleep Mode	–	–	10	μA
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz	–	–	8	mA
		Outputs off	–	–	5	mA
		Sleep Mode	–	–	10	μA
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		V_{DD}×0.7	–	–	V
	$V_{IN(0)}$		–	–	V_{DD}×0.3	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}×0.7	–20	<1.0	20	μA
	$I_{IN(0)}$	V_{IN} = V_{DD}×0.3	–20	<1.0	20	μA
Logic Input Pull-down	R_{IN02}		–	100	–	kΩ
	R_{IN12}		–	50	–	kΩ
Logic Input Hysteresis	$V_{HYS(IN)}$	As a % of V_{DD}	5	11	19	%
Blank Time	t_{BLANK}		0.7	1	1.3	μs
Fixed Off-Time	t_{OFF}	OSC = VDD or GND	20	30	40	μs
		R_{OSC} = 25 kΩ	23	30	37	μs
Reference Input Voltage Range	V_{REF}		0	–	4	V
Reference Input Current	I_{REF}		–3	0	3	μA
Current Trip-Level Error[3]	err_I	V_{REF} = 2 V, %$I_{TripMAX}$ = 33.3%	–	–	±15	%
		V_{REF} = 2 V, %$I_{TripMAX}$ = 66.7%	–	–	±5	%
		V_{REF} = 2 V, %$I_{TripMAX}$ = 100.00%	–	–	±5	%
Crossover Dead Time	t_{DT}		100	475	800	ns
Protection						
Overcurrent Protection Threshold	I_{OCPST}		1.1	–	–	A
Thermal Shutdown Temperature	T_{TSD}		–	165	–	°C
Thermal Shutdown Hysteresis	T_{TSDHYS}		–	15	–	°C
VDD Undervoltage Lockout	V_{DDUVLO}	V_{DD} rising	2.7	2.8	2.9	V
VDD Undervoltage Hysteresis	$V_{DDUVLOHYS}$		–	90	–	mV

[1]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

[2]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

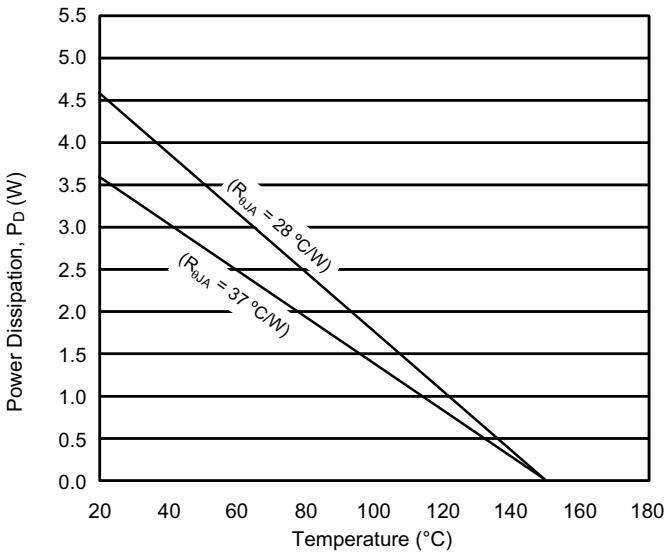
[3]$V_{ERR} = [(V_{REF}/8) – V_{SENSE}] / (V_{REF}/8)$.

THERMAL CHARACTERISTICS may require derating at maximum conditions

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	ES package; estimated, on 4-layer PCB, based on JEDEC standard	37	ºC/W
		LP package; on 4-layer PCB, based on JEDEC standard	28	ºC/W

*In still air. Additional thermal information available on Allegro Web site.

Maximum Power Dissipation, $P_{D(max)}$



Functional Description

Device Operation. The A4987 is designed to operate one stepper motor in full, half, or quarter step mode. The currents in each of the output full-bridges, all N-channel DMOS, are regulated with fixed off-time pulse width modulated (PWM) control circuitry. Each full-bridge peak current is set by the value of an external current sense resistor, R_{Sx}, and a reference voltage, V_{REFx}.

Percentages of the peak current are set using a 2-bit nonlinear DAC that programs 33%, 66%, or 100% of the peak current, or disables the outputs.

Internal PWM Current Control. Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value, I_{TRIP}. Initially, a diagonal pair of source and sink FET outputs are enabled and current flows through the motor winding and the current sense resistor, R_{Sx}. When the voltage across R_{Sx} equals the DAC output voltage, the current sense comparator resets the PWM latch. The latch then turns off the appropriate source driver and initiates a fixed off time decay mode.

The maximum value of current limiting is set by the selection of R_{Sx} and the voltage at the VREF pin. The transconductance function is approximated by the maximum value of current limiting, $I_{TripMAX}$ (A), which is set by

$$I_{TripMAX} = V_{REF} / (8 \times R_S)$$

where R_S is the resistance of the sense resistor (Ω) and V_{REF} is the input voltage on the REF pin (V).

The 2-bit DAC output reduces the V_{REF} output to the current sense comparator in precise steps, such that

$$I_{trip} = (\%I_{TripMAX} / 100) \times I_{TripMAX}$$

It is critical that the maximum rating (0.5 V) on the SENSE1 and SENSE2 pins is not exceeded.

Fixed Off-Time. The internal PWM current control circuitry uses a one-shot circuit to control the duration of time that the DMOS FETs remain off. The off-time, t_{OFF}, is determined by the ROSC terminal. The ROSC terminal has two settings:

- ROSC tied to VDD or ground — off-time internally set to 30 µs
- ROSC through a resistor to ground — off-time is determined by the following formula:

$$t_{OFF} \approx R_{OSC} / 825$$

Blanking. This function blanks the output of the current sense comparators when the outputs are switched by the internal current control circuitry. The comparator outputs are blanked to prevent false overcurrent detection due to reverse recovery currents of the clamp diodes, and switching transients related to the capacitance of the load. The blank time, t_{BLANK} (µs), is approximately

$$t_{BLANK} \approx 1 \text{ µs}$$

Shorted-Load and Short-to-Ground Protection. If the motor leads are shorted together, or if one of the leads is shorted to ground, the driver will protect itself by sensing the overcurrent event and disabling the driver that is shorted, protecting the device from damage. In the case of a short-to-ground, the device will remain disabled (latched) until the $\overline{\text{SLEEP}}$ input goes high or VDD power is removed. A short-to-ground overcurrent event is shown in figure 1.

When the two outputs are shorted together, the current path is through the sense resistor. After the blanking time (≈1 µs) expires, the sense resistor voltage is exceeding its trip value, due to the overcurrent condition that exists. This causes the driver to go into a fixed off-time cycle. After the fixed off-time expires the driver turns on again and the process repeats. In this condition the driver is completely protected against overcurrent events, but the short is repetitive with a period equal to the fixed off-time of the driver. This condition is shown in figure 2.

During a shorted load event it is normal to observe both a positive and negative current spike as shown in figure 3, due to the direction change implemented by the Mixed decay feature. This is shown in figure 3. In both instances the overcurrent circuitry is protecting the driver and prevents damage to the device.

Charge Pump (CP1 and CP2). The charge pump is used to generate a gate supply greater than that of VBB for driving the source-side FET gates. A 0.1 µF ceramic capacitor, should be connected between CP1 and CP2. In addition, a 0.1 µF ceramic capacitor is required between VCP and VBB, to act as a reservoir for operating the high-side FET gates.

Capacitor values should be Class 2 dielectric ±15% maximum, or tolerance R, according to EIA (Electronic Industries Alliance) specifications.

V_{REG} (VREG). This internally-generated voltage is used to operate the sink-side FET outputs. The nominal output voltage of the VREG terminal is 7 V. The VREG pin must be decoupled with a 0.22 µF ceramic capacitor to ground. V_{REG} is internally monitored. In the case of a fault condition, the FET outputs of the A4987 are disabled.

Capacitor values should be Class 2 dielectric ±15% maximum, or tolerance R, according to EIA (Electronic Industries Alliance) specifications.

Shutdown. In the event of a fault, overtemperature (excess T_J) or an undervoltage (on VCP), the FET outputs of the A4987 are disabled until the fault condition is removed. At power-on, the UVLO (undervoltage lockout) circuit disables the FET outputs and resets the translator to the Home state.

Sleep Mode ($\overline{\text{SLEEP}}$). To minimize power consumption when the motor is not in use, this input disables much of the internal circuitry including the output FETs, current regulator, and charge pump. A logic low on the $\overline{\text{SLEEP}}$ pin puts the A4987 into Sleep mode. When emerging from Sleep mode, in order to allow the charge pump to stabilize, provide a delay of 1 ms before issuing a logic command.

Mixed Decay Operation. The bridge operates in Mixed Decay mode, as shown in figures 5 through 7. As the trip point is reached, the A4987 initially goes into a fast decay mode for 31.25% of the off-time, t_{OFF}. After that, it switches to Slow Decay mode for the remainder of t_{OFF}. A timing diagram for this feature appears in figure 4.

Synchronous Rectification. When a PWM-off cycle is triggered by an internal fixed-off time cycle, load current recirculates in Mixed Decay mode. This synchronous rectification feature turns on the appropriate FETs during current decay, and effectively shorts out the body diodes with the low FET $R_{DS(ON)}$. This reduces power dissipation significantly, and can eliminate the need for external Schottky diodes in many applications. Synchronous rectification turns off when the load current approaches zero (0 A), preventing reversal of the load current.

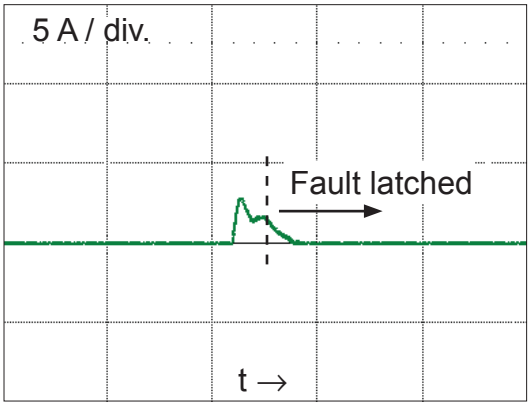


Figure 1. Short-to-ground event

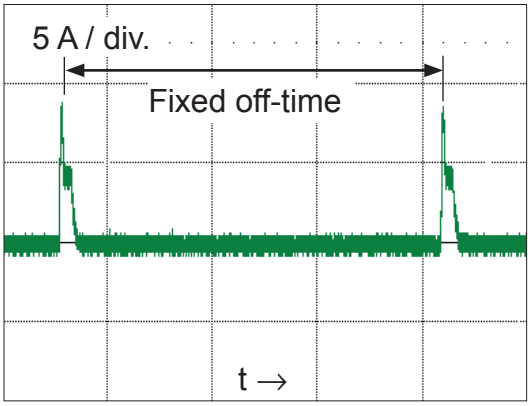


Figure 2. Shorted load (OUTxA → OUTxB) in Slow decay mode

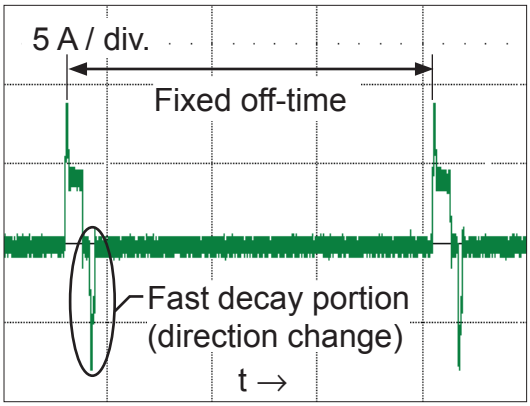
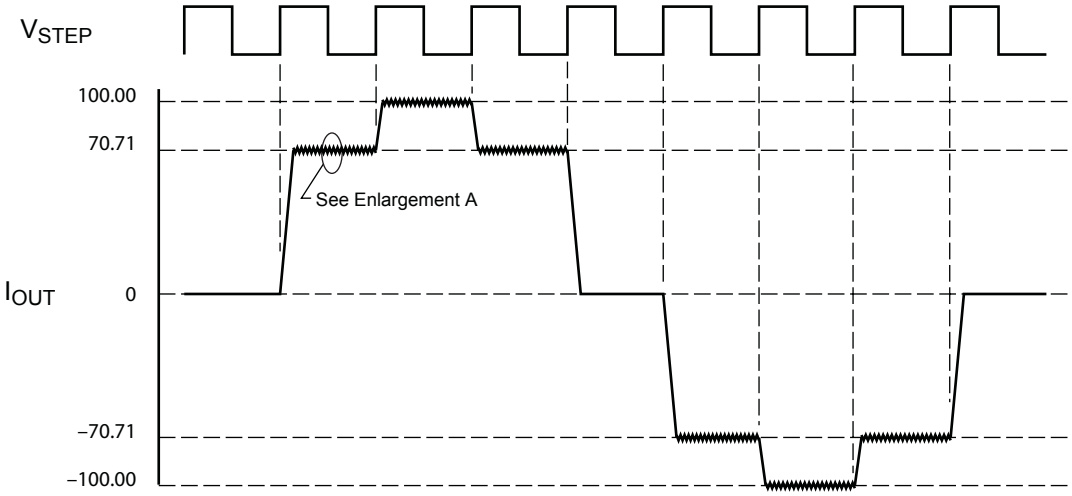
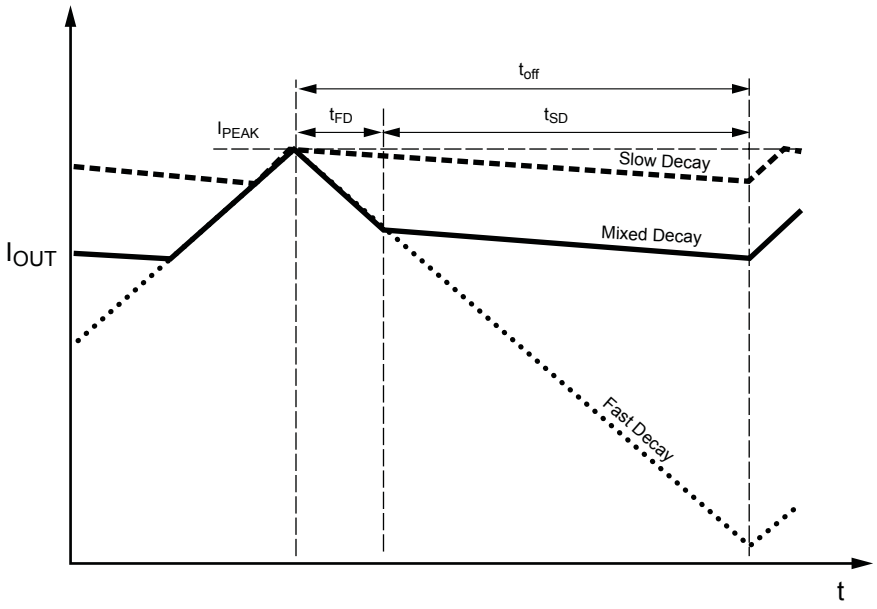


Figure 3. Shorted load (OUTxA → OUTxB) in Mixed decay mode



Enlargement A



Symbol	Characteristic
t_{off}	Device fixed off-time
I_{PEAK}	Maximum output current
t_{SD}	Slow decay interval
t_{FD}	Fast decay interval
I_{OUT}	Device output current

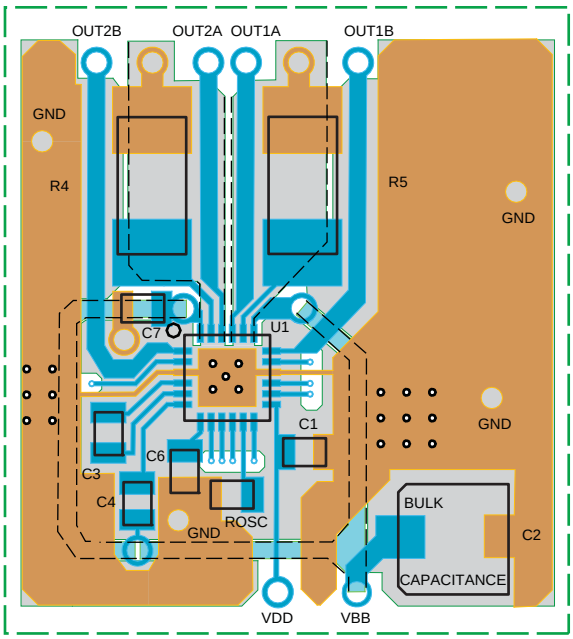
Figure 4. Current Decay Modes Timing Chart

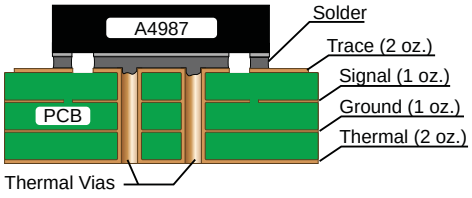
Application Layout

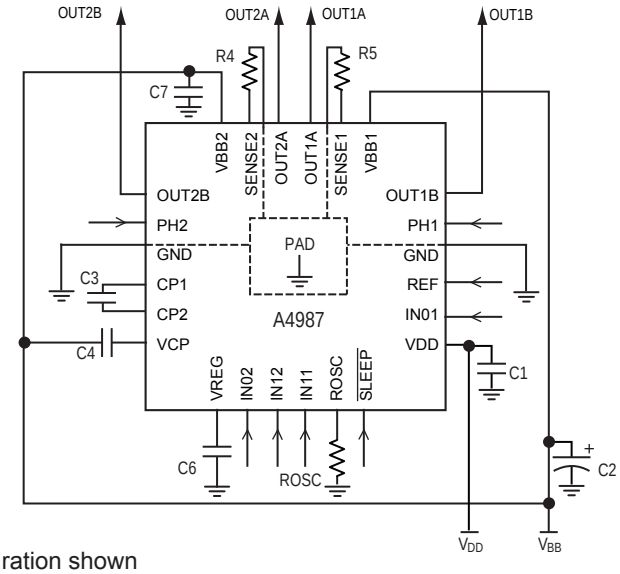
Layout. The printed circuit board should use a heavy ground-plane. For optimum electrical and thermal performance, the A4987 must be soldered directly onto the board. On the underside of the A4987 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance single-point ground, known as a *star ground*, located very close to the device. By making the connection between the pad and the ground plane directly under the A4987, that area becomes an ideal location for a star ground point. A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal.

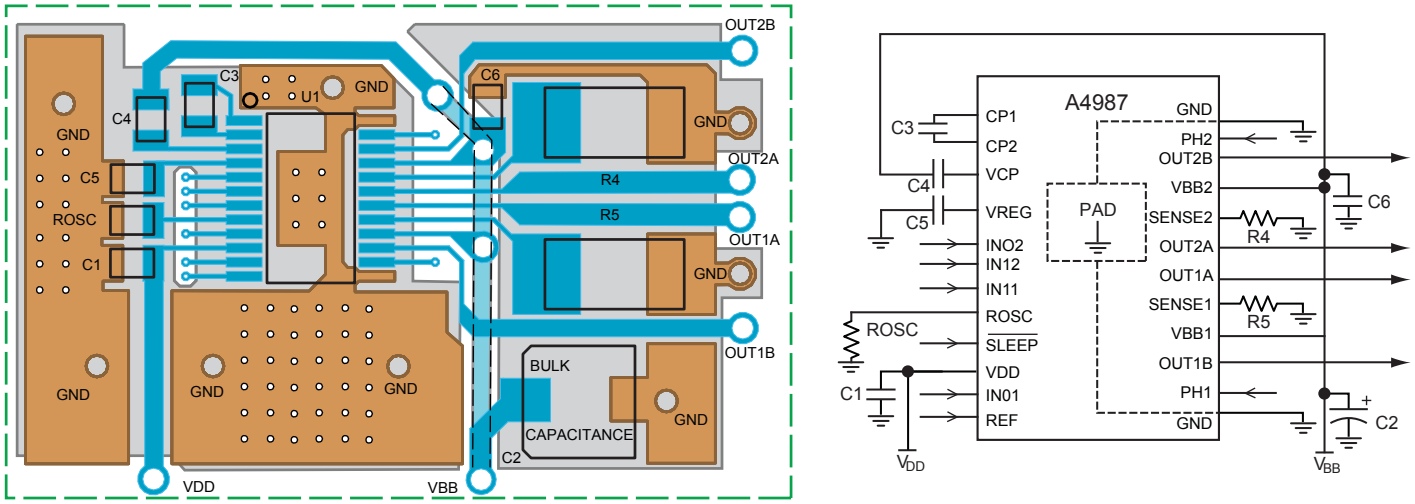
The two input capacitors should be placed in parallel, and as close to the device supply pins as possible. The ceramic capacitor (CIN1) should be closer to the pins than the bulk capacitor (CIN2). This is necessary because the ceramic capacitor will be responsible for delivering the high frequency current components. The sense resistors, R_{Sx}, should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. The SENSEx pins have very short traces to the R_{Sx} resistors and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.





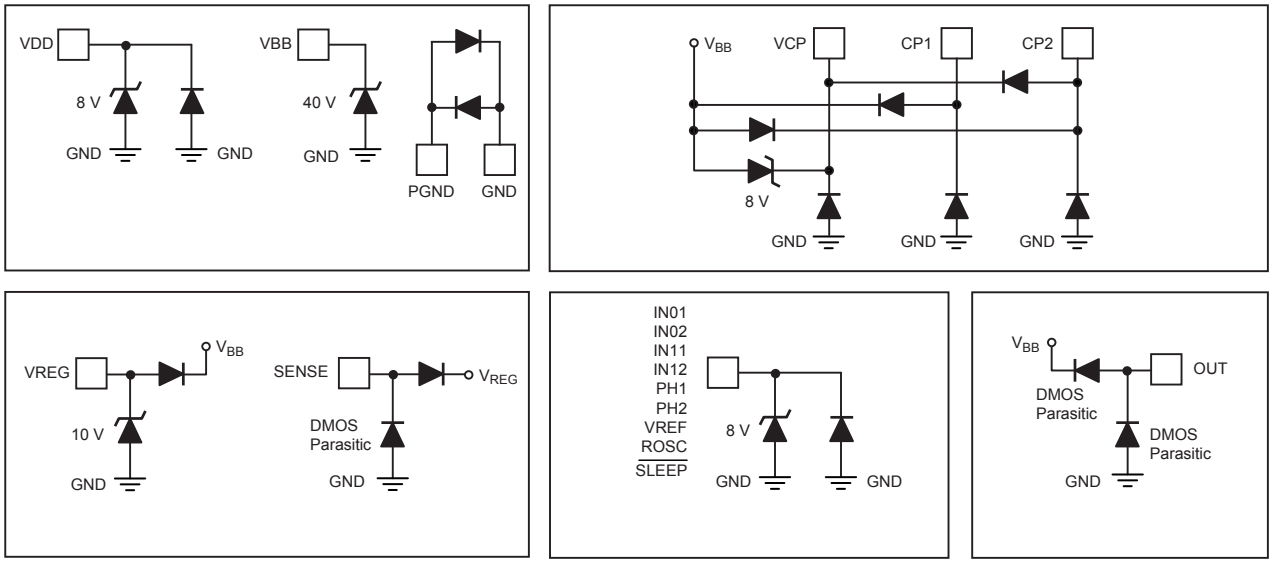


ES package configuration shown

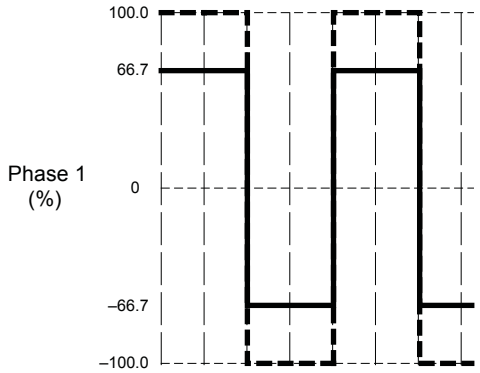


LP package typical application and circuit layout

Pin Circuit Diagrams



Step Sequencing Diagrams



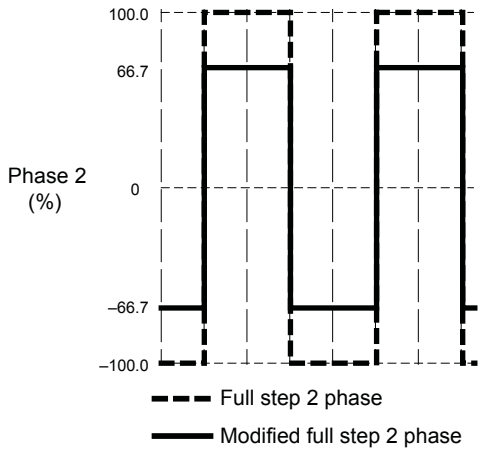
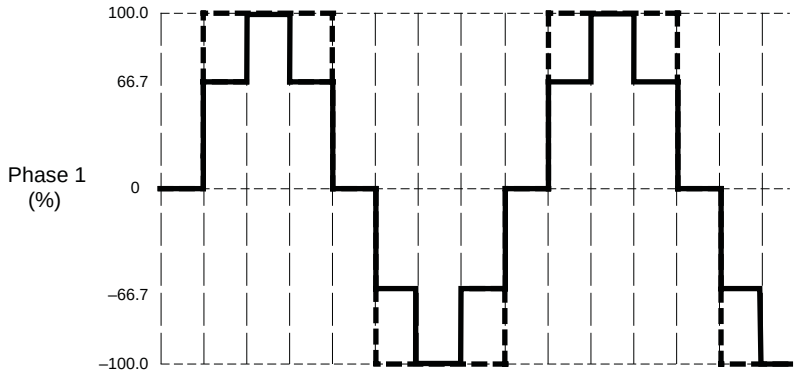


Figure 5. Step Sequencing for Full-Step Increments.



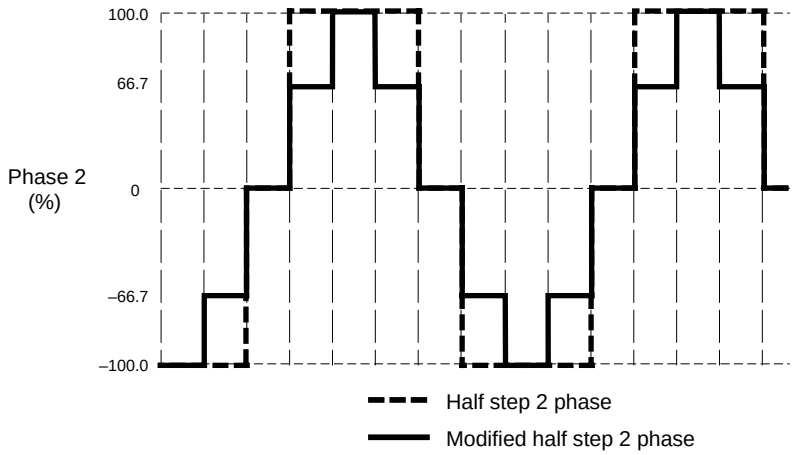


Figure 6. Step Sequencing for Half-Step Increments.

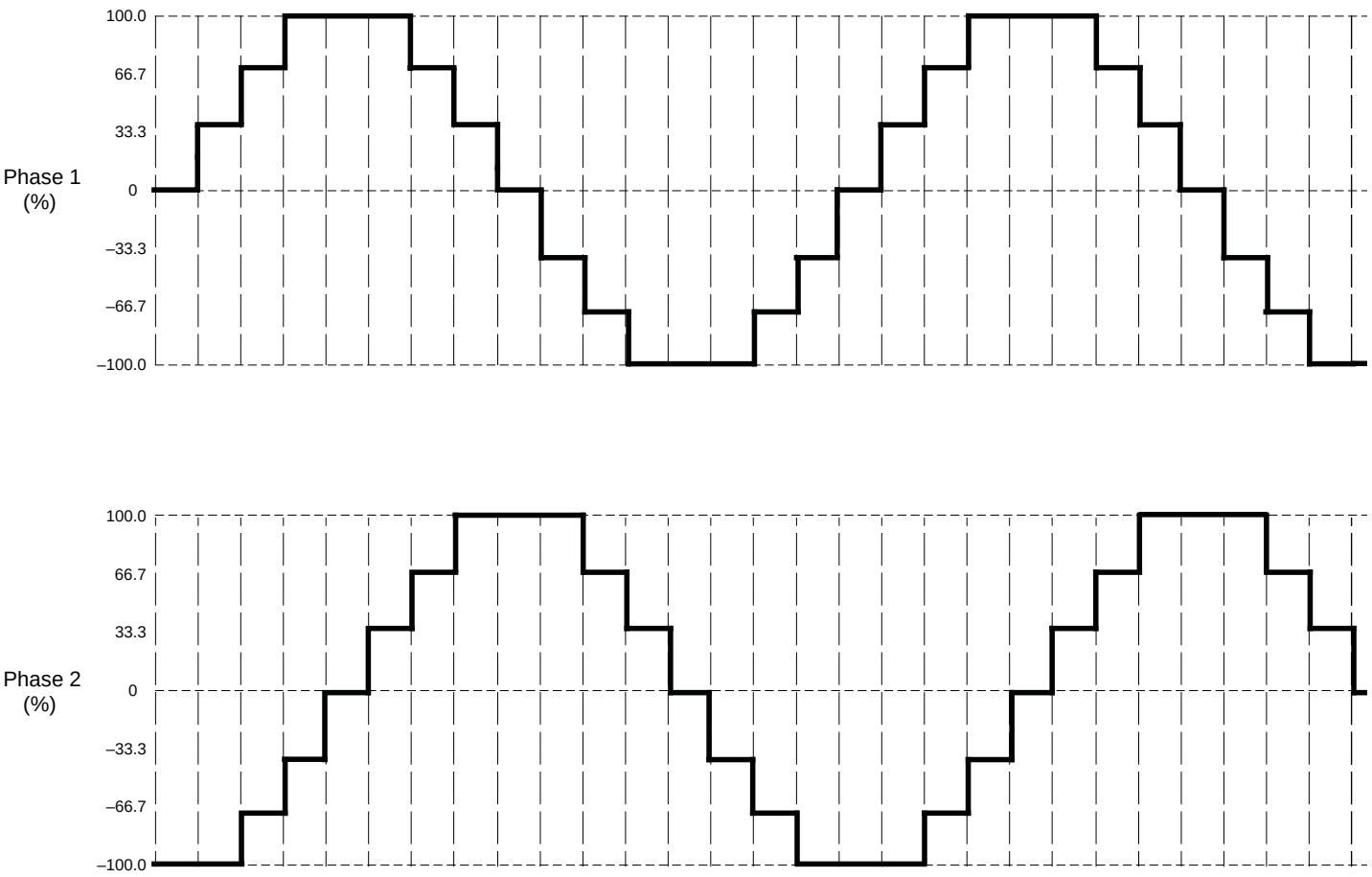


Figure 7. Step Sequence for Quarter-Step Increments

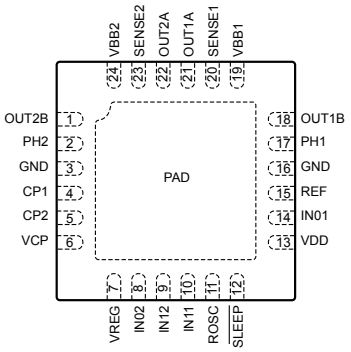
Step Sequencing Settings

Full	1/2	1/4	Phase 1 (%$I_{TripMax}$)	I01	I02	PHASE	Phase 2 (%$I_{TripMax}$)	I11	I12	PHASE
	1	1	0	H	H	x	100	L	L	1
		2	33	L	H	1	100	L	L	1
1	2	3	100/66*	L/H*	L	1	100/66*	L/H*	L	1
		4	100	L	L	1	33	L	H	1
	3	5	100	L	L	1	0	H	H	X
		6	100	L	L	1	33	L	H	0
2	4	7	100/66*	L/H*	L	1	100/66*	L/H*	L	0
		8	33	L	H	1	100	L	L	0
	5	9	0	H	H	x	100	L	L	0
		10	33	L	H	0	100	L	L	0
3	6	11	100/66*	L/H*	L	0	100/66*	L/H*	L	0
		12	100	L	L	0	33	L	H	0
	7	13	100	L	L	0	0	H	H	X
		14	100	L	L	0	33	L	H	1
4	8	15	100/66*	L/H*	L	0	100/66*	L/H*	L	1
		16	33	L	H	0	100	L	L	1

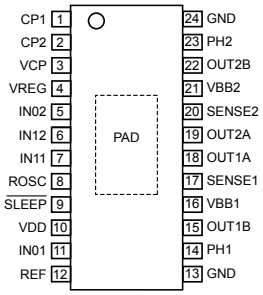
* Denotes modified step mode

Pin-out Diagrams

ES Package



LP Package

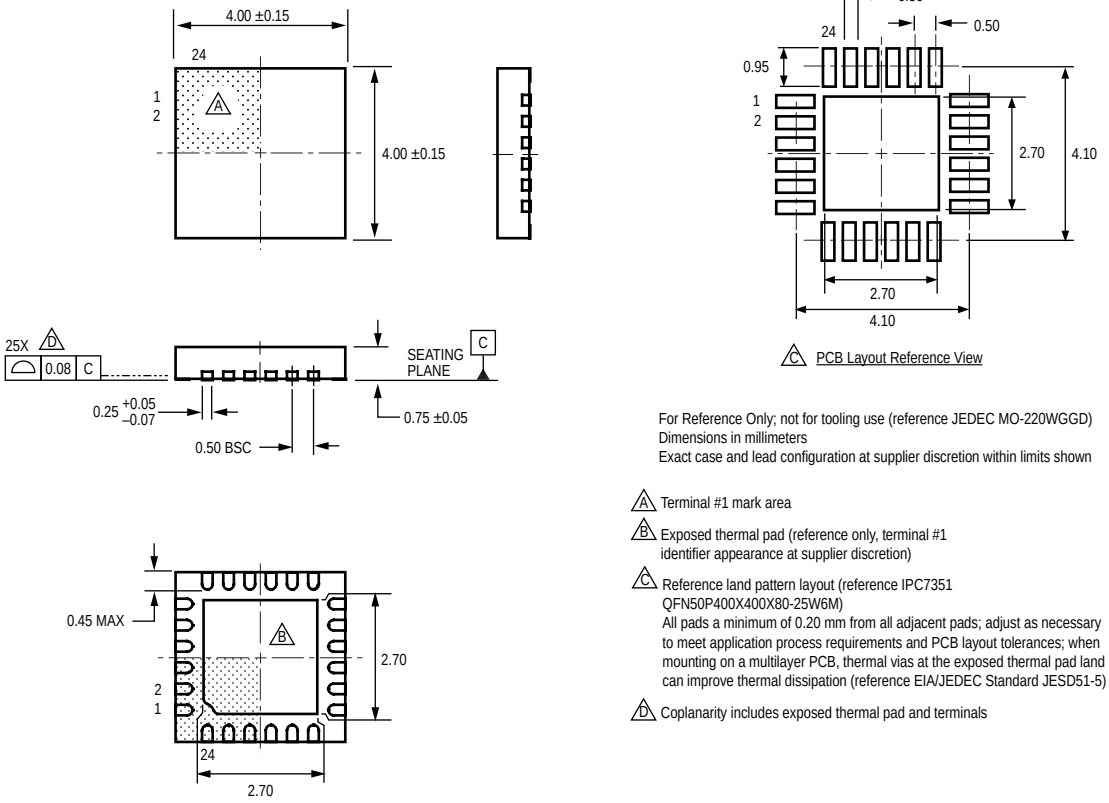


Terminal List Table

Name	Number		Description
	ES	LP	
CP1	4	1	Charge pump capacitor terminal
CP2	5	2	Charge pump capacitor terminal
PH1	17	14	Logic input
PH2	2	23	Logic input
GND	3, 16	13, 24	Ground*
IN02	8	5	Logic input
IN12	9	6	Logic input
NC	–	–	No connection
OUT1A	21	18	DMOS Full Bridge 1 Output A
OUT1B	18	15	DMOS Full Bridge 1 Output B
OUT2A	22	19	DMOS Full Bridge 2 Output A
OUT2B	1	22	DMOS Full Bridge 2 Output B
REF	15	12	G_m reference voltage input
IN11	10	7	Logic input
ROSC	11	8	Timing set
SENSE1	20	17	Sense resistor terminal for Bridge 1
SENSE2	23	20	Sense resistor terminal for Bridge 2
$\overline{\text{SLEEP}}$	12	9	Logic input
IN01	14	11	Logic input
VBB1	19	16	Load supply
VBB2	24	21	Load supply
VCP	6	3	Reservoir capacitor terminal
VDD	13	10	Logic supply
VREG	7	4	Regulator decoupling terminal
PAD	–	–	Exposed pad for enhanced thermal dissipation*

*The GND pins must be tied together externally by connecting to the PAD ground plane under the device.

ES Package, 24-Pin QFN with Exposed Thermal Pad



For Reference Only; not for tooling use (reference JEDEC MO-220WGGD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

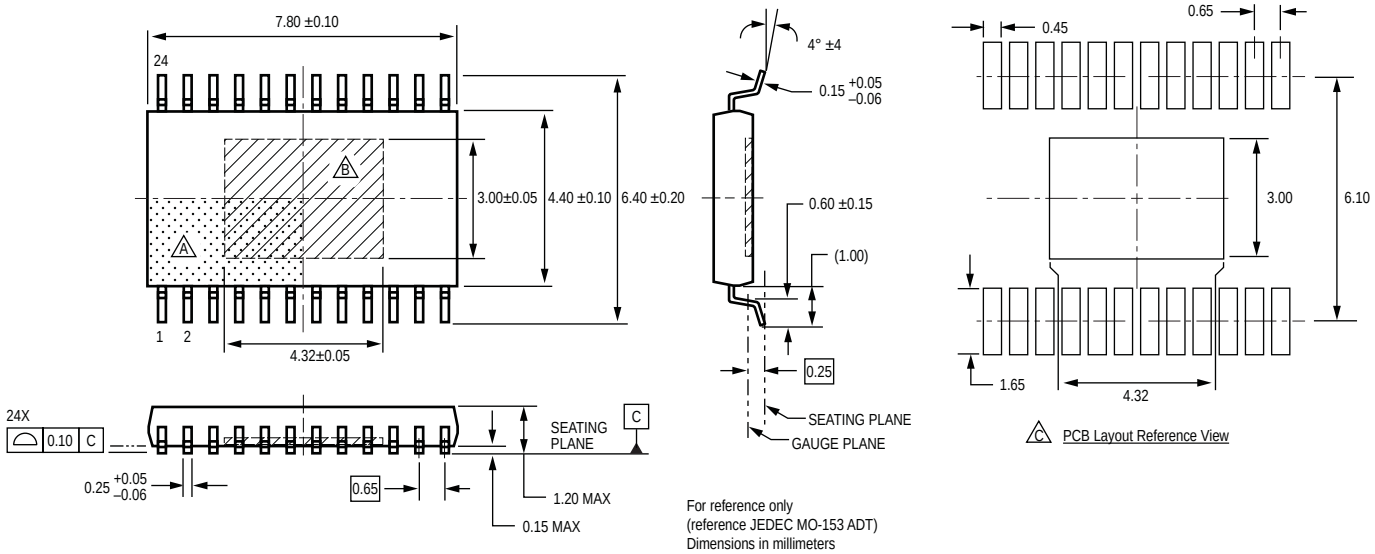
A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

LP Package, 24-Pin TSSOP with Exposed Thermal Pad



For reference only
(reference JEDEC MO-153 ADT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Revision	Revision Date	Description of Revision
Rev. 1	April 11, 2011	Clarification of VREG

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