

OLED DISPLAY MODULE

Application Notes

PRODUCT NUMBER	DD-160128FC-1A/2B with EVK board
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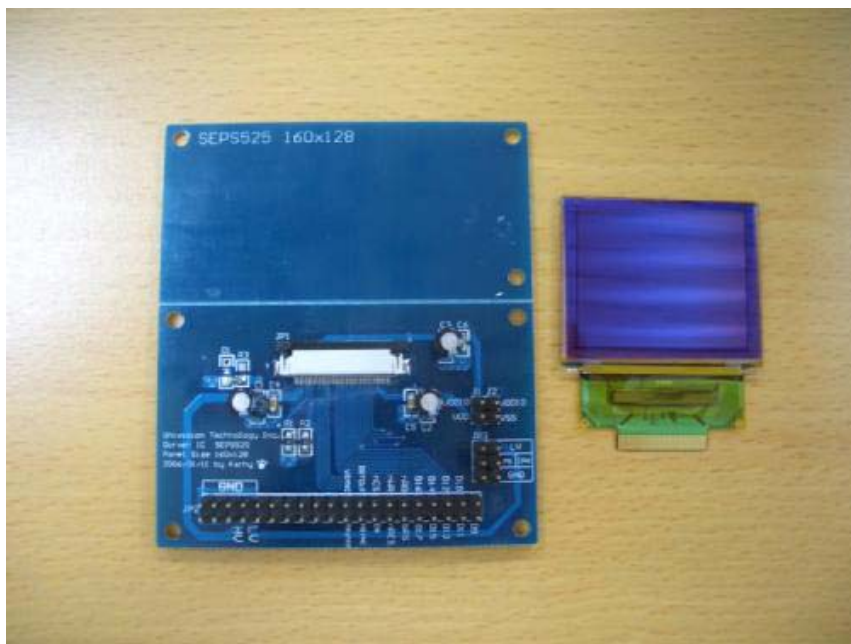


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REVISION RECORD

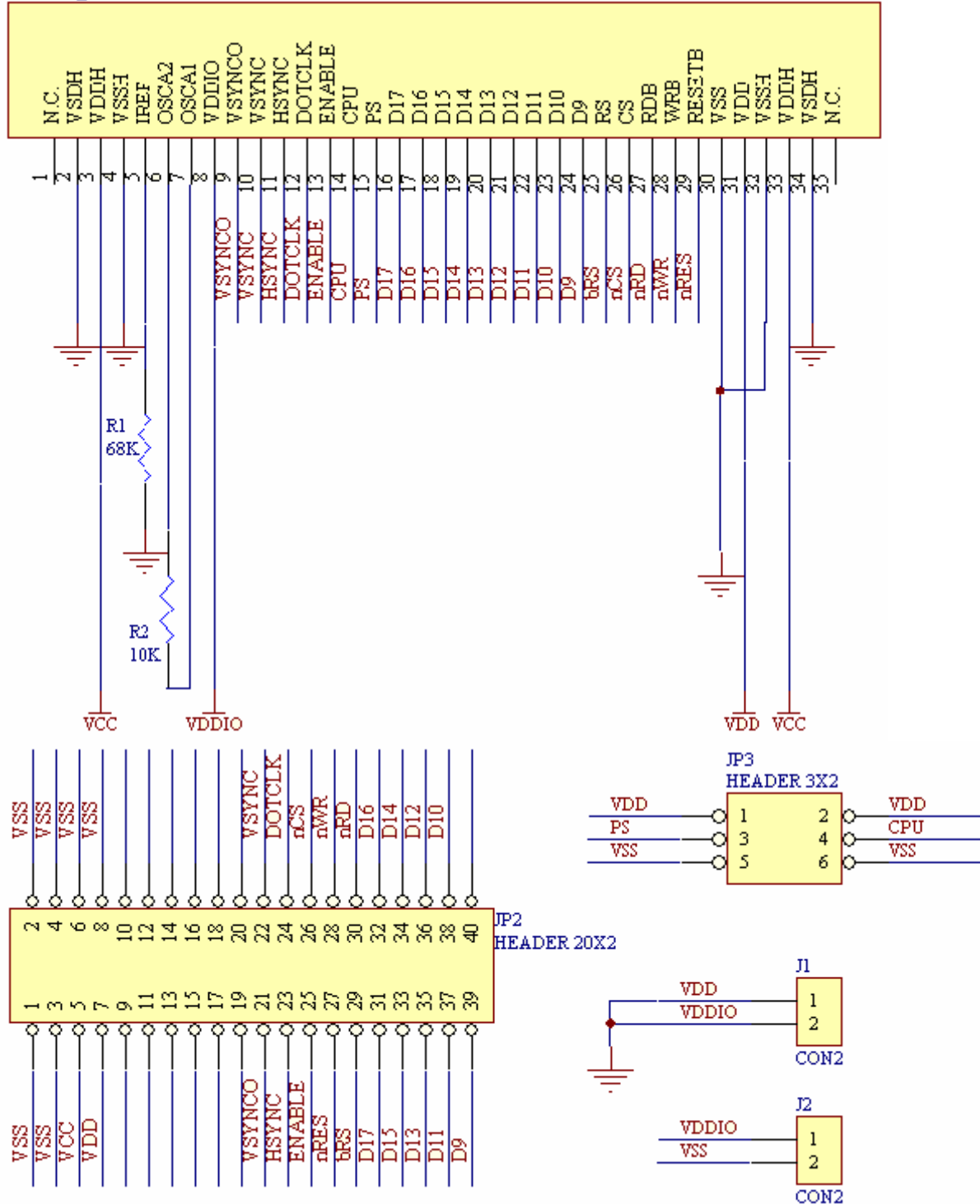
Rev.	Date	Page	Chapt.	Comment	ECR no.
A	30 Sep 06			First Issue	
B	13 Jan 09			Second Issue	
C	01 Mar 11			Changes on the initialisation	

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1 EVK Schematic

JP1
SEPS525_35PIN



Note: The schematic is already removed R3 and D1. VSDH connect to GND.

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Symbol Definition

D17-D9 : These pins are 9-bit bi-directional data bus to be connected to the MCU's data bus.

D17-D10 : These are for command and data inputs (8bit parallel interface).

CSB : These pins are CSB pins for master and slave driver IC. This pin is the chip select input. The chip is enabled for MCU communication only when CSB is pulled low.

CPU : Selects the CPU type.

Low: 80-series CPU
High: 68-Series CPU

PS : Selects parallel/Serial interface type.

Low: serial
High: parallel.

RDB : For an 80-system bus interface, read strobe signal(active low).

For a 68-system bus interface, bus enable strobe (active high).
When using SPI, fix it to VDD or VSS level.

WRB : For an 80-system bus interface, write strobe signal (active low).

For a 68-system bus interface, read/write select.

Low: Write
High: Read.

When using SPI, fix it to VDD or VSS level.

RESB : Reset SEPS525F(active low).

VCC : External Column Driving Power Supply.

VDD : Logic power supply.

VSS : Power supply ground.

HV : External Column Driving Power Supply.

LV : Logic power supply.

GND : Power supply ground.

Note1: Please ground the unused data pins

Note2: If you do not use RGB Interface, please ground VSYNC, HSYNC, Enable, DOTCLK and leave the VSYNCO floating.

Note3: If you do not use VDDIO, please connect it to LV (VDD).

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2 Timing characteristics

80-Series MPU parallel Interface (write timing)

(VDD = 2.8V, Ta = 25°C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	tAH8	-	5	-	ns	CSB
Address setup timing	tAS8		5		ns	RS
System cycle timing	tCYC8	-	100	-	ns	WRB
Write "L" pulse width	tWRLW8		45		ns	
Write "H" pulse width	tWRHW8		45		ns	
Data setup timing	tDS8	-	30	-	ns	DB[17:0]
Data hold timing	tDH8		10		ns	

All the timing reference is 10% and 90% of VDD

Table 1 80-Series MPU Parallel Interface Timing Characteristics (Write)

(Write Timing)

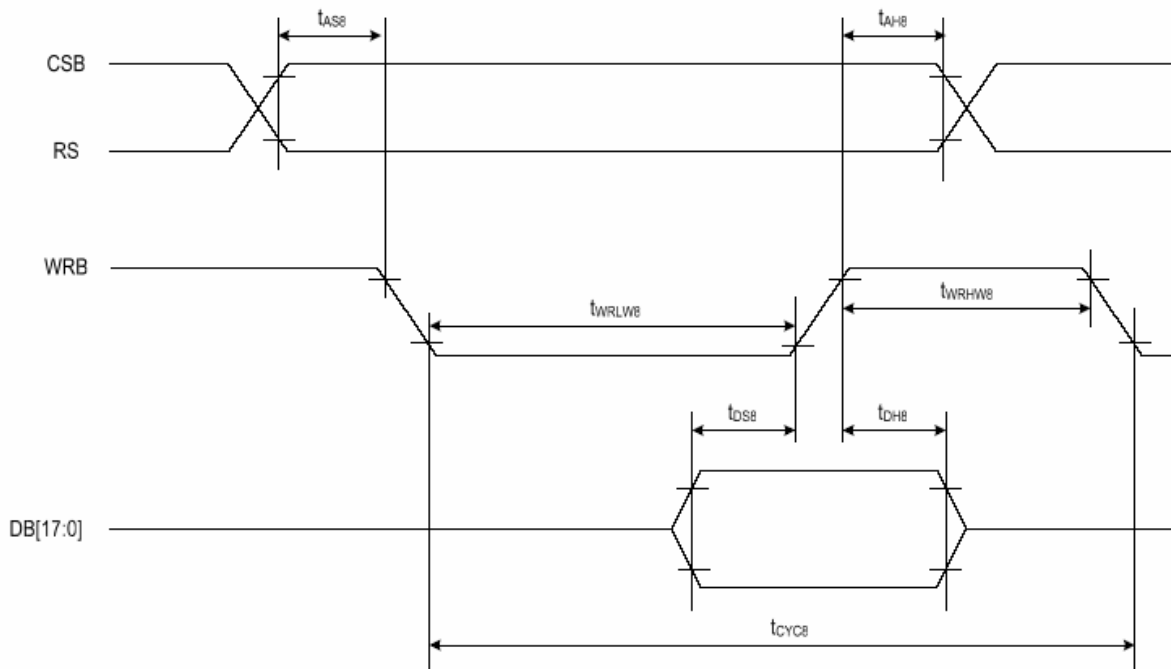


Figure 1 80-Series MPU parallel Interface Timing Diagram (Write)

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80-Series MPU parallel Interface (Read timing)

(VDD = 2.8V, Ta = 25°C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	tAH8	-	5	-	ns	CSB
Address setup timing	tAS8		5		ns	RS
System cycle timing	tCYC8	-	200	-	ns	RDB
Read "L" pulse width	tWRLW8		90		ns	
Read "H" pulse width	tWRHW8		90		ns	
Data setup timing	tDS8	CL = 15 pF	-	60	ns	DB[17:0]
Data hold timing	tDH8		0		ns	

All the timing reference is 10% and 90% of VDD

Table 2 80-Series MPU Parallel Interface Timing Characteristics (Read)

(Read Timing)

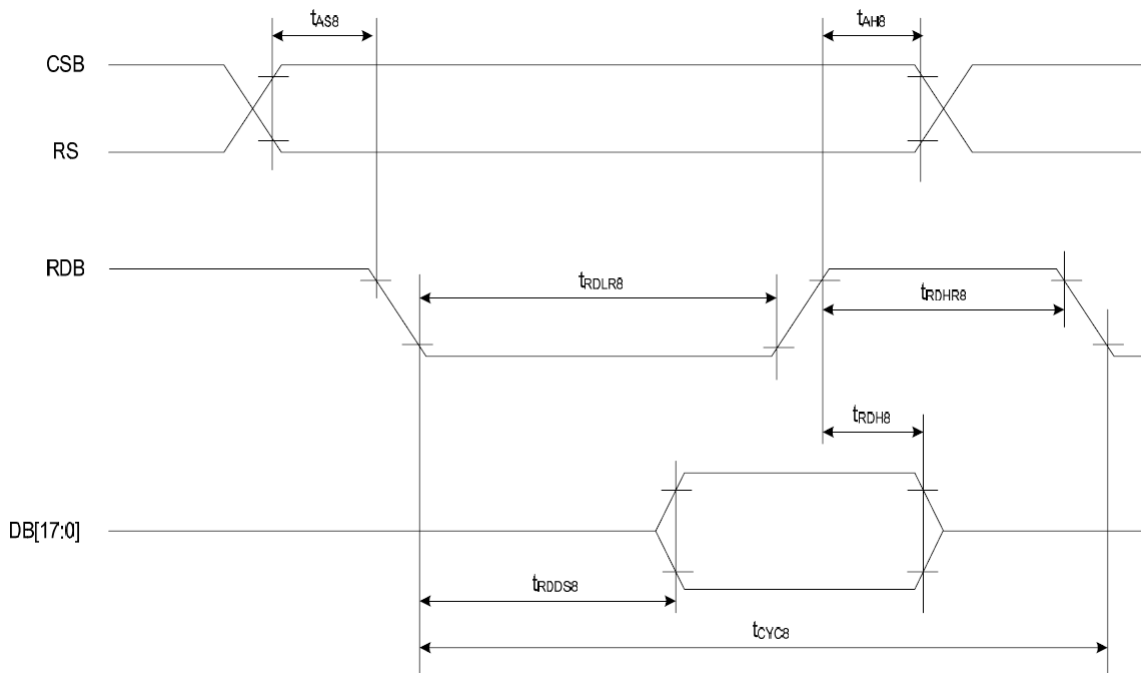


Figure 2 80-Series MPU parallel Interface Timing Diagram (Read)

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6800-Series MPU parallel Interface (write timing)

(VDD = 2.8V, Ta = 25°C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	tAH8	-	5	-	ns	CSB
Address setup timing	tAS8		5		ns	RS
System cycle timing	tCYC8	-	100	-	ns	E
Write "L" pulse width	tWRLW8		45		ns	
Write "H" pulse width	tWRHW8		45		ns	
Data setup timing	tDS8		40	-	ns	DB[17:0]
Data hold timing	tDH8		10		ns	

All the timing reference is 10% and 90% of VDD

Table 3 6800-Series MPU Parallel Interface Timing Characteristics (Write)

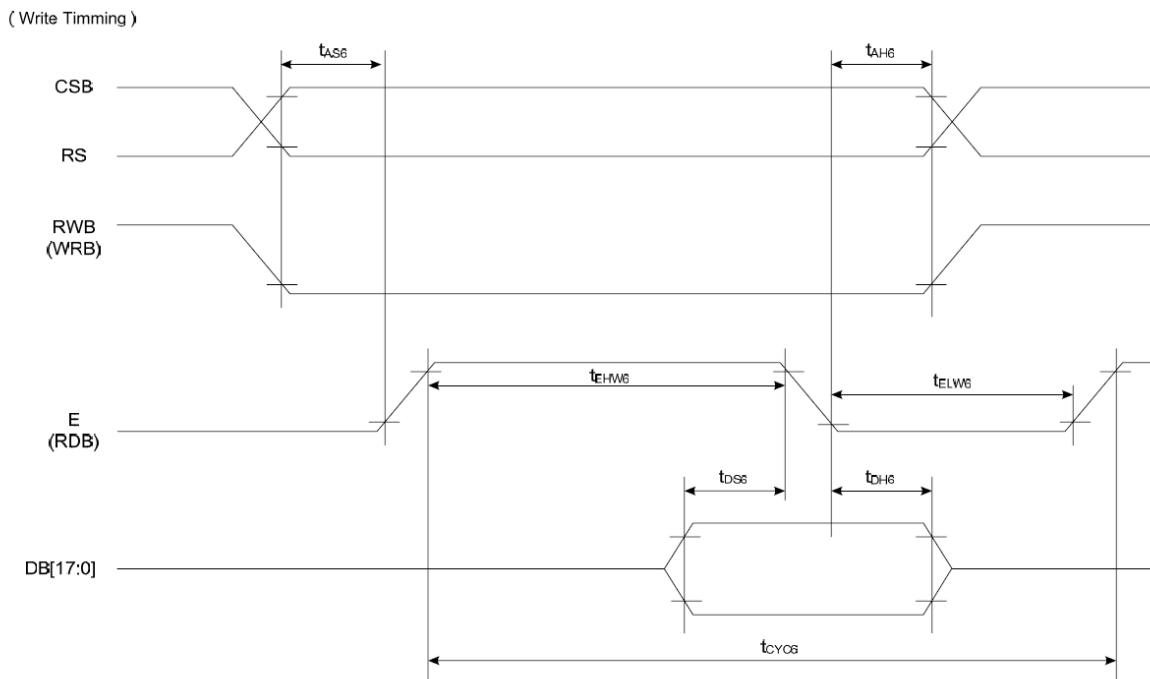


Figure 3 6800-Series MPU parallel Interface Timing Diagram (Write)

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68-Series MPU parallel Interface (Read timing)

(VDD = 2.8V, Ta = 25°C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	tAH8	-	10	-	ns	CSB
Address setup timing	tAS8		10		ns	RS
System cycle timing	tCYC8	-	200	-	ns	E
Read "L" pulse width	tWRLW8		90		ns	
Read "H" pulse width	tWRHW8		90		ns	
Data setup timing	tDS8	CL = 15 pF	0	70	ns	DB[17:0]
Data hold timing	tDH8				ns	

All the timing reference is 10% and 90% of VDD

Table 4 80-Series MPU Parallel Interface Timing Characteristics (Read)

(Read Timing)

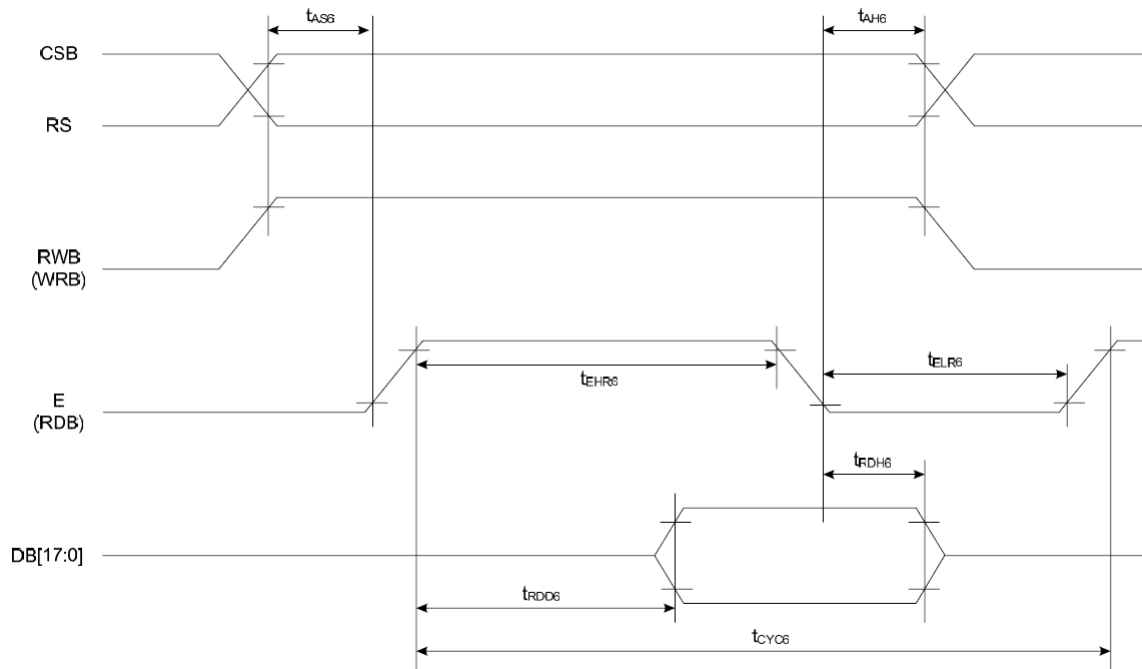


Figure 4 6800-Series MPU parallel Interface Timing Diagram (Read)

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SPI Interface

(VDD = 2.8V, Ta = 25°C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Serial clock cycle	tCYCS		60		ns	SCL
SCL “H” pulse width	tSHW	-	25	-	ns	
SCL “L” pulse width	tSLW		25		ns	
Data setup timing	tDSS		25		ns	SDI
Data hold timing	tDHS	-	25	-	ns	
CSB □ SCL timing	tCSS				ns	CSB
CSB □ hold timing	tCSH	-	25	-	ns	

All the timing reference is 10% and 90% of VDD

Table 5 SPI Interface Timing Characteristics

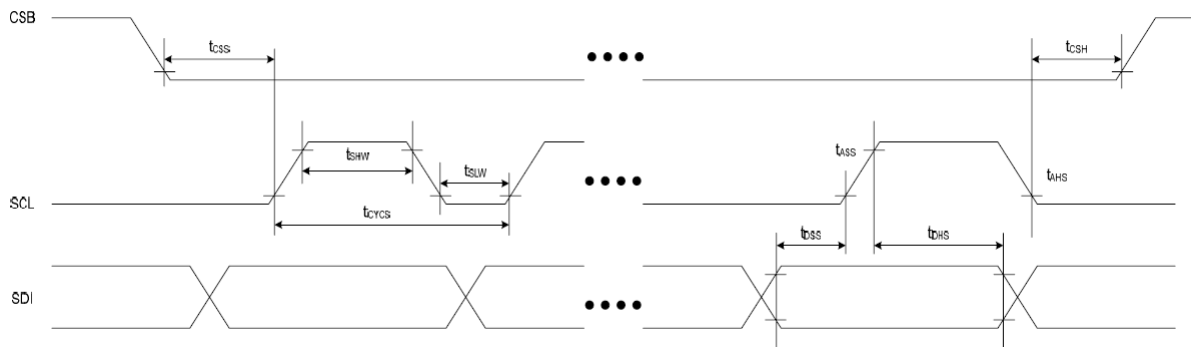


Figure 5 SPI Interface Timing Characteristics

3 Connection Between OLED and EVK

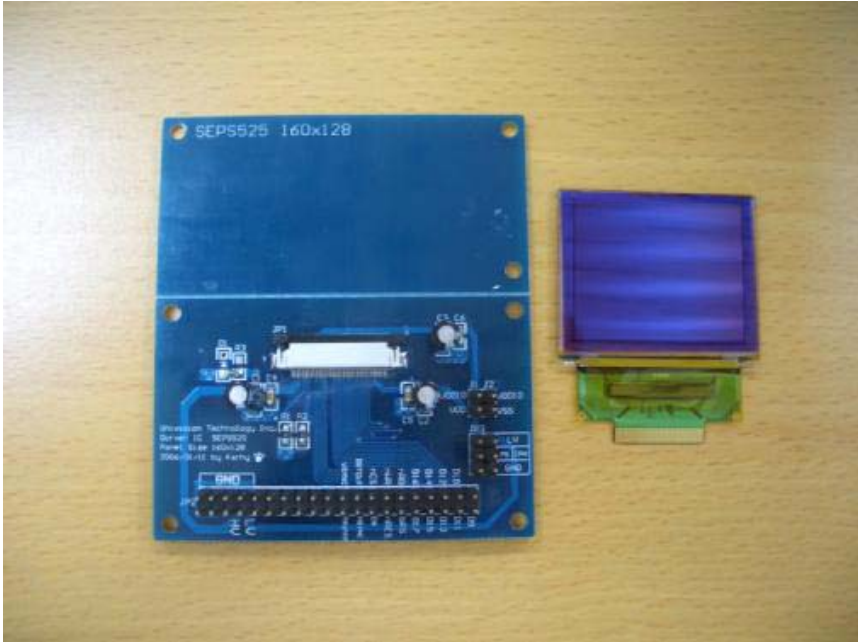


Figure 6 EVK PCB and DD-160128FC-1A/2A Module



Figure 7 DD-160128FC-1A/2A and EVK assembled (Top view)

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The SEPS525F is a COF type package, which means that the connect pads are on the top of the display connector. When the EVK and display are assembled, finally push the locking pad to hold the display in place, see Figure 6 and Figure 7.

User can use wires to connect the EVK with the system. The example is shown below in figure 8;

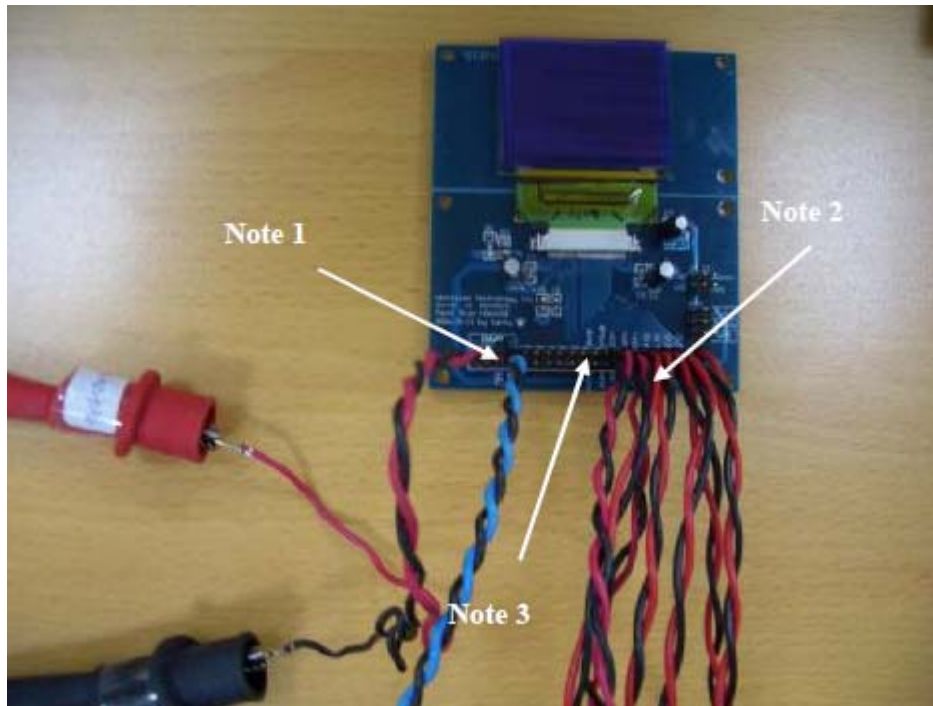


Figure 8 control MCU (not supplied) connected with EVK

Note 1 : It is the external most positive voltage supply. In this sample it is connected to power supply.

Note 2 : The leading wire has 14 pins totally in this case.
(D17-D9, RDB,RS, WRB, RESB, CSB)

Note 3 : If used RGB Interface, please connected to platform.

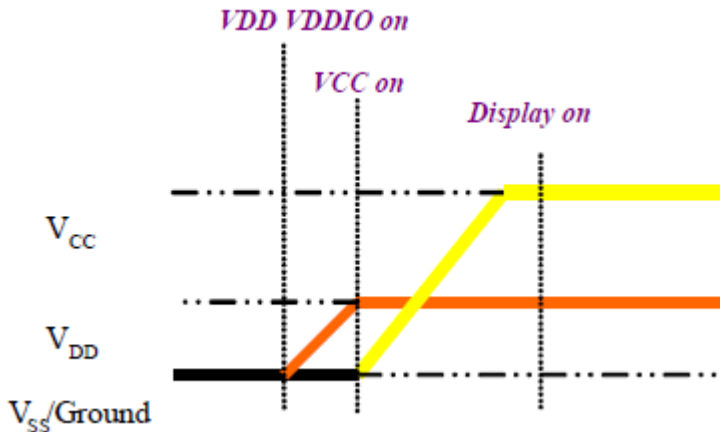
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6. Power down and Power up Sequence

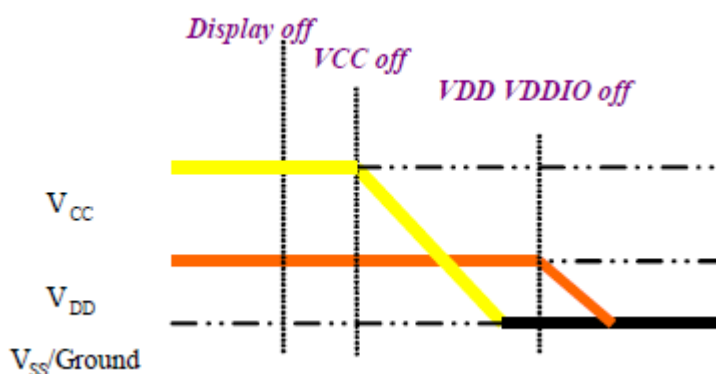
To protect OLED panel and to extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

Power up Sequence:



1. Power up VDD
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up VDDH
6. Delay 100ms
(When V_{DD} is stable)
7. Send Display on command

Power down Sequence:

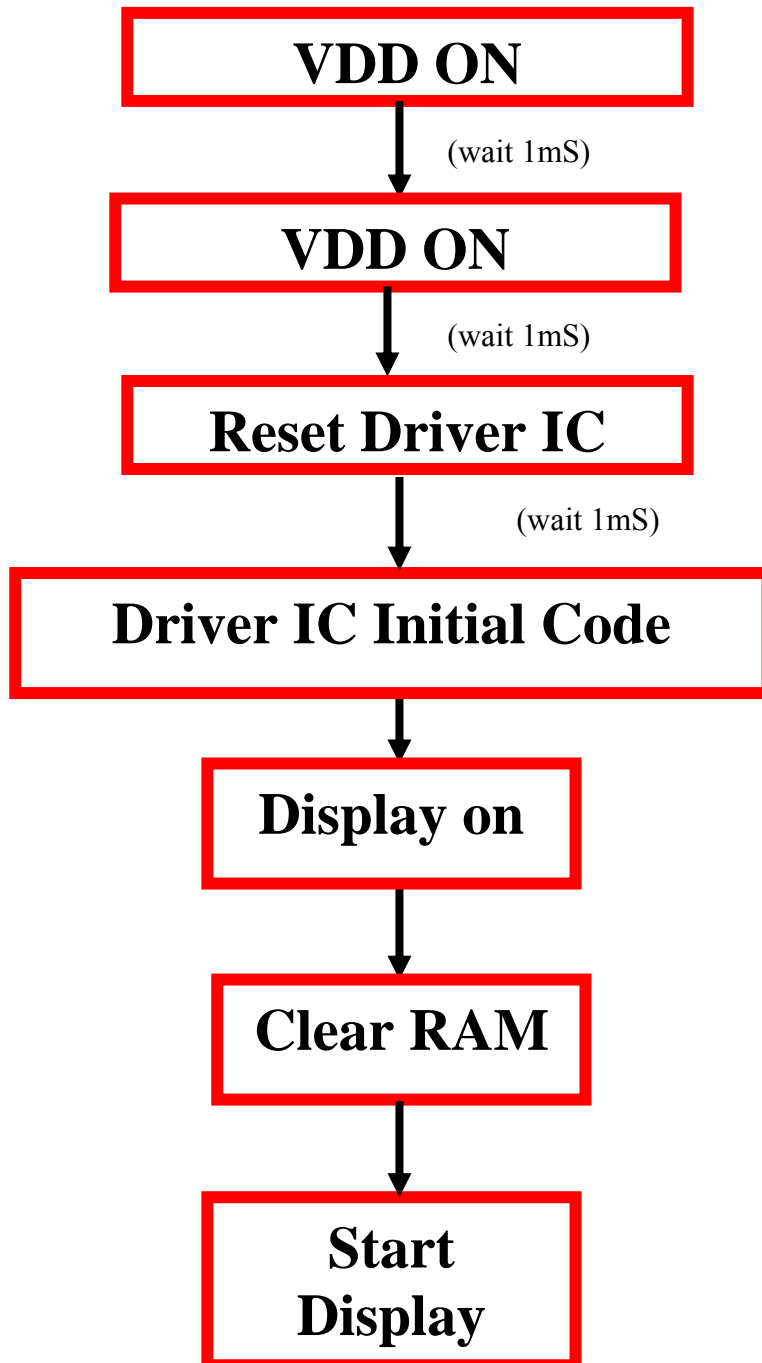


1. Send Display off command
2. Power down VDDH
3. Delay 100ms
(When VDDH is reach 0 and panel is completely discharges)
4. Power down VDD

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4 How to use the DD-160128FC-1A/2A



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4.1 Recommended Initial code for 80 interface

```
//Reg:04h Action:Normal current and PS ON / Internal osc power off
Write_Command(rREDUCE_CURRENT,0x03);
T0_05sec();
//Reg:04h Action:Normal current and PS OFF
Write_Command(rREDUCE_CURRENT,0x00);
T0_05sec();
//Reg:3Bh Action:Screen Saver OFF
Write_Command(rSCREEN_SAVER_CONTEROL,0x00);
//Reg:02h Action:Export1 internal clock/OSC with external resistor/Internal OSC ON
Write_Command(rOSC_CTL,0x01);
//Reg:03h Action:FR=120Hz DIV=1
Write_Command(rCLOCK_DIV,0x90);
//Reg:80h Action:PDAC OFF,DDAC OFF/Reference Volt.control with external resistor
Write_Command(rIREF,0x00);
//Reg:08h Action:set color R precharge time
Write_Command(rPRECHARGE_TIME_R,0x03);
//Reg:09h Action:set color G precharge time
Write_Command(rPRECHARGE_TIME_G,0x05);
//Reg:0Ah Action:set color B precharge tiem
Write_Command(rPRECHARGE_TIME_B,0x05);
//Reg:0Bh Action:set color R precharge current
Write_Command(rPRECHARGE_Current_R,0x0a);
//Reg:0Ch Action:set color G precharge current
Write_Command(rPRECHARGE_Current_G,0x0a);
//Reg:0Dh Action:set color B precharge current
Write_Command(rPRECHARGE_Current_B,0x0a);
//Reg:10h Action:set color R dot driving current
Write_Command(rDRIVING_CURRENT_R,0x56);
//Reg:11h Action:set color G dot driving current
Write_Command(rDRIVING_CURRENT_G,0x4D);
//Reg:12h Action:set color B dot driving current
Write_Command(rDRIVING_CURRENT_B,0x46);
//Reg:13h Action:Col D0 to D159/col normal display
Write_Command(rDISPLAY_MODE_SET,0x00);
//Reg:14h Action:MPU mode
Write_Command(rRGB_IF,0x31);
//Reg:16h Action: 6btis triple transfer,262K support
Write_Command(rMEMORY_WRITE_MODE,0x76);
//Reg:17h Action:Memory addr.X start
Write_Command(rMX1_ADDR,0x00);
//Reg:18h Action:Memory addr.X end
Write_Command(rMX2_ADDR,0x9f);
//Reg:18h Action:Memory addr.Y start
Write_Command(rMY1_ADDR,0x00);
//Reg:1Ah Action:Memory addr.Y end
Write_Command(rMY2_ADDR,0x7f);
```

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```
//Reg:20h Action:Memory X start addr.
Write_Command(rMEMORY_ACCESS_POINTER_X,0x00);
//Reg:21h Action:Memory Y start addr.
Write_Command(rMEMORY_ACCESS_POINTER_Y,0x00);
//Reg:28h Action:Display duty ratio
Write_Command(rDUTY,0x7f);
//Reg:29h Action:Display start line
Write_Command(rDSL,0x00);
//Reg:2Eh Action:Display First screen X start point
Write_Command(rD1_DDRAM_FAC,0x00);
//Reg:2Fh Action:Display First screen Y start point
Write_Command(rD1_DDRAM_FAR,0x00);
//Reg:31h Action:Display Second screen X start point
Write_Command(rD2_DDRAM_SAR,0x00);
//Reg:32h Action:Display Second screen Y start point
Write_Command(rD2_DDRAM_SAR,0x00);
//Reg:33h Action:Display size X start
Write_Command(rSCR1_FX1,0x00);
//Reg:34h Action:Display size X end
Write_Command(rSCR1_FX2,0x9f);
//Reg:35h Action:Display size Y start
Write_Command(rSCR1_FY1,0x00);
//Reg:36h Action:Display size Y end
Write_Command(rSCR1_FY2,0x7f);
//Reg:06h Action:Scan signal is high level at precharge period/Dispaly ON
Write_Command(rDISP_ON_OFF,0x01);
//Clear DDRAM
Clear_DDRAM( );
```

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Sub Function for 80 Interface

```

void Write_Register(unsigned char data)
{
IOCLR = 0x0000000ff;//reset D0~D7
IOCLR=bRS;
IOCLR=nCS;
IOCLR=nWR;
IOSET=data;
IOSET=nWR;
IOSET=nCS;
IOSET=bRS;
}
void Write_Parameter(unsigned char data)
{
IOCLR = 0x0000000ff;//reset D0~D7
IOSET=bRS;
IOCLR=nCS;
IOCLR=nWR;
IOSET=data;
IOSET=nWR;
IOSET=nCS;
}
void Write_Command(unsigned char Reg, unsigned char data)
{
Write_Register(Reg);
Write_Parameter(data);
})
void Write_6BitDDRAM(unsigned char data)
{
IOCLR = 0x0000000ff;//reset D0~D7
IOSET=bRS;
IOCLR=nCS;
IOCLR=nWR;
IOSET=data<<2; //Send R5~R0 ( G5~G0 or B5~B0 ) to D17~D12
IOSET=nWR;
IOSET=nCS;
}
void fill_block(unsigned char R,unsigned char G,unsigned char B)
{
unsigned char i,j;
Write_Register(rDDRAM_DATA_ACCESS_PORT);
for(i=0;i<128;i++)
{
for(j=0;j<160;j++)
{
Write_6BitDDRAM(R);

```

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```

Write_6BitDDRAM(G);
Write_6BitDDRAM(B);
}
}
}
void ColorR(void)
{
fill_block(0x3f,0x00,0x00);
}
void ColorG(void)
{
fill_block(0x00,0x3f,0x00);
}
void ColorB(void)
{
fill_block(0x00,0x00,0x3f);
}
void ColorW(void)
{
fill_block(0x3f,0x3f,0x3f);
}
void Clear_DDRAM(void)
{
fill_block(0x00,0x00,0x00);
}

```

RD recommends Initial Code and Sub Function

Note 1: For 80 series CPU interface.

Note 2: For 6bits DDRAM transfer.

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