CY62148EV30 MoBL®

4-Mbit (512 K × 8) Static RAM

Features

- Very high speed: 45 ns
  - Wide voltage range: 2.20 V to 3.60 V
- Temperature range:
  - Industrial: –40 °C to +85 °C
  - Automotive-A: –40 °C to +85 °C
- Pin compatible with CY62148DV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA (Industrial)
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 36-ball very fine ball grid array (VFBGA), 32-pin thin small outline package (TSOP) II, and 32-pin small outline integrated circuit (SOIC) [1] packages

Functional Description

The CY62148EV30 is a high performance CMOS static RAM organized as 512 K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

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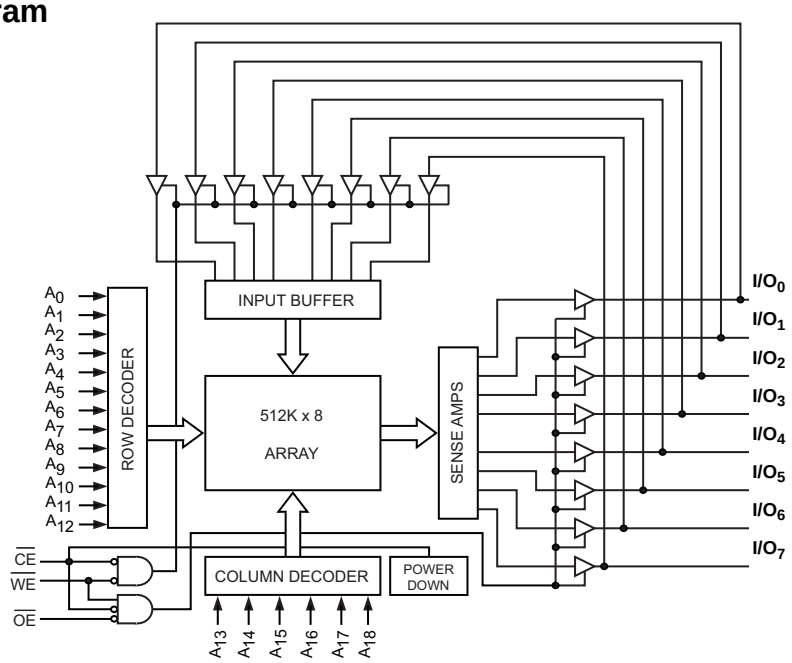
Logic Block Diagram

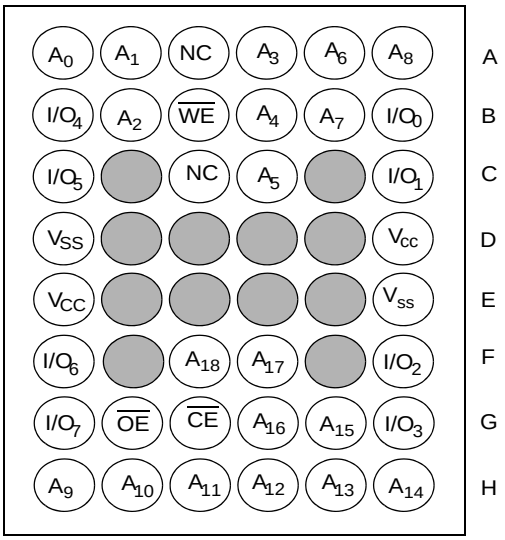


Note
1. SOIC package is available only in 55 ns speed bin.

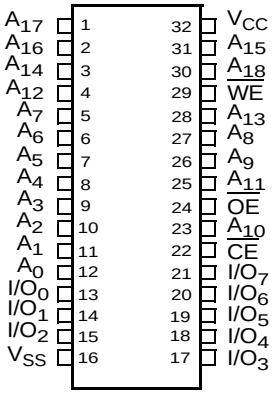
Contents

Pin Configuration [2, 3]

36-Ball VFBGA Pinout
Top View



32-Pin SOIC/TSOP II Pinout
Top View



Product Portfolio

Product		Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
							Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
							f = 1 MHz		f = f_{max}			
			Min	Typ[4]	Max		Typ[4]	Max	Typ[4]	Max	Typ[4]	Max
CY62148EV30LL	VFBGA	Industrial	2.2	3.0	3.6	45	2	2.5	15	20	1	7
	TSOP II	Industrial/Auto-A										
	SOIC	Industrial	2.2	3.0	3.6	55	2	2.5	15	20	1	7

Notes
2. SOIC package is available only in 55 ns speed bin.
3. NC pins are not connected on the die.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... 55 °C to +125 °C

Supply voltage to ground potential .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in High-Z State [5, 6] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage [5, 6].....–0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (MIL-STD-883, Method 3015)

Latch up current.....> 200 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC}[7]
CY62148EV30	Industrial/ Auto-A	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

(Over the Operating Range)

Parameter	Description	Test Conditions		–45 (Industrial/Auto-A)			–55[8]			Unit
				Min	Typ[9]	Max	Min	Typ[9]	Max	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA		2.0	–	–	2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 0.1 mA		–	–	0.4	–	–	0.2	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V		–	–	0.4	–	–	0.4	V
V_{IH}	Input high voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3 V	1.8	–	V_{CC} + 0.3 V	V
		V_{CC}= 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3 V	2.2	–	V_{CC} + 0.3 V	V
V_{IL}	Input low voltage	V_{CC} = 2.2 V to 2.7 V	For VFBGA and TSOP II package	–0.3	–	0.6	–	–	–	V
			For SOIC package	–	–	–	–0.3	–	0.4[10]	V
		V_{CC} = 2.7 V to 3.6 V	For VFBGA and TSOP II package	–0.3	–	0.8	–	–	–	V
			For SOIC package	–	–	–	–0.3	–	0.6[10]	
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_C		–1	–	+1	–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output disabled		–1	–	+1	–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = 1/t_{RC}	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA, CMOS levels	–	15	20	–	15	20	mA
		f = 1 MHz		–	2	2.5	–	2	2.5	
I_{SB1}[11]	Automatic CE power down current — CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V f = f_{max} (Address and Data Only), f = 0 (OE and WE), V_{CC} = 3.60 V		–	1	7	–	1	7	µA
I_{SB2}[11]	Automatic CE power down current — CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	1	7	–	1	7	µA

Notes

5. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
7. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
8. SOIC package is available only in 55 ns speed bin.
9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
10. Under DC conditions the device meets a V_{IL} of 0.8V (for V_{CC} range of 2.7 V to 3.6 V) and 0.6 V (for V_{CC} range of 2.2 V to 2.7 V). However, in dynamic conditions Input LOW voltage applied to the device must not be higher than 0.6V and 0.4V for the above ranges. This is applicable to SOIC package only. Refer to AN13470 for details.
11. Chip Enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

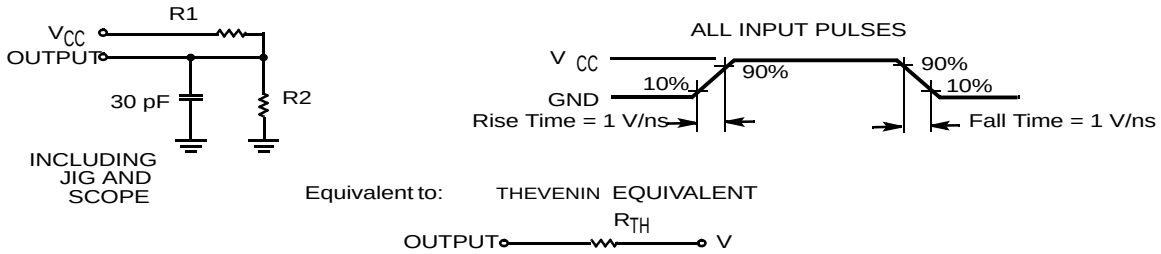
Capacitance

Parameter[12]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter[12]	Description	Test Conditions	VFBGA Package	TSOP II Package	SOIC Package	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	72	75.13	55	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		8.86	8.95	22	°C/W

Figure 1. AC Test Loads and Waveforms

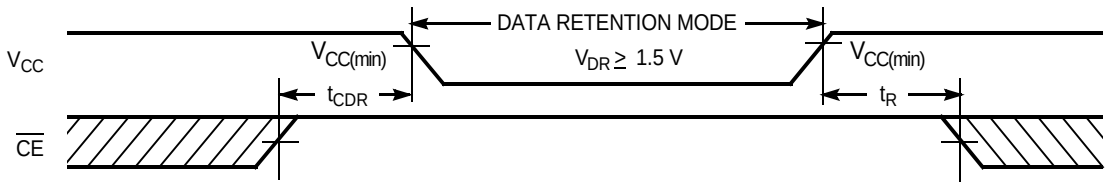


Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min	Typ[13]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR}[14]	Data retention current	V_{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Ind'l/Auto-A	–	0.8	7	µA
t_{CDR}[15]	Chip deselect to data retention time			0	–	–	ns
t_R[16]	Operation recovery time		CY62148EV30LL-45	45	–	–	ns
			CY62148EV30LL-55	55	–	–	–

Figure 2. Data Retention Waveform



Notes
12. Tested initially and after any design or process changes that may affect these parameters.
13. .Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
14. Chip Enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
15. .Tested initially and after any design or process changes that may affect these parameters.
16. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

(Over the Operating Range)

Parameter[17]	Description	-45 (Industrial/Auto-A)		-55[18]		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[19]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[19, 20]	–	18	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[19]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[19, 20]	–	18	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power up	–	45	–	55	ns
Write Cycle[21]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[19, 20]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[19]	10	–	10	–	ns

Notes

17. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the AC Test Loads and Waveforms on page 5.
18. SOIC package is available only in 55 ns speed bin.
19. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
20. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
21. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [22, 23]

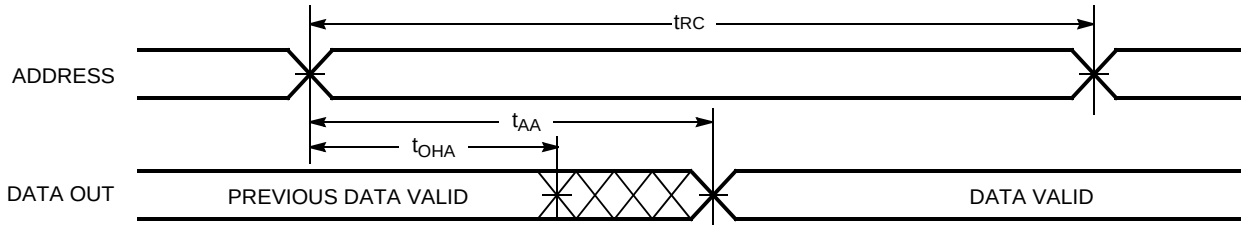


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [23, 24]

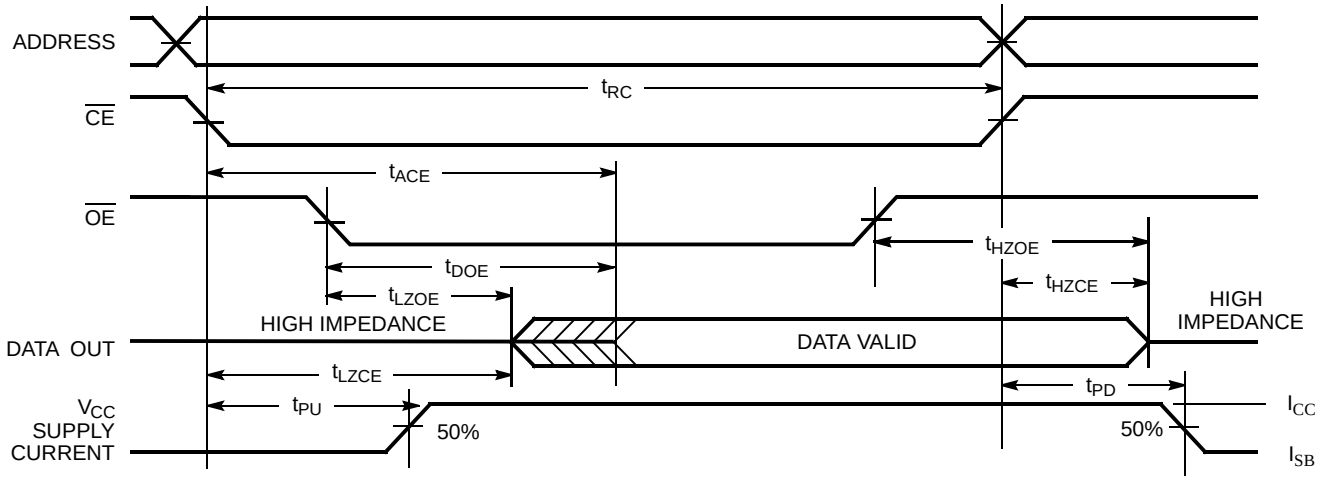
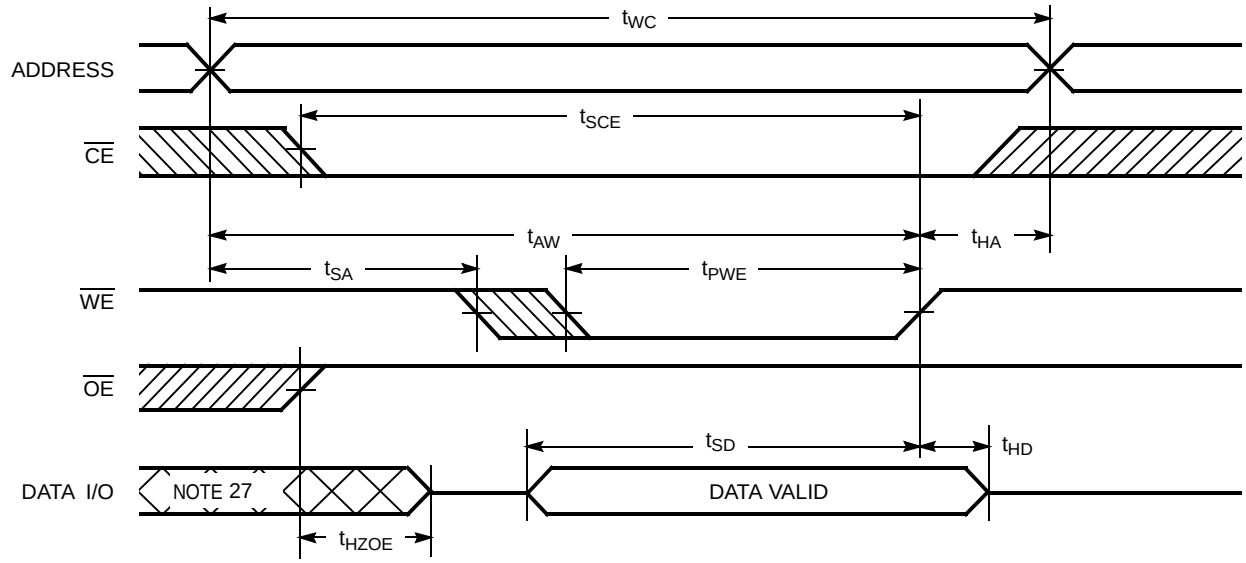


Figure 5. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [25, 26]



Notes
22. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
23. $\overline{WE}$ is HIGH for read cycles.
24. Address valid before or similar to $\overline{CE}$ transition LOW.
25. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
26. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
27. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ($\overline{CE}$ Controlled) [28, 29]

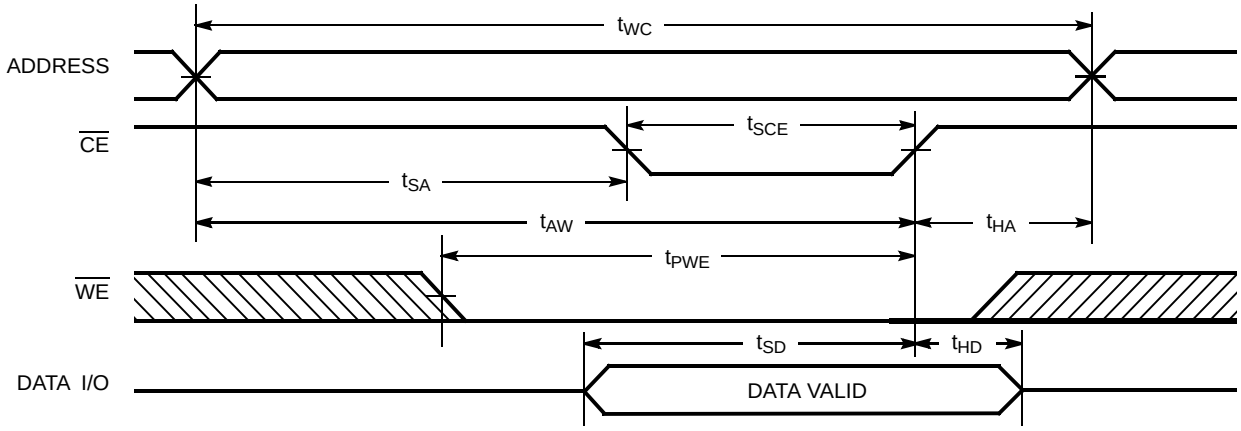
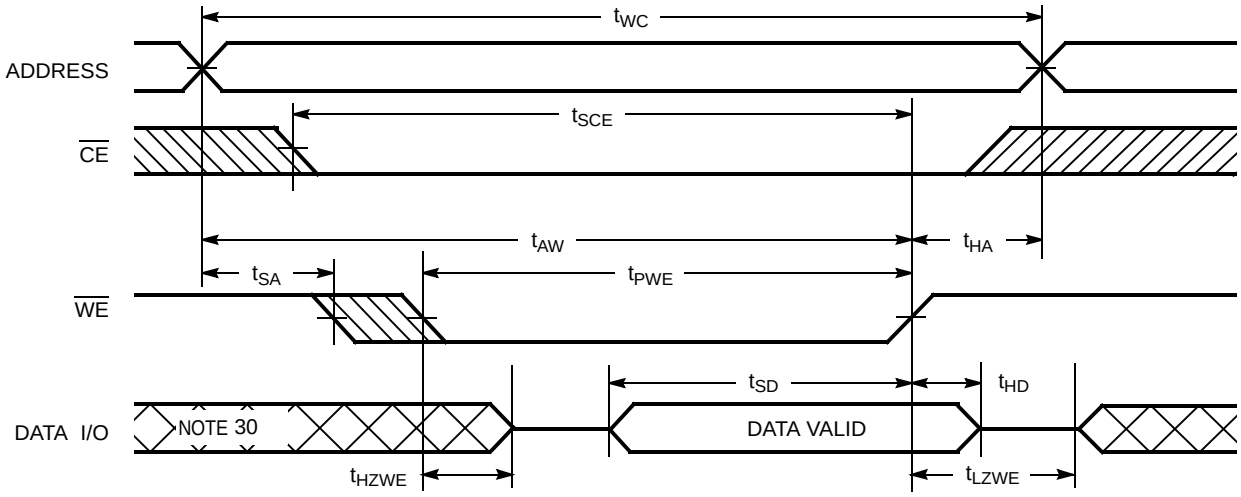


Figure 7. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[29]



Truth Table

$\overline{CE}$[31]	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	H	H	High Z	Output disabled	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})

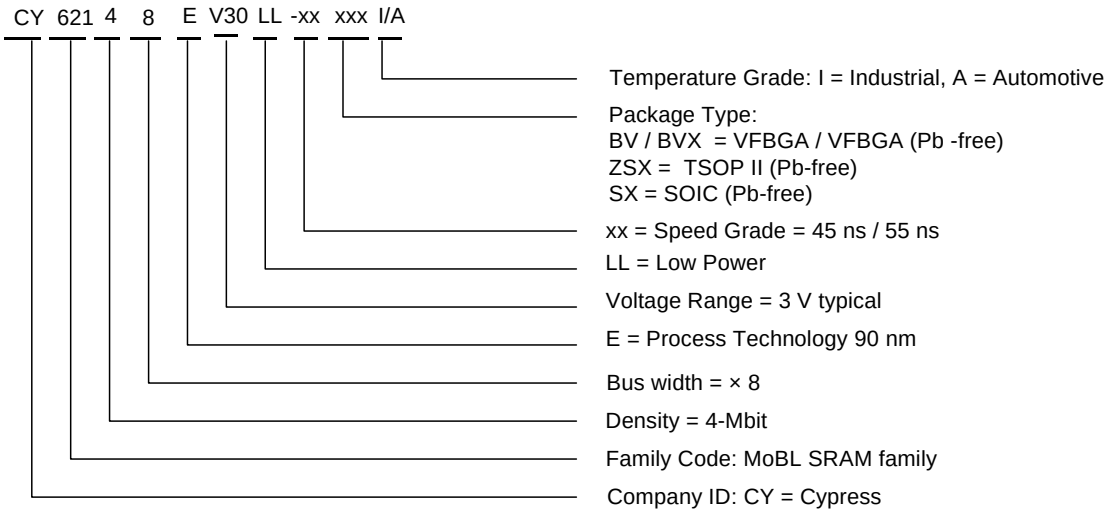
Notes
28. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
29. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
30. During this period, the I/Os are in output state. Do not apply input signals.
31. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62148EV30LL-45BVI	51-85149	36-ball VFBGA	Industrial
	CY62148EV30LL-45BVXI	51-85149	36-ball VFBGA (Pb-free)	
	CY62148EV30LL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	
	CY62148EV30LL-45ZSXA	51-85095	32-pin TSOP II (Pb-free)	Automotive-A
55	CY62148EV30LL-55SXI	51-85081	32-pin SOIC (Pb-free)	Industrial

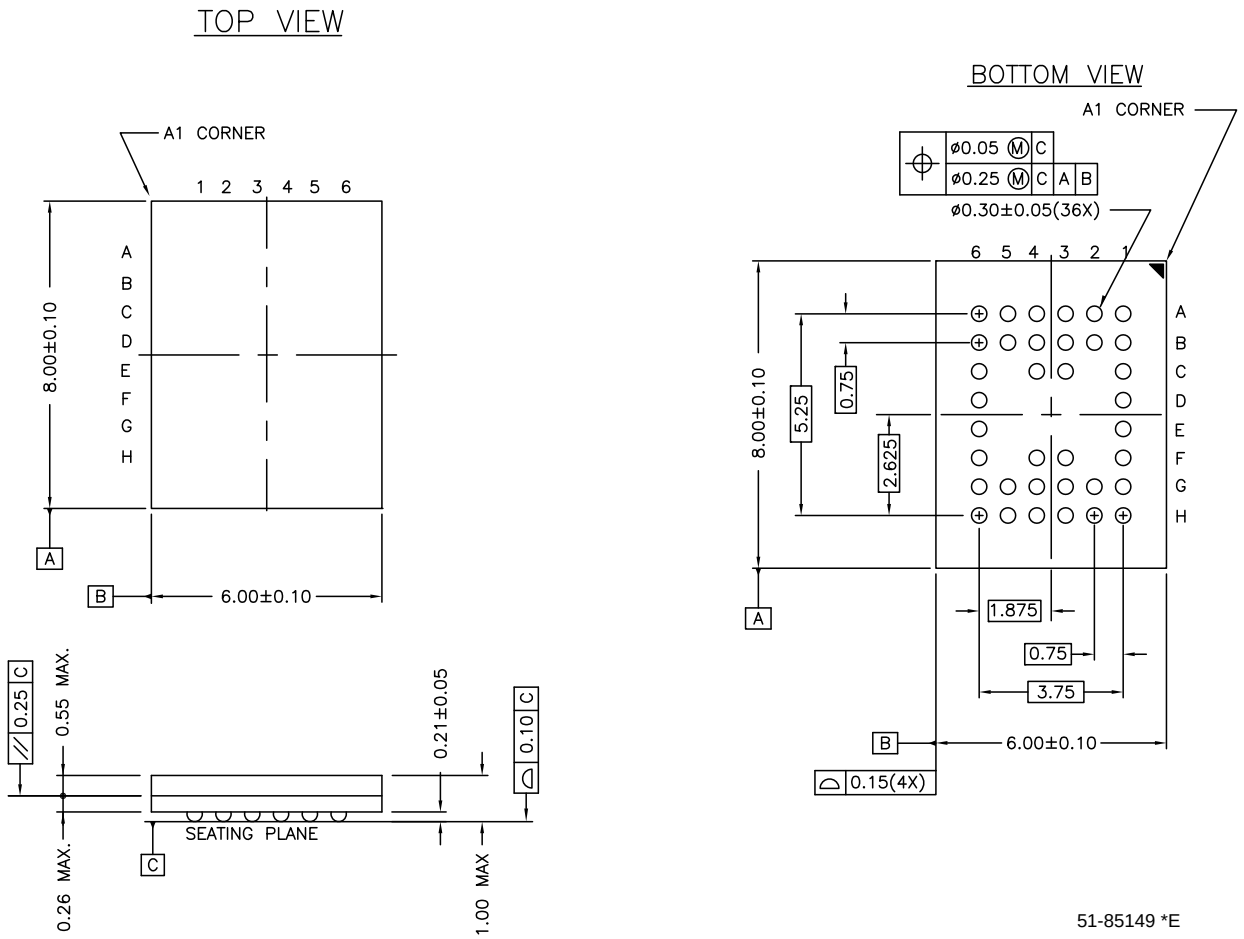
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



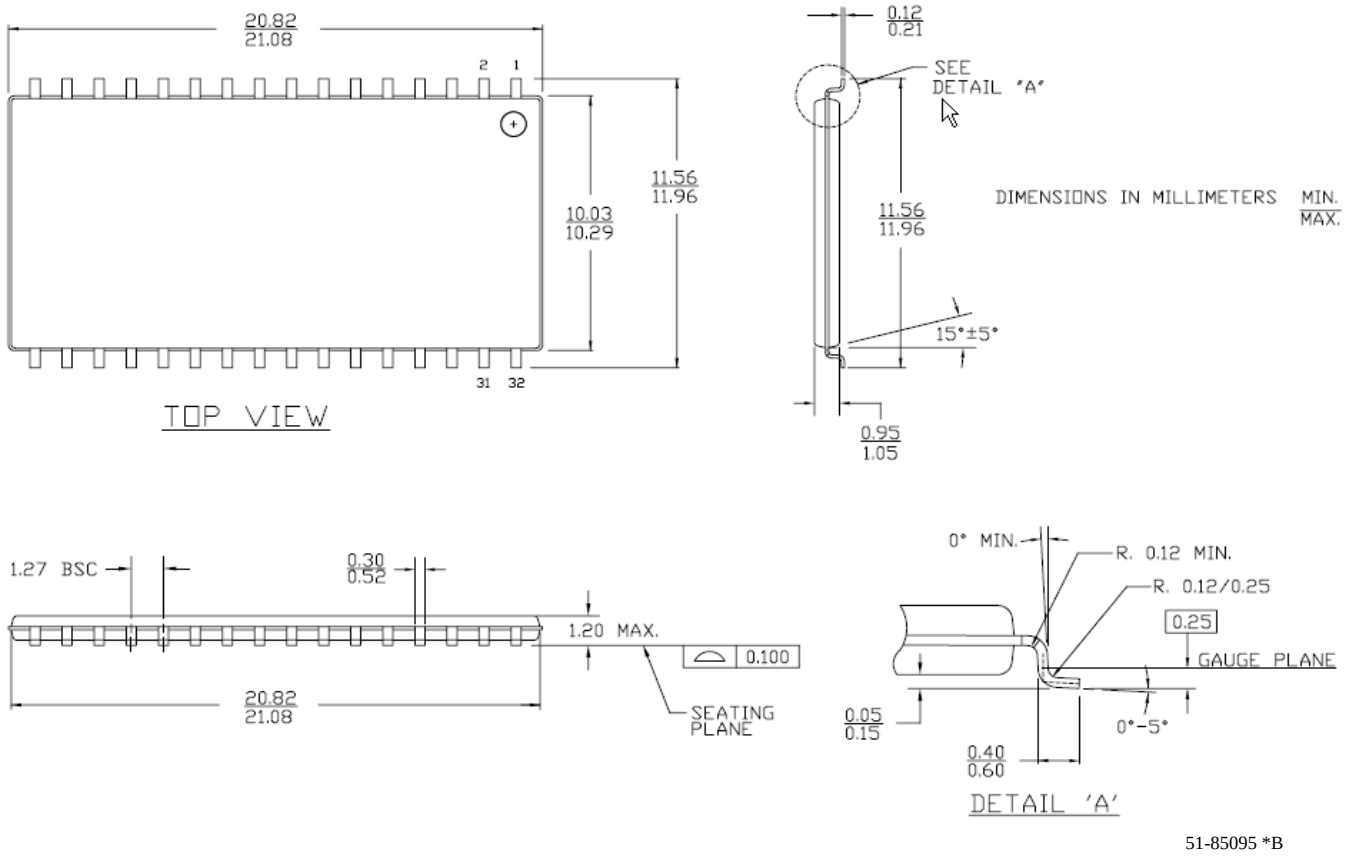
Package Diagrams

Figure 8. 36-ball VFBGA (6 x 8 x 1 mm), 51-85149



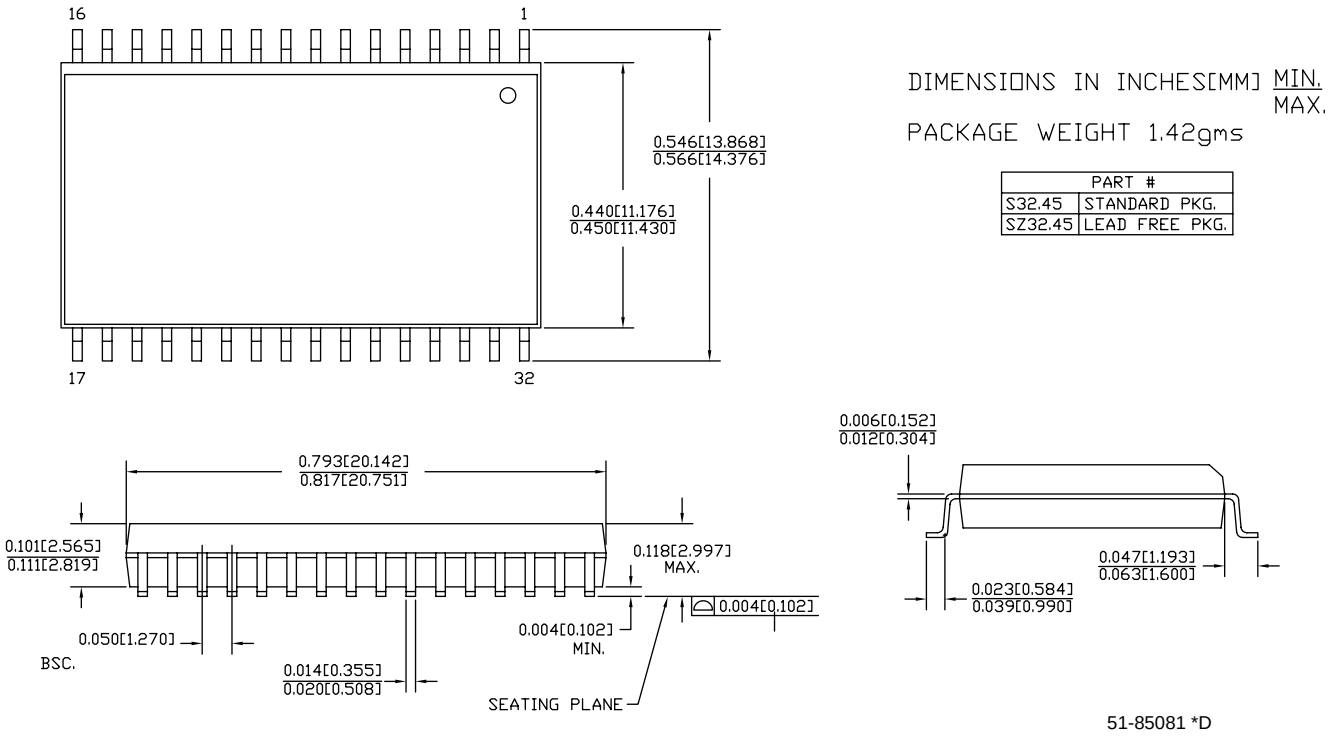
Package Diagrams (continued)

Figure 9. 32-pin TSOP II, 51-85095



Package Diagrams (continued)

Figure 10. 32-pin (450 Mil) Molded SOIC, 51-85081



Acronyms

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
CMOS	complementary metal oxide semiconductor
$\overline{CE}$	chip enable
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine ball grid array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	volts
µA	micro amperes
mA	milli amperes
pF	pico Farad
°C	degree Celsius
W	watts

Document History Page

Document Title: CY62148EV30 MoBL® 4-Mbit (512 K × 8) Static RAM Document Number: 38-05576				
Rev.	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	223225	See ECN	AJU	New data sheet
*A	247373	See ECN	SYT	Changed from Advance Information to Preliminary Moved Product Portfolio to Page 2 Changed V_{CC} stabilization time in footnote #7 from 100 μs to 200 μs Changed I_{CCDR} from 2.0 μA to 2.5 μA Changed typo in Data Retention Characteristics (t_R) from 100 μs to t_{RC} ns Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin Changed t_{HZOE}, t_{HZWE} from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin Changed t_{SCE} from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin Changed t_{HZCE} from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin Changed t_{SD} from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin Changed Ordering Information to include Pb-Free Packages
*B	414807	See ECN	ZSD	Changed from Preliminary information to Final Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court" Removed 35ns Speed Bin Removed "L" version of CY62148EV30 Changed ball C3 from DNU to NC. Removed the redundant footnote on DNU. Changed I_{CC} (max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at f=1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f = f_{max} Changed I_{SB1} and I_{SB2} Typ values from 0.7 μA to 1 μA and Max values from 2.5 μA to 7 μA. Changed the AC test load capacitance value from 50pF to 30pF. Changed I_{CCDR} from 2.5 μA to 7 μA. Added I_{CCDR} typical value. Changed t_{LZOE} from 3 ns to 5 ns Changed t_{LZCE} and t_{LZWE} from 6 ns to 10 ns Changed t_{HZCE} from 22 ns to 18 ns Changed t_{PWE} from 30 ns to 35 ns. Changed t_{SD} from 22 ns to 25 ns. Updated the package diagram 36-pin VFBGA from *B to *C Added 32-pin SOIC package diagram and pin diagram Updated the ordering information table and replaced the Package Name column with Package Diagram.
*C	464503	See ECN	NXR	Included Automotive Range in product offering Updated Thermal Resistance table Updated the Ordering Information
*D	833080	See ECN	VKN	Added footnote 8 Added V_{IL} spec for SOIC package
*E	890962	See ECN	VKN	Removed Automotive part and its related information Added footnote 2 related to SOIC package Added footnote 9 related to I_{SB2} Added AC values for 55 ns Industrial-SOIC range Updated Ordering Information table

Document Title: CY62148EV30 MoBL® 4-Mbit (512 K × 8) Static RAM Document Number: 38-05576				
Rev.	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*F	987940	See ECN	VKN	Changed V_{OL} spec from 0.4V to 0.2V for SOIC package at I_{OL} = 0.1 mA Changed V_{IL} spec from 0.6V to 0.4V for SOIC package at V_{CC} = 2.2V to 2.7V Updated footnote 8 Made footnote 9 applicable for both I_{SB2} and I_{CCDR}
*G	2548575	08/05/08	NXR	Added Auto-A information. Included -45BVI
*H	2769239	09/25/09	VKN/AESA	Included -45BVI in the Ordering Information table
*I	2944332	06/04/2010	VKN	Added footnote related to chip enable in Truth Table Updated Package Diagrams
*J	3007403	08/13/2010	AJU	Updated new template.
*K	3110202	12/14/2010	PRAS	Updated Logic Block Diagram and Ordering Code Definitions.
*L	3302901	07/06/2011	RAME	Updated all the notes. Updated Package diagram 51-85095. Updated Ordering Code Definitions. Removed the references of AN1094. Updated as per template.
*M	3363097	09/07/2011	AJU	Corrected footnote cross-reference for I_{CCDR} spec. Updated 36-ball VFBGA and 32-pin SOIC package specs.

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