FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13749-1E

16-bit Microcontroller

CMOS

F²MC-16LX MB90960 Series

MB90F962(S)/V340E-101/V340E-102

■ DESCRIPTION

The MB90960-series is a 16-bit general-purpose microcontroller. Fujitsu now offers on-chip Flash-ROM program memory up to 64 Kbytes.

The power supply (3 V) is supplied to the internal MCU core from an internal regulator circuit. This creates a major advantage in terms of EMI and power consumption.

The unit features a 4 channel input capture unit, 1 channel 16-bit free-run timer, 2-channel LIN-UART, and 16-channel 8/10-bit A/D converter as the peripheral resource.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- **Clock**
  - Built-in PLL clock frequency multiplying circuit
  - Machine clock (PLL clock) selectable from frequency division by 2 of oscillation clock or 1 to 6-multiplied oscillation clock (4 MHz to 24 MHz when oscillation clock is 4 MHz) .
  - Sub clock operation : Up to 50 kHz (devices without S-suffix only)
  - Minimum instruction execution time : 42 ns (4 MHz oscillation clock and 6-multiplied PLL clock) .

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

FUJITSU

- **Instruction system optimized controllers**
  - 16 Mbytes CPU memory space : Internal 24-bit addressing
  - Various data types (bit, byte, word, and long word)
  - Various addressing modes (23 types)
  - Enhanced signed instructions of multiplication/division and RETI
  - Enhanced high-accuracy operations by 32-bit accumulator
- **Instruction system for high-level language (C language) / multitask**
  - System stack pointer
  - Enhanced pointer indirect instructions
  - Barrel shift instructions
- **Higher execution speed**
  - 4-byte instruction queue
- **Powerful interrupt function**
  - Powerful interrupt function with 8 levels and 34 factors
  - Corresponds to 8-channel external interrupt
- **CPU-independent automatic data transfer function**
  - Expanded intelligent I/O service function (EI^{2}OS) : Maximum 16 channels
- **Low-power consumption mode**
  - Clock mode
    PLL clock mode (a PLL clock that is a multiple of the oscillation clock is used to operate the CPU and peripheral functions.)
    Main clock mode (the main clock, with the oscillation clock frequency divided by 2 is used to operate the CPU and peripheral functions.)
    Sub clock mode (the sub clock is used to operate the CPU and peripheral functions.)
  - Standby mode
    Sleep mode (stops the operation clock to the CPU.)
    Watch mode (operates the sub clock and watch timer only.)
    Time-base timer mode (operates the oscillation clock, sub clock, time-base timer and watch timer only.)
    Stop mode (stops the operates the oscillation clock and sub clock.)
  - CPU intermittent operation mode
- **I/O port**
  - General-purpose input/output ports (CMOS output)
    - 34 ports (products without S-suffix)
    - 36 ports (products with S-suffix)
- **Sub clock pin (X0A, X1A)**
  - Yes : (external oscillator used), products without S-suffix
  - No : products with S-suffix
- **Timer**
  - Time-base timer, watch timer (products without S-suffix), watchdog timer : 1 channel
  - 8/16-bit PPG timer : 8-bit × 4 channels or 16-bit × 2 channels
  - 16-bit reload timer : 2 channels
  - 16- bit input/output timer
    - 16-bit free-run timer : 1 channel
    - 16- bit input capture (ICU) : 4 channels

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- **LIN-UART (LIN/SCI) : Maximum 2 channels**
  - Full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transfer
- **DTP/External interrupt : 8 channels**
  - Module for activation of expanded intelligent I/O service (EI^2OS) and generation of external interrupt by external input.
- **Delayed interrupt generator module**
  - Generates interrupt request for task switching.
- **8/10-bit A/D converter : 16 channels**
  - 8-bit and 10-bit resolution.
  - Start by external trigger input.
  - Conversion time : 3 μs (frequency, including sampling time at 24 MHz machine clock)
- **Program patch function**
  - Detects address match for 6 address pointers.
- **Changeable port input voltage level**
  - Automotive input level/CMOS Schmitt input level (initial value in single-chip mode is Automotive level).

■ PRODUCT LINEUP

Parameter \ Part number	MB90F962	MB90F962S	MB90V340E-101	MB90V340E-102
Type	Flash memory product		Evaluation product	
CPU	F²MC-16LX CPU			
System clock	PLL clock multiplier (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz oscillation clock, PLL × 6)			
ROM	Flash memory 64 Kbytes (60 Kbytes + 4 Kbytes Sectors)		External	
RAM capacitance	3 Kbytes		30 Kbytes	
Power supply for emulator*1	—		Yes	
Sub clock pin (X0A, X1A)	Yes	No		Yes
Operating voltage range	3.5 V to 5.5 V : at normal operation (not using A/D converter and not doing flash programming) 4.0 V to 5.5 V : at normal operation		5 V ± 10%	
Operating temperature range	− 40 °C to + 125°C *2		—	
Package	LQFP-48P		PGA-299C	
LIN-UART	2 channels		5 channels	
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
8/10-bit A/D Converter	16 channels		24 channels	
	10-bit or 8-bit resolution Conversion time: Min. 3 μs includes sample time (per one channel)			
16-bit Reload Timer	2 channels		4 channels	
	Operation clock frequency: fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function			
16-bit I/O Timer	1 channel		4 channels	
	Signals an interrupt when overflowing. Operating clock frequency: fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)			
16-bit Input Capture	4 channels		6 channels	
	Maintains I/O timer value by pin input (rising edge, falling edge, or both edge), and generates interrupt			

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Parameter \ Part number	MB90F962	MB90F962S	MB90V340E-101	MB90V340E-102
8/16-bit PPG timer	2 channels (16-bit) / 4 channels (8-bit) 8-bit reload counters × 4 8-bit reload registers for "L" pulse width × 4 8-bit reload registers for "H" pulse width × 4		8 channels (16-bit) / 16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for "L" pulse width × 16 8-bit reload registers for "H" pulse width × 16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operating clock frequency: fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, or 128 µs @ fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
External Interrupts	8 channels			
	Can be used rising edge, falling edge, starting up by "H"/"L" level input, external input,extended intelligent I/O services (EI^{2}OS) and DMA.			
Corresponding evaluation product	MB90V340E-102	MB90V340E-101	—	

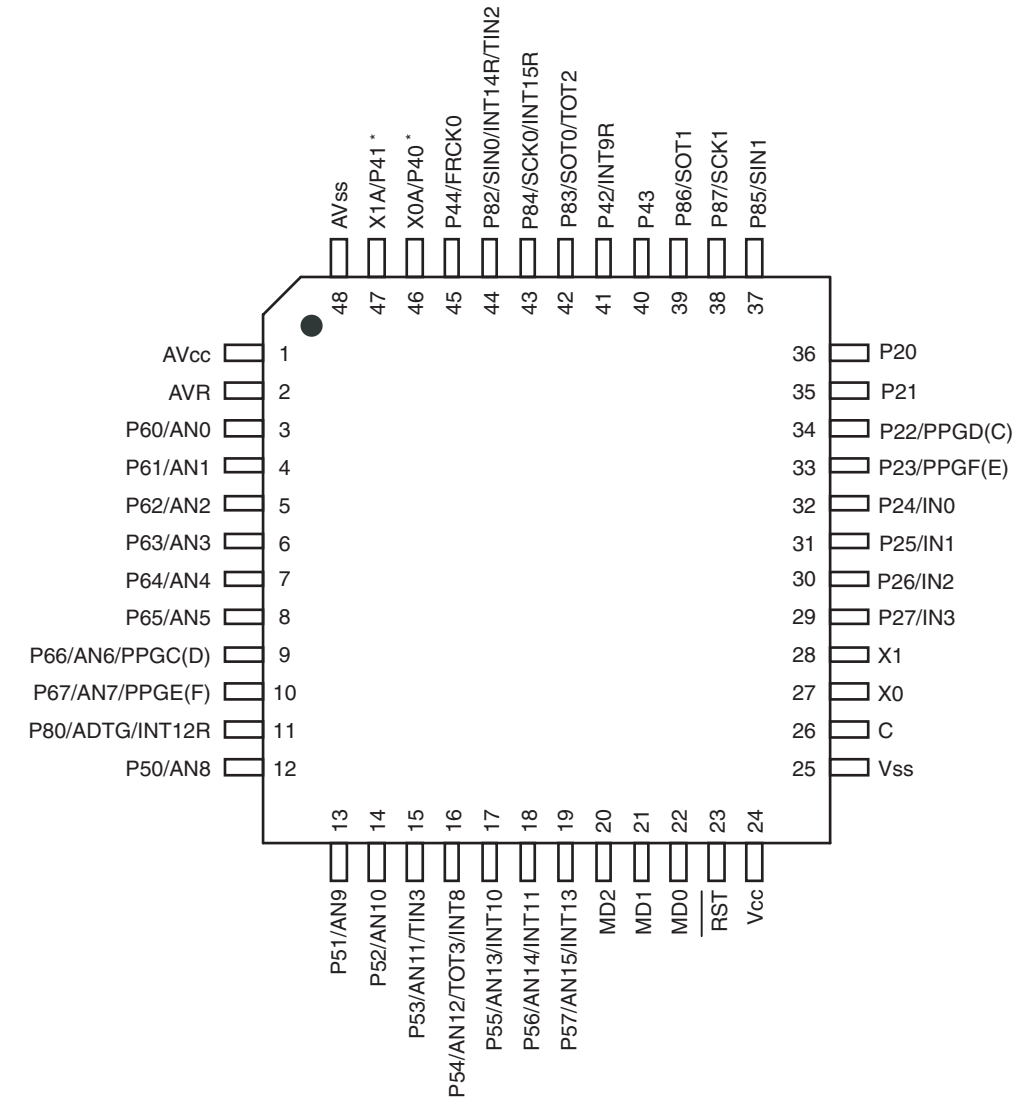
*1 : It is setting of Jumper switch (TOOL V_{CC}) when emulator (MB2147-01) is used. Please refer to the Emulator hardware manual for the details.

*2 : If used exceeding T_A = +105°C, be sure to contact Fujitsu for reliability limitations.

■ PIN ASSIGNMENT

• MB90F962(S)

(TOP VIEW)
(LQFP-48P)



(FPT-48P-M26)

* : MB90F962: X0A, X1A
MB90F962S: P40, P41

■ PIN DESCRIPTION

Pin No. LQFP-48P*	Pin name	Circuit type	Function
1	AV_{CC}	I	V_{CC} power input pin for analog circuit.
2	AVR	—	Power (Vref+) input pin for A/D converter. AVR should not exceed V_{CC}.
3 to 8	P60 to P65	H	General-purpose I/O ports.
	AN0 to AN5		Analog input pins for A/D converter.
9, 10	P66, P67	H	General-purpose I/O ports.
	AN6, AN7		Analog input pins for A/D converter.
	PPGC (D) , PPGE (F)		Output pins for PPG.
11	P80	F	General-purpose I/O port.
	ADTG		Trigger input pin for A/D converter.
	INT12R		External interrupt request input pin for INT12R.
12 to 14	P50 to P52	H	General-purpose I/O ports (I/O circuit type of P50 is different from that of MB90V340E) .
	AN8 to AN10		Analog input pins for A/D converter.
15	P53	H	General-purpose I/O port.
	AN11		Analog input pin for A/D converter.
	TIN3		Event input pin for reload timer 3.
16	P54	H	General-purpose I/O port.
	AN12		Analog input pin for A/D converter.
	TOT3		Output pin for reload timer 3.
	INT8		External interrupt request input pin for INT8.
17 to 19	P55 to P57	H	General-purpose I/O ports.
	AN13 to AN15		Analog input pins for A/D converter.
	INT10, INT11, INT13		External interrupt request input pins for INT10, INT11, INT13.
20	MD2	D	Input pin for selecting operation mode.
21, 22	MD1, MD0	C	Input pins for selecting operation mode.
23	$\overline{RST}$	E	Reset input.
24	V_{CC}	—	Power input pin (3.5 V to 5.5 V) .
25	V_{SS}	—	Power input pin (0 V) .
26	C	I	Capacity pin for stabilizing power supply. It should be connected to a higher than or equal to 0.1 μF ceramic capacitor.
27	X0	A	Oscillation input pin.
28	X1		Oscillation output pin.

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Pin No. LQFP-48P*	Pin name	Circuit type	Function
29 to 32	P27 to P24	G	General-purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	IN3 to IN0		Event input pins for input capture 0 to 3.
33, 34	P23, P22	G	General-purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	PPGF (E) , PPGD (C)		Output pins for PPG.
35, 36	P21, P20	G	General-purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
37	P85	K	General-purpose I/O port.
	SIN1		Serial data input pin for LIN-UART1.
38	P87	F	General-purpose I/O port.
	SCK1		Clock I/O pin for LIN-UART1.
39	P86	F	General-purpose I/O port.
	SOT1		Serial data output pin for LIN-UART1.
40	P43	F	General-purpose I/O port.
41	P42	F	General-purpose I/O port.
	INT9R		External interrupt request input pin for INT9R.
42	P83	F	General-purpose I/O port.
	SOT0		Serial data output pin for LIN-UART0.
	TOT2		Output pin for reload timer 2
43	P84	F	General-purpose I/O port.
	SCK0		Clock I/O pin for LIN-UART0.
	INT15R		External interrupt request input pin for INT15R.
44	P82	K	General-purpose I/O port.
	SIN0		Serial data input pin for LIN-UART0.
	INT14R		External interrupt request input pin for INT14R.
	TIN2		Event input pin for reload timer 2.
45	P44	F	General-purpose I/O port (I/O circuit type of P44 is different from that of MB90V340E) .
	FRCK0		Free-run timer 0 clock input pin.

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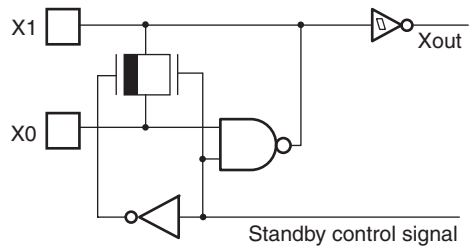
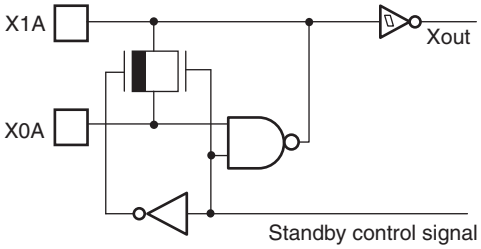
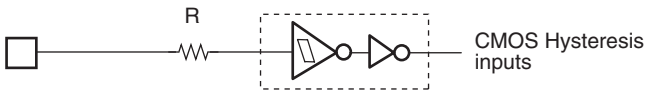
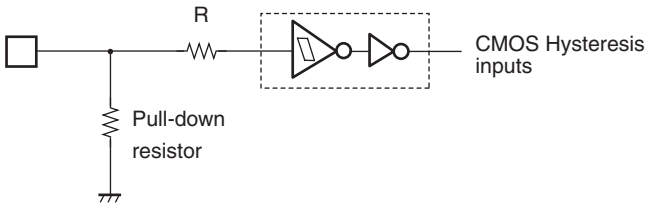
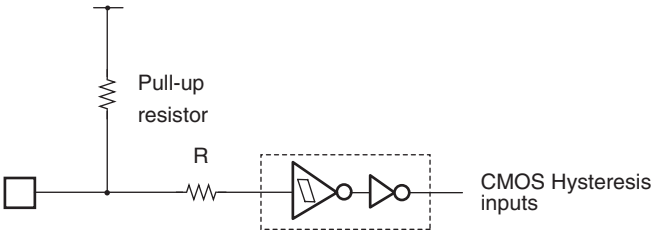
Pin No. LQFP-48P*	Pin name	Circuit type	Function
46, 47	P40, P41	F	General-purpose I/O ports. (products with S-suffix and MB90V340E-101)
	X0A, X1A	B	X0A: Oscillation input pin for sub clock X1A: Oscillation output pin for sub clock (products without S-suffix and MB90V340E-102)
48	AV_{SS}	I	V_{SS} power input pin for analog circuit.

* : FPT-48P-M26

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		CMOS input
D		• CMOS input • No Pull-down
E		CMOS hysteresis input Pull-up resistor value : approx. 50 kΩ

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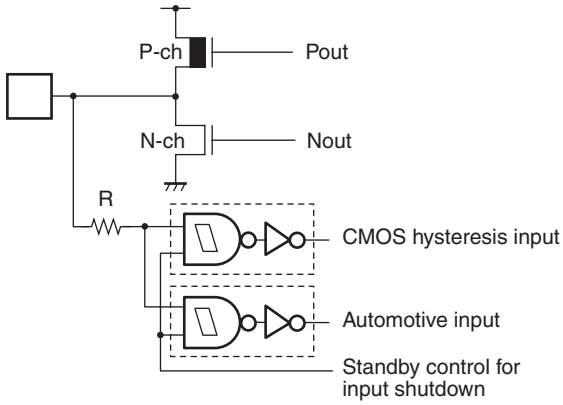
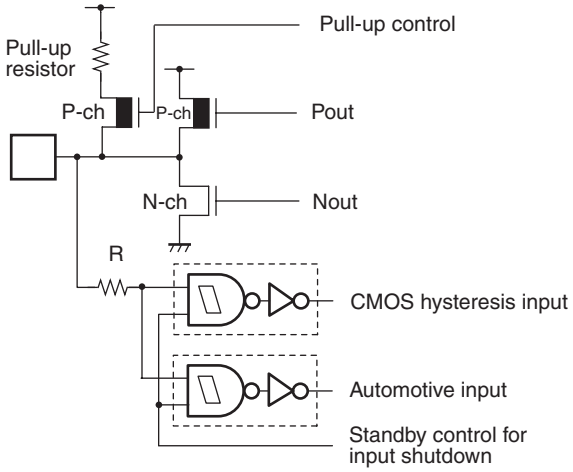
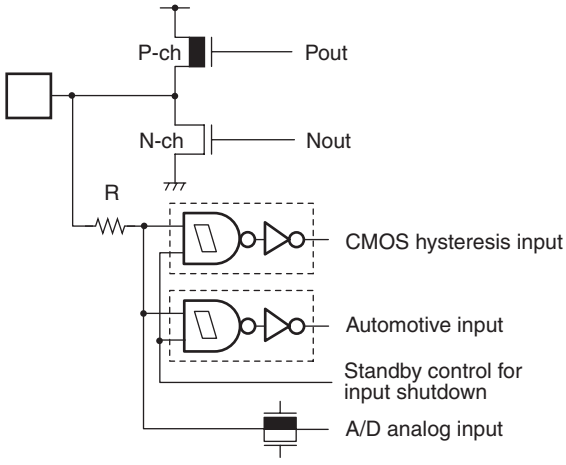
Type	Circuit	Remarks
F		• CMOS level output (I_{OL} = 4 mA, I_{OH} = − 4 mA) • CMOS hysteresis input (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
G		• CMOS level output (I_{OL} = 4 mA, I_{OH} = − 4 mA) • CMOS hysteresis input (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • Programmable pull-up resistor : approx. 50 kΩ
H		• CMOS level output (I_{OL} = 4 mA, I_{OH} = − 4 mA) • CMOS hysteresis input (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input

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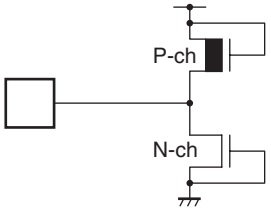
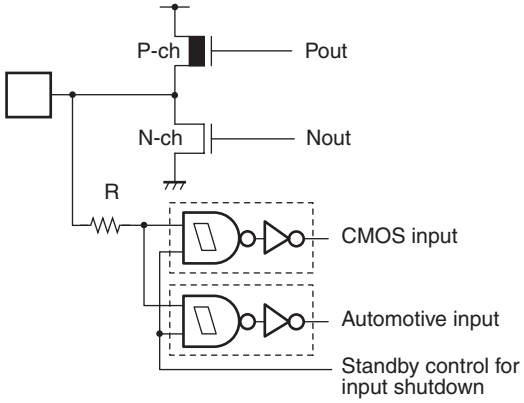
Type	Circuit	Remarks
I		Power supply input protection circuit
K		• CMOS level output (I_{OL} = 4 mA, I_{OH} = − 4 mA) • CMOS input (With standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)

■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Treatment of unused pins
- Using external clock
- Notes on during operation of PLL clock mode
- Power supply pins (V_{CC}/V_{SS})
- Pull-up/down resistors
- Crystal oscillator circuit
- Turning-on sequence of power supply to A/D converter and analog inputs
- Connection of unused pins of A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Initialization
- Correspondence with +105 °C or more

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

When used, note that maximum rated voltage is not exceeded.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVR) exceed the digital power-supply voltage.

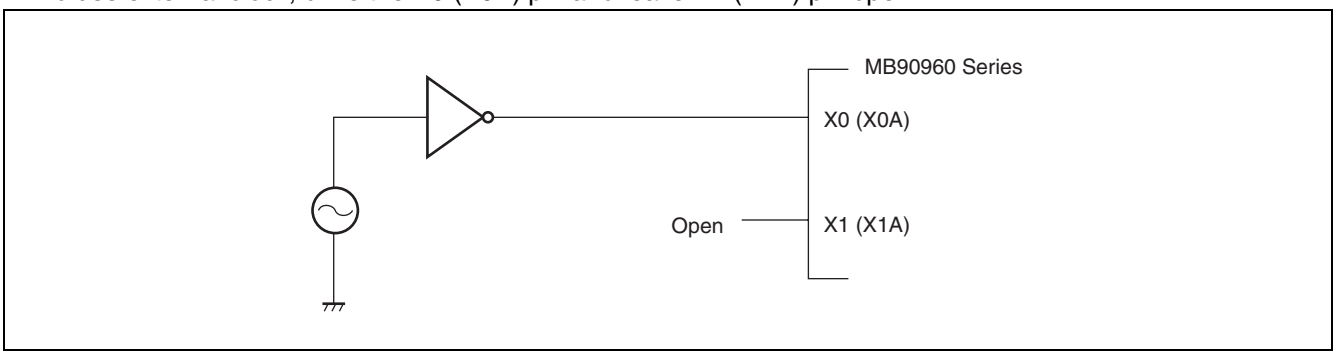
2. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch-up and possible permanent damage of the device. Therefore, they must be pulled up or pulled down through resistors. In this case, those resistors should be more than 2 kΩ .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

3. Using external clock

To use external clock, drive the X0 (X0A) pin and leave X1 (X1A) pin open.

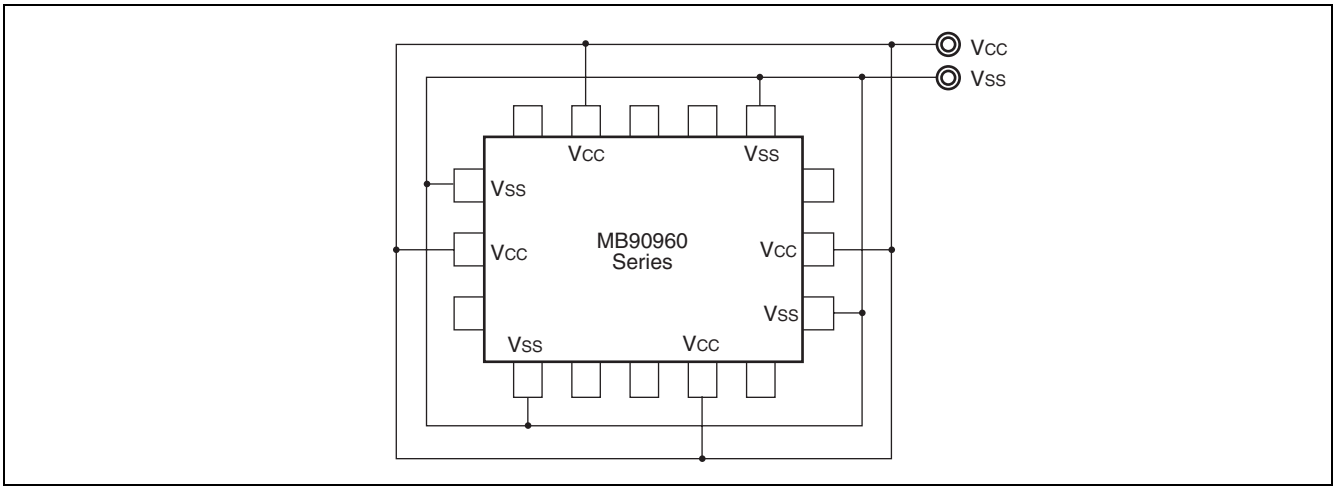


4. Notes on during operation of PLL clock mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

5. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch-up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and to keep the recommended DC characteristics specified as the total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
- Connect V_{CC} and V_{SS} to the device from the power supply source with lowest possible impedance.
- It is recommended to connect a capacitor of about 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} in the vicinity of V_{CC} and V_{SS} pins of the device.



6. Pull-up/down resistors

The MB90960 series does not support internal pull-up/down resistors (except Port 2 : programmable pull-up resistors) . Use pull-up/down handling where needed.

7. Crystal oscillator circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

8. Turning-on sequence of power supply to A/D converter and analog inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVR) and analog inputs (AN0 to AN15) after turning-on the digital power supply (V_{CC}) . Turn-off the digital power supply after turning off the A/D converter power supply and analog inputs. In this case, make sure that the voltage does not exceed AVR or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

9. Connection of unused pins of A/D converter if A/D converter is not used

Connect unused pins of A/D converter to AV_{CC} = V_{CC}, AV_{SS} = AVR = V_{SS}.

10. Notes on energization

To prevent malfunction of the internal voltage regulator , supply voltage profile while turning on the power supply should be slower than 50 μs (0.2 V to 2.7 V) .

11. Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation assurance range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guide lines, stabilize the power supply voltage so that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50 Hz/60 Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1 V/ms or less in instantaneous fluctuation for power supply switching.

12. Initialization

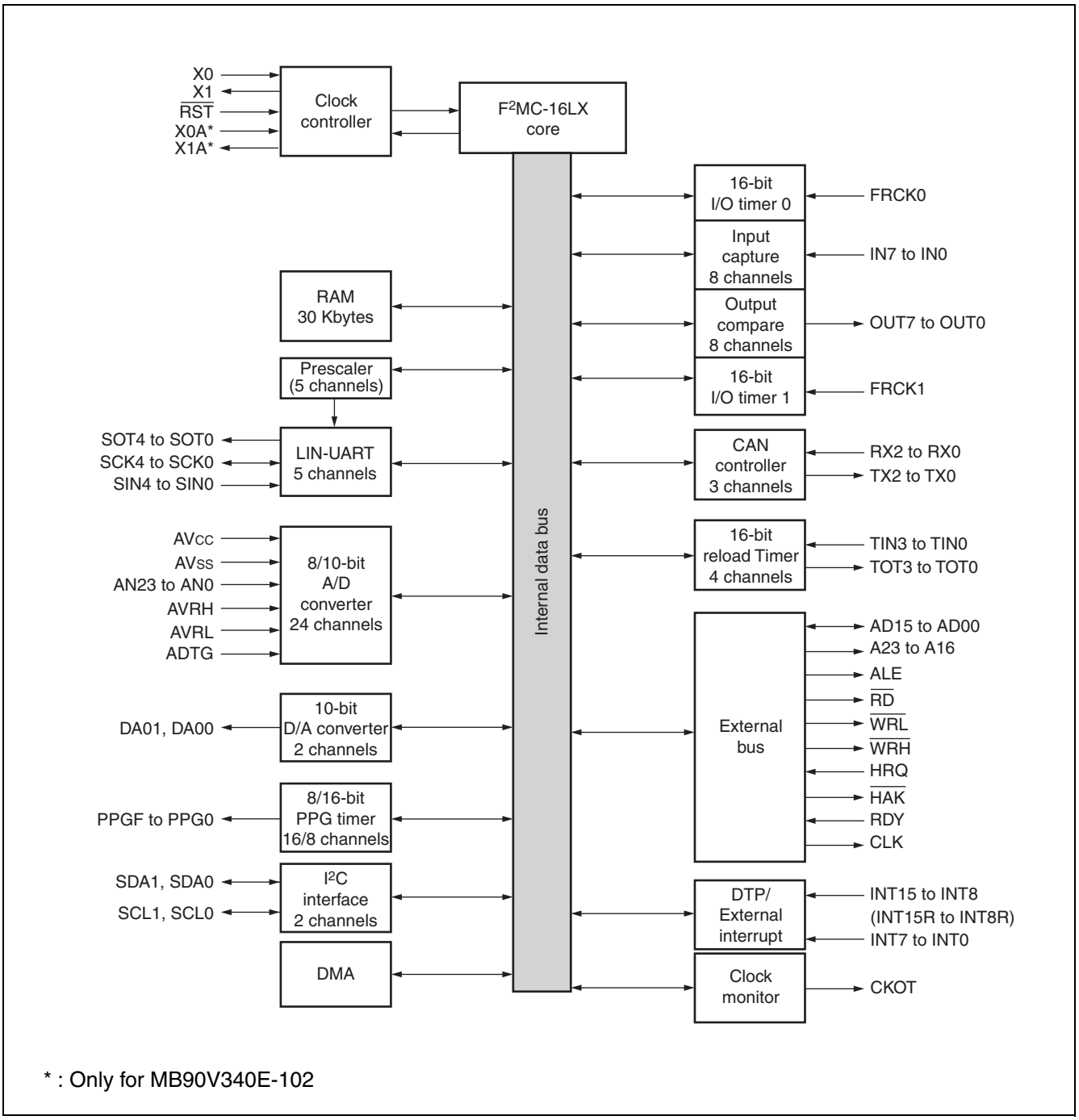
In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

13. Correspondence with +105 °C or more

If used exceeding T_A = +105 °C, please contact Fujitsu for reliability limitations.

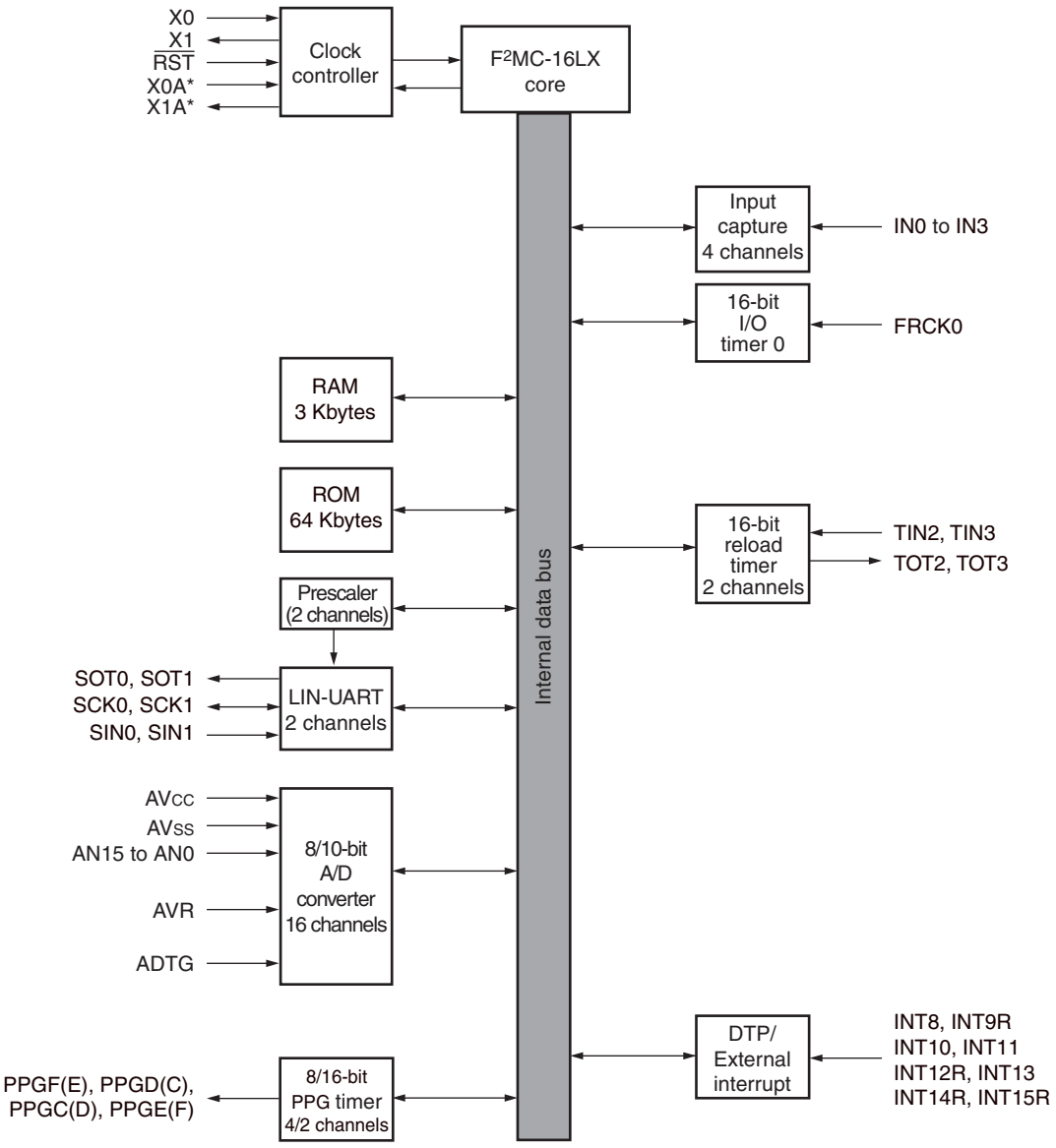
■ BLOCK DIAGRAMS

• MB90V340E-101/V340E-102



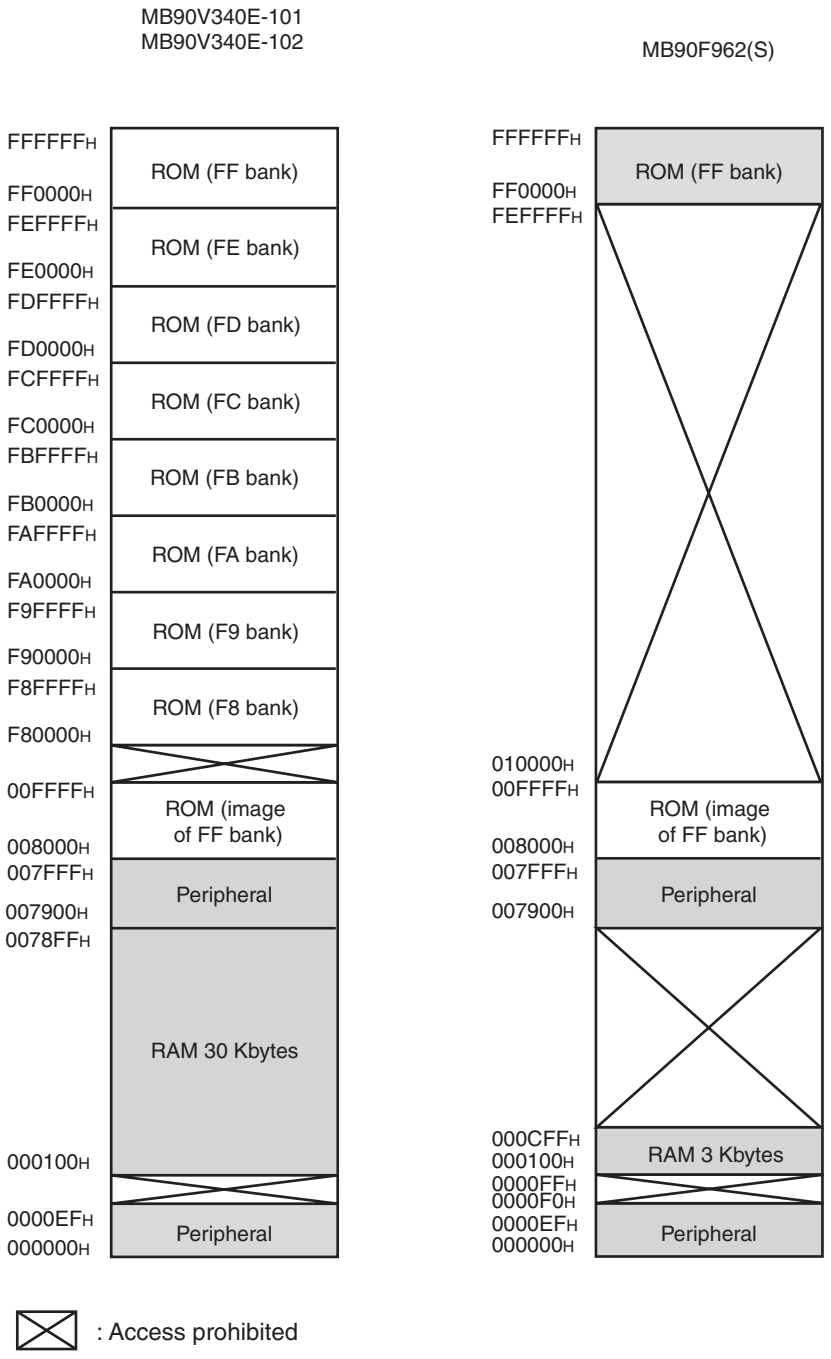
* : Only for MB90V340E-102

• **MB90F962(S)**



* : Only for MB90F962

■ MEMORY MAP



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referred without using the far specification in the pointer declaration.
For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

■ I/O MAP

Address	Register	Abbreviation	Access	Resource name	Initial value
000000H, 000001H	Reserved				
000002H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXXB
000003H	Reserved				
000004H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXXB
000005H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXXB
000006H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXXB
000007H	Reserved				
000008H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXXB
000009H, 00000AH	Reserved				
00000BH	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111B
00000CH	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111B
00000DH	Reserved				
00000EH	Input Level Select Register 0	ILSR0	R/W	Port 2, 4, 5, 6	X000X0XXB
00000FH	Input Level Select Register 1	ILSR1	R/W	Port 8	XXXXXXX0B
0000010H, 000011H	Reserved				
000012H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000B
000013H	Reserved				
000014H	Port 4 Direction Register	DDR4	R/W	Port 4	XXX00000B
000015H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000B
000016H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000B
000017H	Reserved				
000018H	Port 8 Direction Register	DDR8	R/W	Port 8	000000X0B
000019H	Reserved				
00001AH	Port A Direction Register	DDRA	W	Port A	XXX00XXXB
00001BH to 00001DH	Reserved				
00001EH	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000B
00001FH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000020H	Serial Mode Register 0	SMR0	W, R/W	LIN-UART0	00000000B
000021H	Serial Control Register 0	SCR0	W, R/W		00000000B
000022H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000B
000023H	Serial Status Register 0	SSR0	R, R/W		00001000B
000024H	Extended Communication Control Register 0	ECCR0	R, W, R/W		000000XXB
000025H	Extended Status Control Register 0	ESCR0	R/W		00000100B
000026H	Baud Rate Generator Register 00	BGR00	R/W, R		00000000B
000027H	Baud Rate Generator Register 01	BGR01	R/W, R		00000000B
000028H	Serial Mode Register 1	SMR1	W, R/W	LIN-UART1	00000000B
000029H	Serial Control Register 1	SCR1	W, R/W		00000000B
00002AH	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000B
00002BH	Serial Status Register 1	SSR1	R, R/W		00001000B
00002CH	Extended Communication Control Register 1	ECCR1	R, W, R/W		000000XXB
00002DH	Extended Status Control Register 1	ESCR1	R/W		00000100B
00002EH	Baud Rate Generator Register 10	BGR10	R/W, R		00000000B
00002FH	Baud Rate Generator Register 11	BGR11	R/W, R		00000000B
000030H to 00003AH	Reserved				
00003BH	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000B
00003CH to 000047H	Reserved				
000048H	PPGC Operation Mode Control Register	PPGCC	W, R/W	16-bit PPG C/D	0X000XX1B
000049H	PPGD Operation Mode Control Register	PPGCD	W, R/W		0X000001B
00004AH	PPGC/PPGD Count Clock Select Register	PPGCD	R/W		000000X0B
00004BH	Reserved				
00004CH	PPGE Operation Mode Control Register	PPGCE	W, R/W	16-bit PPG E/F	0X000XX1B
00004DH	PPGF Operation Mode Control Register	PPGCF	W, R/W		0X000001B
00004EH	PPGE/PPGF Count Clock Select Register	PPGEF	R/W		000000X0B
00004FH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000050H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000B
000051H	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XXB
000052H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000B
000053H	Input Capture Edge 2/3	ICE23	R		XXXXXXXXB
000054H to 000063H	Reserved				
000064H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000B
000065H	Timer Control Status 2	TMCSR2	R/W		XXXX0000B
000066H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000B
000067H	Timer Control Status 3	TMCSR3	R/W		XXXX0000B
000068H	A/D Control Status 0	ADCS0	R/W	A/D Converter	000XXXX0B
000069H	A/D Control Status 1	ADCS1	R/W, W		0000000XB
00006AH	A/D Data Register 0	ADCR0	R		00000000B
00006BH	A/D Data Register 1	ADCR1	R		XXXXXX00B
00006CH	A/D Converter Setting 0	ADSR0	R/W		00000000B
00006DH	A/D Converter Setting 1	ADSR1	R/W		00000000B
00006EH	Reserved				
00006FH	ROM Mirror Function Select	ROMM	W	ROM Mirror	XXXXXXX1B
000070H to 00009DH	Reserved				
00009EH	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000B
00009FH	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt generation module	XXXXXXX0B
0000A0H	Low-power Consumption Mode Control Register	LPMCR	W, R/W	Low-Power consumption Control Circuit	00011000B
0000A1H	Clock Selection Register	CKSCR	R, R/W	Low-Power consumption Control Circuit	11111100B
0000A2H to 0000A7H	Reserved				
0000A8H	Watchdog Timer Control Register	WDTC	R, W	Watchdog Timer	XXXXX111B
0000A9H	Time-base Timer Control Register	TBTC	W, R/W	Time-base Timer	1XX00100B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0000AA$_H$	Watch Timer Control Register	WTC	R, R/W	Watch Timer	1X001000$_B$
0000AB$_H$ to 0000AD$_H$	Reserved				
0000AE$_H$	Flash Control Status	FMCS	R, R/W	Flash Memory	000X0000$_B$
0000AF$_H$	Reserved				
0000B0$_H$	Interrupt Control Register 00	ICR00	W, R/W	Interrupt Control	00000111$_B$
0000B1$_H$	Interrupt Control Register 01	ICR01	W, R/W		00000111$_B$
0000B2$_H$	Interrupt Control Register 02	ICR02	W, R/W		00000111$_B$
0000B3$_H$	Interrupt Control Register 03	ICR03	W, R/W		00000111$_B$
0000B4$_H$	Interrupt Control Register 04	ICR04	W, R/W		00000111$_B$
0000B5$_H$	Interrupt Control Register 05	ICR05	W, R/W		00000111$_B$
0000B6$_H$	Interrupt Control Register 06	ICR06	W, R/W		00000111$_B$
0000B7$_H$	Interrupt Control Register 07	ICR07	W, R/W		00000111$_B$
0000B8$_H$	Interrupt Control Register 08	ICR08	W, R/W		00000111$_B$
0000B9$_H$	Interrupt Control Register 09	ICR09	W, R/W		00000111$_B$
0000BA$_H$	Interrupt Control Register 10	ICR10	W, R/W		00000111$_B$
0000BB$_H$	Interrupt Control Register 11	ICR11	W, R/W		00000111$_B$
0000BC$_H$	Interrupt Control Register 12	ICR12	W, R/W		00000111$_B$
0000BD$_H$	Interrupt Control Register 13	ICR13	W, R/W		00000111$_B$
0000BE$_H$	Interrupt Control Register 14	ICR14	W, R/W		00000111$_B$
0000BF$_H$	Interrupt Control Register 15	ICR15	W, R/W		00000111$_B$
0000C0$_H$ to 0000C9$_H$	Reserved				
0000CA$_H$	DTP/External Interrupt Enable 1	ENIR1	R/W	External Interrupt 1	00000000$_B$
0000CB$_H$	DTP/External Interrupt Source 1	EIRR1	R/W		XXXXXXXX$_B$
0000CC$_H$	Detection Level Setting 1	ELVR1	R/W		00000000$_B$
0000CD$_H$	Detection Level Setting 1	ELVR1	R/W		00000000$_B$
0000CE$_H$	External Interrupt factor Select	EISSR	R/W		00000000$_B$
0000CF$_H$	PLL/Sub clock Control Register	PSCCR	W	PLL	XXXX0000$_B$
0000D0$_H$ to 0000FF$_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007900H to 007917H	Reserved				
007918H	Reload Register LC	PRLLC	R/W	16-bit PPG C/D	XXXXXXXXB
007919H	Reload Register HC	PRLHC	R/W		XXXXXXXXB
00791AH	Reload Register LD	PRLLD	R/W		XXXXXXXXB
00791BH	Reload Register HD	PRLHD	R/W		XXXXXXXXB
00791CH	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	XXXXXXXXB
00791DH	Reload Register HE	PRLHE	R/W		XXXXXXXXB
00791EH	Reload Register LF	PRLLF	R/W		XXXXXXXXB
00791FH	Reload Register HF	PRLHF	R/W		XXXXXXXXB
007920H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXXB
007921H	Input Capture 0	IPCP0	R		XXXXXXXXB
007922H	Input Capture 1	IPCP1	R		XXXXXXXXB
007923H	Input Capture 1	IPCP1	R		XXXXXXXXB
007924H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXXB
007925H	Input Capture 2	IPCP2	R		XXXXXXXXB
007926H	Input Capture 3	IPCP3	R		XXXXXXXXB
007927H	Input Capture 3	IPCP3	R		XXXXXXXXB
007928H to 00793FH	Reserved				
007940H	Timer Data 0	TCDT0	R/W	I/O Timer 0	00000000B
007941H	Timer Data 0	TCDT0	R/W		00000000B
007942H	Timer Control Status 0	TCCSL0	R/W		00000000B
007943H	Timer Control Status 0	TCCSH0	R/W		0XXXXXXXB
007944H to 00794BH	Reserved				
00794CH	Timer 2/Reload 2	TMR2/TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXXB
00794DH			R/W		XXXXXXXXB
00794EH	Timer 3/Reload 3	TMR3/TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXXB
00794FH			R/W		XXXXXXXXB
007950H to 0079DFH	Reserved				

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0079E0H	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXXB
0079E1H	Detect Address Setting 0	PADR0	R/W		XXXXXXXXB
0079E2H	Detect Address Setting 0	PADR0	R/W		XXXXXXXXB
0079E3H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E4H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E5H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E6H	Detect Address Setting 2	PADR2	R/W		XXXXXXXXB
0079E7H	Detect Address Setting 2	PADR2	R/W		XXXXXXXXB
0079E8H	Detect Address Setting 2	PADR2	R/W		XXXXXXXXB
0079E9H to 0079EFH	Reserved				
0079F0H	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXXB
0079F1H	Detect Address Setting 3	PADR3	R/W		XXXXXXXXB
0079F2H	Detect Address Setting 3	PADR3	R/W		XXXXXXXXB
0079F3H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F4H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F5H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F6H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F7H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F8H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F9H to 007FFFH	Reserved				

Notes :
- Initial value of “X” represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI²OS corresponding	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N	#08	FFFFDC$_H$	—	—
INT9 instruction	N	#09	FFFFD8$_H$	—	—
Exception processing	N	#10	FFFFD4$_H$	—	—
Reserved	N	#11	FFFFD0$_H$	ICR00	0000B0$_H$
Reserved	N	#12	FFFFCC$_H$		
Reserved	N	#13	FFFFC8$_H$	ICR01	0000B1$_H$
Reserved	N	#14	FFFFC4$_H$		
Reserved	N	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Reserved	N	#16	FFFFBC$_H$		
Reserved	N	#17	FFFFB8$_H$	ICR03	0000B3$_H$
Reserved	N	#18	FFFFB4$_H$		
16-bit reload timer 2	Y1	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit reload timer 3	Y1	#20	FFFFAC$_H$		
Reserved	N	#21	FFFFA8$_H$	ICR05	0000B5$_H$
Reserved	N	#22	FFFFA4$_H$		
PPG C/D	N	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG E/F	N	#24	FFFF9C$_H$		
Time-base timer	N	#25	FFFF98$_H$	ICR07	0000B7$_H$
External interrupt 8 to 11	Y1	#26	FFFF94$_H$		
Watch Timer	N	#27	FFFF90$_H$	ICR08	0000B8$_H$
External interrupt 12 to 15	Y1	#28	FFFF8C$_H$		
A/D converter	Y1	#29	FFFF88$_H$	ICR09	0000B9$_H$
I/O timer 0	N	#30	FFFF84$_H$		
Reserved	N	#31	FFFF80$_H$	ICR10	0000BA$_H$
Reserved	N	#32	FFFF7C$_H$		
Input capture 0 to 3	Y1	#33	FFFF78$_H$	ICR11	0000BB$_H$
Reserved	N	#34	FFFF74$_H$		
LIN-UART 0 reception	Y2	#35	FFFF70$_H$	ICR12	0000BC$_H$
LIN-UART 0 transmission	Y1	#36	FFFF6C$_H$		
LIN-UART 1 reception	Y2	#37	FFFF68$_H$	ICR13	0000BD$_H$
LIN-UART 1 transmission	Y1	#38	FFFF64$_H$		

(Continued)

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Interrupt cause	EI²OS corresponding	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reserved	N	#39	FFFF60H	ICR14	0000BEH
Reserved	N	#40	FFFF5CH		
Flash memory	N	#41	FFFF58H	ICR15	0000BFH
Delayed interrupt generation module	N	#42	FFFF54H		

Y1 : Usable

Y2 : Usable, with EI²OS stop function

N : Unusable

Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When 2 peripheral resources share the ICR register, only one can use extended intelligent I/O service at a time.
- When either of the 2 peripheral resources sharing the ICR register specifies extended intelligent I/O service, the other one cannot use interrupts.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	–2.0	+2.0	mA	*4
Total Maximum clamp current	$\Sigma\|I_{CLAMP}\|$	—	40	mA	*4
“L” level maximum output current	I_{OL}	—	15	mA	*4
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level maximum overall output current	ΣI_{OL}	—	125	mA	*4
“L” level average overall output current	ΣI_{OLAV}	—	40	mA	*4
“H” level maximum output current	I_{OH}	—	–15	mA	*4
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level maximum overall output current	ΣI_{OH}	—	–125	mA	*4
“H” level average overall output current	ΣI_{OHAV}	—	–40	mA	*4
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+105	°C	
		–40	+125	°C	*5
Storage temperature	T_{STG}	–55	+150	°C	

(Continued)

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*1 : This parameter is based on V_{SS} = AV_{SS} = 0 V.

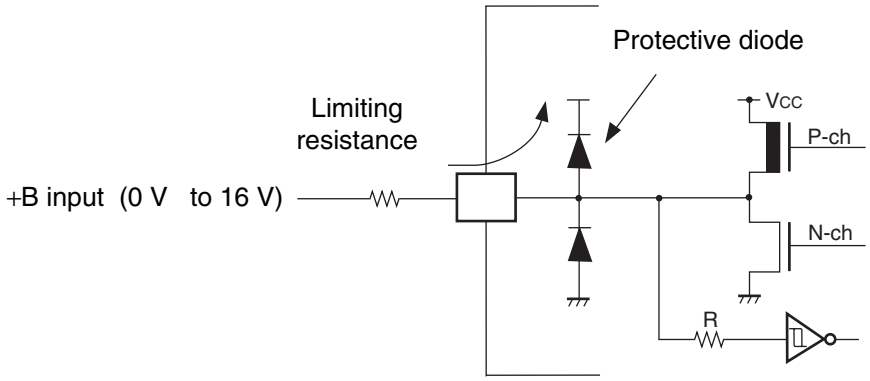
*2 : Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3 : V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4 : Applicable to pins : P20 to P27, P40 to P44, P50 to P57, P60 to P67, P80, P82 to P87

*5 : If used exceeding T_A = +105°C, be sure to contact Fujitsu for reliability limitations.
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is inputted when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits :

• **Input/output equivalent circuits**



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

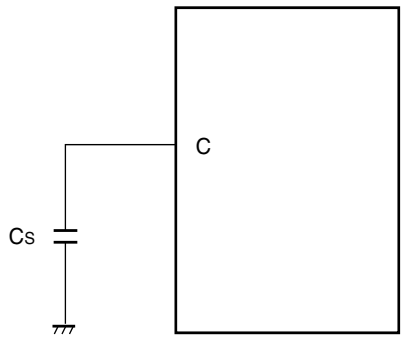
2. Recommended Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation when not using the A/D converter and not Flash programming.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smooth capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or capacitor of better AC characteristics for the C pin. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	–40	—	+105	°C	
		–40	—	+125	°C	*

* : If used exceeding T_A = +105 °C, please contact Fujitsu for reliability limitations.

• **C Pin Connection Diagram**



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(T_A = –40 °C to +125 °C*1, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “H” voltage	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if CMOS hysteresis levels are selected (except P82, P85)
		—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P82, P85 inputs if CMOS input levels are selected
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if Automotive input levels are selected
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	MD input pin
Input “L” voltage	V_{ILS}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Pin inputs if CMOS hysteresis input levels are selected (except P82, P85)
		—	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	P82, P85 inputs if CMOS input levels are selected
	V_{ILA}	—	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	Pin inputs if Automotive input levels are selected
	V_{ILR}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	MD input pin
Output “H” voltage	V_{OH}	—	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Output “L” voltage	V_{OL}	—	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–1	—	+ 1	µA	
Pull-up resistance	R_{UP}	P20 to P27, $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Except Flash memory devices

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(T_A = –40 °C to +125 °C*1, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	35	45	mA	MB90F962(S)
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At writing Flash memory.	—	50	60	mA	MB90F962(S)
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At erasing Flash memory.	—	50	60	mA	MB90F962(S)
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At sleep mode.	—	12	20	mA	MB90F962(S)
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, At main timer mode	—	0.3	0.8	mA	MB90F962(S)
	$I_{CTSPLL6}$		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At PLL timer mode, External frequency = 4 MHz	—	4	7	mA	MB90F962(S)
	I_{CCL}		V_{CC} = 5.0 V, Internal frequency : 8 kHz, At sub clock operation mode, T_A = + 25°C	—	40	100	µA	MB90F962
	I_{CCLS}		V_{CC} = 5.0 V, Internal frequency : 8 kHz, At sub clock sleep mode, T_A = + 25°C	—	10	50	µA	MB90F962
	I_{CCT}		V_{CC} = 5.0 V, Internal frequency : 8 kHz, At watch mode, T_A = + 25°C	—	8	30	µA	MB90F962
	I_{CCH}		V_{CC} = 5.0 V, At stop mode, T_A = + 25°C	—	5	25	µA	MB90F962(S)
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, V_{CC}, V_{SS}, C	—	—	5	15	pF	

*1 : If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.

*2 : The power supply current is measured with an external clock.

4. AC Characteristics

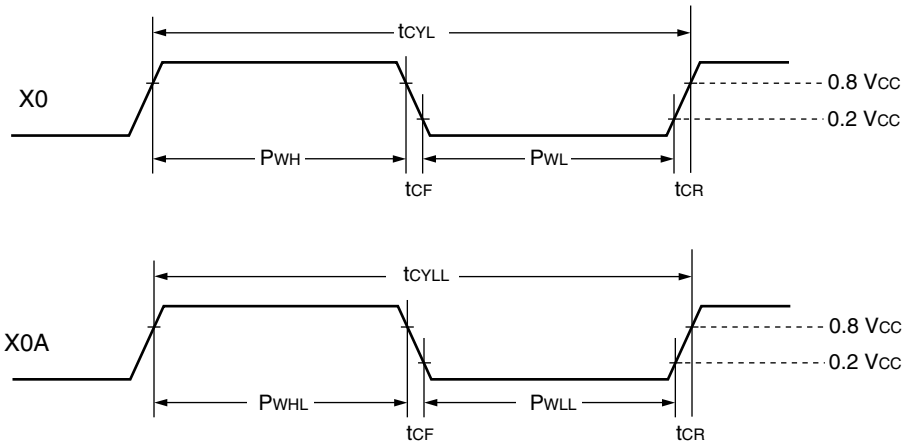
(1) Clock Timing

(T_A = –40 °C to +125 °C*, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

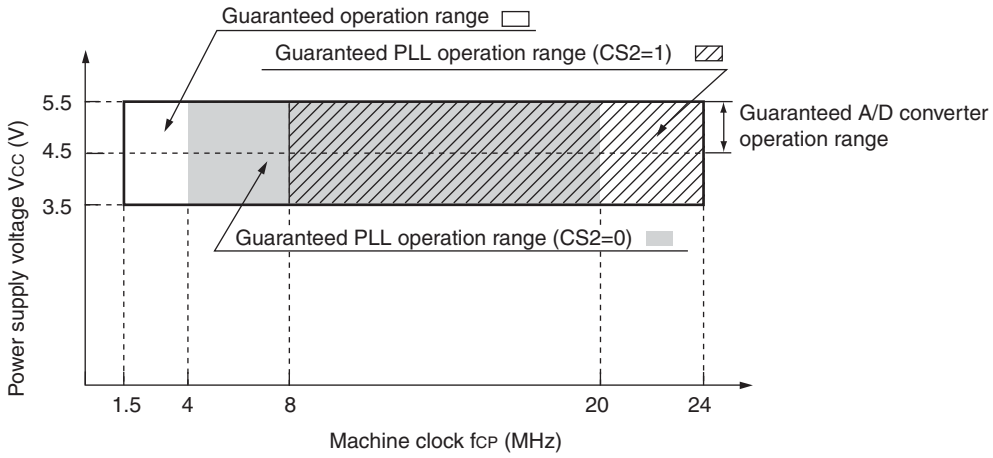
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	1/2 when PLL stops, When using an oscillation circuit
			4		16		PLL × 1, When using an oscillation circuit
			4		12		PLL × 2, When using an oscillation circuit
			4		8		PLL × 3, When using an oscillation circuit
			4		6		PLL × 4, When using an oscillation circuit
			4		4		PLL × 6, When using an oscillation circuit
		X0, X1	3	—	24	MHz	1/2 when PLL stops, When using an external clock
			4		20		PLL × 1, When using an external clock
			4		12		PLL × 2, When using an external clock
			4		8		PLL × 3, When using an external clock
			4		6		PLL × 4, When using an external clock
			4		4		PLL × 6, When using an external clock
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	µs	When using sub clock
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	µs	When using sub clock

*: If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.

• **Clock Timing**

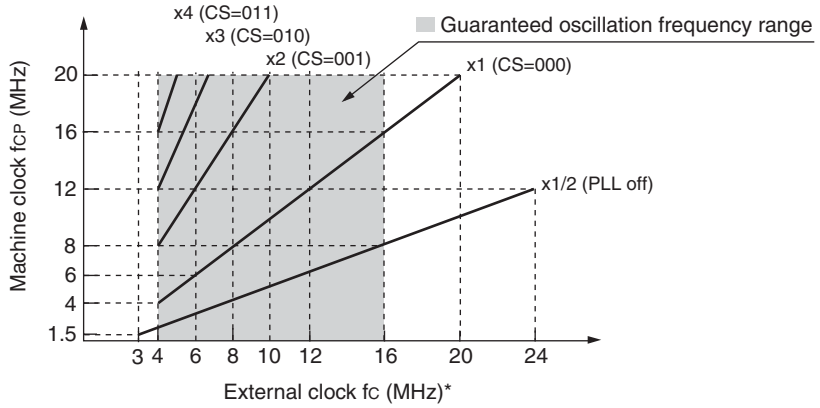


• Guaranteed PLL Operation Range

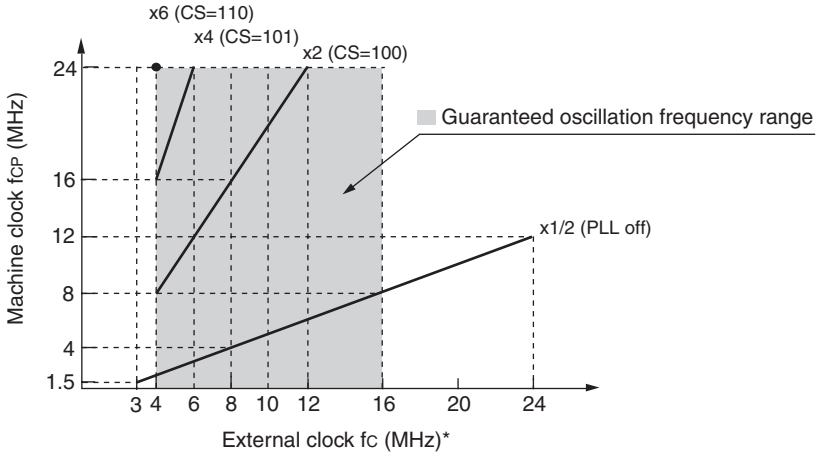


Guaranteed operation range of MB90960 series

• CS2 (bit 0 in PSCCR register) = 0



• CS2 (bit 0 in PSCCR register) = 1



* : When using a crystal oscillator or a ceramic oscillator, the maximum oscillation clock frequency is 16 MHz.

External clock frequency and Machine clock frequency

(2) Reset Standby Input

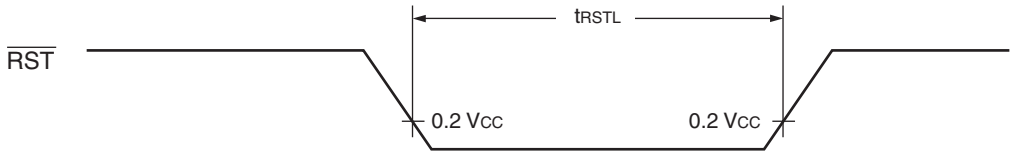
(T_A = –40 °C to +125 °C*1, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 100 µs	—	ns	In stop mode
			100	—	µs	In time-base timer mode

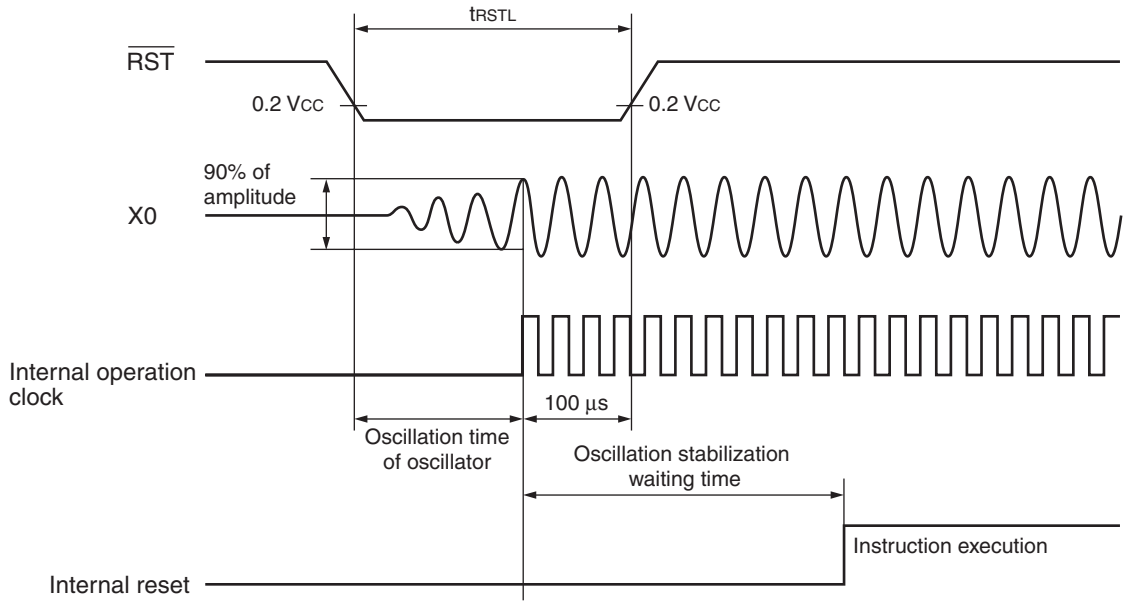
*1: If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%.
In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. With an external clock, the oscillation time is 0 ms.

• **Under normal operation :**



• **In stop mode :**

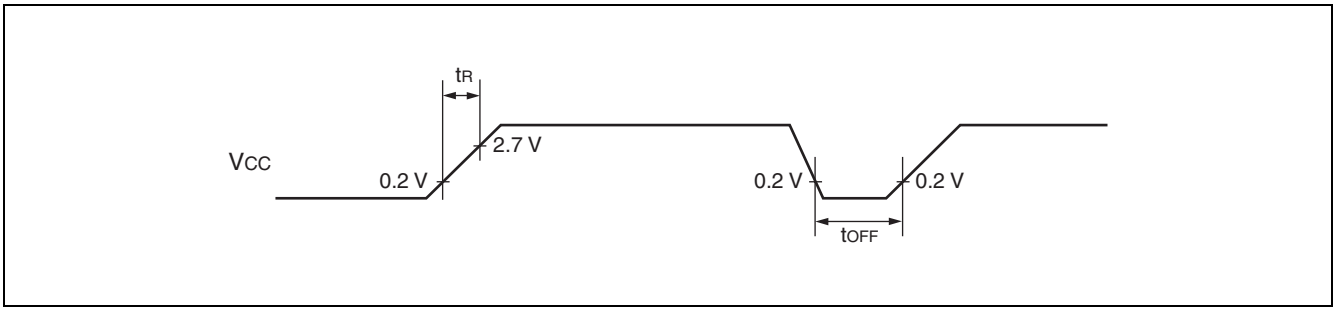


(3) Power-on Reset

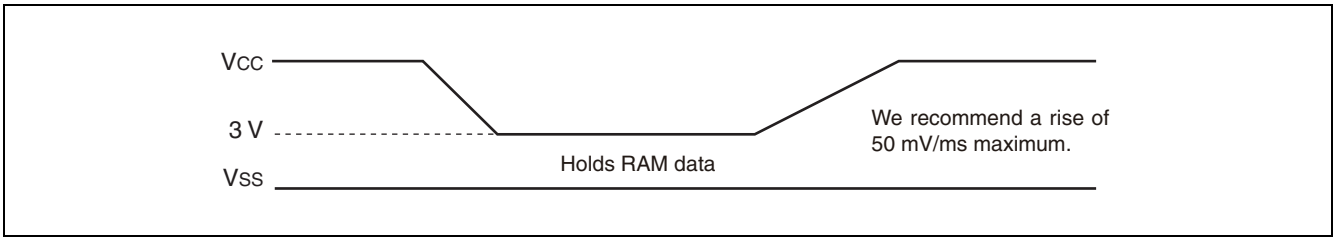
(T_A = –40 °C to +125 °C*, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Due to repetitive operation

*: If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.



Note : If you change the power supply voltage too rapidly, a power-on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



(4) LIN-UART0/1

- **Bit setting: ESCR0/1:SCES = 0, ECCR0/1:SCDE = 0**

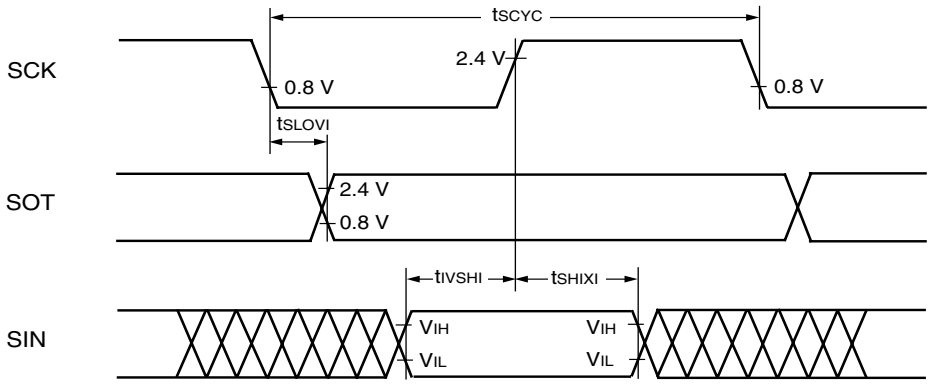
(T_A = –40 °C to +125 °C*, V_{CC} = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal shift clock mode output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0, SCK1, SOT0, SOT1		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0, SCK1, SIN0, SIN1		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0, SCK1, SIN0, SIN1		0	—	ns
Serial clock “L” pulse width	t_{SHSL}	SCK0, SCK1	External shift clock mode output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “H” pulse width	t_{SLSH}	SCK0, SCK1		t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0, SCK1, SOT0, SOT1		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0, SCK1, SIN0, SIN1		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SIN0, SIN1		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK0, SCK1		—	10	ns
SCK rise time	t_R	SCK0, SCK1		—	10	ns

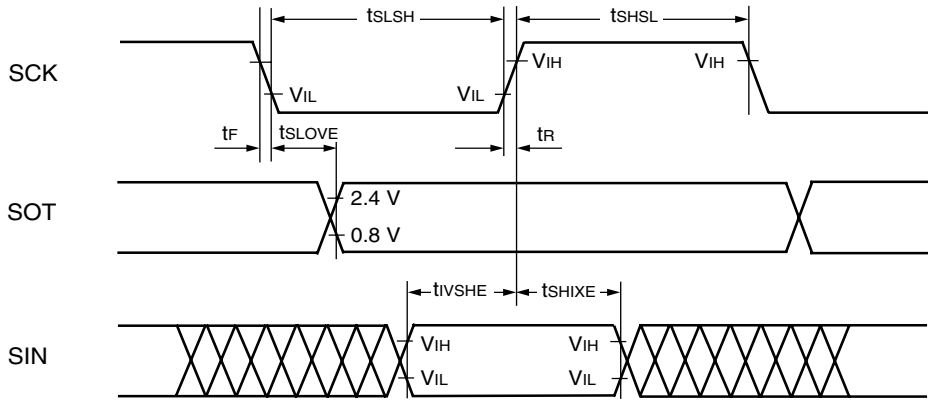
*: If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.

Notes : • AC characteristic in CLK synchronized mode.
• C_L is load capacity value of pins when testing.
• t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

• Internal Shift Clock Mode



• External Shift Clock Mode



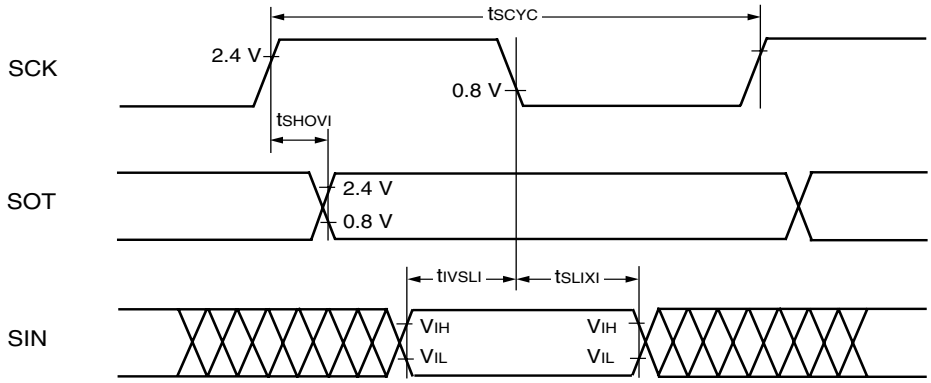
• **Bit setting: ESCR0/1:SCES = 1, ECCR0/1:SCDE = 0**

(T_A = –40 °C to +125 °C*, V_{CC} = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, V_{SS} = 0 V)

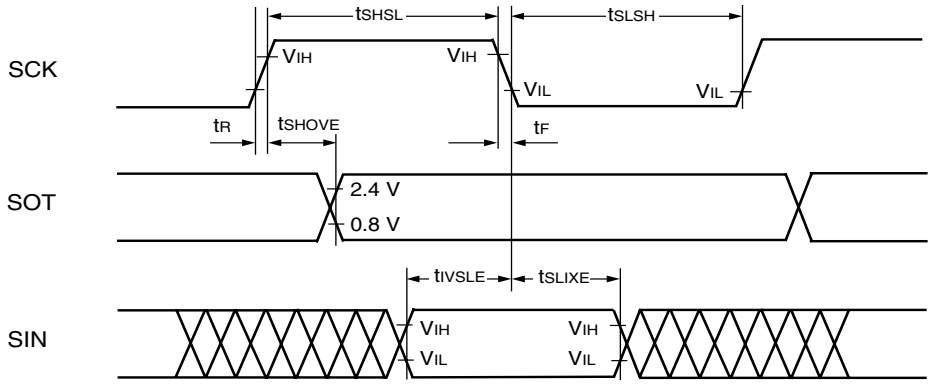
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal shift clock mode output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0, SCK1, SOT0, SOT1		–50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0, SCK1, SIN0, SIN1		t_{CP} + 80	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0, SCK1, SIN0, SIN1		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0, SCK1	External shift clock mode output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0, SCK1		t_{CP} + 10	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0, SCK1, SOT0, SOT1		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK0, SCK1, SIN0, SIN1		30	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXE}	SCK0, SCK1, SIN0, SIN1		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK0, SCK1		—	10	ns
SCK rise time	t_R	SCK0, SCK1		—	10	ns

* : If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.

• Internal Shift Clock Mode



• External Shift Clock Mode



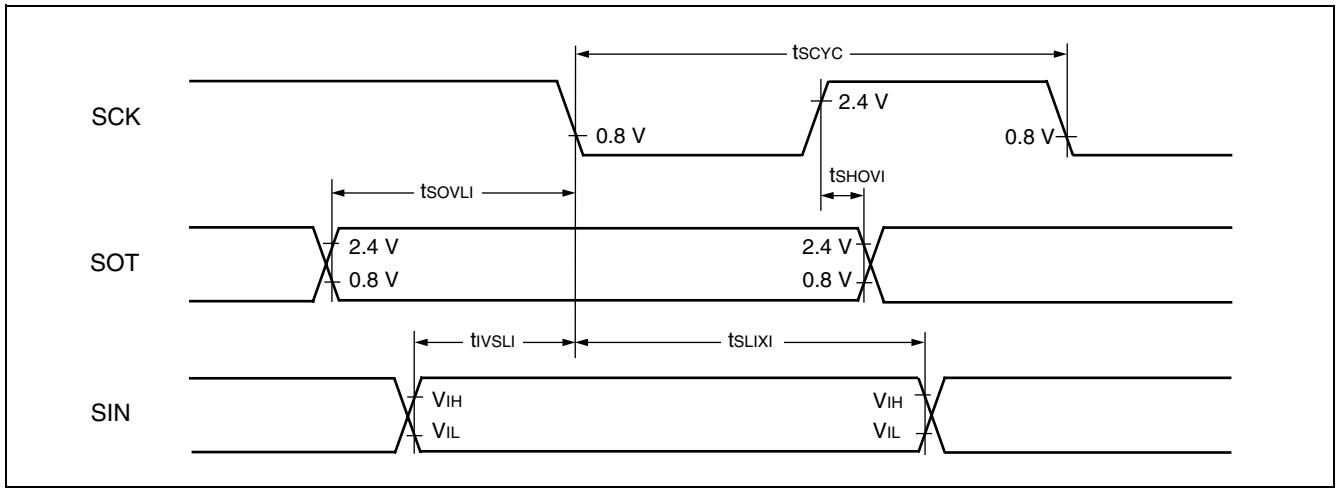
- **Bit setting: ESCR0/1:SCES = 0, ECCR0/1:SCDE = 1**

(T_A = –40 °C to +125 °C*, V_{CC} = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0,SCK1	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0,SCK1 SOT0,SOT1		–50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0,SCK1 SIN0,SIN1		t_{CP} + 80	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0,SCK1 SIN0,SIN1		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK0,SCK1 SOT0,SOT1		3 t_{CP} – 70	—	ns

* : If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.

Note : t_{CP} is the machine clock cycle time (Unit : ns) . Refer to " (1) Clock Timing" rating for t_{CP}.



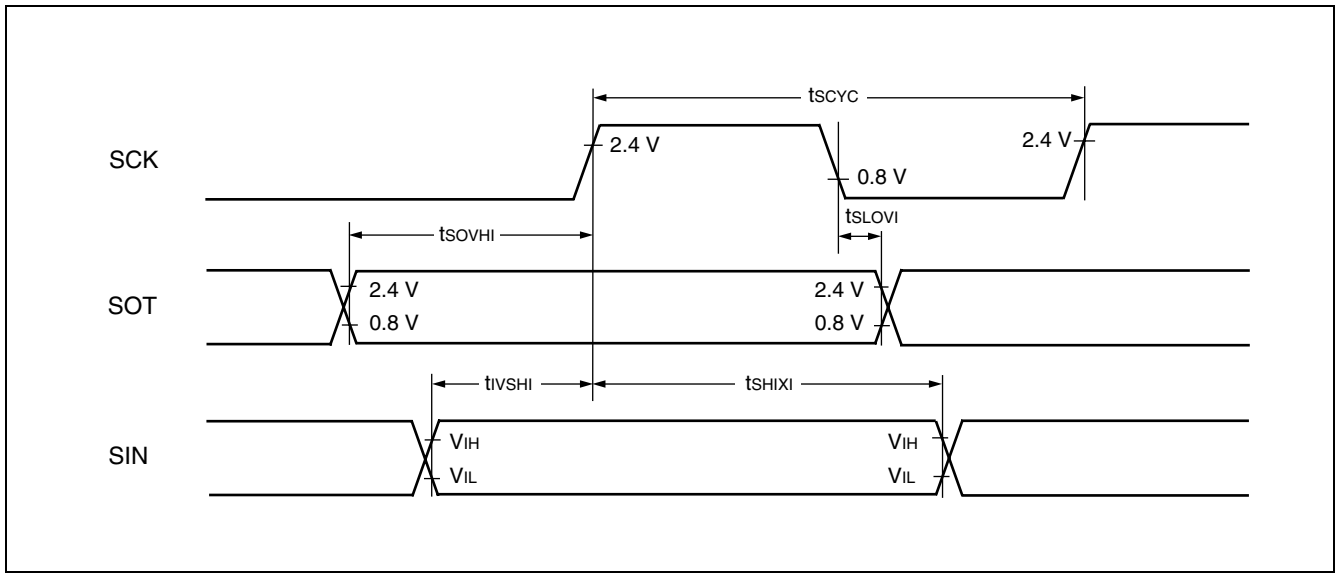
- **Bit setting: ESCR0/1:SCES = 1, ECCR0/1:SCDE = 1**

(T_A = –40 °C to +125 °C*, V_{CC} = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0,SCK1	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0,SCK1 SOT0,SOT1		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0,SCK1 SIN0,SIN1		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0,SCK1 SIN0,SIN1		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0,SCK1 SOT0,SOT1		3 t_{CP} – 70	—	ns

* : If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.

Note : t_{CP} is the machine clock cycle time (Unit : ns) . Refer to " (1) Clock Timing" rating for t_{CP}.



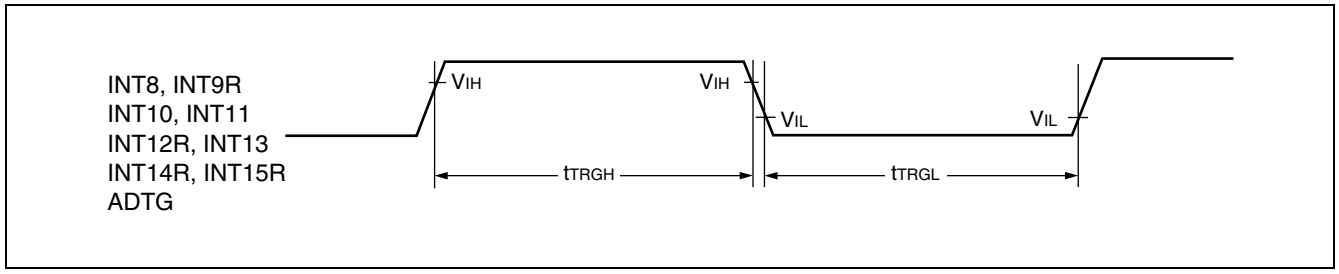
(5) Trigger Input Timing

(T_A = –40 °C to +125 °C*, V_{CC} = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8, INT9R INT10, INT11 INT12R, INT13 INT14R, INT15R	—	200	—	ns
		ADTG	—	t_{CP} + 200	—	ns

* : If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.

Note : t_{CP} is internal operating clock cycle time (machine clock) . Refer to " (1) Clock Timing".



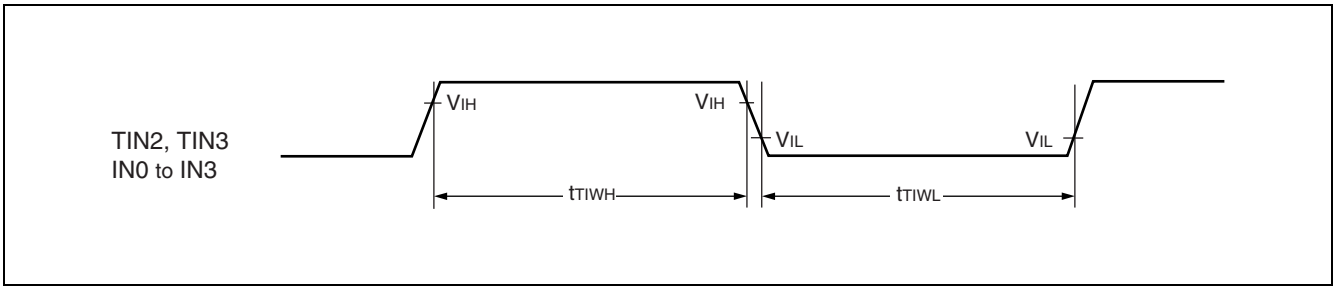
(6) Timer Related Resource Input Timing

(T_A = –40 °C to +125 °C*, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH}	TIN2, TIN3 IN0 to IN3	—	4 t_{CP}	—	ns
	t_{TIWL}					

* : If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.

Note : t_{CP} is internal operating clock cycle time (machine clock) . Refer to " (1) Clock Timing".

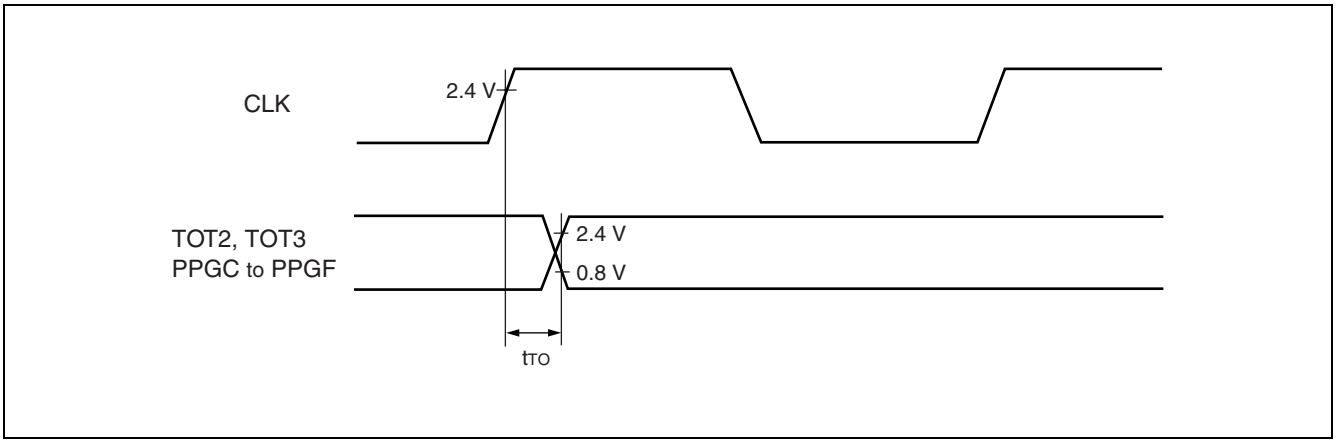


(7) Timer Related Resource Output Timing

(T_A = –40°C to +125 °C*, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT2, TOT3 PPGC to PPGF	—	30	—	ns

* : If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.



5. A/D Converter

(T_A = –40 °C to +125 °C*1, 3.0 V ≤ AVR – AV_{SS}, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN15	AV_{SS} – 1.5	AV_{SS} + 0.5	AV_{SS} + 2.5	LSB	
Full scale reading voltage	V_{FST}	AN0 to AN15	AVR – 3.5	AVR – 1.5	AVR + 0.5	LSB	
Compare time	—	—	1.0	—	16500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			2.0				4.0 V ≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	∞	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			1.2				4.0 V ≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN15	–0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	AN0 to AN15	AV_{SS}	—	AVR	V	
Reference voltage	—	AVR	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*2
Reference voltage supply current	I_R	AVR	—	600	900	µA	
	I_{RH}	AVR	—	—	5	µA	*2
Offset between input channels	—	AN0 to AN15	—	—	4	LSB	

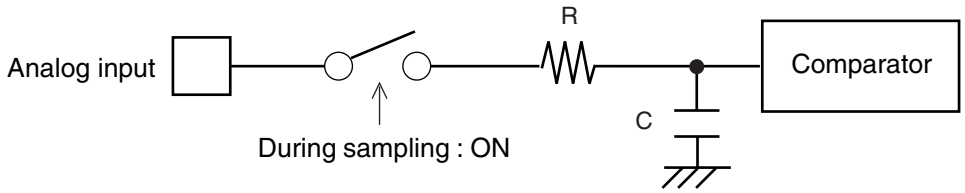
*1 : If used exceeding T_A = + 105 °C, please contact Fujitsu for reliability limitations.

*2 : If A/D converter is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVR = 5.0 V) .

(Continued)

- **About the external impedance of analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage changed to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



Part number	Analog input	R	C
MB90F962(S)	4.5 V ≤ AVcc ≤ 5.5 V	2.0 kΩ (Max)	16.0 pF (Max)
	4.0 V ≤ AVcc < 4.5 V	8.2 kΩ (Max)	16.0 pF (Max)
MB90V340E-101/V340-102	4.5 V ≤ AVcc ≤ 5.5 V	2.0 kΩ (Max)	14.4 pF (Max)
	4.0 V ≤ AVcc < 4.5 V	8.2 kΩ (Max)	14.4 pF (Max)

Note : The values are reference values.

Use the device with external circuits of the following output impedance for analog inputs:

- Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower (4.0 V ≤ AVcc ≤ 5.5 V, sampling period = 0.5 μs)
- If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors an on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.
- If the output impedance of an external circuit is too high, the sampling period for the analog voltage may be insufficient.
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

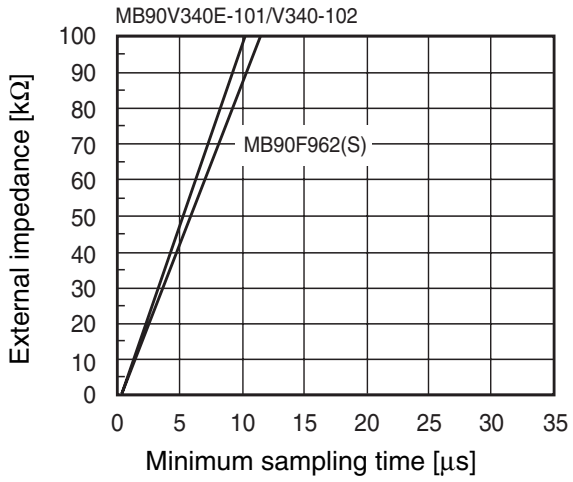
(Continued)

(Continued)

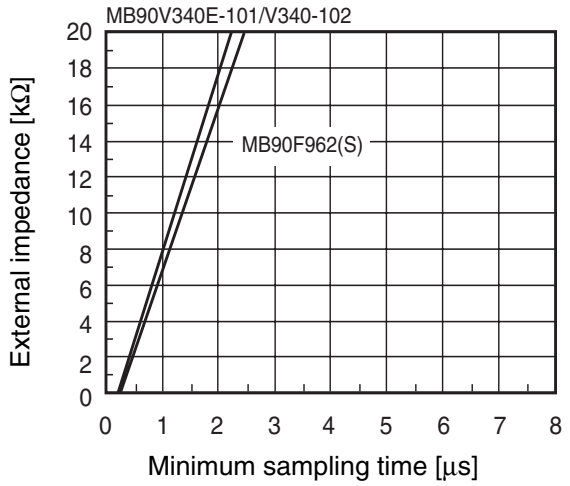
- The relationship between external impedance and minimum sampling time

  - At 4.5 V ≤ AV_{CC} ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)

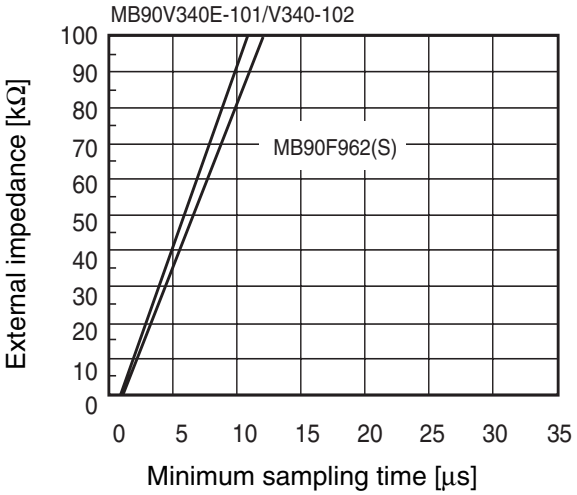


(External impedance = 0 kΩ to 20 kΩ)

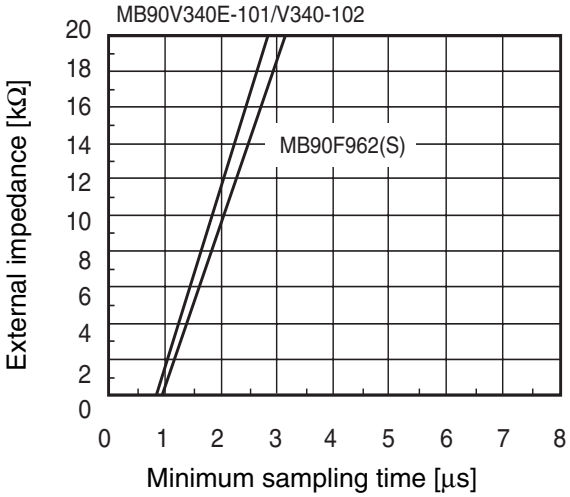


  - At 4.0 V ≤ AV_{CC} < 4.5 V

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



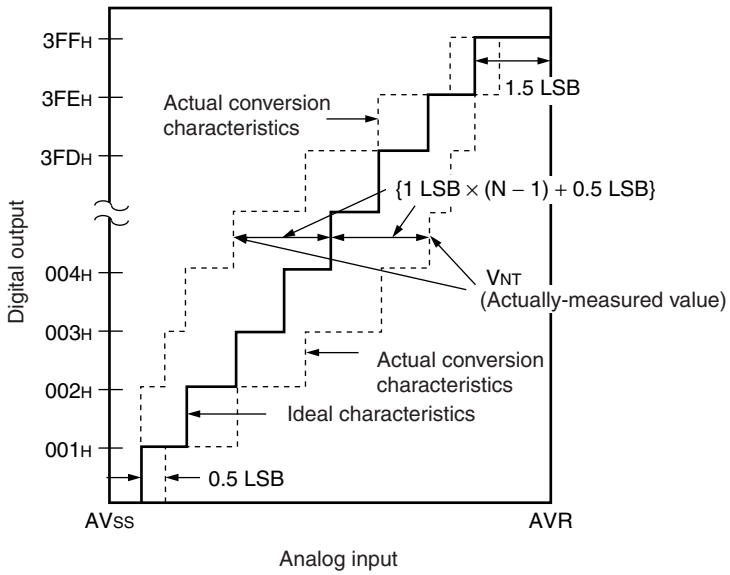
- **About errors**

  As | AVR – AV_{SS} | becomes smaller, values of relative errors grow larger.

6. Definition of A/D Converter Terms

Resolution	:	Analog variation that is recognized by an A/D converter.
Non linearity error	:	Deviation between a line across zero-transition line (“00 0000 0000$_B$” ← → “00 0000 0001$_B$”) and full-scale transition line (“11 1111 1110$_B$” ← → “11 1111 1111$_B$”) and actual conversion characteristics.
Differential linearity error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	:	Difference between an actual value and an theoretical value. A total error includes zero transition error, full-scale transition error, and linear error.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{AVR - AV_{SS}}{1024}\ [\text{V}]$$

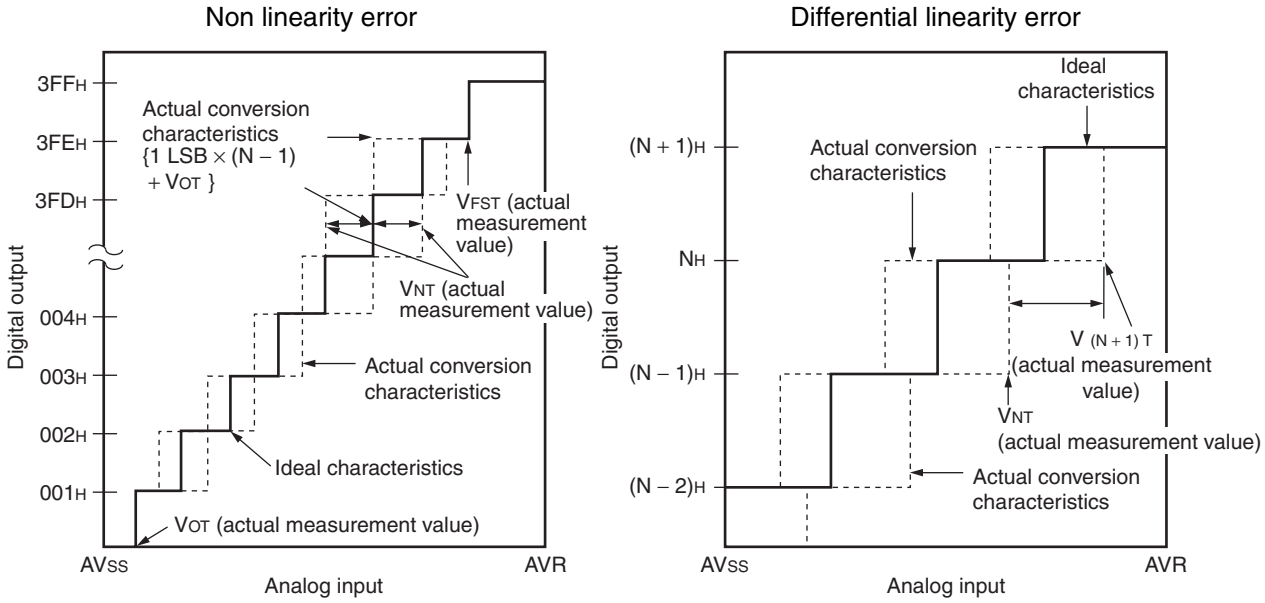
V_{OT} (Ideal value) $= AV_{SS} + 0.5$ LSB [V]

V_{FST} (Ideal value) $= AVR - 1.5$ LSB [V]

V_{NT} : A voltage at which digital output transits from $(N - 1)_H$ to N_H.

(Continued)

(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

7. Flash Memory Program/Erase Characteristics

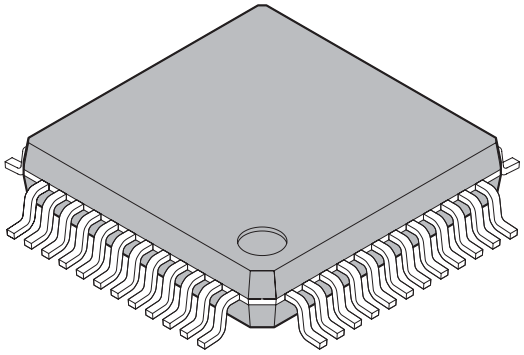
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (60 Kbytes)	T_A = +25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Sector erase time (4 Kbytes)		—	0.2	0.5	s	Excludes programming prior to erasure
Byte programming time		—	21	6100	µs	Except for the overhead time of the system level
Machine clock frequency f_{CP} at Flash programming/erasing	V_{CC} = 5.0 V	—	—	24	MHz	
Program/Erase cycle	—	10000	—	—	cycle	
Flash memory data retention time	Average T_A = +85 °C	20	—	—	year	*

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

■ ORDERING INFORMATION

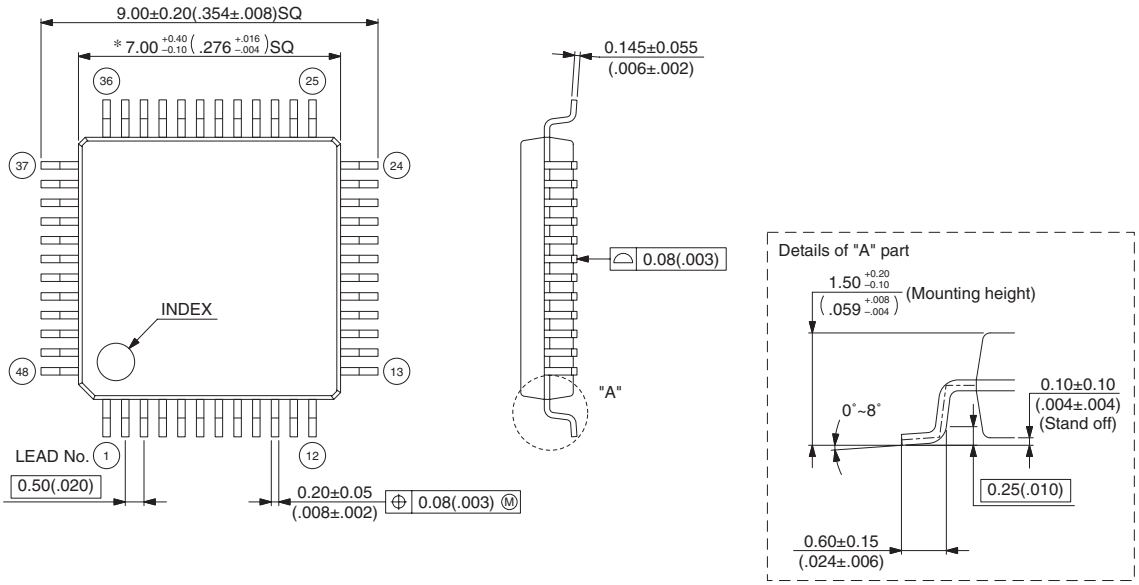
Part number	Package	Remarks
MB90F962PMT	48-pin plastic LQFP FPT-48P-M26 7 mm ❑, 0.50 mm pitch	Flash Memory Product (64Kbytes)
MB90F962SPMT		
MB90V340E-101	299-pin ceramic PGA PGA-299C-A01	Evaluation product
MB90V340E-102		

■ PACKAGE DIMENSION

48-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	7 × 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g
(FPT-48P-M26)	Code (Reference)	P-LFQFP48-7×7-0.50

48-pin plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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