# S25FL004K

## 4-Mbit CMOS 3.0 Volt Flash Memory with 104-MHz SPI (Serial Peripheral Interface) Multi I/O Bus

***Data Sheet*** *(Preliminary)*

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# S25FL004K

## 4-Mbit CMOS 3.0 Volt Flash Memory with 104-MHz SPI (Serial Peripheral Interface) Multi I/O Bus

***Data Sheet*** *(Preliminary)*

# Distinctive Characteristics

## Architectural Advantages

- **Single power supply operation**
  - Full voltage range: 2.7 to 3.6V read and write operations
- **Memory architecture**
  - Uniform 4 KB sectors
  - 256-byte page size
- **Program**
  - Page Program (up to 256 bytes) in 0.7 ms (typical)
  - Program operations are on a page by page basis
  - Quad Page Programming
- **Erase**
  - Bulk erase function
  - Uniform sector erase (4 KB)
  - Uniform block erase (32 KB and 64 KB)
  - Erase/Program Suspend and Resume
- **Cycling endurance**
  - 100,000 erase/program cycles typical
- **Data retention**
  - 20-year data retention typical
- **Process technology**
  - Manufactured on 0.09 µm process technology
- **Package option**
  - Industry Standard Pinouts
  - 8-pin SO package (208 mils)
  - 8-pin SO package (150 mils)

## Performance Characteristics

- **Speed**
  - Normal READ (Serial): 50 MHz clock rate
  - FAST_READ (Serial): 104 MHz clock rate (maximum)
  - 104 MHz Dual SPI/Quad SPI Clocks
  - 208/416 MHz equivalent Dual/Quad SPI
  - 50 MB/s continuous data transfer rate
- **Low Power Consumption**
  - 4 mA active current, <1 µA in Deep Power-down mode (typical)
  - Industrial temperature range (–40°C to +85°C)
- **Efficient "Continuous Read Mode"**
  - Low Instruction overhead
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Allows true XIP (execute in place) operation

## Memory Protection Features

- **Advanced security features**
  - Software and Hardware Write-Protect
  - Top/Bottom, 4 KB complement array protection
  - Power Supply Lock-Down and OTP protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Registers
  - 3x 256-Byte Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits

**Publication Number** S25FL004K_00 **Revision** 02 **Issue Date** October 18, 2010

# General Description

The S25FL004K (4-Mbit) Serial Flash memory provides an ideal storage solution for systems with limited space, pins and power. The device offers flexibility and performance well beyond ordinary Serial Flash devices. It is ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 4 mA active and 1 µA for deep power-down. All devices are offered in space-saving packages.

The S25FL004K array is organized into 2,048 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4 KB sector erase), groups of 128 (32 KB block erase), groups of 256 (64 KB block erase) or the entire chip (chip erase). The S25FL004K has 128 erasable sectors and 8 erasable blocks respectively. The small 4 KB sectors allow for greater flexibility in applications that require data and parameter storage.

The S25FL004K supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI: Serial Clock (CLK), Chip Select (CS#), Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#). SPI clock frequencies of up to 104 MHz are supported allowing equivalent clock rates of 208 MHz (104 MHz x 2) for Dual I/O and 416 MHz (104 MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique Serial Number.

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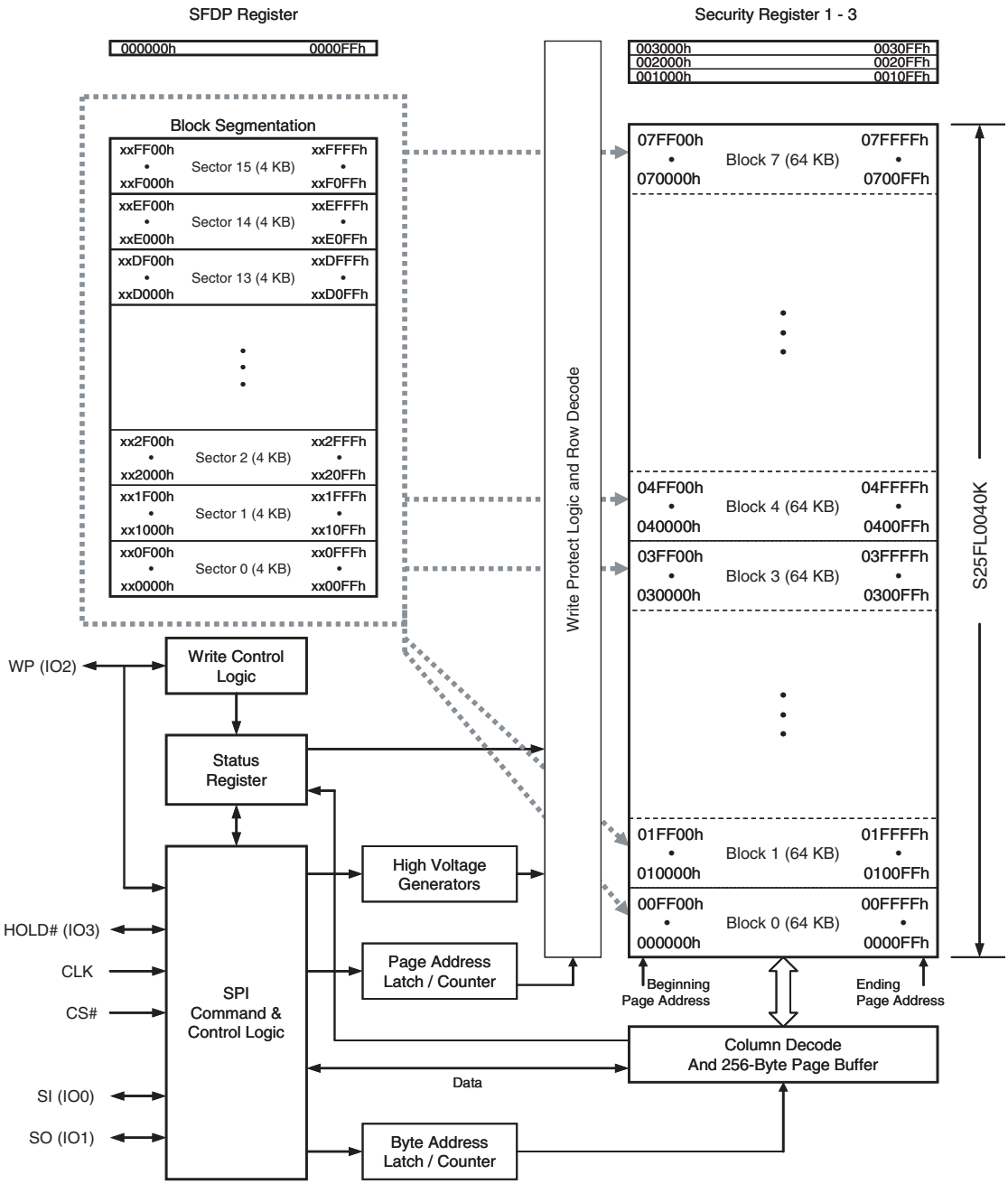
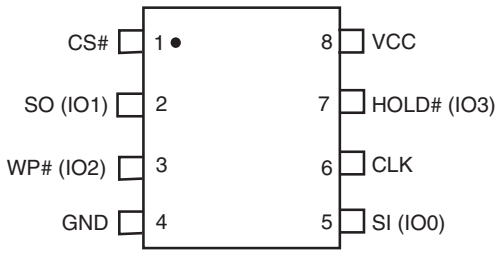
# Tables

# 1. Block Diagram



# 2. Connection Diagrams

**Figure 2.1** 8-pin Plastic Small Outline Package (SO)




# 3. Input/Output Descriptions

**Table 3.1** 8-pin SOIC 150-mil/208-mil

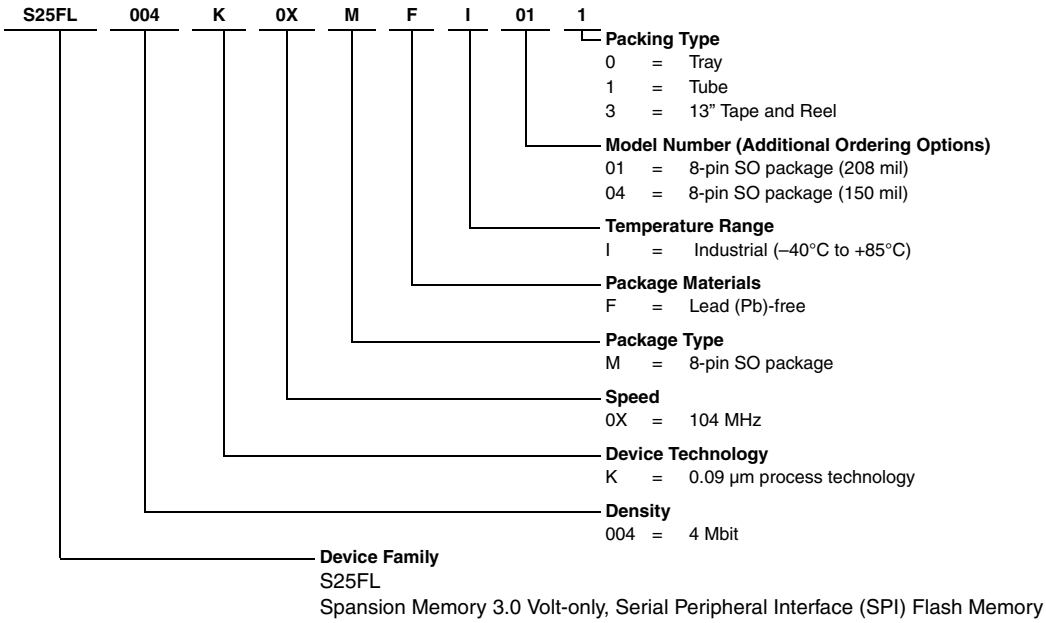
| Pin No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | CS# | I | Chip Select Input |
| 2 | SO (IO1) | I/O | Data Output (Data Input Output 1) (1) |
| 3 | WP# (IO2) | I/O | Write Protect Input (Data Input Output 2) (2) |
| 4 | GND | | Ground |
| 5 | SI (IO0) | I/O | Data Input (Data Input Output 0) (1) |
| 6 | CLK | I | Serial Clock Input |
| 7 | HOLD# (IO3) | I/O | Hold Input (Data Input Output 3) (2) |
| 8 | VCC | | Power Supply |

***Notes:***

1. *IO0 and IO1 are used for Standard and Dual SPI instructions.*
2. *IO0 – IO3 are used for Quad SPI instructions.*

# 4. Ordering Information

The ordering part number is formed by a valid combination of the following:




## 4.1 Valid Combinations

Table 4.1 lists the valid combinations configurations planned to be supported in volume for this device.

**Table 4.1** S25FL004K Valid Combinations

| S25FL004K Valid Combinations | | | | | |
|---|---|---|---|---|---|
| **Base Ordering Part Number** | **Speed Option** | **Package & Temperature** | **Model Number** | **Packing Type** | **Package Marking** |
| S25FL004K | 0X | MFI | 01, 04 | 0, 1, 3 | FL004KIF |

# 5. Functional Description

## 5.1 SPI Operations

### 5.1.1 Standard SPI Instructions

The S25FL004K is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI instructions use the SI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The SO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

### 5.1.2 Dual SPI Instructions

The S25FL004K supports Dual SPI operation when using the “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)” instructions. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

### 5.1.3 Quad SPI Instructions

The S25FL004K supports Quad SPI operation when using the “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)”, “Word Read Quad I/O (E7h)” and “Octal Word Read Quad I/O (E3h)” instructions. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the SI and SO pins become bidirectional IO0 and IO1, and the WP# and HOLD# pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

### 5.1.4 Hold Function

For Standard SPI and Dual SPI operations, the HOLD# signal allows the S25FL004K operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The HOLD# function is only available for standard SPI and Dual SPI operation, not during Quad SPI.

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will terminate after the next falling edge of CLK. During a HOLD# condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device.

## 5.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the S25FL004K provides several means to protect the data from inadvertent writes.

### 5.2.1 Write Protect Features

- Device resets when $V_{CC}$ is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (WP# pin) write protection using Status Register
- Write Protection using Deep Power-down instruction
- Lock Down write protection until next power-up
- One Time Program (OTP) write protection

Upon power-up or at power-down, the S25FL004K will maintain a reset condition while $V_{CC}$ is below the threshold value of VWI, (see Figure 8.1, *Power-up Timing and Voltage Levels on page 53*). While reset, all operations are disabled and no instructions are recognized. During power-up and after the $V_{CC}$ voltage exceeds VWI, all program and erase related instructions are further disabled for a time delay of $t_{PUW}$. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (CS#) must track the $V_{CC}$ supply level at power-up until the $V_{CC}$-min level and $t_{VSL}$ time delay is reached. If needed a pull-up resistor on CS# can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, SEC,TB, BP2, BP1 and BP0) bits. These settings allow a portion as small as 4 KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See *Status Register on page 13.* for further information. Additionally, the Deep Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release from Deep Power-down instruction.

# 6. Control and Status Registers

The Read Status Register-1 and Status Register-2 instructions can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status and Erase/Program Suspend status. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting and Security Register OTP lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and during Standard/Dual SPI operations, the WP# pin.

## 6.1 Status Register

### 6.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see $t_W$, $t_{PP}$, $t_{SE}$, $t_{BE}$, and $t_{CE}$ in Section 8.6, *AC Electrical Characteristics on page 54*). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

### 6.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

### 6.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see $t_W$ in *AC Electrical Characteristics on page 54*). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Table 6.2 on page 15). The factory default setting for the Block Protection Bits is 0 (none of the array is protected.)

### 6.1.4 Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Table 6.1, *Status Register Protection Bits on page 14*. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

### 6.1.5 Sector/Block Protect (SEC)

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4 KB Sectors (SEC=1) or 64 KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in Table 6.1. The default setting is SEC=0.

### 6.1.6 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4 KB sector can be protected while the rest of the array is not; when CMP=1, the top 4 KB sector will become unprotected while the rest of the array become read-only. Please refer to Table 6.1 for details. The default setting is CMP=0.

### 6.1.7 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

**Table 6.1** Status Register Protection Bits

| SRP1 | SRP0 | WP# | Status Register | Description |
|---|---|---|---|---|
| 0 | 0 | X | Software Protection | WP# pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default] |
| 0 | 1 | 0 | Hardware Protected | When WP# pin is low the Status Register locked and can not be written to. |
| 0 | 1 | 1 | Hardware Unprotected | When WP# pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1. |
| 1 | 0 | X | Power Supply Lock-Down | Status Register is protected and can not be written to again until the next power-down, power-up cycle. (1) |
| 1 | 1 | X | One Time Program (2) | Status Register is permanently protected and can not be written to. |

***Notes:***

1. *When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.*
2. *This feature is available upon special order. Please contact Spansion for details.*

### 6.1.8 Erase/Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

### 6.1.9 Security Register Lock Bits (LB3, LB2, LB1)

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB[3:1] is 0, Security Registers are unlocked. LB[3:1] can be set to 1 individually using the Write Status Register instruction. LB[3:1] are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

### 6.1.10 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default), the WP# pin and HOLD# are enabled. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and WP# and HOLD# functions are disabled.

**Note**: If the WP# or HOLD# pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

**Figure 6.1** Status Register 1

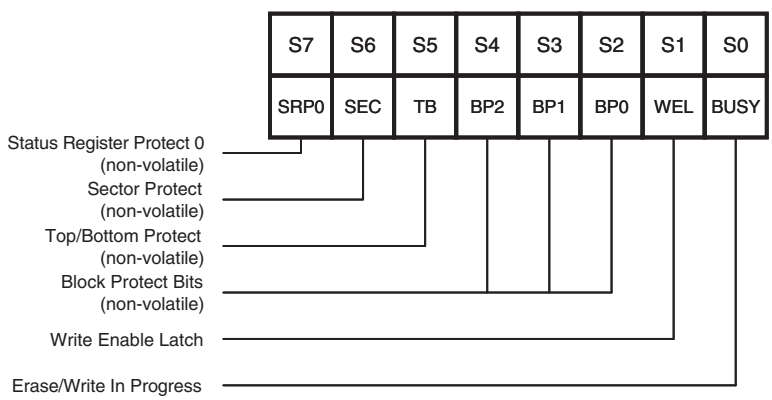


**Figure 6.2** Status Register 2

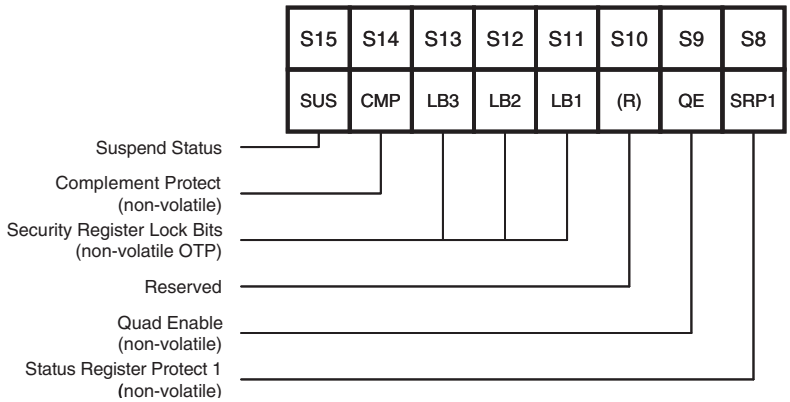



**Table 6.2** Status Register Memory Protection (CMP = 0)

| Status Register (1) | | | | | S25FL004K (4 MBit) Memory Protection (2) | | | |
|---|---|---|---|---|---|---|---|---|
| **SEC** | **TB** | **BP2** | **BP1** | **BP0** | **Block(s)** | **Addresses** | **Density** | **Portion** |
| X | X | 0 | 0 | 0 | None | None | None | None |
| 0 | 0 | 0 | 0 | 1 | 7 | 070000h – 07FFFFh | 64 KB | Upper 1/8 |
| 0 | 0 | 0 | 1 | 0 | 6 and 7 | 060000h – 07FFFFh | 128 KB | Upper 1/4 |
| 0 | 0 | 0 | 1 | 1 | 4 thru 7 | 040000h – 07FFFFh | 256 KB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 | 000000h – 00FFFFh | 64 KB | Lower 1/8 |
| 0 | 1 | 0 | 1 | 0 | 0 and 1 | 000000h – 01FFFFh | 128 KB | Lower 1/4 |
| 0 | 1 | 0 | 1 | 1 | 0 thru 3 | 000000h – 03FFFFh | 256 KB | Lower 1/2 |
| 0 | X | 1 | X | X | 0 thru 7 | 000000h – 07FFFFh | 512 KB | All |
| 1 | 0 | 0 | 0 | 1 | 7 | 07F000h – 07FFFFh | 4 KB | Upper 1/128 |
| 1 | 0 | 0 | 1 | 0 | 7 | 07E000h – 07FFFFh | 8 KB | Upper 1/64 |
| 1 | 0 | 0 | 1 | 1 | 7 | 07C000h – 07FFFFh | 16 KB | Upper 1/32 |
| 1 | 0 | 1 | 0 | X | 7 | 078000h – 07FFFFh | 32 KB | Upper 1/16 |
| 1 | 0 | 1 | 1 | 0 | 7 | 078000h – 07FFFFh | 32 KB | Upper 1/16 |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000h – 000FFFh | 4 KB | Lower 1/128 |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000h – 001FFFh | 8 KB | Lower 1/64 |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000h – 003FFFh | 16 KB | Lower 1/32 |
| 1 | 1 | 1 | 0 | X | 0 | 000000h – 007FFFh | 32 KB | Lower 1/16 |
| 1 | 1 | 1 | 1 | 0 | 0 | 000000h – 007FFFh | 32 KB | Lower 1/16 |
| 1 | X | 1 | 1 | 1 | 0 thru 7 | 000000h – 07FFFFh | 512 KB | All |

***Notes:***

1. *X = don't care*
2. *If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.*

**Table 6.3** Status Register Memory Protection (CMP = 1)

| Status Register (1) | | | | | S25FL004K (4 MBit) Memory Protection (2) | | | |
|---|---|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | Block(s) | Addresses | Density | Portion |
| X | X | 0 | 0 | 0 | 0 thru 7 | 000000h – 07FFFFh | 512 KB | All |
| 0 | 0 | 0 | 0 | 1 | 0 thru 6 | 000000h – 06FFFFh | 448 KB | Lower 7/8 |
| 0 | 0 | 0 | 1 | 0 | 0 thru 5 | 000000h – 05FFFFh | 384 KB | Lower 3/4 |
| 0 | 0 | 0 | 1 | 1 | 0 thru 3 | 000000h – 03FFFFh | 256 KB | Lower 1/2 |
| 0 | 1 | 0 | 0 | 1 | 1 thru 7 | 010000h – 07FFFFh | 448 KB | Upper 7/8 |
| 0 | 1 | 0 | 1 | 0 | 2 thru 7 | 020000h – 07FFFFh | 384 KB | Upper 3/4 |
| 0 | 1 | 0 | 1 | 1 | 4 thru 7 | 040000h – 07FFFFh | 256 KB | Upper 1/2 |
| 1 | 0 | 0 | 0 | 1 | 0 thru 7 | 000000h – 07EFFFh | 508 KB | Lower 127/128 |
| 1 | 0 | 0 | 1 | 0 | 0 thru 7 | 000000h – 07DFFFh | 504 KB | Lower 63/64 |
| 1 | 0 | 0 | 1 | 1 | 0 thru 7 | 000000h – 07BFFFh | 496 KB | Lower 31/32 |
| 1 | 0 | 1 | 0 | X | 0 thru 7 | 000000h – 077FFFh | 480 KB | Lower 15/16 |
| 1 | 0 | 1 | 1 | 0 | 0 thru 7 | 000000h – 077FFFh | 480 KB | Lower 15/16 |
| 1 | 1 | 0 | 0 | 1 | 0 thru 7 | 001000h – 07FFFFh | 508 KB | Upper 127/128 |
| 1 | 1 | 0 | 1 | 0 | 0 thru 7 | 002000h – 07FFFFh | 504 KB | Upper 63/64 |
| 1 | 1 | 0 | 1 | 1 | 0 thru 7 | 004000h – 07FFFFh | 496 KB | Upper 31/32 |
| 1 | 1 | 1 | 0 | X | 0 thru 7 | 008000h – 07FFFFh | 480 KB | Upper 15/16 |
| 1 | 1 | 1 | 1 | 0 | 0 thru 7 | 008000h – 07FFFFh | 480 KB | Upper 15/16 |
| X | X | 1 | 1 | 1 | None | None | None | None |

***Notes:***
1. *X = don't care*
2. *If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.*

# 7. Instructions

The instruction set of the S25FL004K consists of thirty five basic instructions that are fully controlled through the SPI bus (see Table 7.3 to Table 7.5 on page 19). Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the SI input provides the instruction code. Data on the SI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge CS#. Clock relative timing diagrams for each instruction are included in the figures below. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

**Table 7.1** Manufacturer Identification

| Manufacturer ID | Value |
|---|---|
| (MF7-MF0) | EFh |

**Table 7.2** Device Identification

| Device ID | Instruction | Value |
|---|---|---|
| (ID7-ID0) | ABh, 90h, 92h, 94h | 12h |
| (ID15-ID0) | 9Fh | 4013h |

**Table 7.3** Instruction Set (Erase, Program Instructions (1))

| Instruction Name | BYTE 1 (CODE) | BYTE 2 | BYTE 3 | BYTE 4 | BYTE 5 | BYTE 6 |
|---|---|---|---|---|---|---|
| Write Enable | 06h | | | | | |
| Write Enable for Volatile Status Register | 50h | | | | | |
| Write Disable | 04h | | | | | |
| Read Status Register-1 | 05h | (S7–S0) (2) | | | | |
| Read Status Register-2 | 35h | (S15–S8) (2) | | | | |
| Write Status Register | 01h | (S7–S0) | (S15–S8) | | | |
| Page Program | 02h | A23–A16 | A15–A8 | A7–A0 | (D7–D0) | |
| Quad Page Program | 32h | A23–A16 | A15–A8 | A7–A0 | (D7–D0, …) (3) | |
| Sector Erase (4 KB) | 20h | A23–A16 | A15–A8 | A7–A0 | | |
| Block Erase (32 KB) | 52h | A23–A16 | A15–A8 | A7–A0 | | |
| Block Erase (64 KB) | D8h | A23–A16 | A15–A8 | A7–A0 | | |
| Chip Erase | C7h/60h | | | | | |
| Erase / Program Suspend | 75h | | | | | |
| Erase / Program Resume | 7Ah | | | | | |
| Power-down | B9h | | | | | |
| Continuous Read Mode Reset (4) | FFh | FFh | | | | |

***Notes:***

1. *Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data being read from the device on the SO pin.*
2. *The Status Register contents will repeat continuously until CS# terminates the instruction.*
3. *Quad Page Program Input Data: IO0 = (D4, D0, ……) IO1 = (D5, D1, ……) IO2 = (D6, D2, ……) IO3 = (D7, D3, ……)*
4. *This instruction is recommended when using the Dual or Quad "Continuous Read Mode" feature. See Section 7.0.15 and Section 7.0.16 on page 33 for more information.*

**Table 7.4** Instruction Set (Read Instructions)

| Instruction Name | BYTE 1 (CODE) | BYTE 2 | BYTE 3 | BYTE 4 | BYTE 5 | BYTE 6 |
|---|---|---|---|---|---|---|
| Read Data | 03h | A23–A16 | A15–A8 | A7–A0 | (D7–D0) | |
| Fast Read | 0Bh | A23–A16 | A15–A8 | A7–A0 | dummy | (D7–D0) |
| Fast Read Dual Output | 3Bh | A23–A16 | A15–A8 | A7–A0 | dummy | (D7–D0, …) (1) |
| Fast Read Quad Output | 6Bh | A23–A16 | A15–A8 | A7–A0 | dummy | (D7–D0, …) (3) |
| Fast Read Dual I/O | BBh | A23–A8 (2) | A7–A0, M7–M0 (2) | (D7–D0, …) (1) | | |
| Fast Read Quad I/O | EBh | A23–A0, M7–M0 (4) | (x,x,x,x, D7–D0, …) (5) | (D7–D0, …) (3) | | |
| Word Read Quad I/O (7) | E7h | A23–A0, M7–M0 (4) | (x,x, D7–D0, …) (6) | (D7–D0, …) (3) | | |
| Octal Word Read Quad I/O (8) | E3h | A23–A0, M7–M0 (4) | (D7–D0, …) (3) | | | |
| Set Burst with Wrap | 77h | xxxxxx, W6–W4 (4) | | | | |

***Notes:***

1. *Dual Output data*
   *IO0 = (D6, D4, D2, D0)*
   *IO1 = (D7, D5, D3, D1)*
2. *Dual Input Address*
   *IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0*
   *IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1*
3. *Quad Output Data*
   *IO0 = (D4, D0, …..)*
   *IO1 = (D5, D1, …..)*
   *IO2 = (D6, D2, …..)*
   *IO3 = (D7, D3, …..)*
4. *Quad Input Address*
   *IO0 = A20, A16, A12, A8, A4, A0, M4, M0*
   *IO1 = A21, A17, A13, A9, A5, A1, M5, M1*
   *IO2 = A22, A18, A14, A10, A6, A2, M6, M2*
   *IO3 = A23, A19, A15, A11, A7, A3, M7, M3*

   *Set Burst with Wrap Input*
   *IO0 = x, x, x, x, x, x, W4, x*
   *IO1 = x, x, x, x, x, x, W5, x*
   *IO2 = x, x, x, x, x, x, W6 x*
   *IO3 = x, x, x, x, x, x, x, x*
5. *Fast Read Quad I/O Data*
   *IO0 = (x, x, x, x, D4, D0, …..)*
   *IO1 = (x, x, x, x, D5, D1, …..)*
   *IO2 = (x, x, x, x, D6, D2, …..)*
   *IO3 = (x, x, x, x, D7, D3, …..)*
6. *Word Read Quad I/O Data*
   *IO0 = (x, x, D4, D0, …..)*
   *IO1 = (x, x, D5, D1, …..)*
   *IO2 = (x, x, D6, D2, …..)*
   *IO3 = (x, x, D7, D3, …..)*
7. *The lowest address bit must be 0. (A0 = 0)*
8. *The lowest 4 address bits must be 0. (A0, A1, A2, A3 = 0)*

**Table 7.5** Instruction Set (ID, Security Instructions)

| Instruction Name | BYTE 1 (CODE) | BYTE 2 | BYTE 3 | BYTE 4 | BYTE 5 | BYTE 6 |
|---|---|---|---|---|---|---|
| Release Power down / Device ID | ABh | dummy | dummy | dummy | (ID7-ID0) (1) | |
| Manufacturer/ Device ID (2) | 90h | dummy | dummy | 00h | (MF7-MF0) | (ID7-ID0) |
| Manufacturer/Device ID by Dual I/O | 92h | A23-A8 | A7-A0, M[7:0] | (MF[7:0], ID[7:0]) | | |
| Manufacture/Device ID by Quad I/O | 94h | A23-A0, M[7:0] | xxxx, (MF[7:0], ID[7:0]) | (MF[7:0], ID[7:0], …) | | |
| JEDEC ID | 9Fh | (MF7-MF0) Manufacturer | (ID15-ID8) Memory Type | (ID7-ID0) Capacity | | |
| Read Unique ID | 4Bh | dummy | dummy | dummy | dummy | (ID63-ID0) |
| Read SFDP Register | 48h, 5Ah | 00h | 00h | A7-A0 | dummy | (D7-0) |
| Erase Security Registers (3) | 44h | A23-A16 | A15-A8 | A7-A0 | | |
| Program Security Registers (3) | 42h | A23-A16 | A15-A8 | A7-A0 | (D7-0) | (D7-0) |
| Read Security Registers (3) | 48h | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-0) |

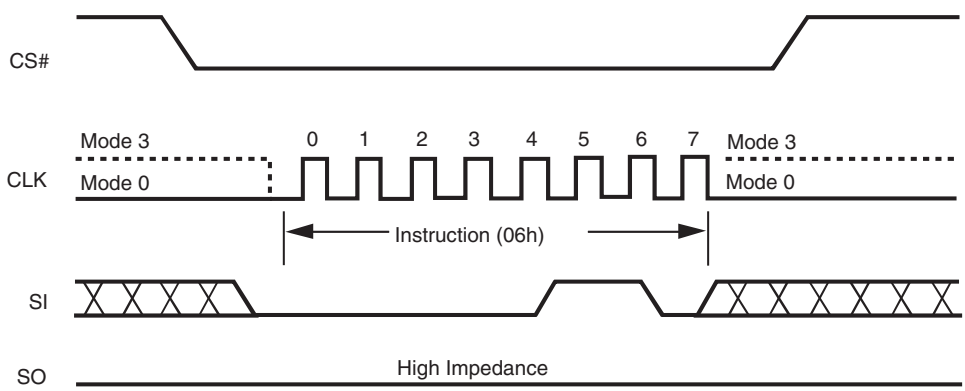
***Notes:***

1. *The Device ID will repeat continuously until CS# terminates the instruction.*
2. *See Manufacturer and Device Identification table for Device ID information.*
3. *Security Register Address:*
   *Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address*
   *Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address*
   *Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address*

## 7.0.1 Write Enable (06h)

The Write Enable instruction (Figure 7.1) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving CS# low, shifting the instruction code “06h” into the Data Input (SI) pin on the rising edge of CLK, and then driving CS# high.

**Figure 7.1** Write Enable Instruction Sequence Diagram

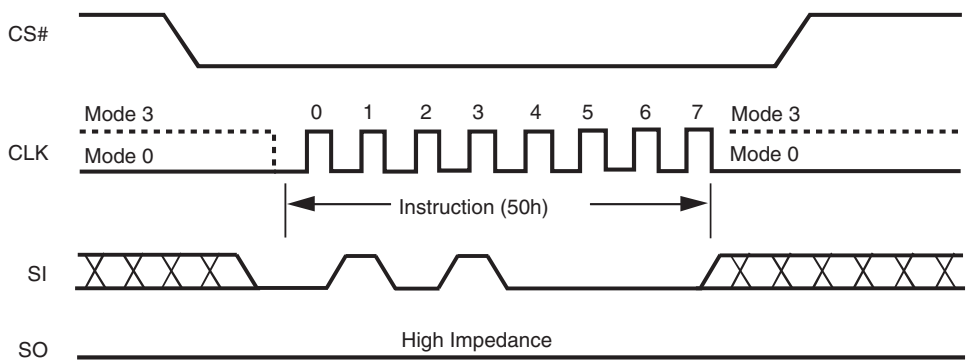



## 7.0.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in Section 6.1, *Status Register on page 13* can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for

Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 7.2) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

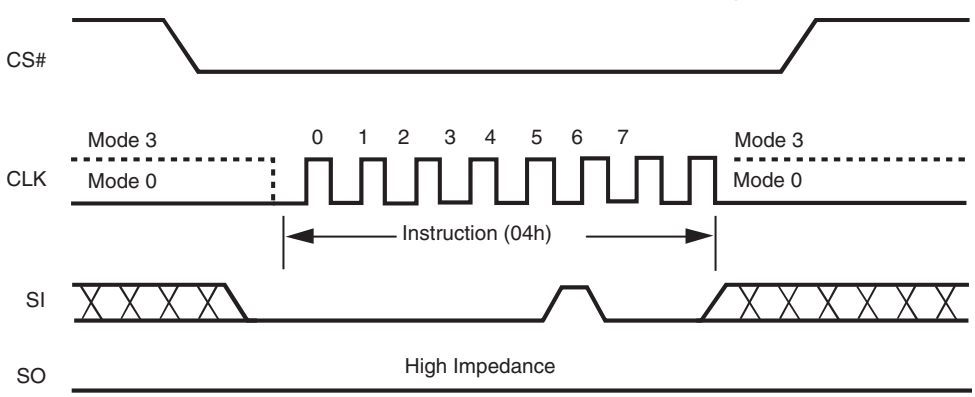
**Figure 7.2** Write Enable for Volatile Status Register Instruction Sequence Diagram




## 7.0.3 Write Disable (04h)

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving CS# low, shifting the instruction code “04h” into the SI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase and Chip Erase instructions.

**Figure 7.3** Write Disable Instruction Sequence Diagram



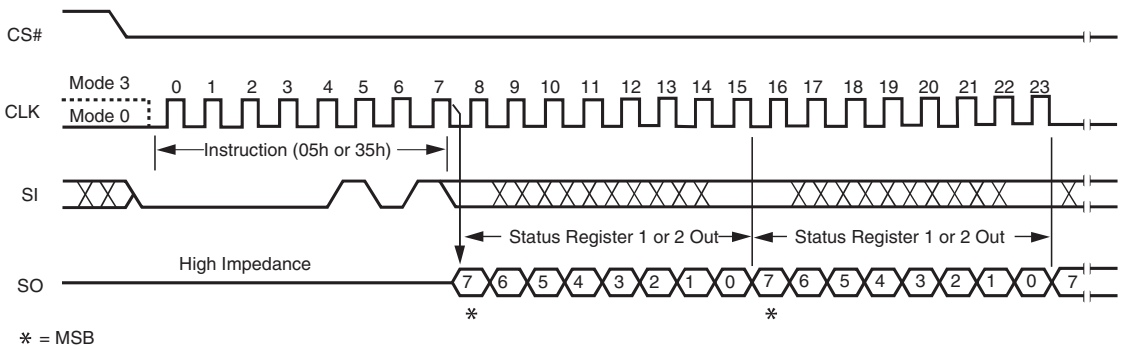

## 7.0.4 Read Status Register-1 (05h) and Read Status Register-2 (35h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving CS# low and shifting the instruction code “05h” for Status Register-1 or “35h” for Status Register-2 into the SI pin on the rising edge of CLK. The status register bits are then shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.4. The Status Register bits are shown in Figure 6.1 and Figure 6.2 and include the BUSY, WEL, BP2-BP0, TB, SEC, SRP0, SRP1, QE, LB3-1, CMP and SUS bits (see Section 6.1, *Status Register on page 13*).

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is

complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 7.4. The instruction is completed by driving CS# high.

**Figure 7.4** Read Status Register Instruction Sequence Diagram




## 7.0.5 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. Only non-volatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7 thru 2 of Status Register-1) and CMP, LB3, LB2, LB1, QE, SRP1 (bits 14 thru 8 of Status Register-2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB3-1 are non-volatile OTP bits; once each is set to 1, it can not be cleared to 0. The Status Register bits are shown in Figure 6.1 and Figure 6.2 on page 15, and described Section 6.1, *Status Register on page 13*.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in Figure 7.5.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRP1 and LB3, LB2, LB1 can not be changed from “1” to “0” because of the OTP protection for these bits. Upon power off, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored when power on again.

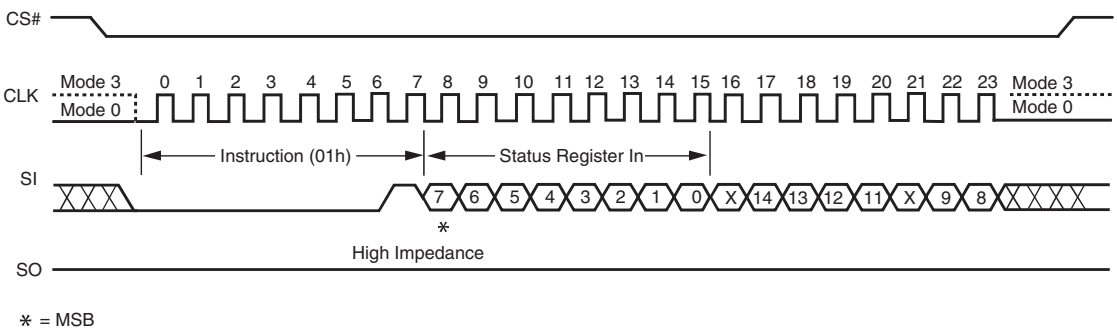
To complete the Write Status Register instruction, the CS# pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done the Write Status Register instruction will not be executed. If CS# is driven high after the eighth clock the CMP, QE and SRP1 bits will be cleared to 0.

During non-volatile Status Register write operation (06h combined with 01h), after CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of $t_W$ (see Section 8.6, *AC Electrical Characteristics on page 54*). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h), after CS# is driven high, the Status Register bits will be refreshed to the new values within the time period of $t_{SHSL2}$ (see Section 8.6, *AC Electrical Characteristics on page 54*). BUSY bit will remain 0 during the Status Register bit refresh period.

Refer to Section 6.1, *Status Register on page 13* for detailed Status Register Bit descriptions. Factory default for all status Register bits are 0.

**Figure 7.5** Write Status Register Instruction Sequence Diagram

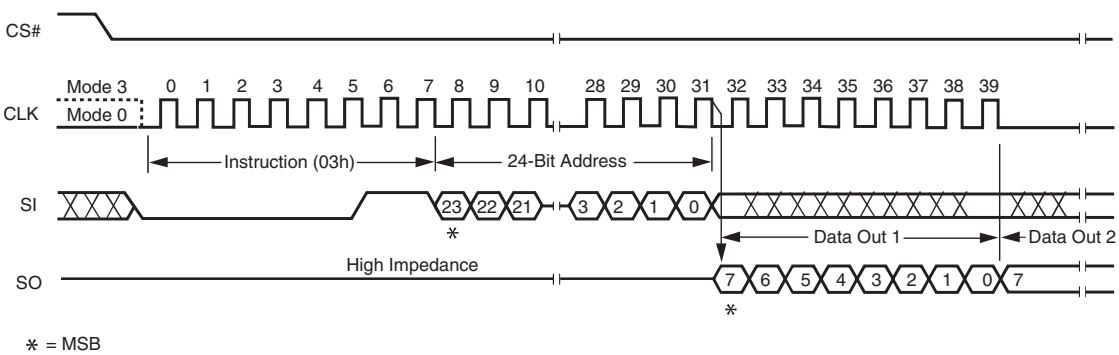



## 7.0.6 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the SI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

The Read Data instruction sequence is shown in Figure 7.6. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from DC to a maximum of $f_R$ (see See *AC Electrical Characteristics on page 54.*).

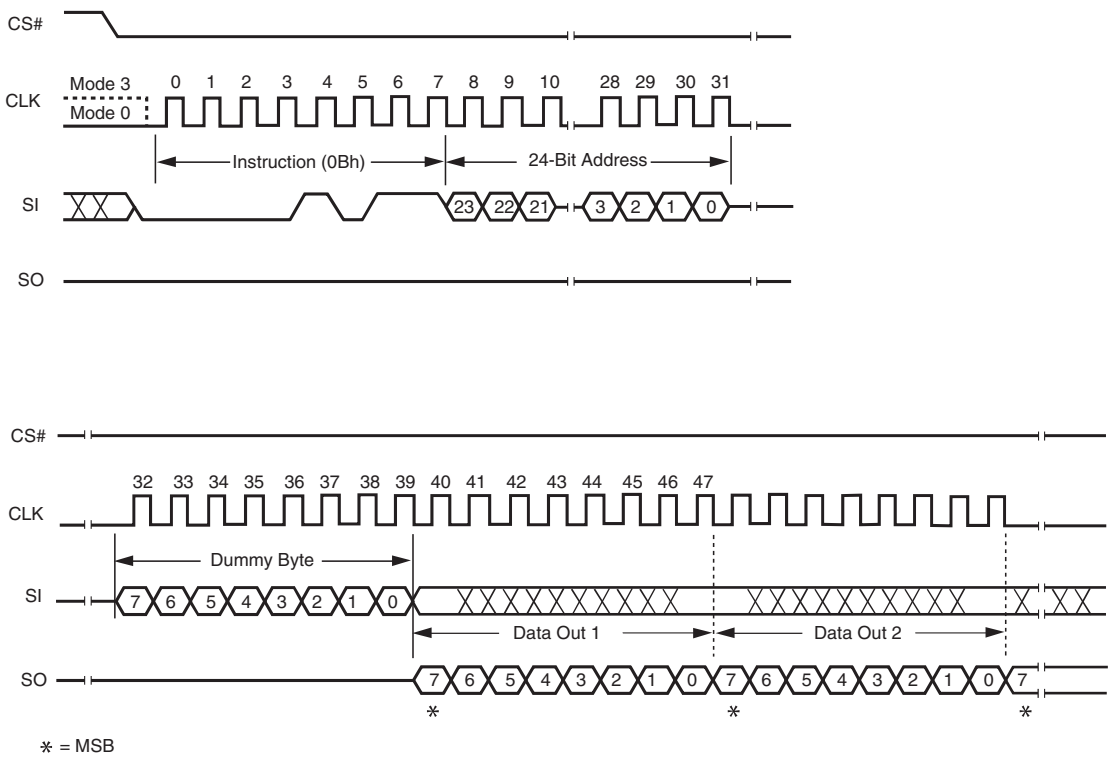
**Figure 7.6** Read Data Instruction Sequence Diagram



### 7.0.7 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of $F_R$ (see See *AC Electrical Characteristics on page 54*.). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 7.7. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the SO pin is a “don’t care”.

**Figure 7.7** Fast Read Instruction Sequence Diagram

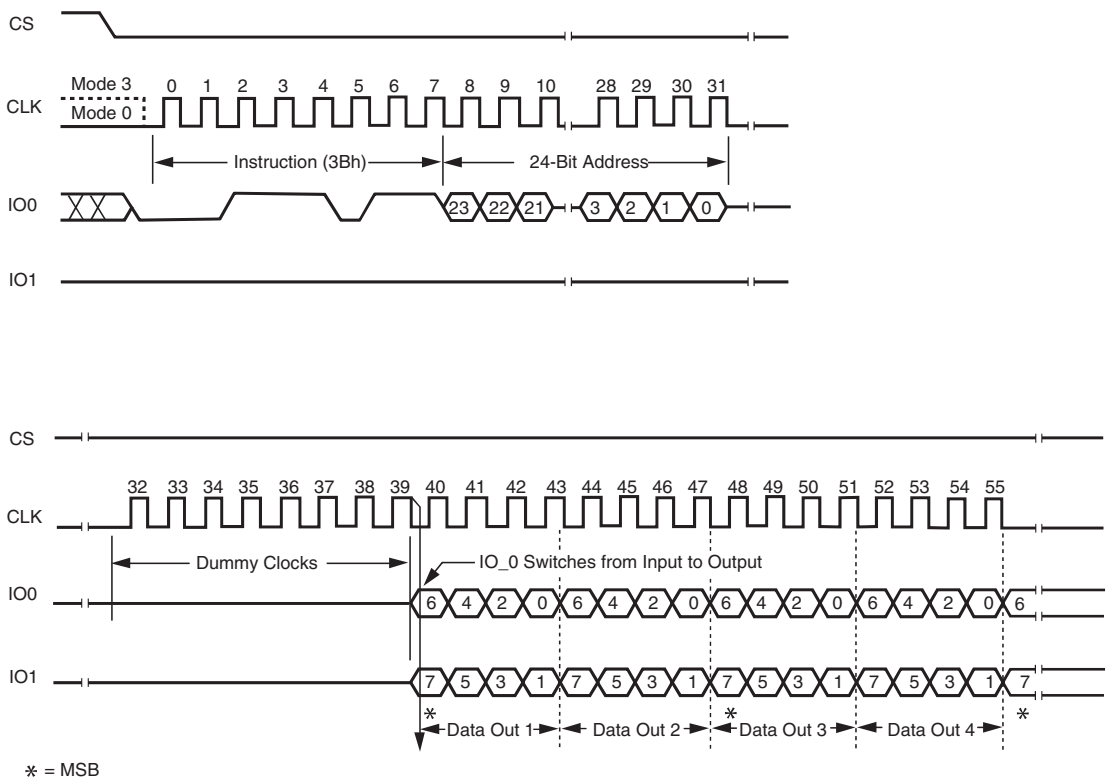


### 7.0.8 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO0 and IO1. This allows data to be transferred from the S25FL004K at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of $F_R$ (see See *AC Electrical Characteristics on page 54*.). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 7.8. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO0 pin should be high-impedance prior to the falling edge of the first data out clock.

**Figure 7.8** Fast Read Dual Output Instruction Sequence Diagram

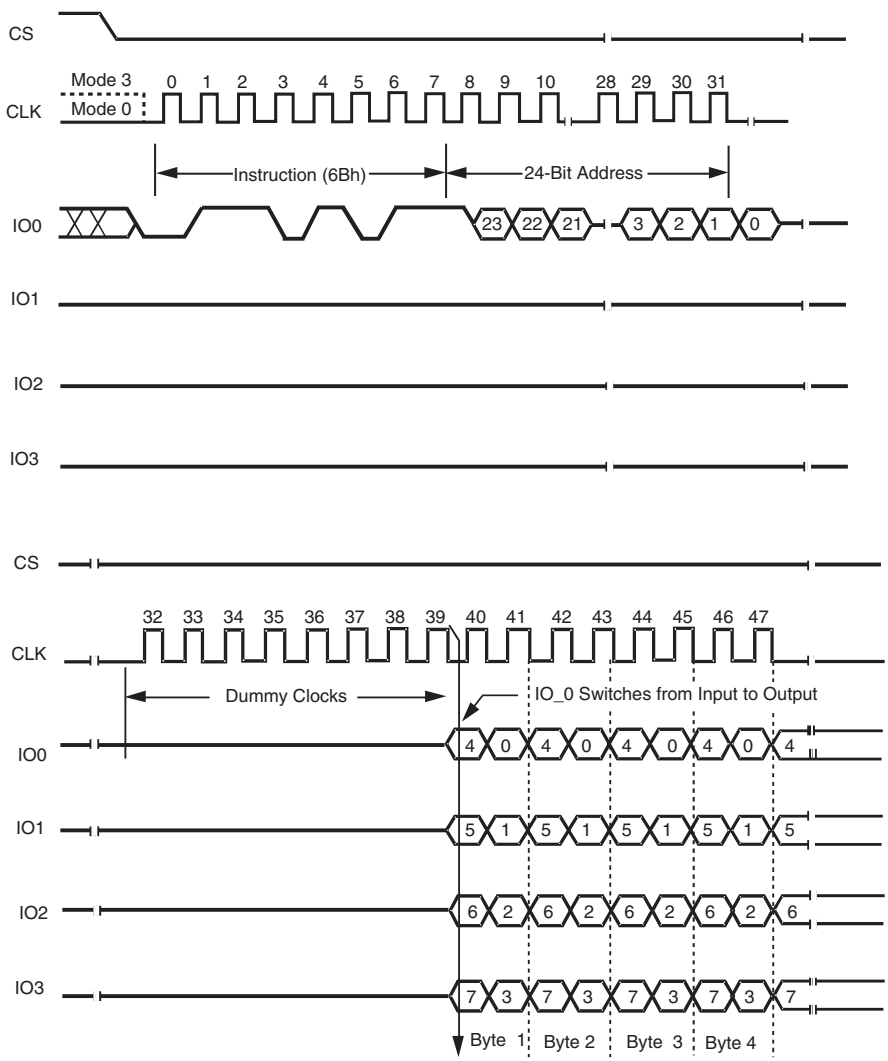


### 7.0.9 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO0, IO1, IO2, and IO3. A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output Instruction (Status Register bit QE must equal 1). The Fast Read Quad Output Instruction allows data to be transferred from the S25FL004K at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (See *AC Electrical Characteristics on page 54*.). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 7.9. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

**Figure 7.9** Fast Read Quad Output Instruction Sequence Diagram



## 7.0.10 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

### Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 7.10. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after CS# is raised and then lowered) does not require the BBh instruction code, as shown in Figure 7.11. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M7-0) before issuing normal instructions (see See *Continuous Read Mode Reset (FFh or FFFFh) on page 33*.).

**Figure 7.10** Fast Read Dual I/O Instruction Sequence (Initial instruction or previous M5-4 ≠ 10)

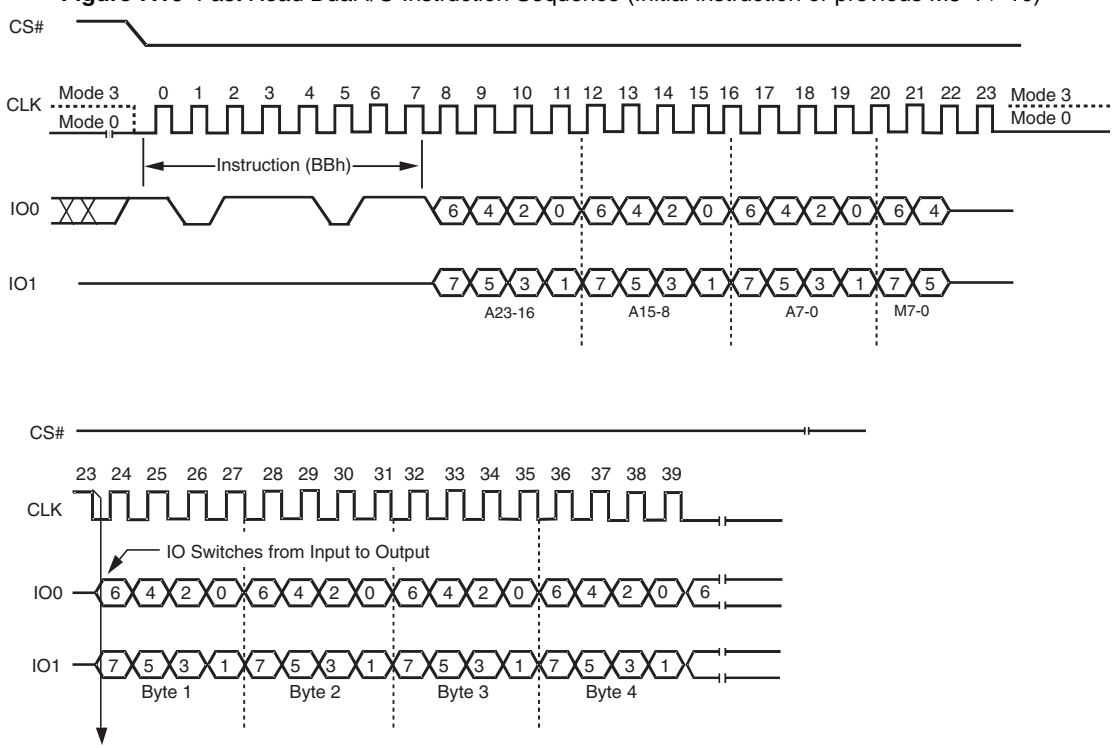
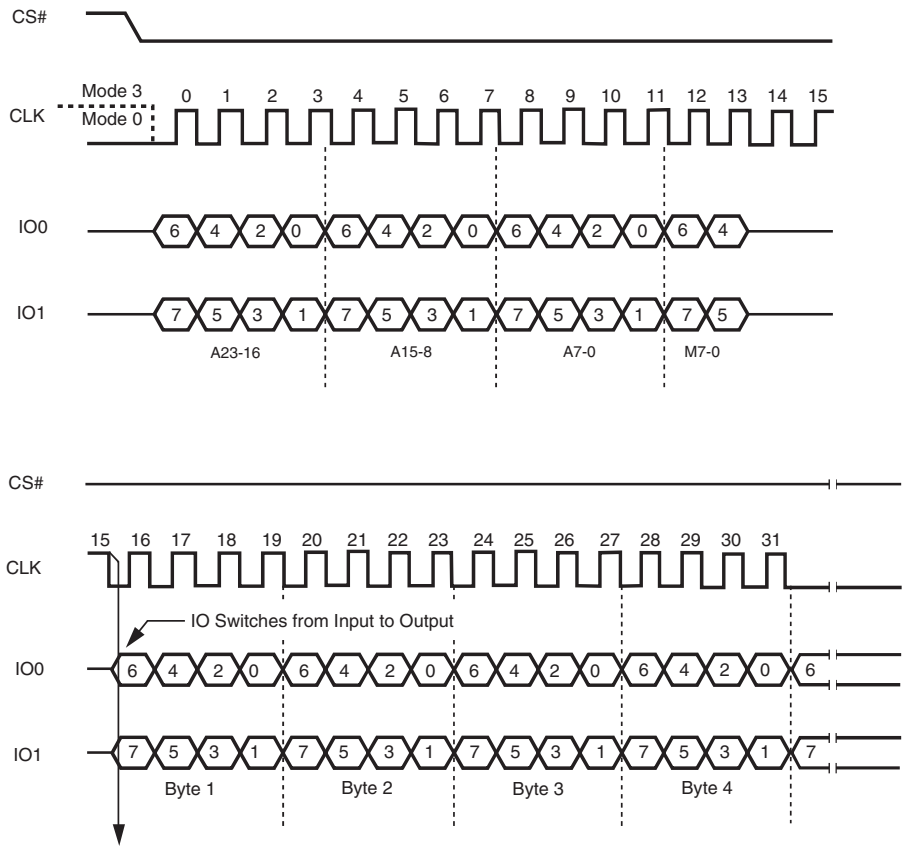


**Figure 7.11** Fast Read Dual I/O Instruction Sequence (Previous instruction set M5-4 = 10)




## 7.0.11 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and four Dummy clock are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

### Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 7.12, *Fast Read Quad I/O Instruction Sequence (Initial instruction or previous M5-4 ¹10) on page 28*. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the EBh instruction code, as shown in Figure 7.13, *Fast Read Quad I/O Instruction Sequence (Previous instruction set M5-4 = 10) on page 28*. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M7-0) before issuing normal instructions (see Section 7.0.16, *Continuous Read Mode Reset (FFh or FFFFh) on page 33*).

**Figure 7.12** Fast Read Quad I/O Instruction Sequence (Initial instruction or previous M5-4 ≠10)

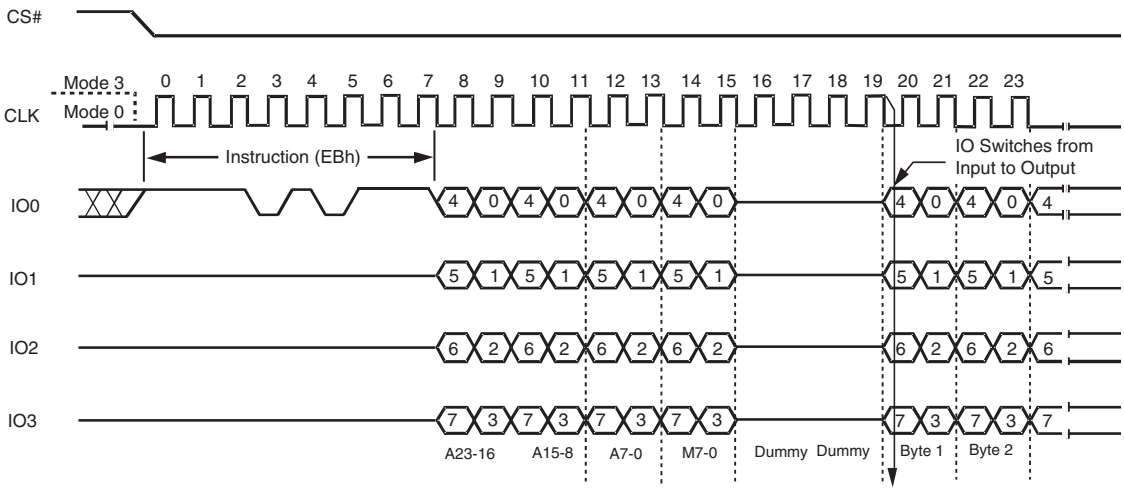
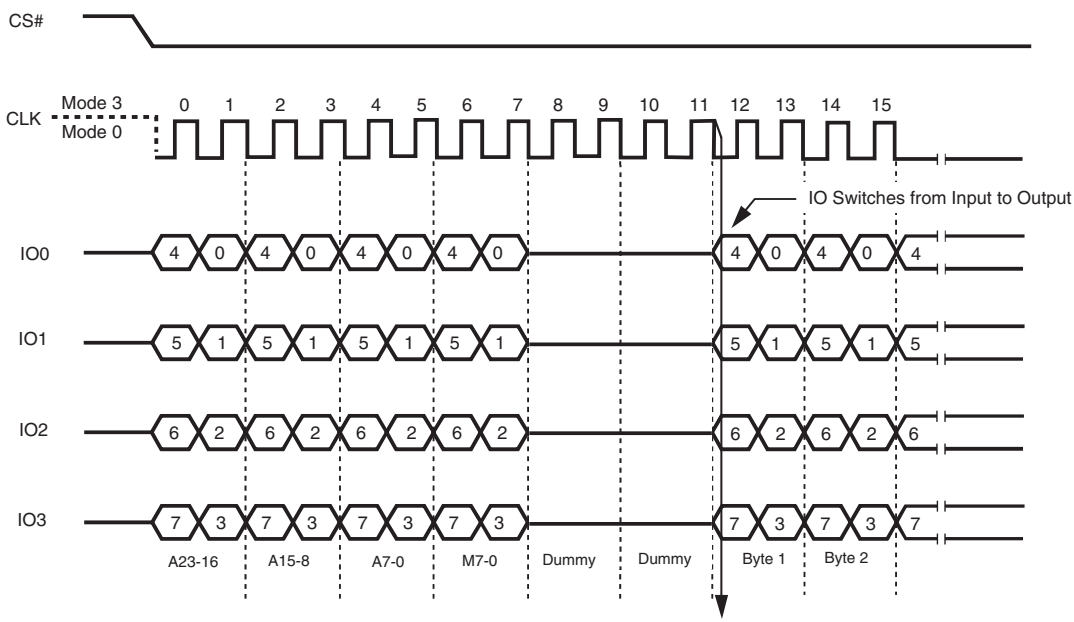



**Figure 7.13** Fast Read Quad I/O Instruction Sequence (Previous instruction set M5-4 = 10)




### Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around"

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" command prior to EBh. The "Set Burst with Wrap" command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See Section 7.0.14, *Set Burst with Wrap (77h) on page 32*.

## 7.0.12 Word Read Quad I/O (E7h)

The Word Read Quad I/O (E7h) instruction is similar to the Fast Read Quad I/O (EBh) instruction except that the lowest Address bit (A0) must equal 0 and only two Dummy clock are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O Instruction.

### Word Read Quad I/O with "Continuous Read Mode"

The Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 7.14. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the E7h instruction code, as shown in Figure 7.15. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M7-0) before issuing normal instructions (see Section 7.0.16, *Continuous Read Mode Reset (FFh or FFFFh) on page 33*).

**Figure 7.14** Word Read Quad I/O Instruction Sequence (Initial instruction or previous M5-4 ≠10)

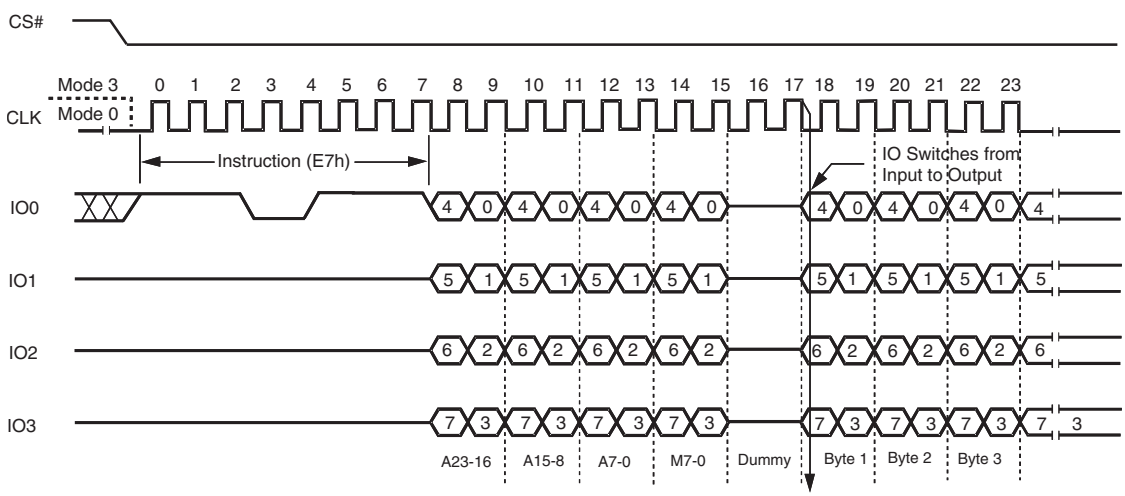
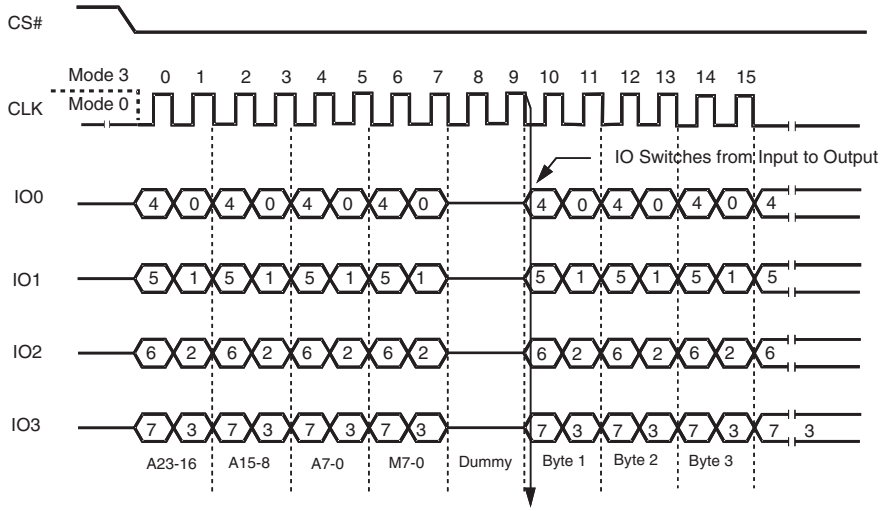


**Figure 7.15** Word Read Quad I/O Instruction Sequence (Previous instruction set M5-4 = 10)




### Word Read Quad I/O with "8/16/32/64-Byte Wrap Around"

The Word Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" command prior to E7h. The "Set Burst with Wrap" command can either enable or disable the "Wrap Around" feature for the following E7h commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See Section 7.0.14, *Set Burst with Wrap (77h) on page 32*.

## 7.0.13 Octal Word Read Quad I/O (E3h)

The Octal Word Read Quad I/O (E3h) instruction is similar to the Fast Read Quad I/O (EBh) instruction except that the lower four Address bits (A0, A1, A2, A3) must equal 0. As a result, the dummy clocks are not required, which further reduces the instruction overhead allowing even faster random access for code execution (XIP). The Quad Enable bit (QE) of Status Register-2 must be set to enable the Octal Word Read Quad I/O Instruction.

### Octal Word Read Quad I/O with "Continuous Read Mode"

The Octal Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 7.16, *Octal Word Read Quad I/O Instruction Sequence (Initial instruction or previous M5-4 ¹ 10) on page 31*. The upper nibble of the (M7-4) controls the length of the next Octal Word Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the E3h instruction code, as shown in Figure 7.17, *Octal Word Read Quad I/O Instruction Sequence (Previous instruction set M5-4 = 10) on page 31*. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M7-0) before issuing normal instructions (see Section 7.0.16, *Continuous Read Mode Reset (FFh or FFFFh) on page 33*).

**Figure 7.16** Octal Word Read Quad I/O Instruction Sequence (Initial instruction or previous M5-4 ≠ 10)

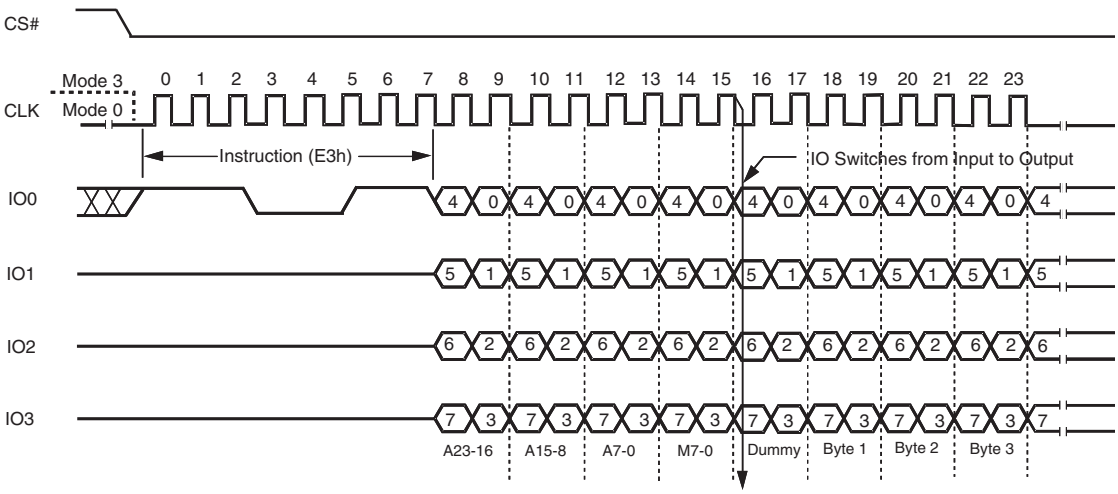
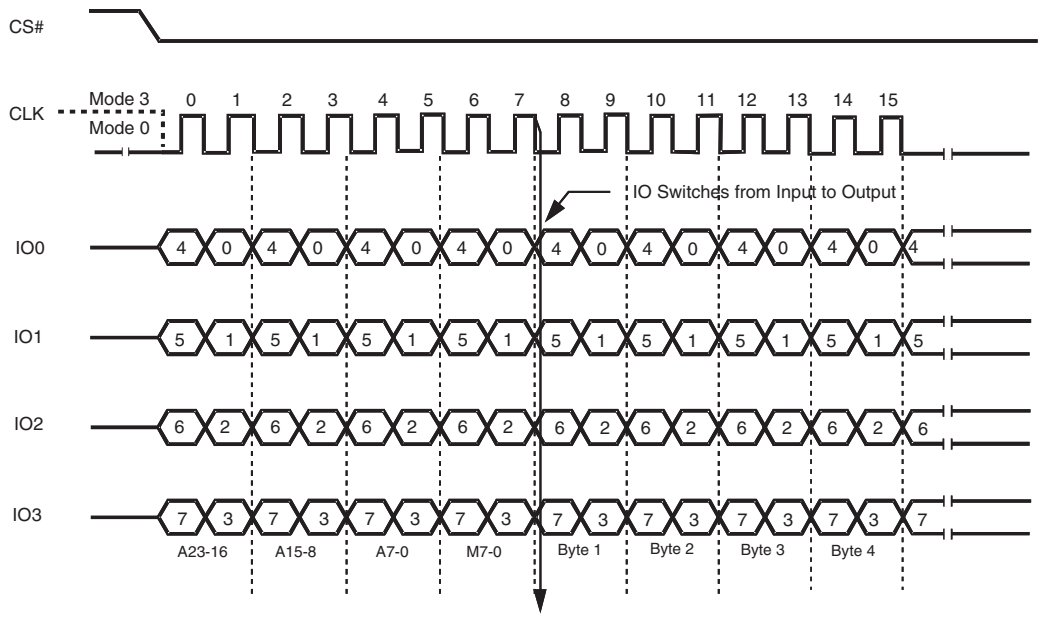



**Figure 7.17** Octal Word Read Quad I/O Instruction Sequence (Previous instruction set M5-4 = 10)



### 7.0.14 Set Burst with Wrap (77h)

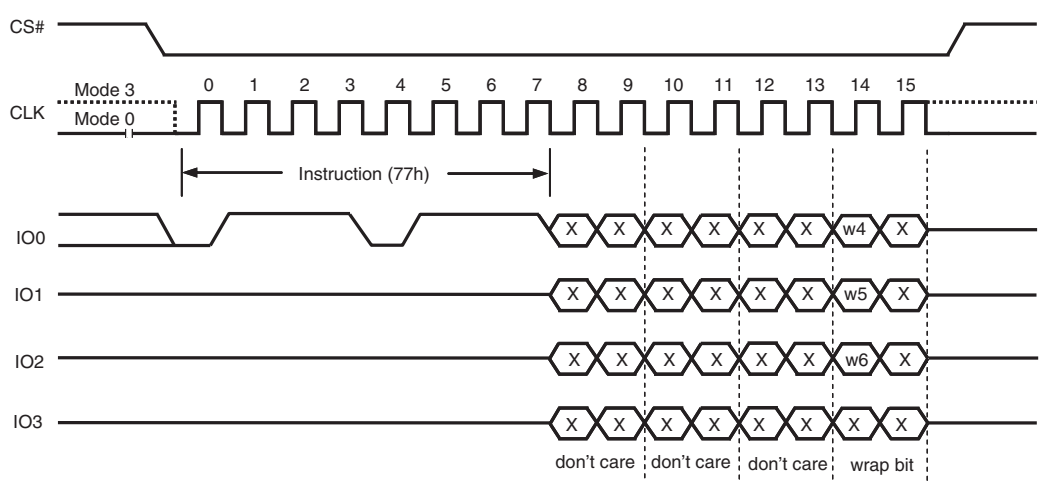
The Set Burst with Wrap (77h) instruction is used in conjunction with “Fast Read Quad I/O” and “Word Read Quad I/O” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the CS# pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 7.18, *Set Burst with Wrap Instruction Sequence on page 32*. Wrap bit W7 and the lower nibble W3-0 are not used.

| W6, W5 | W4 = 0 | | W4 =1 (DEFAULT) | |
|---|---|---|---|---|
| | Wrap Around | Wrap Length | Wrap Around | Wrap Length |
| 0 0 | Yes | 8-byte | No | N/A |
| 0 1 | Yes | 16-byte | No | N/A |
| 1 0 | Yes | 32-byte | No | N/A |
| 1 1 | Yes | 64-byte | No | N/A |

Once W6-4 is set by a Set Burst with Wrap instruction, all the following “Fast Read Quad I/O” and “Word Read Quad I/O” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap instruction to reset W4 = 1 prior to any normal Read instructions since S25FL004K does not have a hardware Reset Pin.

**Figure 7.18** Set Burst with Wrap Instruction Sequence



### 7.0.15 Continuous Read Mode Bits (M7-0)

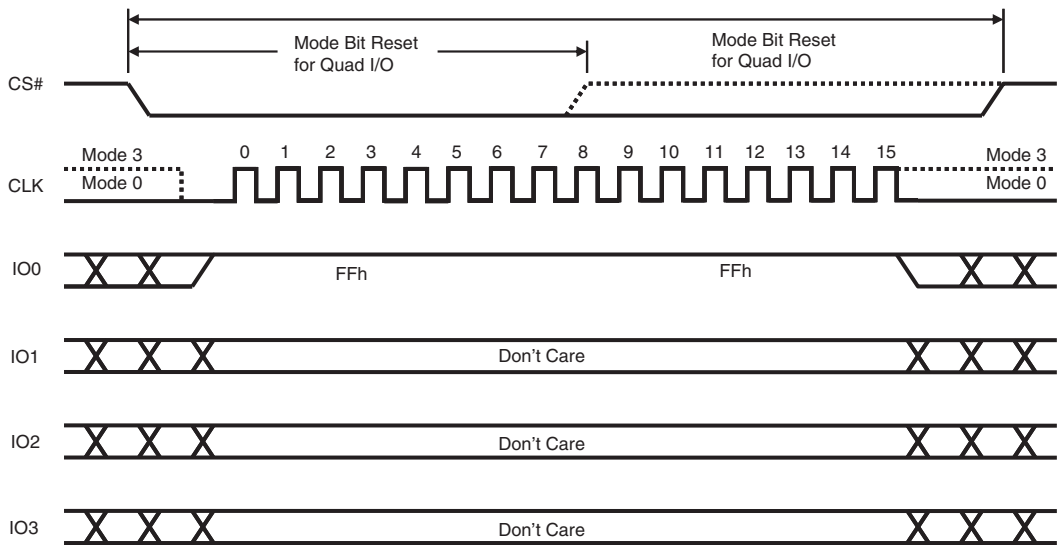
The “Continuous Read Mode” bits are used in conjunction with “Fast Read Dual I/O”, “Fast Read Quad I/O”, “Word Read Quad I/O” and “Octal Word Read Quad I/O” instructions to provide the highest random Flash memory access rate with minimum SPI instruction overhead, thus allow true XIP (execute in place) to be performed on serial flash devices.

M7-0 need to be set by the Dual/Quad I/O Read instructions. M5-4 are used to control whether the 8-bit SPI instruction code (BBh, EBh, E7h or E3h) is needed or not for the next command. When M5-4 = (1,0), the next command will be treated same as the current Dual/Quad I/O Read command without needing the 8-bit instruction code; when M5-4 do not equal to (1,0), the device returns to normal SPI mode, all commands can be accepted. M7-6 and M3-0 are reserved bits for future use, either 0 or 1 values can be used.

### 7.0.16 Continuous Read Mode Reset (FFh or FFFFh)

Continuous Read Mode Reset instruction can be used to set M4 = 1, thus the device will release the Continuous Read Mode and return to normal SPI operation, as shown in Figure 7.19.

**Figure 7.19** Continuous Read Mode Reset for Fast Read Dual/Quad I/O




Since S25FL004K does not have a hardware Reset pin, so if the controller resets while S25FL004K is set to Continuous Mode Read, the S25FL004K will not recognize any initial standard SPI instructions from the controller. To address this possibility, it is recommended to issue a Continuous Read Mode Reset instruction as the first instruction after a system Reset. Doing so will release the device from the Continuous Read Mode and allow Standard SPI instructions to be recognized.

To reset “Continuous Read Mode” during Quad I/O operation, only eight clocks are needed. The instruction is “FFh”. To reset “Continuous Read Mode” during Dual I/O operation, sixteen clocks are needed to shift in instruction “FFFFh”.

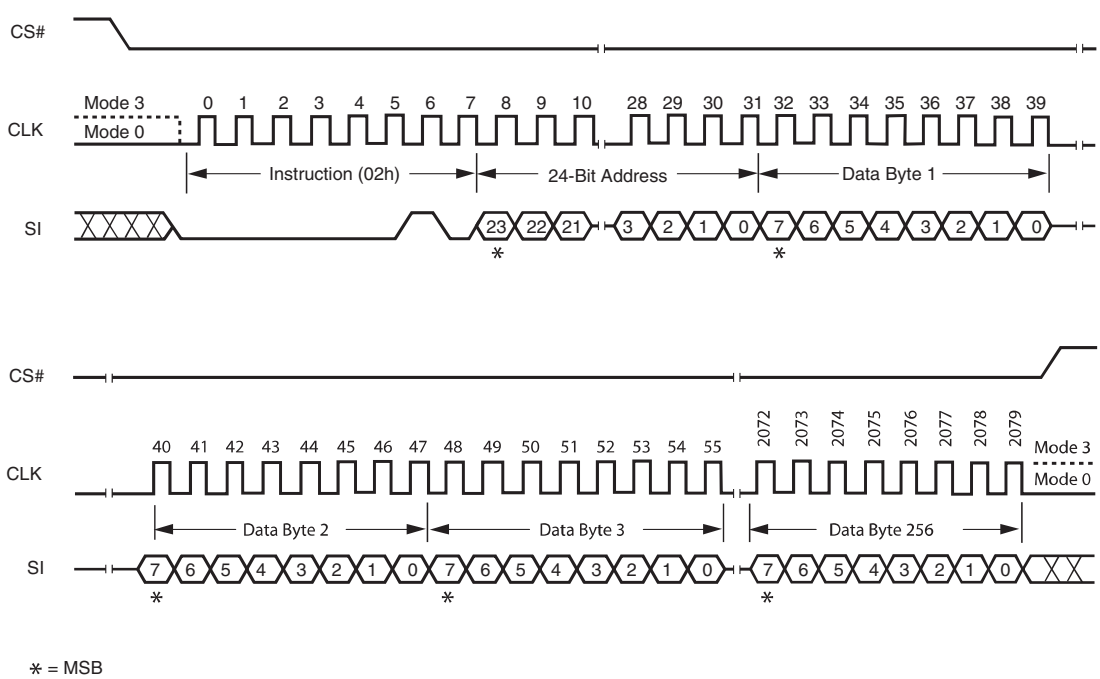
### 7.0.17 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the SI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 7.20, *Page Program Instruction Sequence Diagram on page 34*.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After CS# is driven high, the self-timed Page Program instruction will commence for a time duration of $t_{PP}$ (See *AC Electrical Characteristics on page 54*.). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

**Figure 7.20** Page Program Instruction Sequence Diagram



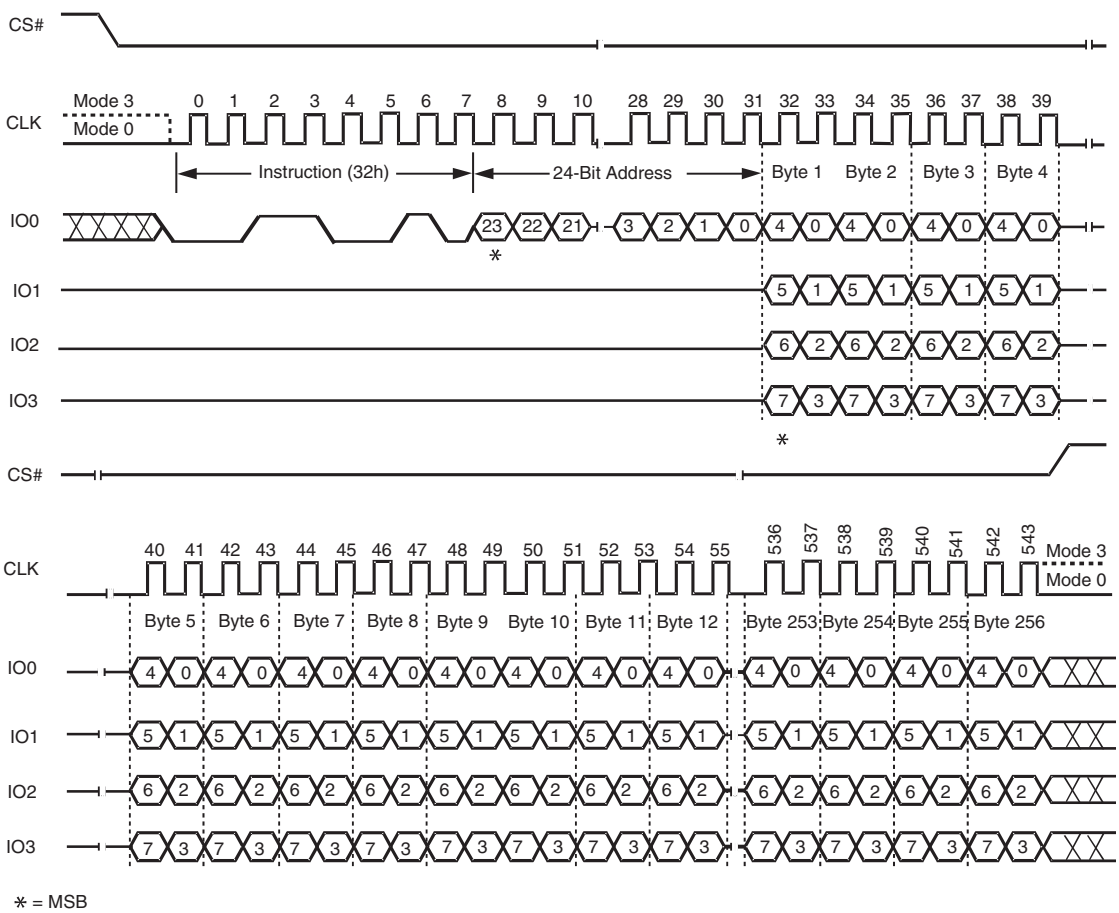

* = MSB

## 7.0.18 Quad Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO0, IO1, IO2, and IO3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5 MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable in Status Register-2 must be set (QE=1). A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the CS# pin low then shifting the instruction code "32h" followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 7.21, *Quad Page Program Instruction Sequence Diagram on page 35*.

**Figure 7.21** Quad Page Program Instruction Sequence Diagram

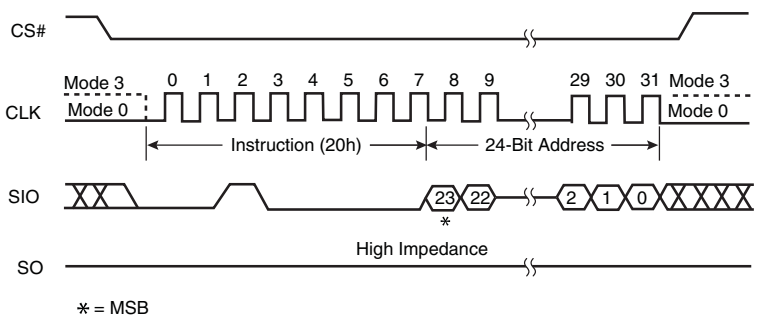


### 7.0.19 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0) See *Block Diagram on page 8.* The Sector Erase instruction sequence is shown in Figure 7.22 on page 36.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed Sector Erase instruction will commence for a time duration of $t_{SE}$. See *AC Electrical Characteristics on page 54.* While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed sector is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (Table 6.2, *Status Register Memory Protection (CMP = 0) on page 15*).

**Figure 7.22** Sector Erase Instruction Sequence Diagram

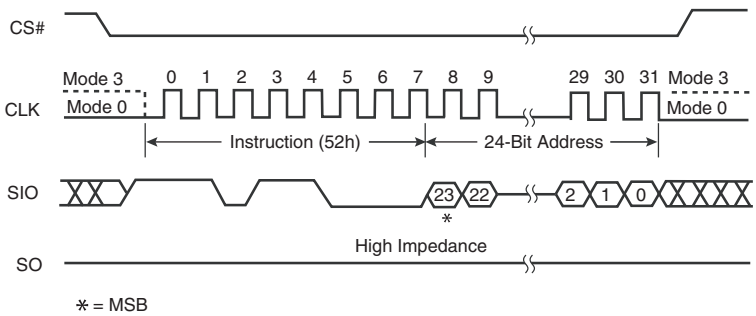



### 7.0.20 32 KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “52h” followed a 24-bit block address (A23-A0) See *Block Diagram on page 8.* The Block Erase instruction sequence is shown in Figure 7.23.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of $t_{BE1}$ (See *AC Electrical Characteristics on page 54.*). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed sector is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Table 6.2, *Status Register Memory Protection (CMP = 0) on page 15*).

**Figure 7.23** 32 KB Block Erase Instruction Sequence Diagram

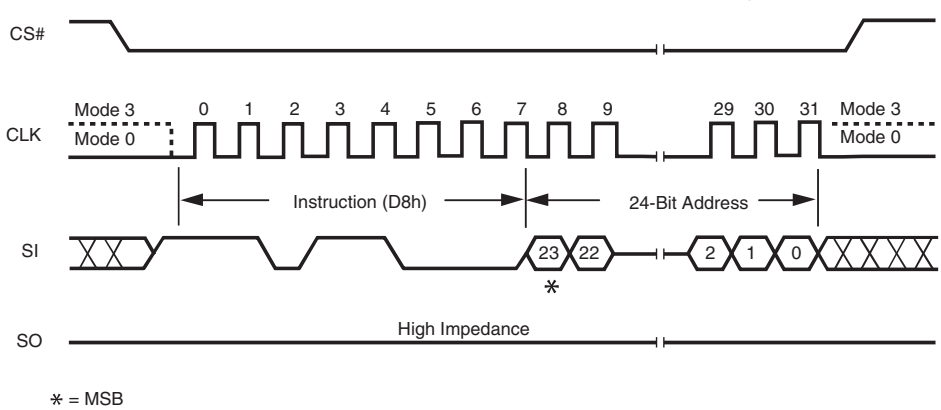



## 7.0.21 64 KB Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0) See *Block Diagram on page 8.* The Block Erase instruction sequence is shown in Figure 7.24.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of $t_{BE}$ (see See *AC Electrical Characteristics on page 54.*). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed sector is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Table 6.2, *Status Register Memory Protection (CMP = 0) on page 15*.

**Figure 7.24** 64 KB Block Erase Instruction Sequence Diagram



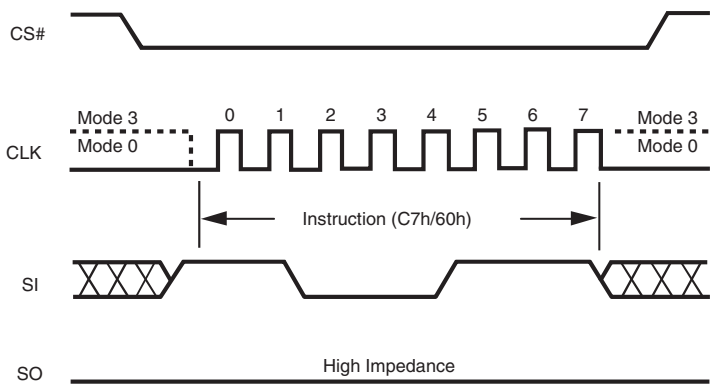

## 7.0.22 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 7.25.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence

for a time duration of $t_{CE}$ (See *AC Electrical Characteristics on page 54.*). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Table 6.2, *Status Register Memory Protection (CMP = 0) on page 15*).

**Figure 7.25** Chip Erase Instruction Sequence Diagram




## 7.0.23 Erase / Program Suspend (75h)

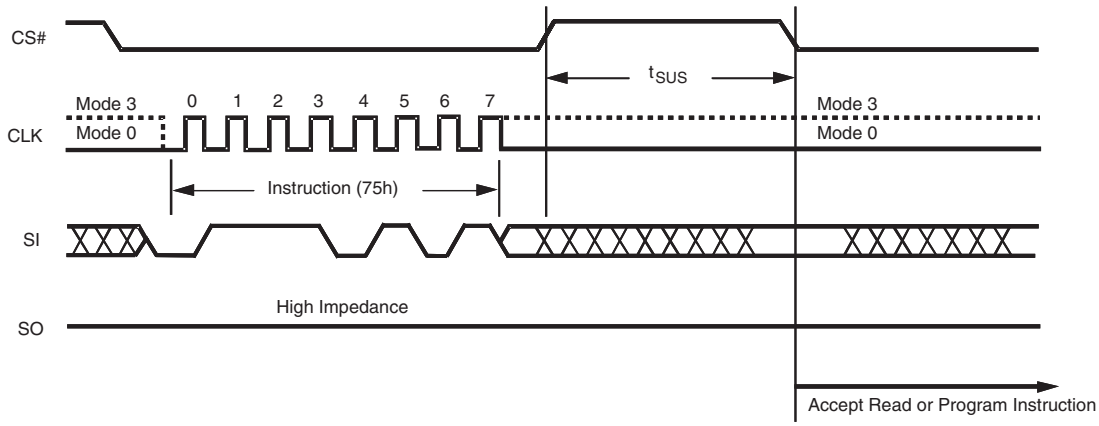
The Erase/Program Suspend instruction 75h, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 7.26, *Erase/Program Suspend Instruction Sequence on page 39*.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction 75h will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of $t_{SUS}$ (See *AC Electrical Characteristics on page 54.*) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within $t_{SUS}$ and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction 75h is not issued earlier than a minimum of time of $t_{SUS}$ following the preceding Resume instruction 7Ah.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

**Figure 7.26** Erase/Program Suspend Instruction Sequence

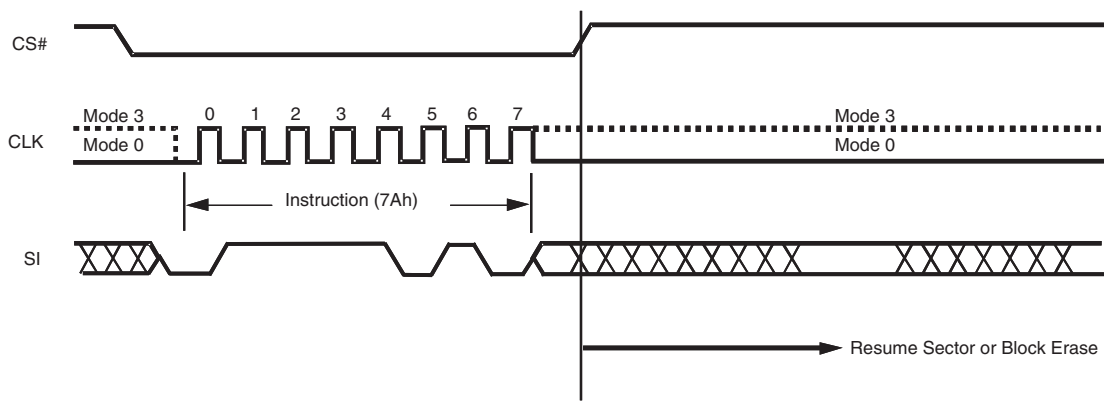



## 7.0.24 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200 ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 7.27.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “$t_{SUS}$” following a previous Resume instruction.

**Figure 7.27** Erase/Program Resume Instruction Sequence

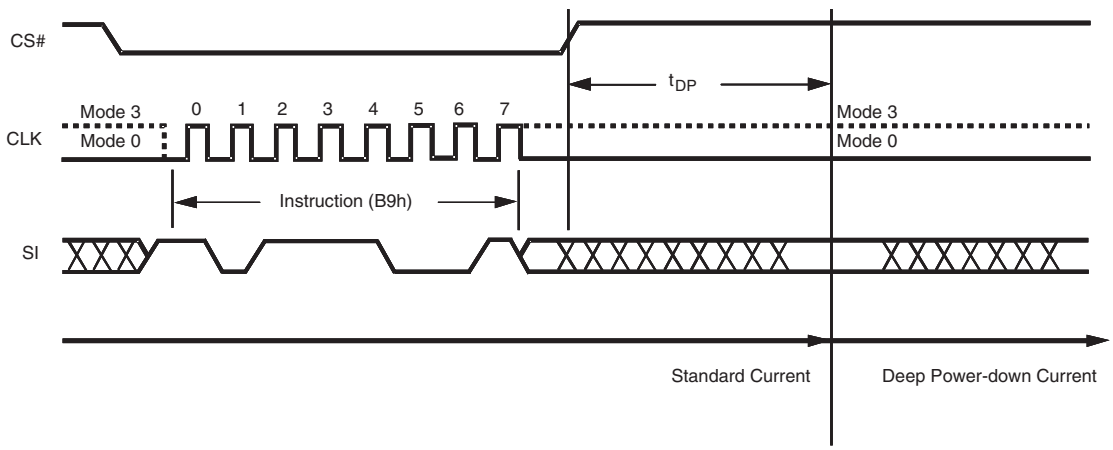


### 7.0.25 Deep Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Deep Power-down instruction especially useful for battery powered applications (see $I_{CC1}$ and $I_{CC2}$ in Section 8.4, *DC Electrical Characteristics on page 53*). The instruction is initiated by driving the CS# pin low and shifting the instruction code “B9h” as shown in Figure 7.28.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power-down instruction will not be executed. After CS# is driven high, the power-down state will entered within the time duration of $t_{DP}$ (See *AC Electrical Characteristics on page 54*.). While in the power-down state only the Release from Deep Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of $I_{CC1}$.

**Figure 7.28** Deep Power-down Instruction Sequence Diagram




### 7.0.26 Release from Deep Power-down / Device ID (ABh)

The Release from Deep Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the deep power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the deep power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in Figure 7.29. Release from deep power-down will take the time duration of $t_{RES1}$ (See *AC Electrical Characteristics on page 54*.) before the device will resume normal operation and other instructions are accepted. The CS# pin must remain high during the $t_{RES1}$ time duration.

When used only to obtain the Device ID while not in the deep power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID values for the S25FL004K is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When used to release the device from the deep power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 7.30, except that after CS# is driven high it must remain high for a time duration of $t_{RES2}$. After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Deep Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

**Figure 7.29** Release from Deep Power-down Instruction Sequence

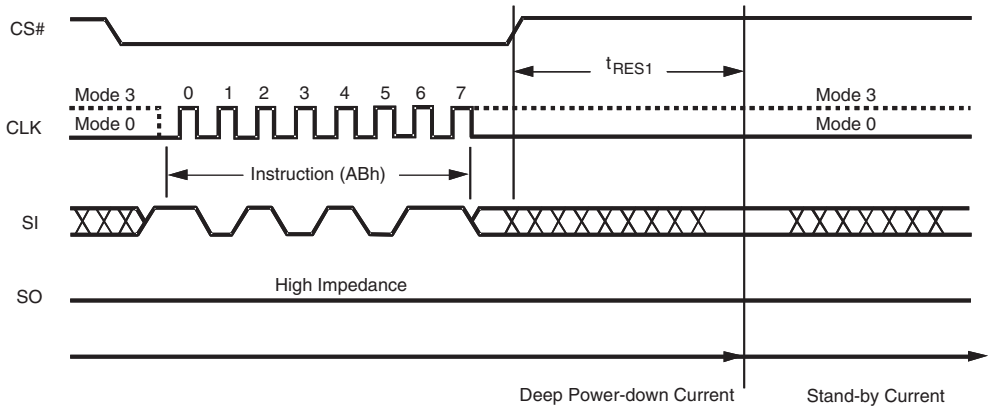
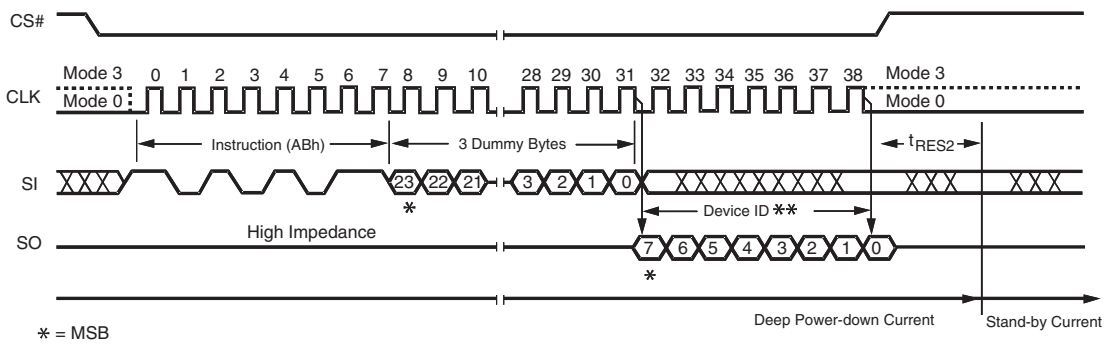



**Figure 7.30** Release from Deep Power-down / Device ID Instruction Sequence Diagram

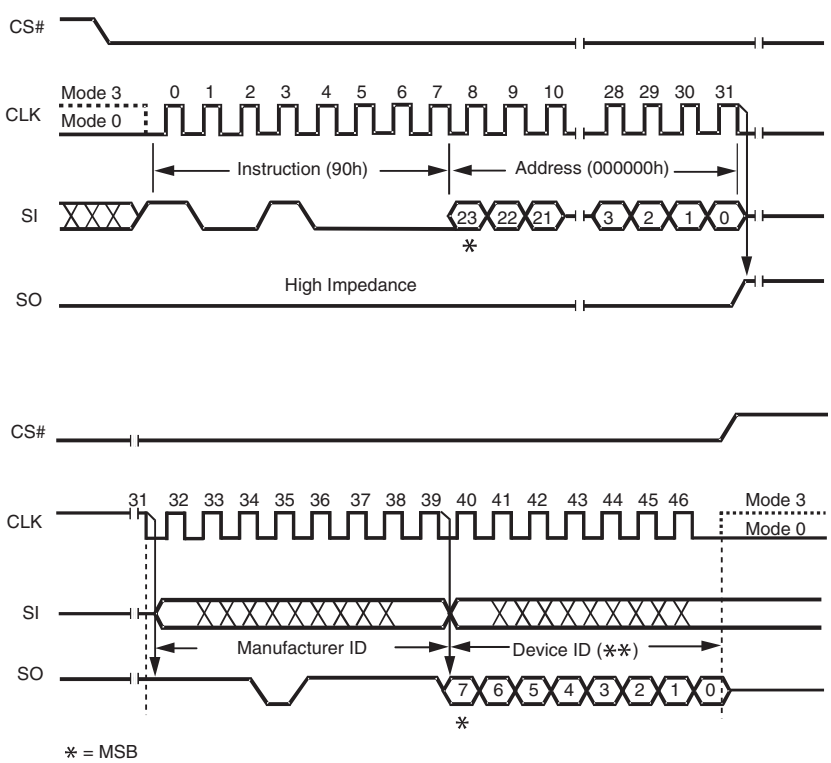


### 7.0.27 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Deep Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Deep Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.31. The Device ID values for the S25FL004K is listed in Table 7.2, *Device Identification on page 17*. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

**Figure 7.31** Read Manufacturer / Device ID Diagram

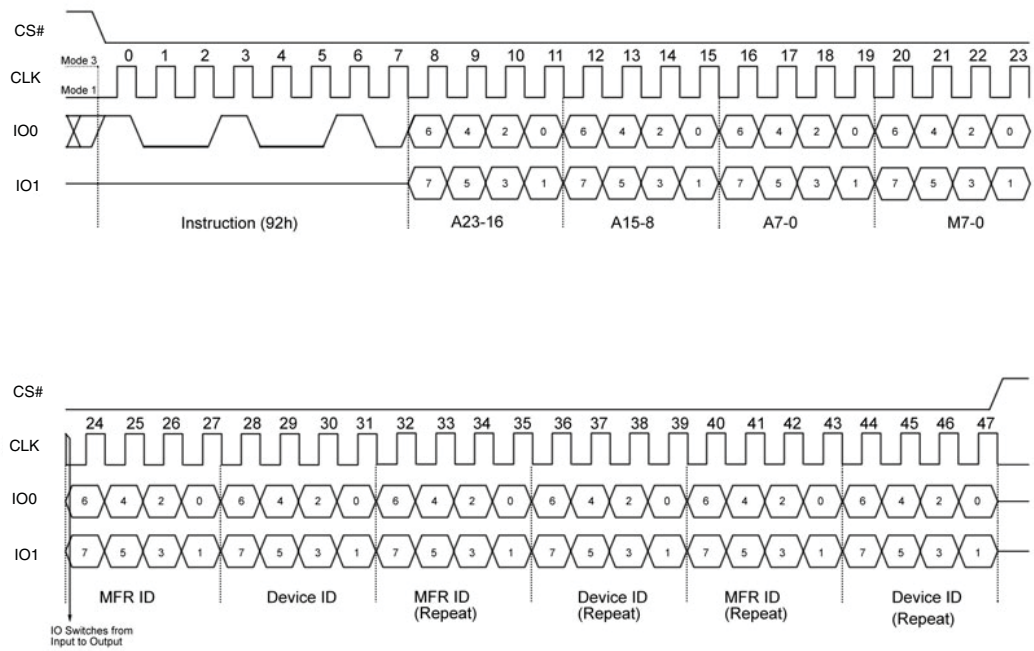


## 7.0.28 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “92h” followed by a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 7.32. The Device ID values for the S25FL004K is listed in Table 7.2, *Device Identification on page 17*. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

**Figure 7.32** Read Manufacturer / Device ID Dual I/O Diagram




***Note:***

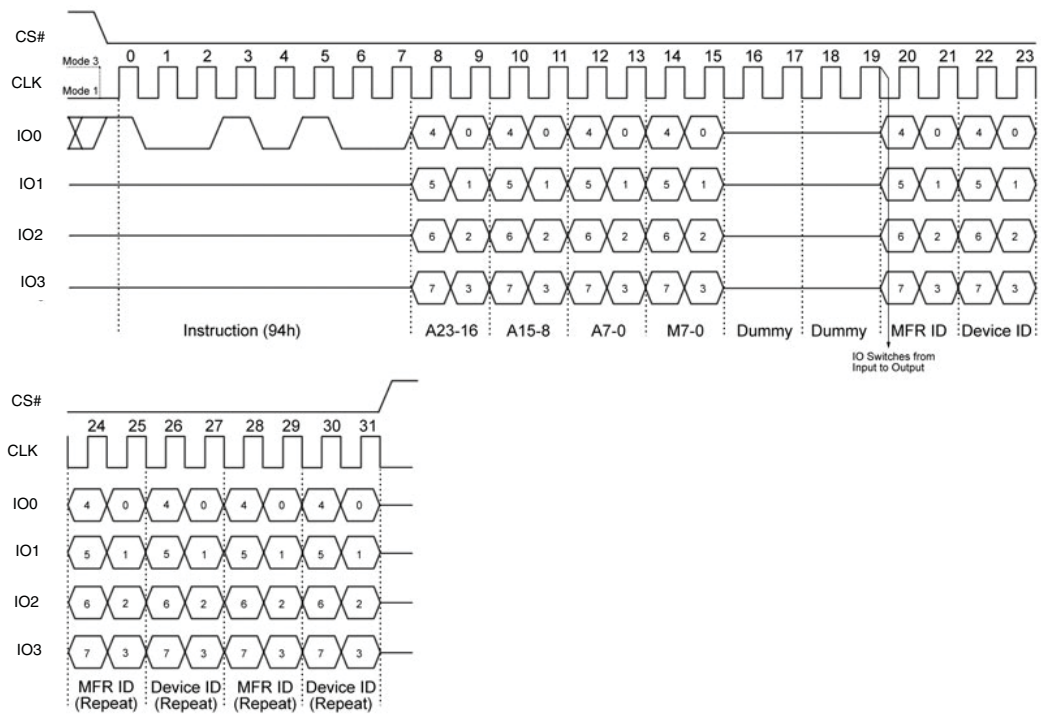
1. *The “Continuous Read Mode” bits M(7-0) must be set to Fxh to be compatible with Fast Read Dual I/O instruction.*

## 7.0.29 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “94h” followed by a four clock dummy cycles and then a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.33. The Device ID values for the S25FL004K is listed in Table 7.2, *Device Identification on page 17*. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

**Figure 7.33** Read Manufacturer / Device ID Quad I/O Diagram



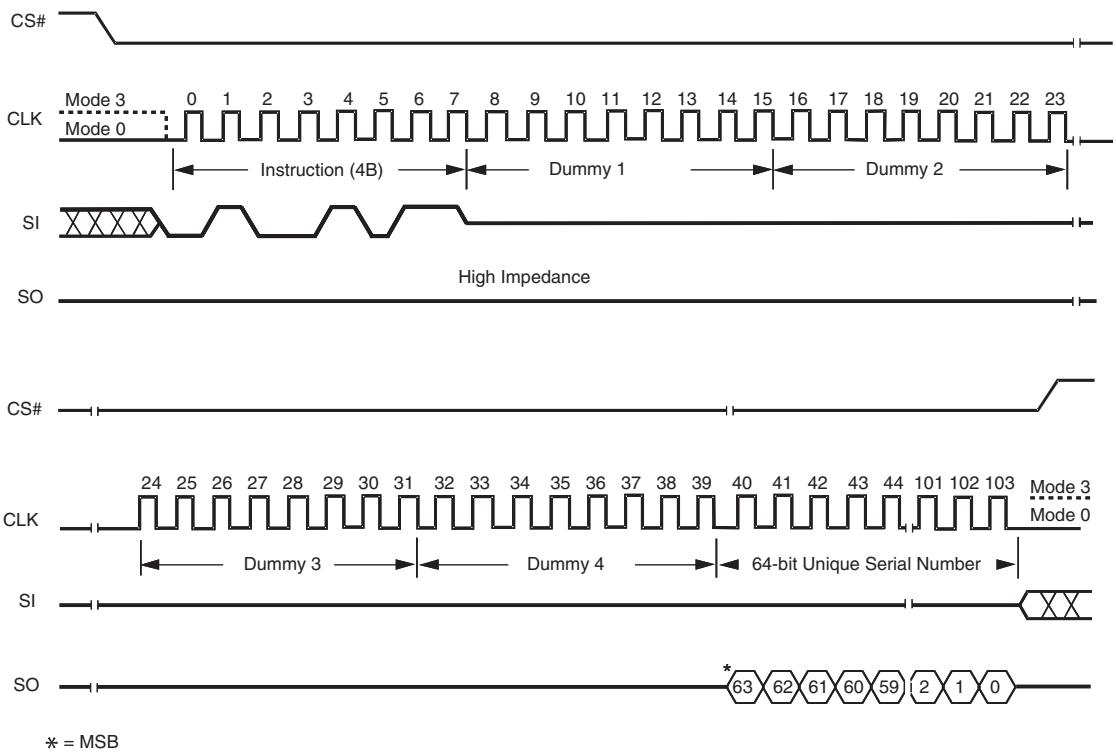

***Note:***

1. *The “Continuous Read Mode” bits M(7-0) must be set to Fxh to be compatible with Fast Read Quad I/O instruction.*

### 7.0.30 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each S25FL004K device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 7.34.

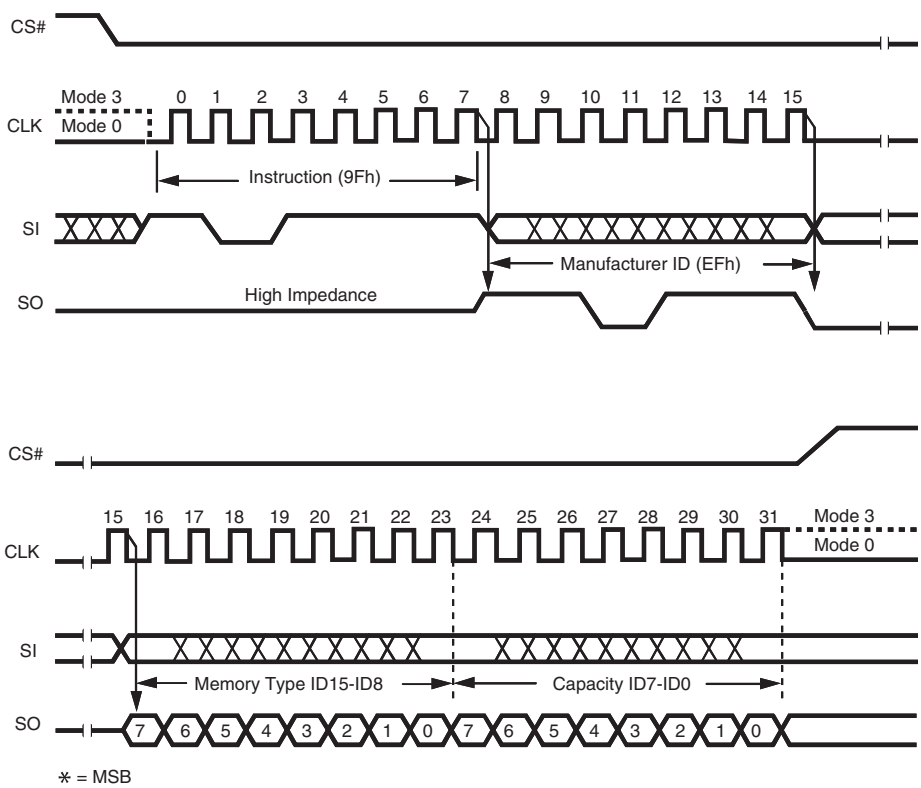
**Figure 7.34** Read Unique ID Number Instruction Sequence



### 7.0.31 Read JEDEC ID (9Fh)

For compatibility reasons, the S25FL004K provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial flash memories that was adopted in 2003. The instruction is initiated by driving the CS# pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.35. For memory type and capacity values refer to Manufacturer and Device Identification table.

**Figure 7.35** Read JEDEC ID Instruction Sequence



## 7.0.32 Read SFDP Register (5Ah)

The S25FL004K features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about devices operational capability such as available commands, timing and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications.

The Read SFDP instruction is initiated by driving the CS# pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0)(1) into the SI pin. Eight “dummy” clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 7.36. For SFDP register values and descriptions, refer to Table 7.6.

**Note:** A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

**Figure 7.36** Read SFDP Register Instruction Sequence Diagram

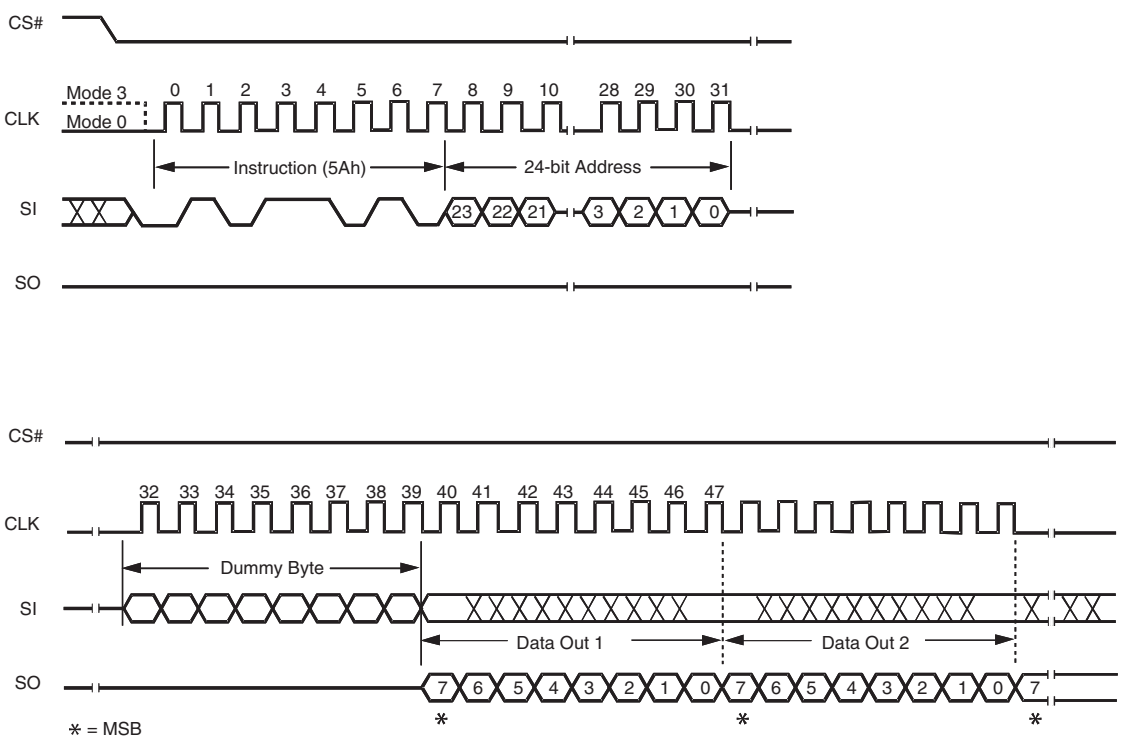



**Table 7.6** Serial Flash Discoverable Parameter Definition Table (Sheet 1 of 2)

| Byte Address | Data | Description | Comment |
|---|---|---|---|
| 00h | 53h | SFDP Signature | SFDP Signature = 50444653h |
| 01h | 46h | SFDP Signature | |
| 02h | 44h | SFDP Signature | |
| 03h | 50h | SFDP Signature | |
| 04h | 01h | SFDP Minor Revisions | SFDP revision 1.1 |
| 05h | 01h | SFDP Major Revisions | |
| 06h | 00h | Number of Parameter Headers (NPH) | 1 Parameter Header |
| 07h | FFh | Reserved | |
| 08h | EFh | PID (3)(0): Manufacturer JEDEC ID | EFh |
| 09h | 00h | PID(0): Serial Flash Basics Minor Revisions | Serial Flash Basics Revision 1.0 |
| 0Ah | 01h | PID(0): Serial Flash Basics Major Revisions | |

**Table 7.6** Serial Flash Discoverable Parameter Definition Table (Sheet 2 of 2)

| Byte Address | Data | Description | Comment |
|---|---|---|---|
| 0Bh | 04h | PID(0): Serial Flash Basics Length | 4 Dwords (2) |
| 0Ch | 80h | PID(0): Address of Parameter ID(0) Table (A7-A0) | PID(0) Table Address = 000080h |
| 0Dh | 00h | PID(0): Address of Parameter ID(0) Table (A15-A8) | |
| 0Eh | 00h | PID(0): Address of Parameter ID(0) Table (A23-A16) | |
| 0Fh | FFh | Reserved | |
| 10h | EFh | PID(1): Manufacturer JEDEC ID | EFh |
| 11h | 00h | PID(1): Serial Flash Properties Minor Revisions | Serial Flash Properties Revision 1.0 |
| 12h | 01h | PID(1): Serial Flash Properties Major Revisions | |
| 13h | 00h | PID(1): Serial Flash Properties Length | 00h = Unimplemented |
| 14h | 90h | PID(1): Address of Parameter ID(1) Table (A7-A0) | PID(1) Table Address = 000090h |
| 15h | 00h | PID(1): Address of Parameter ID(1) Table (A15-A8) | |
| 16h | 00h | PID(1): Address of Parameter ID(1) Table (A23-A16) | |
| 17h | FFh | Reserved | |
| ... (1) | FFh | Reserved | |
| 80h | E5h | Bit[7:5] = 111 Reserved<br>Bit[4:3] = 00 Non-volatile Status Register<br>Bit[2] = 1 Page Programmable<br>Bit[1:0] = 01 Supports 4 KB Erase | |
| 81h | 20h | 4 KByte Erase Opcode | |
| 82h | F1h | Bit[7] = 1 Reserved<br>Bit[6] = 1 Supports Single Input Quad Output<br>Bit[5] = 1 Supports Quad Input Quad Output<br>Bit[4] = 1 Supports Dual Input Dual Output<br>Bit[3] = 0 Dual Transfer Rate not Supported<br>Bit[2:1] = 00 3-Byte/24-Bit Addressing<br>Bit[0] = 1 Supports Single Input Dual Output | |
| 83h | FFh | Reserved | |
| 84h | FFh | Flash Size in Bits | 4 Mega Bits =003FFFFFh |
| 85h | FFh | Flash Size in Bits | |
| 86h | 3Fh | Flash Size in Bits | |
| 87h | 00h | Flash Size in Bits | |
| 88h | 44h | Bit[7:5] = 010 8 Mode Bits are needed<br>Bit[4:0] = 00100 16 Dummy Bits are needed | Fast Read Quad I/O Setting |
| 89h | EBh | Quad Input Quad Output Fast Read Opcode | |
| 8Ah | 08h | Bit[7:5] = 000 No Mode Bits are needed<br>Bit[4:0] = 01000 8 Dummy Bits are needed | Fast Read Quad Output Setting |
| 8Bh | 6Bh | Single Input Quad Output Fast Read Opcode | |
| 8Ch | 08h | Bit[7:5] = 000 No Mode Bits are needed<br>Bit[4:0] = 01000 8 Dummy Bits are needed | Fast Read Dual Output Setting |
| 8Dh | 3Bh | Single Input Dual Output Fast Read Opcode | |
| 8Eh | 80h | Bit[7:5] = 100 8 Mode bits are needed<br>Bit[4:0] = 00000 No Dummy bits are needed | Fast Read Dual I/O Setting |
| 8Fh | BBh | Dual Input Dual Output Fast Read Opcode | |
| ... (1) | FFh | Reserved | |
| FFh | FFh | Reserved | |

***Notes:***

1. *Data stored in Byte Address 18h to 7Fh and 90h to FFh are Reserved, the value is FFh.*
2. *1 Dword = 4 Bytes*
3. *PID(x) = Parameter Identification Table (x)*

### 7.0.33 Erase Security Registers (44h)

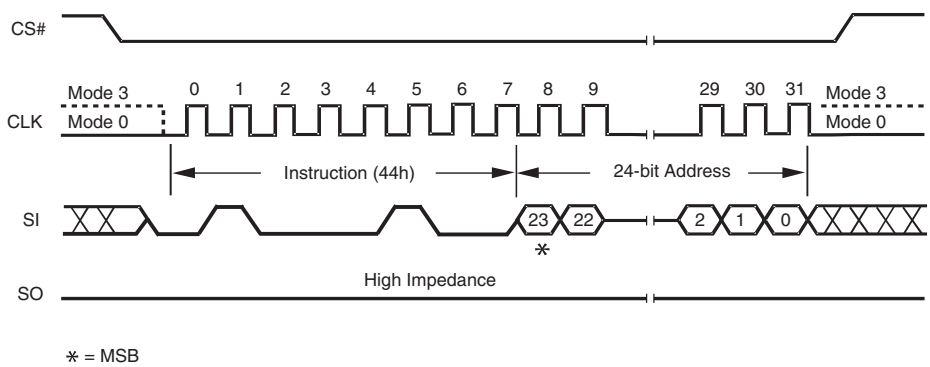
The S25FL004K offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “44h” followed by a 24-bit address (A23-A0) to erase one of the three security registers.

| Address | A23-16 | A15-12 | A11-8 | A7-0 |
|---|---|---|---|---|
| Security Register #1 | 00h | 0 0 0 1 b | 0 0 0 0 b | Don’t Care |
| Security Register #2 | 00h | 0 0 1 0 b | 0 0 0 0 b | Don’t Care |
| Security Register #3 | 00h | 0 0 1 1 b | 0 0 0 0 b | Don’t Care |

The Erase Security Register instruction sequence is shown in Figure 7.37. The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After CS# is driven high, the self-timed Erase Security Register operation will commence for a time duration of $t_{SE}$ (see *AC Electrical Characteristics on page 54*). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3:1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, and an Erase Security Register instruction to that register will be ignored (see *Security Register Lock Bits (LB3, LB2, LB1) on page 14*).

**Figure 7.37** Erase Security Registers Instruction Sequence



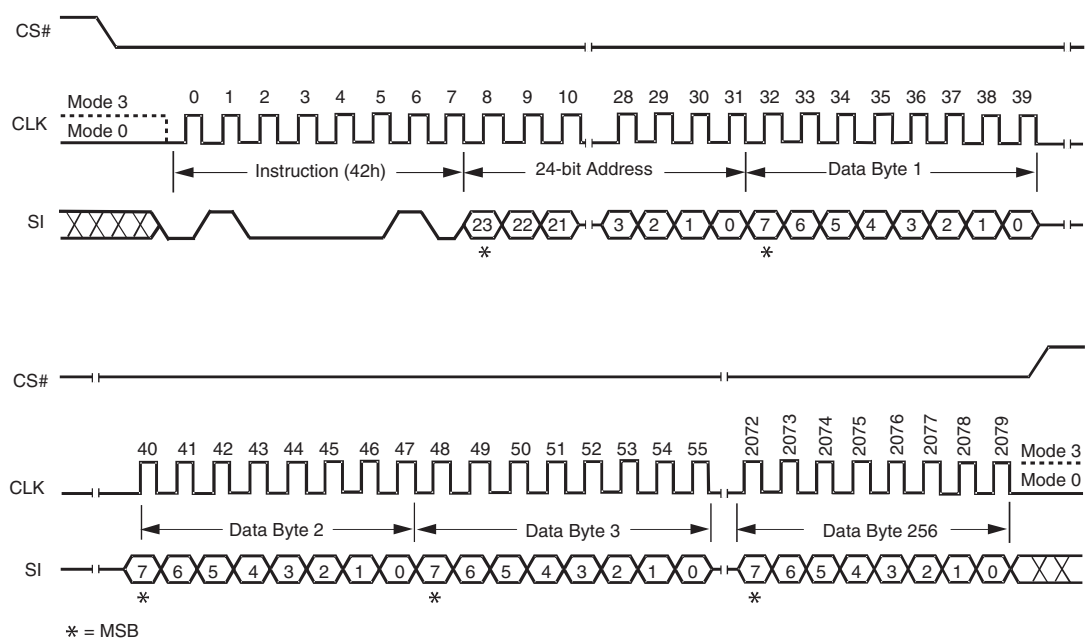
### 7.0.34 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) and at least one data byte, into the SI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device.

| Address | A23-16 | A15-12 | A11-8 | A7-0 |
|---|---|---|---|---|
| Security Register #1 | 00h | 0 0 0 1 b | 0 0 0 0 b | Byte Address |
| Security Register #2 | 00h | 0 0 1 0 b | 0 0 0 0 b | Byte Address |
| Security Register #3 | 00h | 0 0 1 1 b | 0 0 0 0 b | Byte Address |

The Program Security Register instruction sequence is shown in Figure 7.38. The Security Register Lock Bits (LB3:1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, and a Program Security Register instruction to that register will be ignored (see *Security Register Lock Bits (LB3, LB2, LB1)* on page 14 and *Page Program (02h)* on page 34 for detail descriptions).

**Figure 7.38** Program Security Registers Instruction Sequence

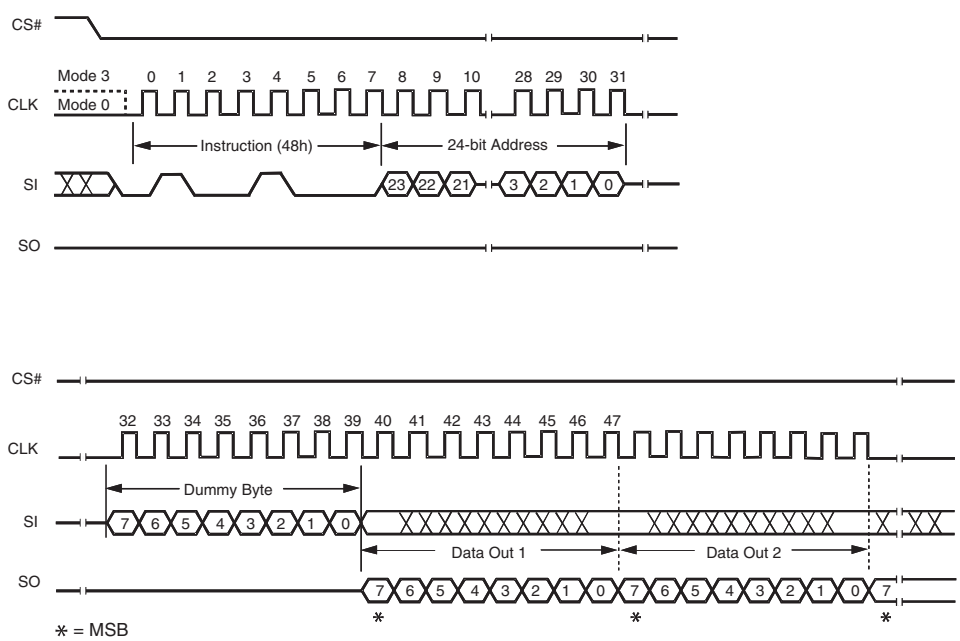


### 7.0.35 Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the three security registers. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the SI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte FFh), it will reset to 00h, the first byte of the register, and continue to increment. The instruction is completed by driving CS# high. The Read Security Register instruction sequence is shown in Figure 7.39. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1), the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from DC to a maximum of $F_R$ (see Section 8.6, *AC Electrical Characteristics on page 54*).

| Address | A23-16 | A15-12 | A11-8 | A7-0 |
|---|---|---|---|---|
| Security Register #1 | 00h | 0 0 0 1 b | 0 0 0 0 b | Byte Address |
| Security Register #2 | 00h | 0 0 1 0 b | 0 0 0 0 b | Byte Address |
| Security Register #3 | 00h | 0 0 1 1 b | 0 0 0 0 b | Byte Address |

**Figure 7.39** Read Security Registers Instruction Sequence



# 8. Electrical Characteristics

Specification for S25FL004K is Advance Information. See *Advance Information* designation at the beginning of this document.

## 8.1 Absolute Maximum Ratings

| Parameters(1) | Symbol | Conditions | Range | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | –0.6 to +4.0 | V |
| Voltage Applied to Any Pin | $V_{IO}$ | Relative to Ground | –0.6 to $V_{CC}$+0.4 | V |
| Transient Voltage on any Pin | $V_{IOT}$ | <20 ns Transient Relative to Ground | –2.0V to $V_{CC}$+2.0V | V |
| Storage Temperature | $T_{STG}$ | | –65 to +150 | °C |
| Lead Temperature | $T_{LEAD}$ | | (Note 2) | °C |
| Electrostatic Discharge Voltage | $V_{ESD}$ | Human Body Model (3) | –2000 to +2000 | V |

***Notes:***

1. *This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.*
2. *Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.*
3. *JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).*

## 8.2 Operating Ranges

| Parameter | Symbol | Conditions | Spec | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Supply Voltage (1) | $V_{CC}$ | $F_R$ = 104 MHz, $f_R$ = 50MHz | 3.0 | 3.6 | V |
| | | $F_R$ = 80 MHz, $f_R$ = 50MHz | 2.7 | | |
| Ambient Temperature, Operating | $T_A$ | Industrial | –40 | +85 | °C |

***Note:***

1. *$V_{CC}$ voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.*

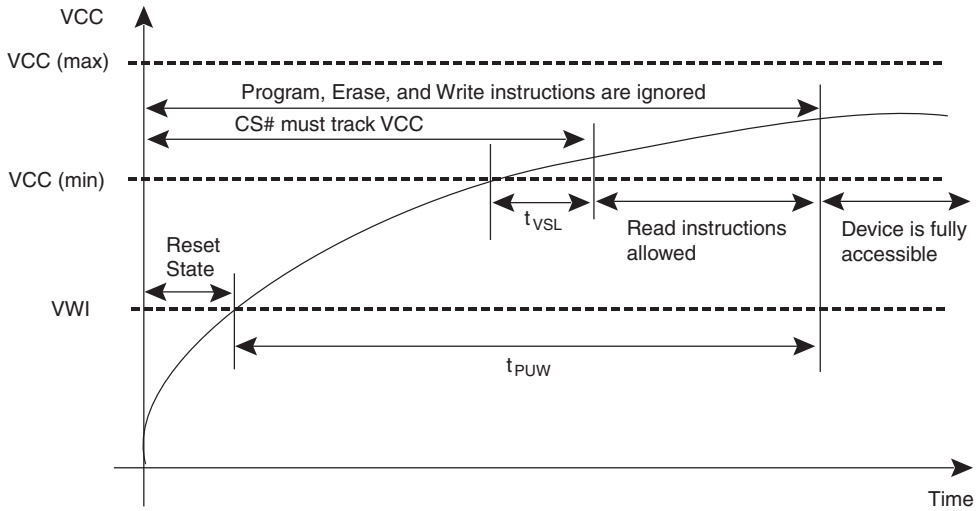
## 8.3 Power-up Timing and Write Inhibit Threshold

| Parameter | Symbol | Spec | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ (min) to CS# Low | $t_{VSL}$ (1) | 10 | | µs |
| Time Delay Before Write Instruction | $t_{PUW}$ (1) | 1 | 10 | ms |
| Write Inhibit Threshold Voltage | $V_{WI}$ (1) | 1.0 | 2.0 | V |

***Note:***

1. *These parameters are characterized only.*

**Figure 8.1** Power-up Timing and Voltage Levels




## 8.4 DC Electrical Characteristics

| Parameter | Symbol | Conditions | Spec | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Input Capacitance | $C_{IN}$ (1) | $V_{IN}$ = 0V (1) | | | 6 | pF |
| Output Capacitance | $C_{OUT}$ (1) | $V_{OUT}$ = 0V (1) | | | 8 | pF |
| Input Leakage | $I_{LI}$ | | | | ±2 | µA |
| I/O Leakage | $I_{LO}$ | | | | ±2 | µA |
| Standby Current | $I_{CC1}$ | CS# = $V_{CC}$, $V_{IN}$ = GND or $V_{CC}$ | | 25 | 50 | µA |
| Power-down Current | $I_{CC2}$ | CS# = $V_{CC}$, $V_{IN}$ = GND or $V_{CC}$ | | 1 | 5 | µA |
| Current: Read Data / Dual /Quad 1 MHz (2) | $I_{CC3}$ | C = 0.1 $V_{CC}$ / 0.9 $V_{CC}$<br>SO = Open | | 4/5/6 | 6/7.5/9 | mA |
| Current: Read Data / Dual /Quad 33 MHz (2) | $I_{CC3}$ | C = 0.1 $V_{CC}$ / 0.9 $V_{CC}$<br>SO = Open | | 6/7/8 | 9/10.5/12 | mA |
| Current: Read Data / Dual Output Read/ Quad Output Read 50 MHz (2) | $I_{CC3}$ | C = 0.1 $V_{CC}$ / 0.9 $V_{CC}$<br>SO = Open | | 7/8/9 | 10/12/13.5 | mA |
| Current: Read Data / Dual Output Read/ Quad Output Read 80 MHz (2) | $I_{CC3}$ | C = 0.1 $V_{CC}$ / 0.9 $V_{CC}$<br>SO = Open | | 10/11/12 | 15/16.5/18 | mA |
| Current: Write Status Register | $I_{CC4}$ | CS# = $V_{CC}$ | | 8 | 12 | mA |
| Current Page Program | $I_{CC5}$ | CS# = $V_{CC}$ | | 20 | 25 | mA |
| Current Sector/Block Erase | $I_{CC6}$ | CS# = $V_{CC}$ | | 20 | 25 | mA |
| Current Chip Erase | $I_{CC7}$ | CS# = $V_{CC}$ | | 20 | 25 | mA |
| Input Low Voltage | $V_{IL}$ | | | | $V_{CC}$ x 0.3 | V |
| Input High Voltage | $V_{IH}$ | | $V_{CC}$ x 0.7 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 100 µA | | | 0.2 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = –100 µA | $V_{CC}$ – 0.2 | | | V |

***Notes:***

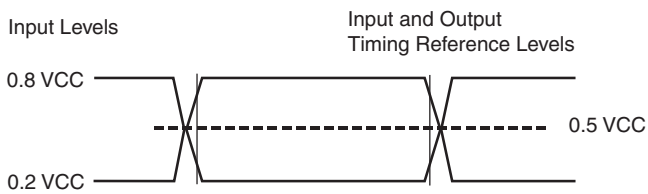
1. *Tested on sample basis and specified through design and characterization data. TA = 25°C, $V_{CC}$ = 3V.*
2. *Checker Board Pattern.*

## 8.5 AC Measurement Conditions

| Parameter | Symbol | Spec | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Load Capacitance | $C_L$ | | 30 | pF |
| Input Rise and Fall Times | $T_R$, $T_F$ | | 5 | ns |
| Input Pulse Voltages | $V_{IN}$ | 0.2 $V_{CC}$ to 0.8 $V_{CC}$ | | V |
| Input Timing Reference Voltages | IN | 0.3 $V_{CC}$ to 0.7 $V_{CC}$ | | V |
| Output Timing Reference Voltages | OUT | 0.5 $V_{CC}$ to 0.5 $V_{CC}$ | | V |

***Note:***
*1. Output Hi-Z is defined as the point where data out is no longer driven.*

**Figure 8.2** AC Measurement I/O Waveform




## 8.6 AC Electrical Characteristics

**Table 8.1** AC Electrical Characteristics (Sheet 1 of 2)

| Description | Symbol | Alt | Spec | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Clock frequency for all instructions except for Read Data instruction (03h)<br>3.0V-3.6V $V_{CC}$ and Industrial Temperature | $F_R$ | $f_C$ | D.C. | | 104 | MHz |
| Clock frequency for all instructions except for Read Data instruction (03h)<br>2.7V-3.6V $V_{CC}$ and Industrial Temperature | $F_R$ | $f_C$ | D.C. | | 80 | MHz |
| Clock frequency for Read Data instruction (03h) | $f_R$ | | D.C. | | 50 | MHz |
| Clock High, Low Time for all instructions except Read Data (03h) | $t_{CLH1}$, $t_{CLL1}$ (1) | $t_{CH}$, $t_{CL}$ | 6 | | | ns |
| Clock High, Low Time for Read Data (03h) instruction | $t_{CRLH}$, $t_{CRLL}$ (1) | | 8 | | | ns |
| Clock Rise Time peak to peak | $t_{CLCH}$ (2) | | 0.1 | | | V/ns |
| Clock Fall Time peak to peak | $t_{CHCL}$ (2) | | 0.1 | | | V/ns |
| CS# Active Setup Time relative to CLK | $t_{SLCH}$ | $t_{CSS}$ | 5 | | | ns |
| CS# Not Active Hold Time relative to CLK | $t_{CHSL}$ | | 5 | | | ns |
| Data In Setup Time | $t_{DVCH}$ | $t_{DSU}$ | 2 | | | ns |
| Data In Hold Time | $t_{CHDX}$ | $t_{DH}$ | 5 | | | ns |
| CS# Active Hold Time relative to CLK | $t_{CHSH}$ | | 5 | | | ns |
| CS# Not Active Setup Time relative to CLK | $t_{SHCH}$ | | 5 | | | ns |
| CS# Deselect Time (for Array Read -> Array Read) | $t_{SHSL1}$ | $t_{CSH}$ | 10 | | | ns |
| CS# Deselect Time (for Erase or Program -> Read Status Registers)<br>Volatile Status Register Write Time | $t_{SHSL2}$ | $t_{CSH}$ | 50<br>50 | | | ns |

**Table 8.1** AC Electrical Characteristics (Sheet 2 of 2)

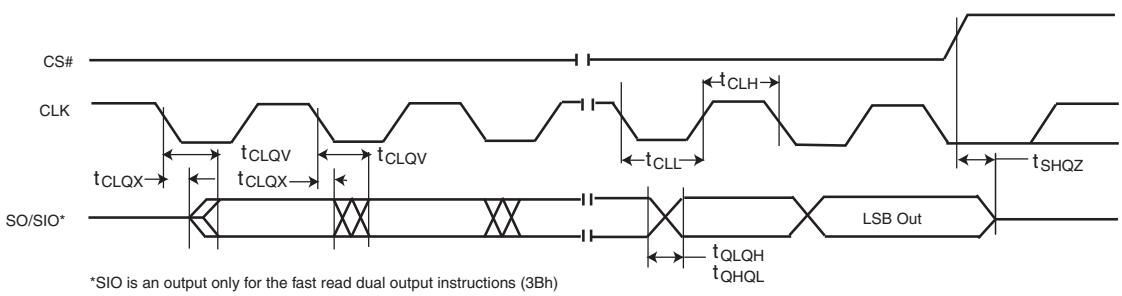
| Description | Symbol | Alt | Spec | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Output Disable Time | $t_{SHQZ}$ (2) | $t_{DIS}$ | | | 7 | ns |
| Clock Low to Output Valid | $t_{CLQV1}$ | $t_{V1}$ | | | 7 | ns |
| Clock Low to Output Valid (for Read ID instructions) | $t_{CLQV2}$ | $t_{V2}$ | | | 7.5 | ns |
| Output Hold Time | $t_{CLQX}$ | $t_{HO}$ | 0 | | | ns |
| HOLD# Active Setup Time relative to CLK | $t_{HLCH}$ | | 5 | | | ns |
| HOLD# Active Hold Time relative to CLK | $t_{CHHH}$ | | 5 | | | ns |
| HOLD# Not Active Setup Time relative to CLK | $t_{HHCH}$ | | 5 | | | ns |
| HOLD# Not Active Hold Time relative to CLK | $t_{CHHL}$ | | 5 | | | ns |
| HOLD# to Output Low-Z | $t_{HHQX}$ (2) | $t_{LZ}$ | | | 7 | ns |
| HOLD# to Output High-Z | $t_{HLQZ}$ (2) | $t_{HZ}$ | | | 12 | ns |
| Write Protect Setup Time Before CS# Low | $t_{WHSL}$ (3) | | 20 | | | ns |
| Write Protect Hold Time After CS# High | $t_{SHWL}$ (3) | | 100 | | | ns |
| CS# High to Power-down Mode | $t_{DP}$ (2) | | | | 3 | µs |
| CS# High to Standby Mode without Electronic Signature Read | $t_{RES1}$ (2) | | | | 3 | µs |
| CS# High to Standby Mode with Electronic Signature Read | $t_{RES2}$ (2) | | | | 1.8 | µs |
| CS# High to next Instruction after Suspend | $t_{SUS}$ (2) | | | | 20 | µs |
| Write Status Register Time | $t_W$ | | | 10 | 15 | ms |
| Byte Program Time (First Byte) (4) | $t_{BP1}$ | | | 20 | 50 | µs |
| Additional Byte Program Time (After First Byte) (4) | $t_{BP2}$ | | | 2.5 | 12 | µs |
| Page Program Time | $t_{PP}$ | | | 0.7 | 3 | ms |
| Sector Erase Time (4 KB) | $t_{SE}$ | | | 30 | 200/400 (5) | ms |
| Block Erase Time (32 KB) | $t_{BE1}$ | | | 120 | 800 | ms |
| Block Erase Time (64 KB) | $t_{BE2}$ | | | 150 | 1,000 | ms |
| Chip Erase Time | $t_{CE}$ | | | 1 | 4 | s |

***Notes:***

1. *Clock high + Clock low must be less than or equal to $1/f_C$.*
2. *Value guaranteed by design and/or characterization, not 100% tested in production.*
3. *Only applicable as a constraint for a Write Status Register instruction when SRP0 Bit is set to 1.*
4. *For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed.*
5. *Max Value $t_{SE}$ with <50K cycles is 200 ms and >50K and <100K cycles is 400 ms.*

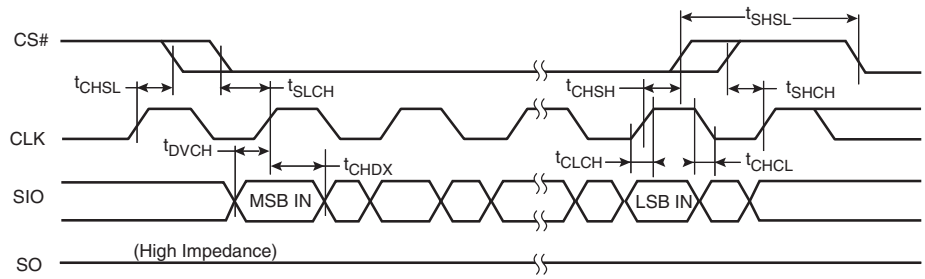
## 8.7 Serial Output Timing

**Figure 8.3** Serial Output Timing



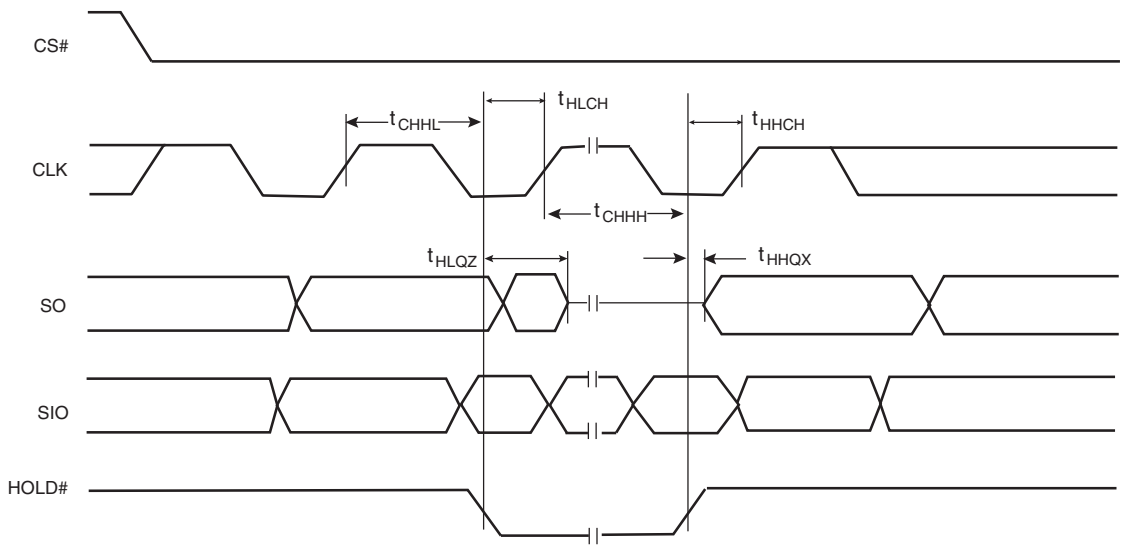
## 8.8 Serial Input Timing

**Figure 8.4** Serial Input Timing



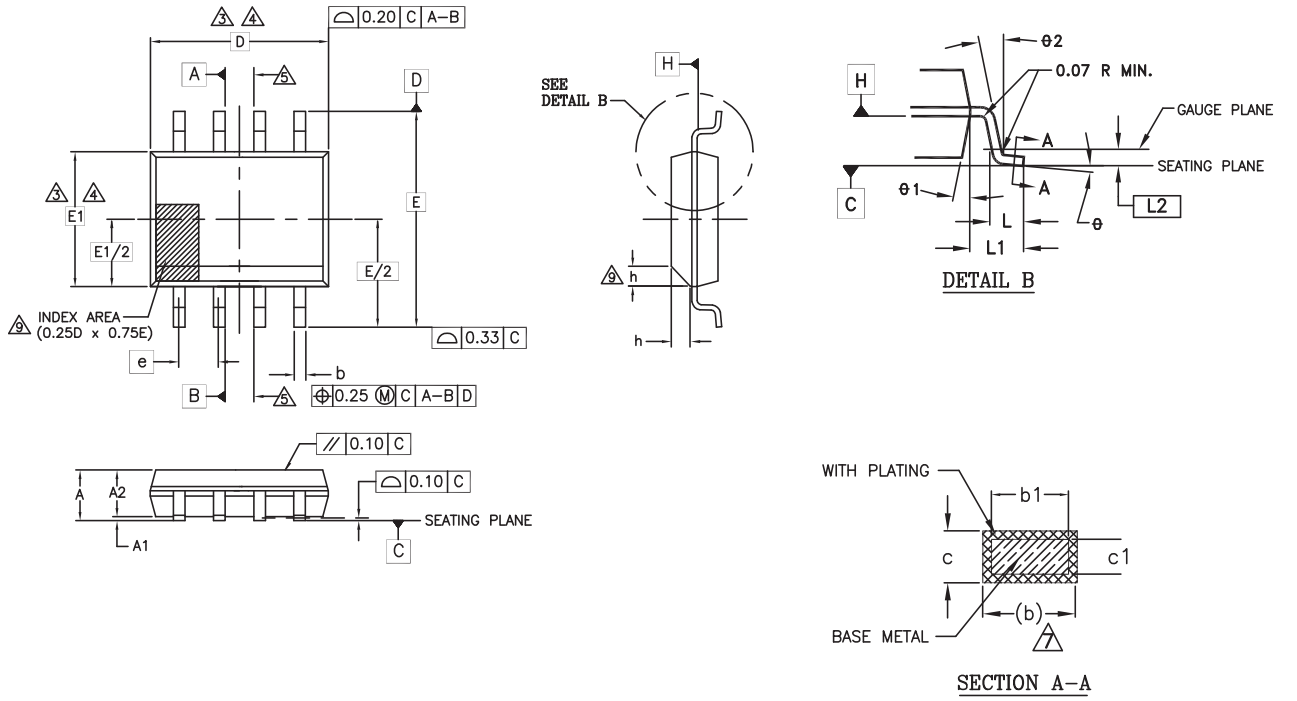

## 8.9 Hold Timing

**Figure 8.5** Hold Timing



# 9. Physical Dimensions

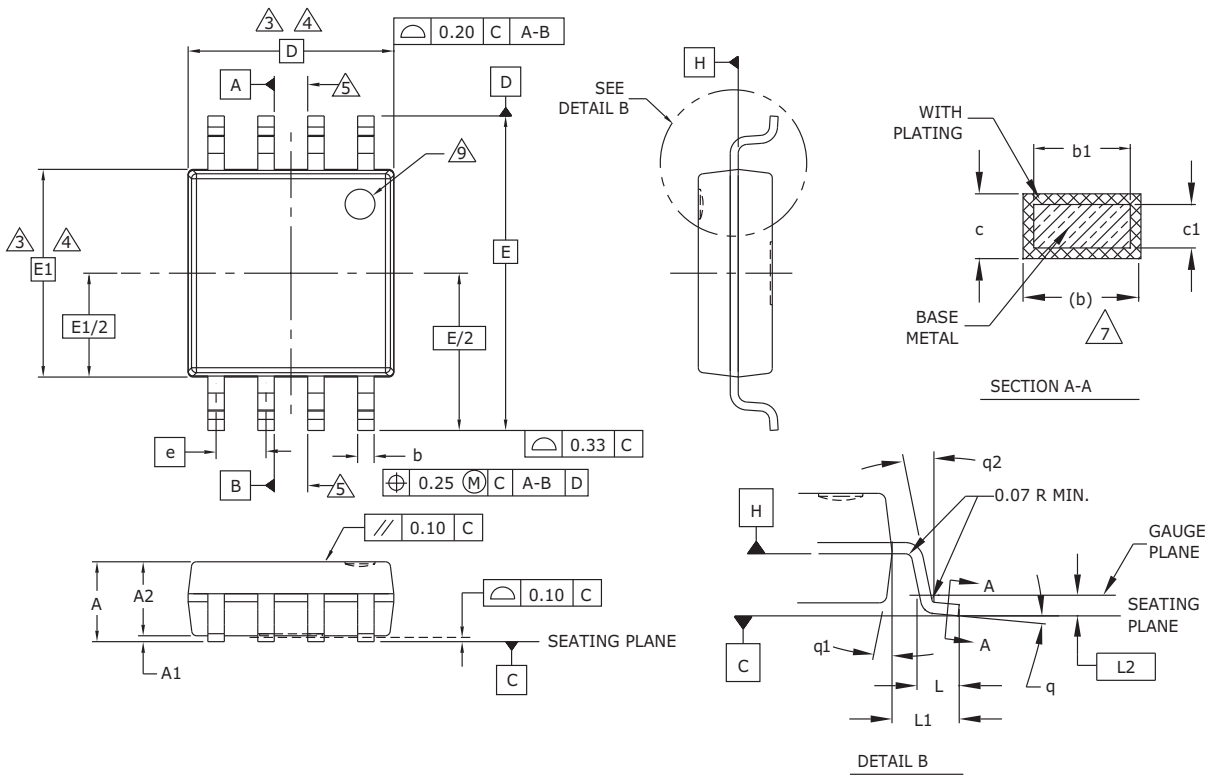
## 9.1 SOA008 narrow — 8-pin Plastic Small Outline Package (150-mils Body Width)




| PACKAGE | SOA 008(INCHES) | | SOA 008(MM) | |
|---|---|---|---|---|
| JEDEC | MS-012(D)AA | | MS-012(D)AA | |
| SYMBOL | MIN | MAX | MIN | MAX |
| A | .0531 | .0688 | 1.35 | 1.75 |
| A1 | .0039 | .0098 | 0.10 | 0.25 |
| A2 | .052 | .061 | 1.32 | 1.55 |
| b | .012 | .020 | 0.31 | 0.51 |
| b1 | .011 | .019 | 0.27 | 0.48 |
| c | .0067 | .0098 | 0.17 | 0.25 |
| c1 | .0067 | .009 | 0.17 | 0.23 |
| D | .193 BSC | | 4.90 BSC | |
| E | .236 BSC | | 6.00 BSC | |
| E1 | .1535 BSC | | 3.90 BSC | |
| e | .050 BSC | | 1.27 BSC | |
| L | .0161 | .035 | 0.41 | 0.89 |
| L1 | .041 REF | | 1.04 REF | |
| L2 | .010 BSC | | 0.25 BSC | |
| N | 8 | | 8 | |
| h | 0.10 | 0.196 | 0.25 | 0.50 |
| θ | 0° | 8° | 0° | 8° |
| θ1 | 5° | 15° | 5° | 15° |
| θ2 | 0° REF | | 0° REF | |

NOTES:
1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

## 9.2 SOC008 wide — 8-pin Plastic Small Outline Package (208-mils Body Width)




| PACKAGE | SOC 008 (inches) | | SOC 008 (mm) | |
|---|---|---|---|---|
| JEDEC | | | | |
| SYMBOL | MIN | MAX | MIN | MAX |
| A | 0.069 | 0.085 | 1.753 | 2.159 |
| A1 | 0.002 | 0.0098 | 0.051 | 0.249 |
| A2 | 0.067 | 0.075 | 1.70 | 1.91 |
| b | 0.014 | 0.019 | 0.356 | 0.483 |
| b1 | 0.013 | 0.018 | 0.330 | 0.457 |
| c | 0.0075 | 0.0095 | 0.191 | 0.241 |
| c1 | 0.006 | 0.008 | 0.152 | 0.203 |
| D | 0.208 BSC | | 5.283 BSC | |
| E | 0.315 BSC | | 8.001 BSC | |
| E1 | 0.208 BSC | | 5.283 BSC | |
| e | .050 BSC | | 1.27 BSC | |
| L | 0.020 | 0.030 | 0.508 | 0.762 |
| L1 | .055 REF | | 1.40 REF | |
| L2 | .010 BSC | | 0.25 BSC | |
| N | 8 | | 8 | |
| $\theta$ | 0° | 8° | 0° | 8° |
| $\theta$1 | 5° | 15° | 5° | 15° |
| $\theta$2 | 0° | | 0° | |

NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

3432 \ 16-038.03 \ 10.28.04

# 10. Revision History

| Section | Description |
|---|---|
| **Revision 01 (July 30, 2010)** | |
| | Initial release |
| **Revision 02 (October 18, 2010)** | |
| Global | Changed data sheet designation from Advanced Information to Preliminary |
| Instructions | Moved Instructions as a separate section<br>Updated Instruction Set Table to add 48h code to Read SFDP Register |
| Write Status Register | Updated instruction sequence diagram |
| Sector Erase | Corrected description |
| 32 KB Block Erase | Corrected description |
| 64 KB Block Erase | Corrected description |
| Erase Security Registers | Corrected table |
| Program Security Registers | Corrected table |
| Read Security Registers | Corrected table |
| AC Electrical Characteristics | Added Alternate description for Clock High, Low Time except Read Data (03h) |
| Serial Output Timing | Update timing diagram |
| Physical Dimensions | Corrected SOA008 package outline drawing |

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