Hi-Fi Voice Synthesis LSI
BU6940FV

Index

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revision history

Date	Rev No	remarks
Apl/10/07	1.00	Initial Version
Apl/11/07	1.01	P28(at 12.4.2.14Serial Flash commands list modified "BF"h (dummy command) to write data at 2nd byte of write status register)
Apl/18/07	2.00	Changed operating voltage from 2.7V~5.5V to 2.7V~3.6V
Dec/01/08	2.01	Change phrase numbers from 512 to 480
Jan/23/09	2.09	add DAC characteristics changed REFOUT discription cahnged RXCB discription add caution use STBY add CLK Timing (8.192/4.096/2.048MHz) P19(add notice command timing) P19(correct TXD bit2 bit4,bit3 bit5) P22(add CLK16SEL="L",at 4MHz 32kHz samplig) P23(add Notice STOP command) P27(fade Interval setting 8bit 7bit) P41(add caution STOP command) new LOGO

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1. Function overview and Features

BU6940FV is a voice synthesis IC which can playback highly compressed voice/audio data stored in external SPI-interface ROM by commands from serial interface or from the pins. Maximum 2 channels of voice/audio data can be decoded and playback simultaneously. The main functions are described below.

1) High compression algorithm ("ROHM-HiFi") is adopted. Available bit-rate is 16kbps   192kbps. At 2ch simultaneous playback mode, Available bit-rate is 16kbps - 64kbps at 32kHz sampling or 16kbps~32kbps at 16kHz sampling.

2) Voice/audio data is stored in serial Flash ROM which is connected to BU6940FV through SPI-serial Interface   See chapter13.9. for available SPI serial ROM   . Duration for playback is 32seconds/Mbits(standard) or max 64s/Mbits(Maximum).

3) The package is SSOP-B28, which is one of the smallest size for voice synthesis LSI. Also,BU6940FV is completely pin-compatible architecture with BU6954FV/BU6952FV(except for pins for direct mode pins). For this feature, BU6940FV is also used for pre-production system before mass-production using BU6954FV.

4) Input system clock: 16.384MHz/8.192MHz/4.096MHz/2.048MHz (see Chapter 11).

5) Audio sampling rate is 32KHz or 16kHz and Built-in 16bits DAC.

6) Operation by single power supply. Available voltage:2.7 to 3.6V

7) Max numbers of tunes : 480

8)HOST-I/F is selectable from serial interface with status or direct-mode   pin.

9) Enable to access(read/write) data stored in serial ROM connected directly to BU6940FV.   Available Serial ROM is described at chapter 13.9. Access unit is 512kbit.

10) Various play modes are available.

    play modes from serial Interface

      - decodable   2 channels simultaneously

      -adjustable volume at each track independently.

    -enable to playback tunes which are registered in the sequencer list. Order of tunes are randomly selected. Max 16 tunes can be registered.

     -For each track, enable to playback a selected tune or to playback tunes in the sequencer list with/without loop.

    -fade-in and fade-out functions are supported.

    Play modes from direct pin control

    -decodable only 1channel.

    -maximum 8 tunes are registered to play.

    -sequencer is not supported. Normal play mode only.

2. Applicable products

    electronics/electric products,   home appliance, factory appliance, etc.

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3.Absolute maximum rating

Ta=25

Item	Symbol	Ratings	Unit
Power dissipation[*)]	Pd	640	mW
Applied voltage	V_{DD}	-0.2 7.0	V
Input voltage	V_{IN}	-0.2 VDD+0.3	V
Operating temperature range	T_{OPR}	-40 +85	
Storage temperature range	TSTG	-50 125	

*)   Over Ta = 25C or more, reducing   6.4mW per   .

Radiation resistance design is not arranged.

4. Operating conditions

(Ta=-40   +85   unless otherwise specified)

Item	Symbol	Specified value			Unit	Condition
		Min	Typ	Max		
Operation power-supply voltage	VDD5_IN	2.7		3.6	V	

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5. Electric characteristic (DC characteristic)
5.1.DC Characteristics

VDD5_IN=3V   Ta=25

Item	Symbol	Specified value			Unit	Condition	Circuit form
		Min	Typ	Max			
"H" Input Voltage	V_{IH}	0.7VDD			V		
"L" Input Voltage	V_{IL}			0.3VDD	V		
"H" Output Voltage	V_{OH}	VDD-0.4			V	IO=2.0mA	
"L" Output Voltage	V_{OL}			0.4	V	IO=2.0mA	
"H" Input current	I_{IH}			10	µA	VIH=VDD	
"L" Input current	I_{IL}			-10	µA	VIL=GND	
Static consumption current	I_{ST}			10	µA	$V_i=V_{DD}$orGND	

5.2.DAC characteristics

VDD5_IN=3V   (Ta=25)

Item	Symbol	Specified Value			Unit	Condition
		Min.	Typ.	max.		
DACOUT output load registance	R_{AOUT}	10			K	at No signal
DACOUT Output Voltage	V_{AOUT}	GND		VDD	V	at No load

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6. Outline dimensions
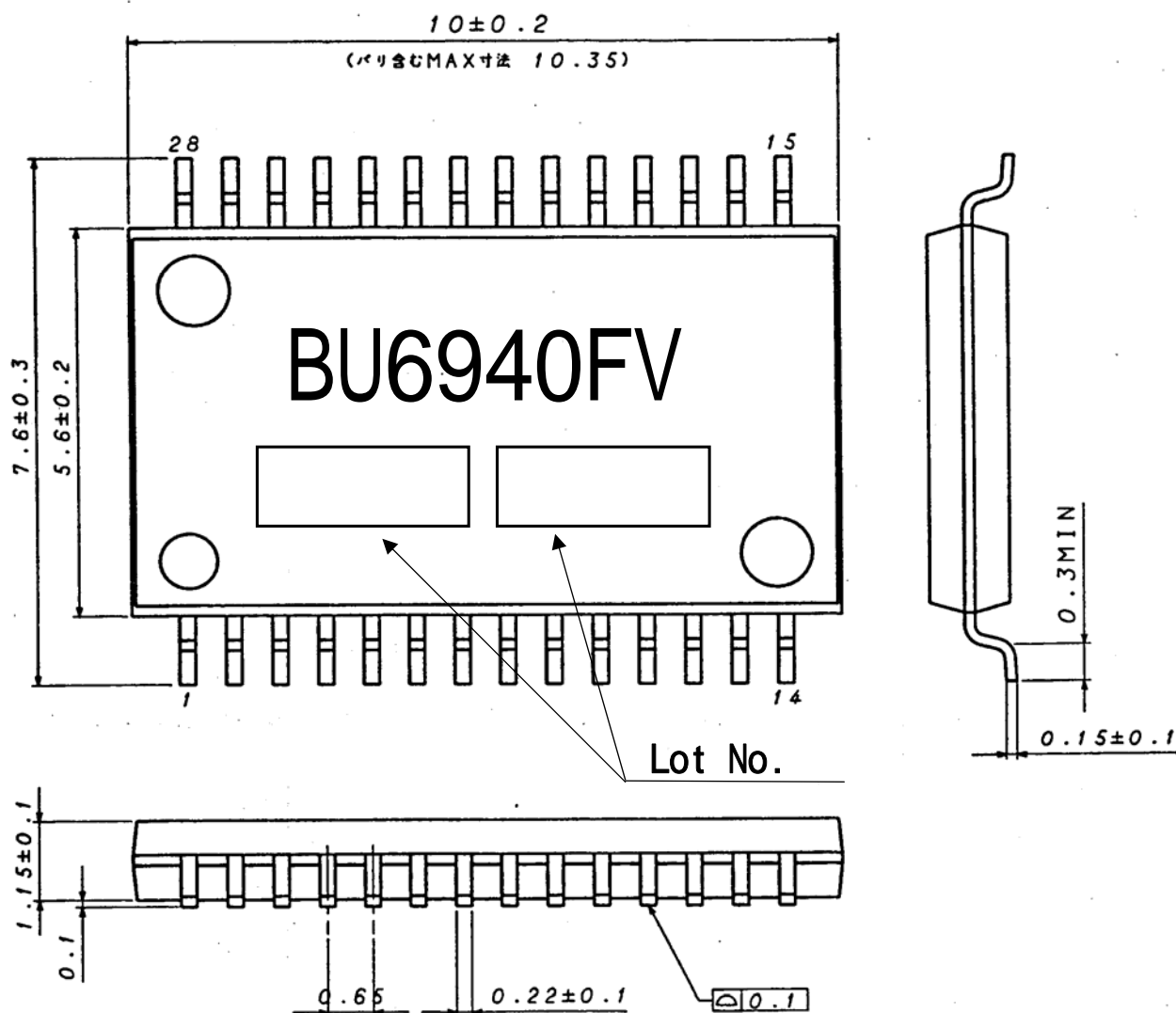
(UNIT:mm)

7. Block Diagram

Figure7-1. Block Diagram

8. Pin No. and Pin Name

8.1. Pin name Detailed table

Table 8-1.Pin name Detailed table

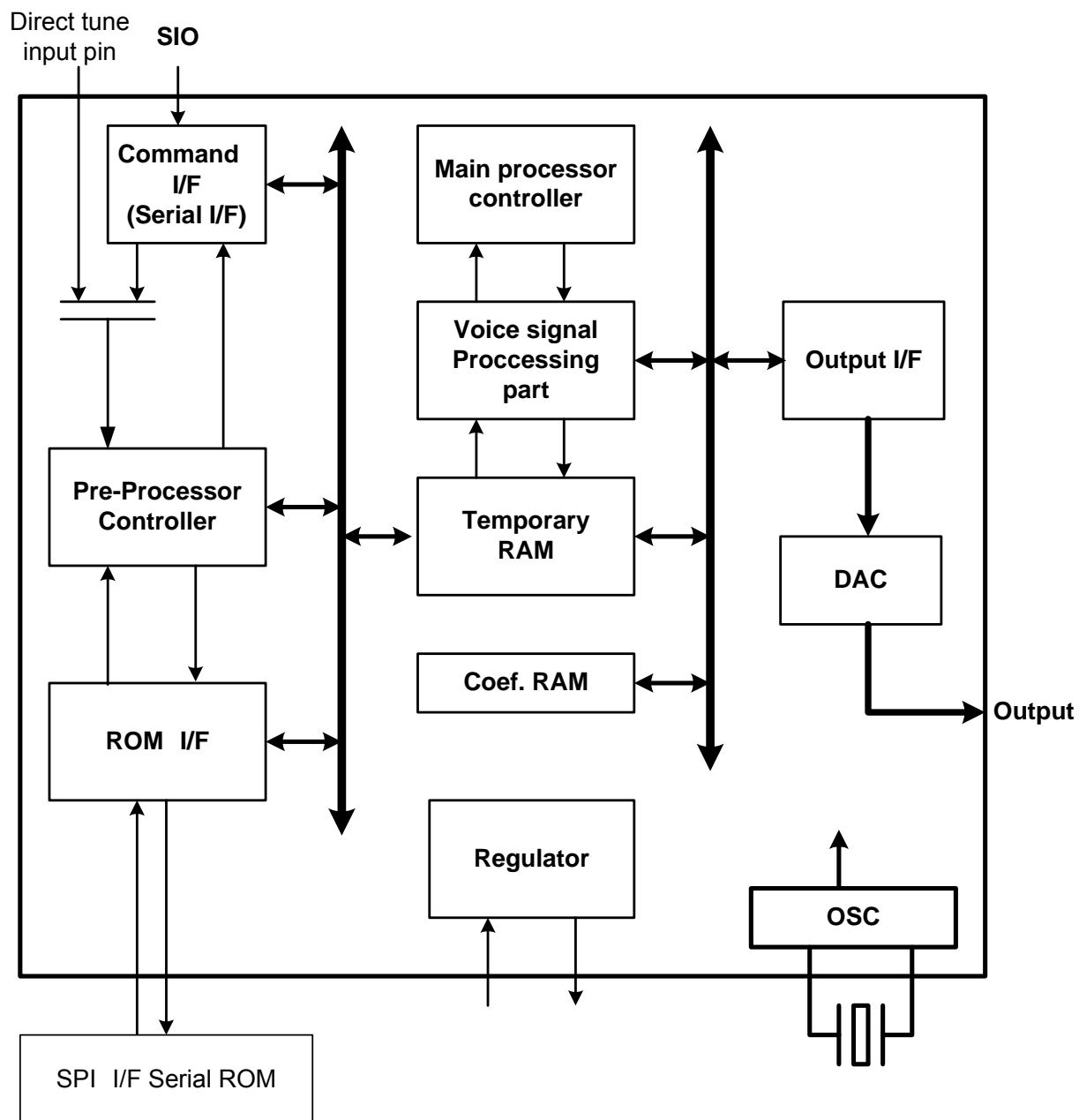| PIN NO.	Pin Name	I/O	IO Circuit form	Function
1	GND			GND
2	VSEL2/TXD	IO		tune number pin#2 / Serial Interface output data
3	VSEL1/RXD	I	A	tune number pin#1 / Serial Interface input data
4	VSEL0/RXCB	I	A	tune number pin#0 / Serial Interface CLK
5	TSEVENT/BUSY	O	A	Playing / ending flag("H":playing "L":stop) accessing Flash ROM ("H" busy "L" not busy)
6	VSEL3/SYNCREQ	IO		tune number pin#3/Synchronous character request ("H" synchronization error)
7	GND			GND
8	VDD1.8_IN	I	C	Core power supply input [3]
9	REG18	O	B	Core power supply output [3]
10	STBY	I	A	Standby ("H" oscillation stop) normally "L"
11	TESTEN	I	A	Test Input("L" fixation
12	VDD5_IN			Power supply input
13	SPISCK	O	A	Clock for serial SPI-ROM
14	SPISO	O	A	Serial output data to serial SPI-ROM
15	SPISI	I	A	Serial Input data from serial SPI-ROM
16	SPICEB	O	A	chip enable for serial SPI-ROM
17	GND			GND
18	VSEL4/BFULLB	IO		tune number pin#4 /command buffer Full signal
19	APOFF	I	A	DAC Circuit Power off
20	CLK16SEL	I	A	Clock selection "H":16.384Mhz mode "L":4.096MHzmode
21	REFOUT	O	B	LSI TEST Pin (attach capacitance(>10uF))
22	DACOUT	O	B	DACout
23	GND			GND
24	VDD5_IN			Power supply input
25	RESETB	I	B	Reset pin (low active)
26	SIO_ENBL	I	A	Selection of host interface(SIO or direction pin input[*1])
27	XIN	I		Oscillation cell input [*2]
28	XOUT	O		Oscillation cell Output [*2]

*1) At SIO_ENBL ="L", VSEL2, VSEL1, VSEL0 and VVOLH is valid, and SIO is invalid.

*2) At no setting CLK setting Register, Clock is 16.384MHz at CLK16SEL="H",,4.096MHz at CLK16SEL ="L".

*3) pin#8 and pin#9 should be connected in a shortest pass, and attach capacitance(>10uF) as following figure.
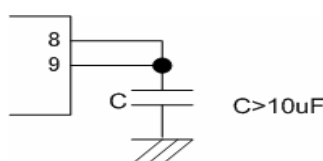
8.2. Circuit form

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(A) CMOS   (B)   (C)

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(A) CMOS   (B)

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CMOS

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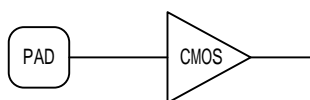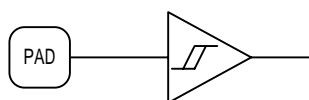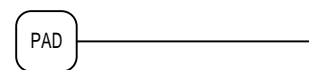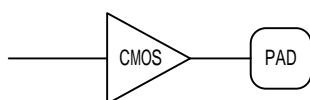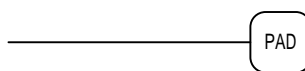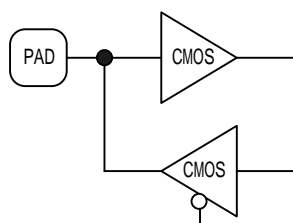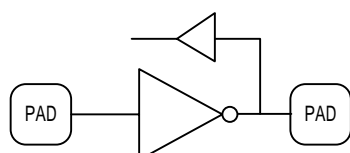
9 Application examples
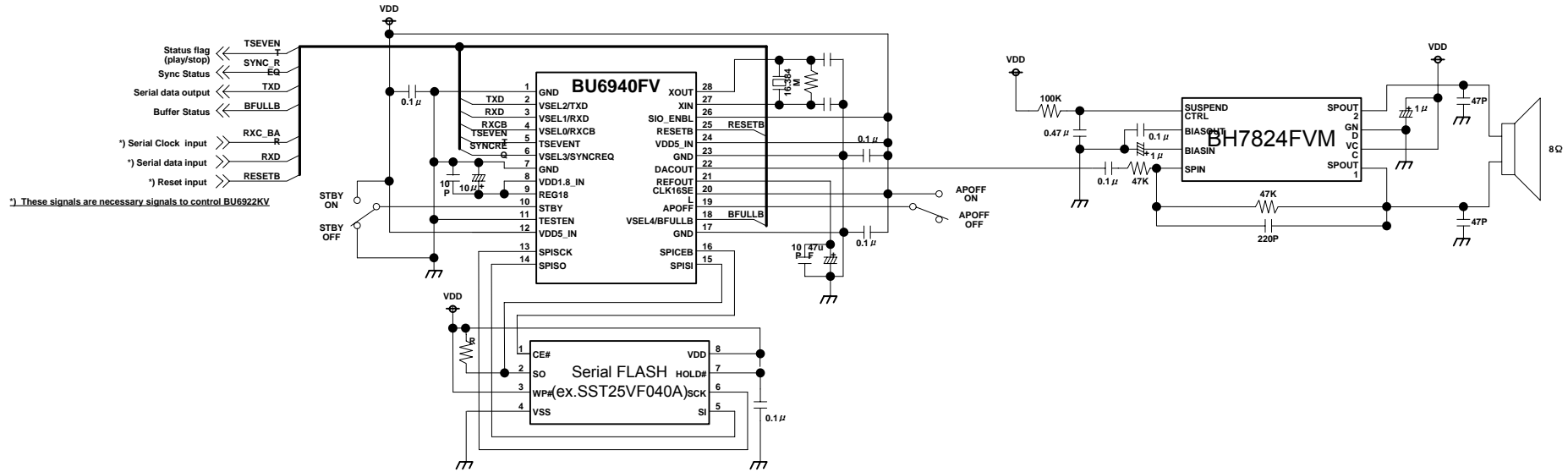
10.Interface Timing

10.1. XIN
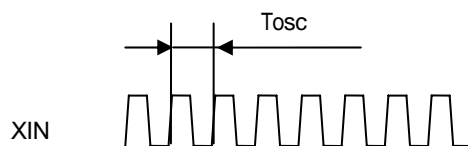
Figure 10-1. XIN Timing

Items	Name	Min	Typ	Max	Unit
Clock Frequency*1)	fosc		16.384		MHz
			8.192		
			4.096		
			2.048		
Clock Duty	Wosc	45		55	%

*1) available Clock Frequency is due to Sysytem CLK setting Registor and PIN assign(CLK16SEL).

10.2. RESETB
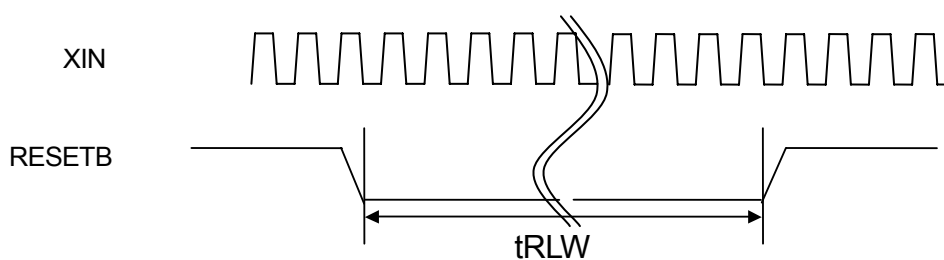
Figure 10-2. Reset timing

Item	Symbol	Min	Typ	Max	Unit
Reset "L" pulse width	tRLW	16			CLK

SIO commands which is invoked within 1ms after reset is discarded because of the chip initialization stage.

10.3. Serial interface　RXCB, RXD, TXD
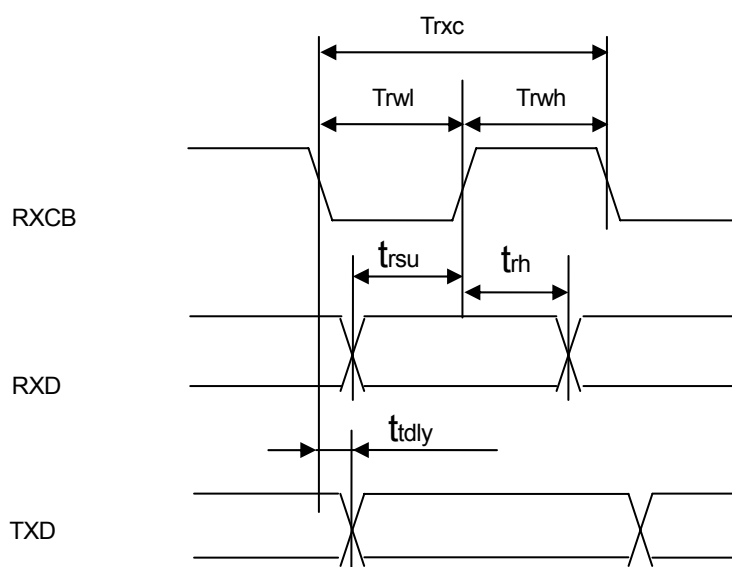
Figure 10-3. Serial interface timing

Item	Symbol	Min	Typ	Max	Condition	Unit
RXCB Cycle	Trxc	10*Tosc			Normal Play	ns
RXCB Lo Cycle	Trwl	*Tosc				ns
RXCB Hi Cycle	Trwh	*Tosc				ns
RXCB Cycle	Trxc	16*Tosc			Flash R/W	ns
RXCB Lo Cycle	Trwl	7*Tosc				ns
RXCB Hi Cycle	Trwh	7*Tosc				ns
RXD Setup Time	trsu	2*Tosc				ns
RXD Hold Time	trh	2*Tosc				ns
TXD Output delay	ttdly			*Tosc		ns

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10.4. Serial Flash ROM Interface
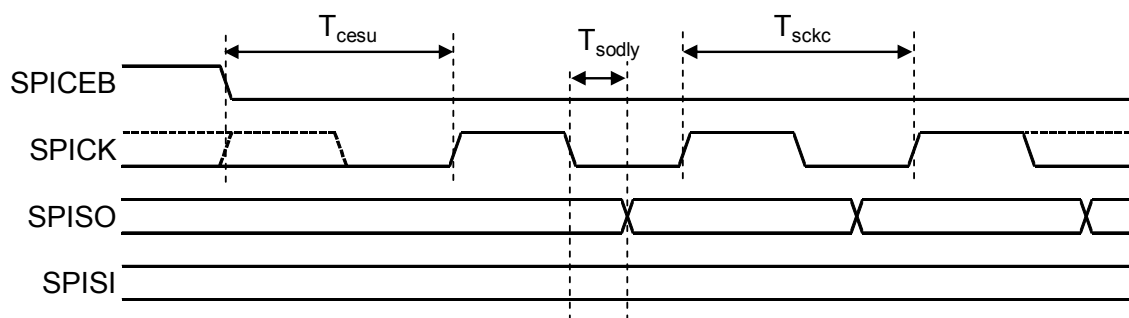
Figure 10-4-1.Serial Flash ROM Output
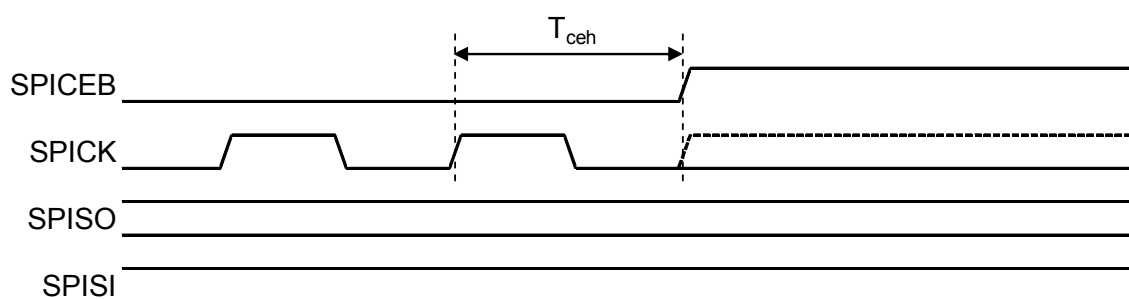
Figure 10-4-2.Serial Flash ROM Output
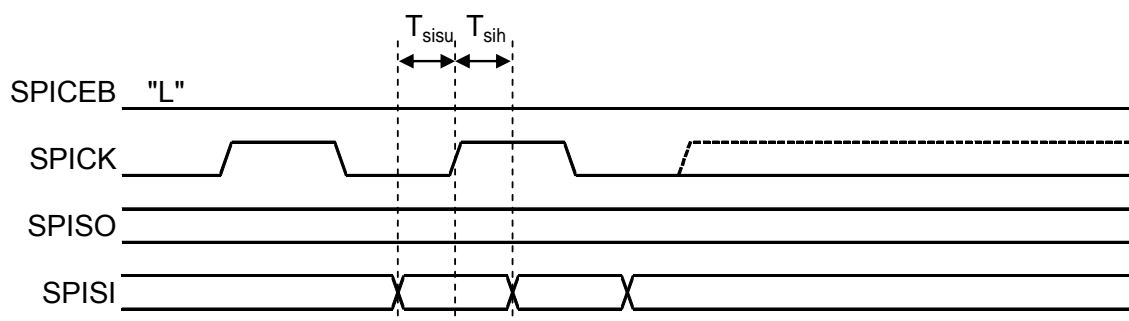
Figure 10-4-3.Serial Flash ROM Intput Timing

Item	Symbol	Min	Typ	Max	Unit
SPISCK Cycle	Tsckc		Tosc		ns
SPICEB Setup Time	Tcesu	Tosc			ns
SPICEB Hold Time	Tceh	Tosc			ns
SPISI Setup Time	Tsisu	10			ns
SPISI Hold Time	Tsih	3			ns
SPISO Output delay	Tsodly			10	ns

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11 System Clock

For System Input Clock, 16.384MHz/8.192MHz/4.096MHz/2.048MHz is available. [1)]

Followings are the table of parameters and performance.

System Clock	Value of CLK16SEL Pin	Setting from SIO	Numbers of channels	Bit rate (kbps) [2)] playing only 1 channel	Available Performance Bit rate (kbps) [2] playing 2 channels simultaneously	
					Sampling frequency 32KHz	Sampling frequency 16KHz
16.384MHz	"H"		2	16 128	16 64	16 32
8.192MHz	"H"	SCLK=001b	2	16 64	16 64	16 32
4.096MHz	"L"		2	16 64	16 64	16 32
2.048MHz	"L"	SCLK=001b	1	16 32	-	-

*1) When SIO is not used, available system clock is 16.384MHz or 4.096MHz only.

*2) Noted that Available bit-rate is different from single playback and multi-channel playback.

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12. Command Interface

Command interface is a serial interface receiving 8 or 16 bits command data synchronized with input clock, non parity, and sync-code (BFh). Sync-code is a fixed value, BF (h). The order of received data is LSB FAST.

12.1. Command communication

The command is communicated with clocks and the data as follows;

(1) Serial data transfer clock input (RXC_BAR); retrieves data by rising edge.
Frequency shall be equal to or less than 1MHz.

(2) Serial data input (RXD); 8 bits or 16 bits serial data (LSB FAST).

(3) Sync-code request output (SYNC_REQ); when this signal is "H", sync-code should be sent followed by the commands.
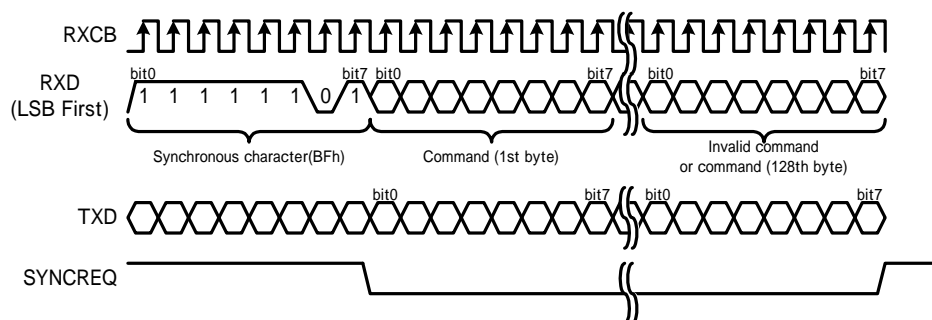
Figure 12-1. Serial interface time chart

At Figure.8-1, sync-code (more than 1 byte) is input before sending command. The maximum chunk of consecutive commands is 128 bytes after sync-code. If more than 129 bytes of command are consecutively input, 129th byte or later is ignored. Noted that, if 128th byte is the first byte of 2 byte command, 129th byte (2nd byte of 2 byte command) can be accepted.

If 128th byte is sync-code, it is ignored. In this case, SYNCREQ becomes "H" and its status becomes "waiting" for sync-code.

After command transfer is completed, interface shall be one of the following states until next command transfer.

1. continue to input sync-code.
2. stop clock (RXC_BAR)

12.2. Command Buffer Full Signal

There are 16 command stack buffer ("play command" and "tune command") for each channel.

BFULLB terminal becomes "L" when stack buffer of any channel becomes FULL.

During "Sequence Play", BFULLB does not become "L" even when Sequence buffer is overflown.

Other commands not stated the above is activated just after being invoked without being qued.
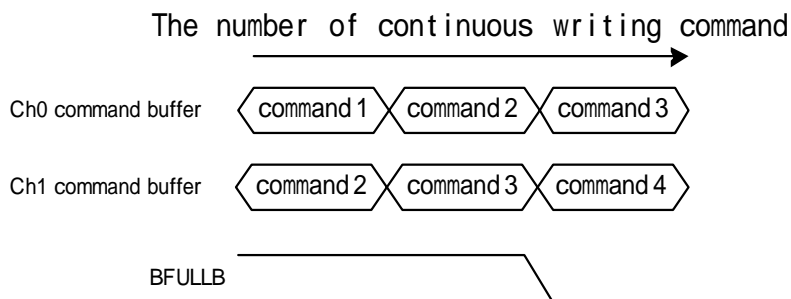
Figure 12-2. Command buffer FULL signal

12.3. Status signal

BU6940FV outputs the following status signals.

12.3.1. SYNCREQ

SYNCREQ is a sync-code request signal. "L" shows the state of synchronization, and "H" shows the state of "waiting for sync-code", or synchronization error.
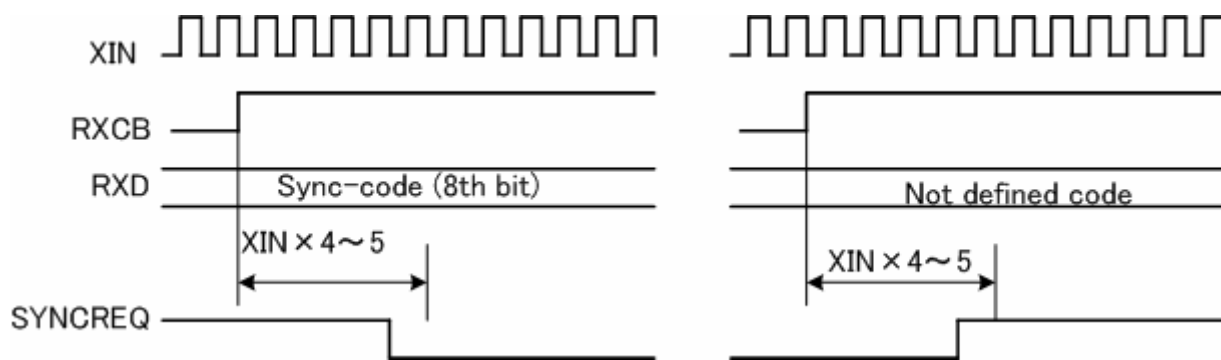
Figure 12-3-1. SYNCREQ timing

12.3.2. TSEVENT

TSEVENT signal becomes "H" when any of the track receives play command.
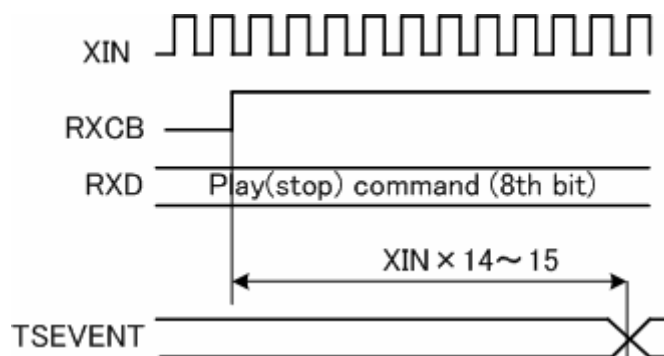
Figure 12-3-2a. TSEVENT timing

Noted that outputting sound has several ms delay after BU6930 accepts play command.
When stop commands are issued and accepted to all tracks, TSEVENT signal becomes "L".
Noted also that there is several ms delay until the sound stops after stop command is issued.
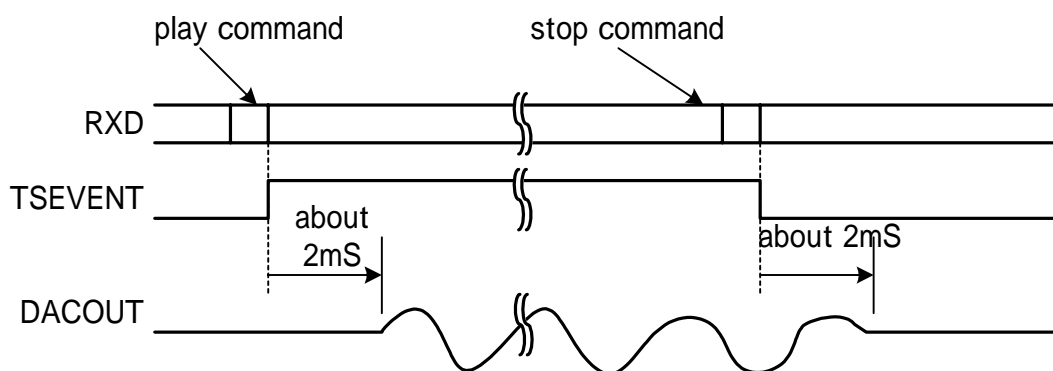
Figure 12-3-2b.TSEVENT and DACOUT timing

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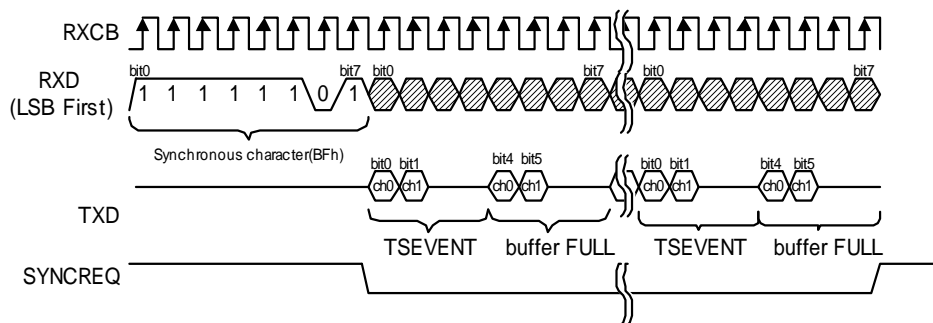
12.3.3. TXD

Figure 12-3-3. TXD output timing chart

bit	Item	Description
0	TSEVENT	Ch0 TSEVENT flag (H: playing)
1		Ch1 TSEVENT flag (H: playing)
4	Command buffer FULL	Ch0 BFULL flag (H: Buffer FULL)
5		Ch1 BFULL flag (H: Buffer FULL)

12.4. Command details

12.4.1. Command list

All commands are 1 byte or 2 bytes command.

Table 12-4-1 shows the command list. Also, details of each command are described from the later page.

Table 12-4-1 command list

Content of command	Bit allocation(CMD[7:0])							
	7	6	5	4	3	2	1	0
System setting	0	0	0	0	0	1	0	MODE
System CLK setting	0	0	0	0	1	SCLK		
Software reset	0	0	0	1	1	1	1	1
LOOP setting	0	1	0	0	1	Loop	ChSel	
Pause	0	1	0	0	0	1	ChSel	
Play	0	0	1	0	Mode	Loop	ChSel	
Stop	0	1	0	0	0	0	ChSel	
Sequence clear	0	1	0	1	1	0	ChSel	
Buffer Clear	0	1	0	1	1	1	ChSel	
Tune selection	1	1	0	1	0	Mode	ChSel	
	Tune (00h DFh,F0h~FFh)							
Tune selection	1	1	0	1	1	Mode	ChSel	
	(Tune-256) (00h DFh, F0h~FFh)							
Volume	1	0	0	1	Fade	Master	ChSel	
	0	0	0	Vol				
Fade volume initial value	1	0	1	0	0	0	ChSel	
	0	0	0	Vol				
Fade interval time	1	0	1	0	0	1	ChSel	
	0	Time						
Flash control	1	1	1	0	FlsCmd			
	12-4-2 See the Detail of each command(14).							
Synchronization	1	0	1	1	1	1	1	1

Noted) When the command which is not specified   is transmitted, operation is not guaranteed.

Commands of "Tune selection" and " play" is in buffered (max 16 commands). Other commands are executed just after a command is received.

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12.4.2. Detail of each command

12.4.2.1. System setting command (1byte command)

Set "channel mode" when active

Content of command	Bit allocation(CMD[7:0])							
	7	6	5	4	3	2	1	0
System setting	0	0	0	0	0	1	0	Mode

Item	Number of bits	Initial value	Description	
Mode	1	0b	The system mode is set.	
			Set value	Function
			0b	NOP mode
			1b	channel mode

12.4.2.2. System Clock Setting (1byte command)

Set system clock frequency (2.048~16.384MHz).

This command is also used for selecting sampling rate(16kHz or 32kHz).

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
System Clock setting	0	0	0	0	1		SCLK	

CLK16SEL=1, settings of clock are follows;

Item	Number of bits	Initial value	Description	
SCLK	3	000b	Setting of System Clock Frequency	
			Set value	Function
			000b	16.384MHz
			001b	8.192MHz
			010b	4.096MH
			011b	2.048MHz
			100b	reserved
			101b	reserved
			110b	(use for 16kHz sampling data.)

CLK16SEL=0, settings of clock are follows;

Item	Number of bits	Initial value	Description		
SCLK	3	000b	Setting of System Clock Frequency		
			Set value	Function	
			000b	4.096MHz	
			001b	2.048MHz	
			010b	reserved	
			011b	reserved	
			100b	reserved	
			101b	reserved	

*) When use 16kHz sampling

16kHz sampling data and 32kHz sampling audio data are available.

When 16kHz sampling data is to be used, following settings are necessary.

Noted   when simultaneous play using multi-channel, each tune should be the same sampling frequency

System Clock	Audio Data Sampling	CLK16SEL	SCLK
16.384MHz	32kHz	1	000b
16.384MHz	16kHz	1	110b
8.192MHz	32kHz	1	001b
8.192MHz	16kHz	1	000b
4.096MHz	32kHz	1	010b
4.096MHz	16kHz	1	001b
2.048MHz	32kHz	1	011b
2.048MHz	16kHz	1	010b
4.096MHz	32kHz	0	000b
2.048MHz	32kHz	0	001b
2.048MHz	16kHz	0	000b

* Not use SIO, SystemCLK is 16.384MHz or 4.096MHz is only.

12.4.2.3. Software reset (1byte command)

This command is for MCU to reset a chip by software.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Software reset	0	0	0	1	1	1	1	1

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12 4 2 4 Play command (1byte command)

Play a tune at a selected track.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Play	0	0	1	0	Mode	Loop	ChSel	

Item	Number of bits	Initial value	Description		
Mode	1	0b	Play mode is set.		
			Set value	Function	
			0b	Normal play	
			1b	Sequencer is executed	
Loop	1	0b	Loop control of Channel is set.		
			Set value	Function	
			0b	Loop disable	
			1b	Loop enable	
ChSel	2	00b	Re-controlled Channel is selected.		
			Set value	Function	
			00b	Channel 0	
			01b	Channel 1	
			10b		
			11b		

12.4.2.5. Stop command (1byte command)

Stop a tune at a selected track.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Stop	0	1	0	0	0	0	ChSel	

Item	Number of bits	Initial value	Description	
ChSel	2	00b	Channel to stop is selected.	
			Set value	Function
			00b	Ch0
			01b	Ch1
			10b	
			11b	

*)During Playback phrase, when you send STOP Comaand and next play command,
Need more than 10mS between STOP command and next play command.

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12.4.2.6. Pause command (1byte command)
Pause or resume at a tune a selected track.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Pause / resume	0	1	0	0	0	1	ChSel	

12.4.2.7. LOOP setting command (1byte command)
Set LOOP at a selected track.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
LOOP setting	0	1	0	0	1	Loop	ChSel	

Item	Number of bits	Initial value	Description		
Loop	1	0b	Set loop control.		
			Set value	Function	
			0b	Loop disable	
			1b	Loop enable	
ChSel	2	00b	Select Channel for looping.		
			Set value	Function	
			00b	Channel 0	
			01b	Channel 1	
			10b		
			11b		

The usage of this command is to disable loop mode during playing with loop mode. The command is also valid for sequencer mode. When disabling loop during playing tunes at sequencer mode,
sequencer stops at the end of the tune in the sequencer list. For example, when five tunes are set for looping, it stops playback at the end of 5th tune after "disable loop" command is issued.

12.4.2.8. Sequence clear command (1 byte command)
Sequence set by selection command is cleared.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Sequence clear	0	1	0	1	1	0	ChSel	

12.4.2.9. Buffer clear command (1 byte command)
Clear the buffer for tune-buffer and play-buffer (normal play buffer).
Selectable at each channel.
Use sequence buffer clear when sequence buffer needs to be cleared.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Buffer clear	0	1	0	1	1	1	ChSel	

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12.4.2.10. Tune selection command (2 Bytes command)

Set tune number to be played.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Selection	1	1	0	1	0	Mode	ChSel	
(#0 #DFh,F0h~FFh)	Tune#							

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Selection	1	1	0	1	1	Mode	ChSel	
(#100h~#1DFh,1F0h~1FFh)	(Tune# - 256)[*]							

[*] set "the selection number -256". For example, set "1" for tune#257.

Item	Number of bits	Initial value	Description		
Mode	1	0b	Set tune-selection mode.		
			Set value	Function	Number of command bytes
			0b	Specify normal tune	2 bytes
			1b	Add to sequence	2 bytes
ChSel	2	00b	Select a Channel.		
			Set value	Function	
			00b	Channel 0	
			01b	Channel 1	
			10b		
			11b		
Tune	8	00h	Select a tune number.		

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12.4.2.11. Volume command (2bytes command)

Control volume at a selected track.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Volume	1	0	0		Fade	Master	ChSel	
	0	0	0		Vol			

Item	Number of bits	Initial value	Description
Fade	1	0b	Set Fade in/out. It fades from the initial value to volume value specified by this command. <table><tr><td>Set value</td><td>Function</td></tr><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></table>
Master	1	0b	Set validity of volume value. When fade-in/fade-out mode, Set "0" at each Channel. <table><tr><td>Set value</td><td>Function</td></tr><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></table>
ChSel	2	00b	Track which sets the volume is selected. <table><tr><td>Set value</td><td>Function</td></tr><tr><td>00b</td><td>Channel 0</td></tr><tr><td>01b</td><td>Channel 1</td></tr><tr><td>10b</td><td></td></tr><tr><td>11b</td><td></td></tr></table>
Vol	5	1Fh	Set the volume value. 0 = mute, 31 = maximum volume.

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12.4.2.12. Fade volume initial value set command (2bytes command)

Set initial value for executing fade in/out.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Fade volume initial value	1	0	1	0	0	0	ChSel	
	0	0	0	Vol				

Item	Number of bits	Initial value	Description		
ChSel	2	00b	Select a channel.		
			Set value	Function	
			00b	Channel 0	
			01b	Channel 1	
			10b		
			11b		
Vol	5	1Fh	Set Volume value. 0 = mute, 31 = maximum volume.		

12.4.2.13. Fade interval time set command (2bytes command)

Set interval time value for fade in/out.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Fade interval of time	1	0	1	0	0	1	ChSel	
	0	Time						

Item	Number of bits	Initial value	Description		
ChSel	2	00b	Select a Channel.		
			Set value	Function	
			00b	Channel 0	
			01b	Channel 1	
			10b		
			11b		
Time	7	00h	Interval time at fading is set. The unit is 1ms. [*)]		

[*)] Interval time of fade-in/fade-out is 16/Tms (T: system CLK frequency) . For example, when system SCLK=16/T (MHz), the interval is 1ms.

12.4.2.14. Serial Flash ROM control command

By the command from SIO, BU6940FV access external ROM via SPI interface. 13 commands are provided (2bytes command).

Command setting value		Symbol	Description
The 1st byte	The 2nd byte		
E0h	Data to be written	WRSR	Write status register
E1h	Sector address	BP	Byte program
E2h	Sector address	PP	Page program
E3h	Sector address	READ	Lead data byte
E4h	BFh	WRDI	Write disable
E5h	-	RDSR	Read status register
E6h	BFh	WREN	Write enable
E7h	-	RDID	Read ID
E8h	BFh	RES	Return from deep power down
E9h	BFh	DP	Deep power down
EAh	BFh	CE	Chip erase
EBh	Sector address	SE	selector erase
EFh	BFh	AC2B	ROM address control (2 bytes)

The access unit for Flash ROM from SIO is 1 sector, which is set to 64kByte(65,536Byte).

Details for access is described at Chapter 13.

12.4.2.15. Synchronization command(1byte command)

This is a command for establishing synchronization.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Synchronization	1	0	1	1	1	1	1	1

The maximum chunk of consecutive commands is 128 bytes. Noted that, if sync-code is input after command transfer, sync-code are accepted.

If more than 129 bytes of command are consecutively input, 129th byte or later is ignored. Noted that, if 128th byte is the first byte of 2 byte command, 129th byte (2nd byte of 2 byte command) can be accepted.

If 128th byte is sync-code, it is ignored. In this case, SYNCREQ becomes "H" and its status becomes "waiting" for sync-code.

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13. command sequence to access Serial Flash ROM

This chapter (13.1~13.9) describes details of the commands for accessing SPI Flash ROM.

Following description is assuming that Flash ROM is controlled by 3-byte address).

13.1. Writing to SPI-interface FLASH ROM

The followings are description for writing SPI Flash ROM from SIO

(1) Sending Sync Req command(BFh).
(2) Sending Write-enable command(E6h, BFh).
(3) Sending Program command. Program commands are different along with Flash ROM type.
At chunk of bytes are 256bytes for writing(SPANSION, ST-Micro), a command of "page program" is set. At writing 1 byte(SST), a command of "Byte Program" is set.
(4) At page program mode, sending 65,536bytes(64kbytes) consequently checking if 256 bytes are done to be written by "BUSY" pin. At byte program mode, sending 1byte by checking if 1byte is done to be written by "BUSY" pin.
(5) Sending software reset command(1Fh).

*) Before writing data, need to unprotect a block-protect register in Status registers at Flash ROM. See Chapt9-4 for the method of writing status registers. Erase command for a sector(or sectors) shall be invoked before writing data into a sector or sectors.
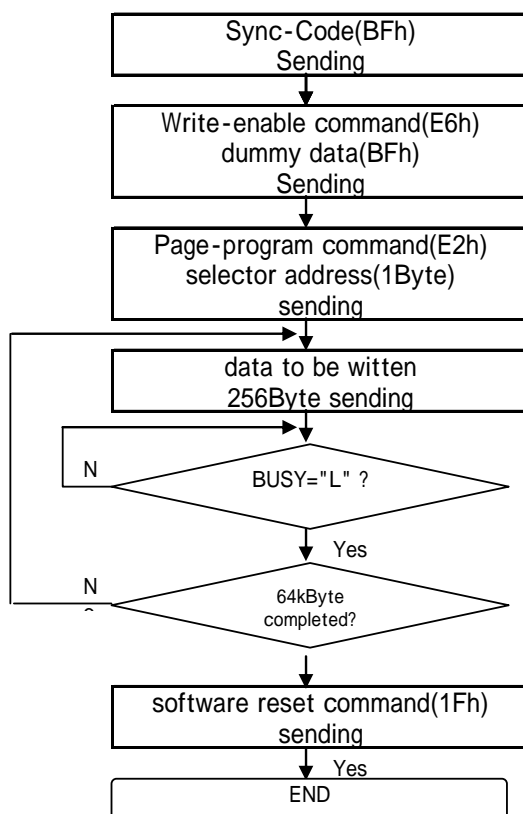
Figure13-1a. Sequence for writing data into Flash ROM(PP)
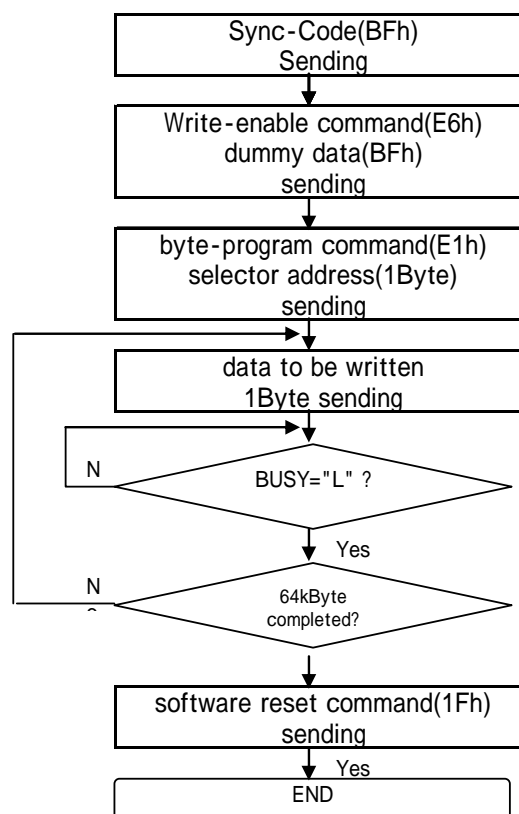
Figure913-1b. Sequence for writing data into FlashROM(BP)

13.2. Reading data from external FLASH ROM

This command is to read data from external Flash ROM. For example, this command is used for verifying data in Flash ROM. Unit for reading data is 64kBytes. When reading data, send "BF"h on RXD.
Followings are procedure for reading.

(1) sending Sync-code (BFh).
(2) sending "read data byte" command(E3h).
(3) After checking that BUSY pin is "L", read 64kByte data consecutively. During reading data, send "BF"h on RXD.
(4) After reading 64kByte data, send Software reset command(1Fh).

```
        ┌─────────────────────────┐
        │   Sync-Code(BFh)        │
        │        send             │
        └─────────────────────────┘
                    │
        ┌─────────────────────────┐
        │ read data byte command(E3h) │
        │        send             │
        └─────────────────────────┘
                    │
        ┌─────────────────────────┐
        │   sector address        │
        │        send             │
        └─────────────────────────┘
        ────────────────►│
                 ◇ BUSY="L" ? ◇
                    │ Yes
        ┌─────────────────────────┐
        │      Reading            │
        │      64kByte            │
        └─────────────────────────┘
                    │
        ┌─────────────────────────┐
        │ Software reset command(1Fh) │
        │        send             │
        └─────────────────────────┘
                    │ Yes
        ┌─────────────────────────┐
        │        END              │
        └─────────────────────────┘
```
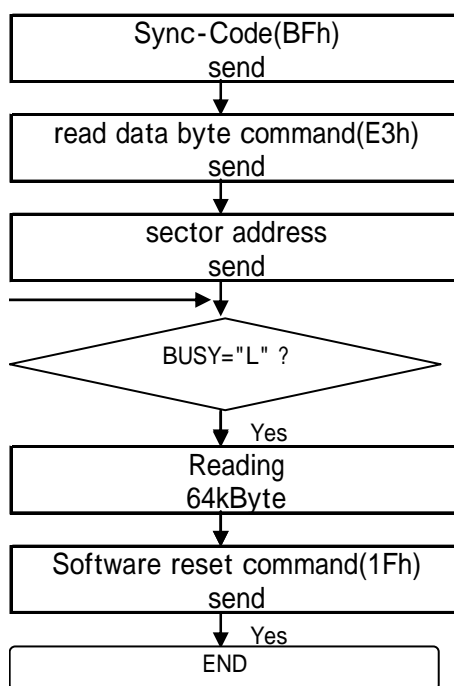
Figure 13-2.   read data sequence

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13.3. Reading JEDEC-ID of external FLASH ROM

This command is for reading device info of external flash ROM.

During receiving 3bytes of JEDEC-ID, send BFh at RXD pin.

Followingings are the command sequence.

(1) sending Sync-Req command(BFh).

(2) Sending read-ID command(E7h).

(3) After comfirming that BUSY pin is "L", read 3bytes data from TXD. When reading 3bytes, send BFh at RXD pin.

(4) Sending software reset command(1Fh).

```
          ┌──────────────────────┐
          │   Sync-Code(BFh)     │
          │        send          │
          └──────────────────────┘
                    │
          ┌──────────────────────┐
          │ Read ID Command(E7h) │
          │        Send          │
          └──────────────────────┘
                    │
        ┌──────────►│
        │        ╱──┴──╲
      N │       ╱ BUSY= ╲
        └──────╱  "L" ?  ╲
               ╲         ╱
                ╲───┬───╱
                    │ Yes
          ┌──────────────────────┐
          │ reading JEDEC-ID 3Byte│
          └──────────────────────┘
                    │
          ┌──────────────────────┐
          │ software reset command│
          │        send          │
          └──────────────────────┘
                    │
          ┌──────────────────────┐
          │         END          │
          └──────────────────────┘
```
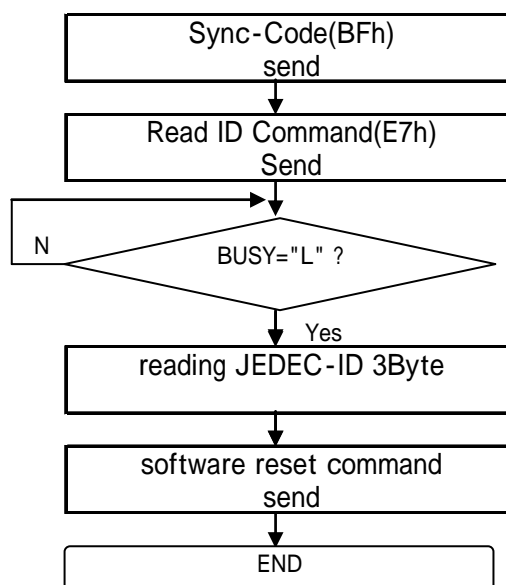
Figure 13-3.   JEDEC-ID reading sequence

13.4. Setting status register in an external Flash ROM

This command is setting status register in external ROM.   The access to   Flash ROM is valid after this command is invoked.   Block test function shall be always unlocked when writing/erasing data into Flash ROM.   See   flash ROM manual   for details of status registers.

Followings are procedure to set value into status registers.

(1) Sending a Sync-Code (BFh).

(2) Sending a write-enable command(E6h, BFh).

(3) Sending a write-status register command(E0h).

(4) Sending value into a status register.

*)   A certain time is required until the value is set after sending a command.   For the exact time, see the manual of flash ROM.

```
        ┌─────────────────────────┐
        │     Sync-code(BFh)       │
        │        send              │
        └─────────────────────────┘
                     │
                     ▼
        ┌─────────────────────────┐
        │ write enable command(E6h)│
        │     dummy data(BFh)      │
        │        send              │
        └─────────────────────────┘
                     │
                     ▼
        ┌─────────────────────────────┐
        │ write status register command(E0h)│
        │        wite data(1Byte)      │
        │           send               │
        └─────────────────────────────┘
                     │
                     ▼
        ┌─────────────────────────┐
        │           END            │
        └─────────────────────────┘
```

Figure13-4   writing sequence for status-register

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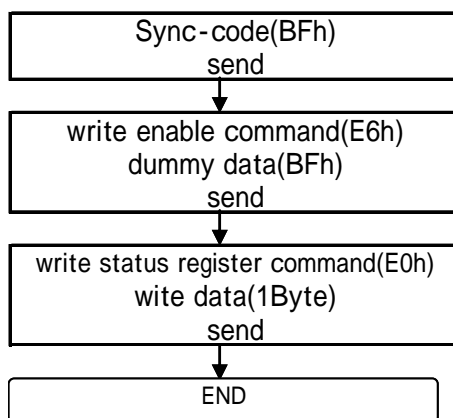### 13.5. Reading status registers in an external Flash ROM

This command is to read status register in an external flash ROM. When reading status register, send Sync-Code(BFh) command on RXD.　See manuals of flash ROM device for the details of status register. Followings are the procedure for reading status registers.

(1) Sending Sync-Code(BFh).
(2) Sending　read-status register command(E5h).
(3) Read 1 byte data from TXD after checking that BUSY-pin is "L.　BHh shall be sent on RXD.

```
        ┌─────────────────────────┐
        │   Sync-code(BFh)        │
        │       send              │
        └─────────────────────────┘
                    │
        ┌─────────────────────────┐
        │ read status register    │
        │ command(E5h)            │
        │       send              │
        └─────────────────────────┘
                    │
           ┌────────▼────────┐
      N    │   BUSY="L" ?    │
    ◄──────┤                 │
           └────────┬────────┘
                    │ Yes
        ┌─────────────────────────┐
        │  status register 1Byte  │
        │       read              │
        └─────────────────────────┘
                    │
        ┌─────────────────────────┐
        │          END            │
        └─────────────────────────┘
```
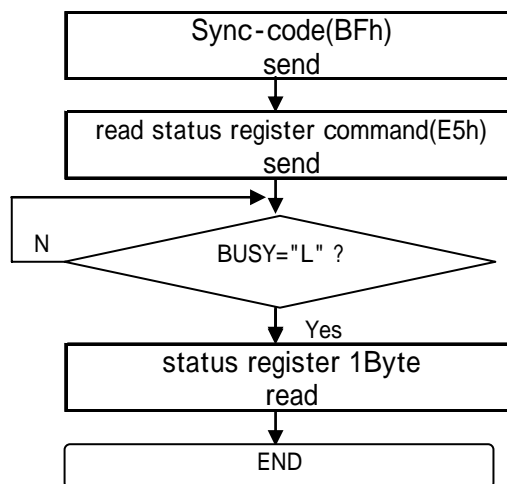
Figure 13-5　　reading sequence for status-register

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13.6. Erasing data in an external Flash ROM

For erase function for an external ROM, 2 commands are supported, chip-erasing and sector-erasing. Chip-erasing command erases all area in Flash ROM at once. A sector-erase command erases one sector, which has 64kbyte area.

The following the procedure for chip-erasing command.

    (1) sending Sync-code (BFh).

    (2) Sending write-enable command(E6h, BFh).

    (3) Sending Chip-erase command(Eah, BFh).

    (4) Wait for the necessary time to erase flash ROM.

    See Flash ROM manual for necessary erase time.

    Before chip erase, Block protect register (Flash ROM) shall be unlocked.

    The procedure of status-register , see Chapt13-4.

```
        ┌─────────────────────────────┐
        │      Sync-Code(BFh)         │
        │          sned               │
        └──────────────┬──────────────┘
                       ▼
        ┌─────────────────────────────┐
        │  write-enable command(E6h)  │
        │      dummy data(BFh)        │
        │          send               │
        └──────────────┬──────────────┘
                       ▼
        ┌─────────────────────────────┐
        │   chip erase command(EAh)   │
        │      dummy data(BFh)        │
        │          send               │
        └──────────────┬──────────────┘
                       ▼
        ┌─────────────────────────────┐
        │     wait required time      │
        │  described in Flash ROM spec│
        └──────────────┬──────────────┘
                       ▼
        ┌─────────────────────────────┐
        │            END              │
        └─────────────────────────────┘
```

Figure 13-6a.   Chip Erase Sequence

Followings are steps for sector erase.

(1) Sending Sync-req command(BFh).

(2) Sending write-enable command(E6h, BFh).

(3) Sending sector-erase command(Ebh).

(4) Sending a sector address(1byte) to be erased.

(5) Waiting for erase time required for each Flash ROM.

   See Flash ROM manual for necessary erase time.

   Before chip erase, Block protect register (Flash ROM) shall be unlocked.
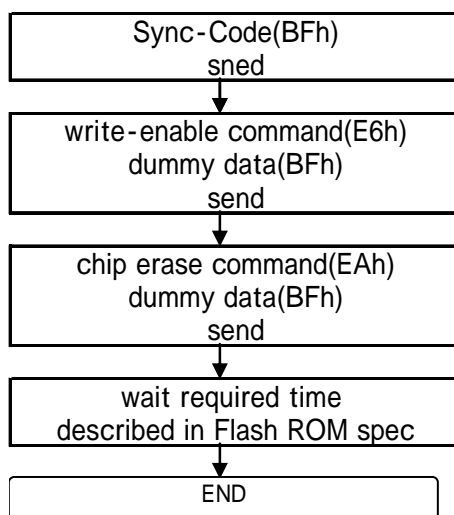
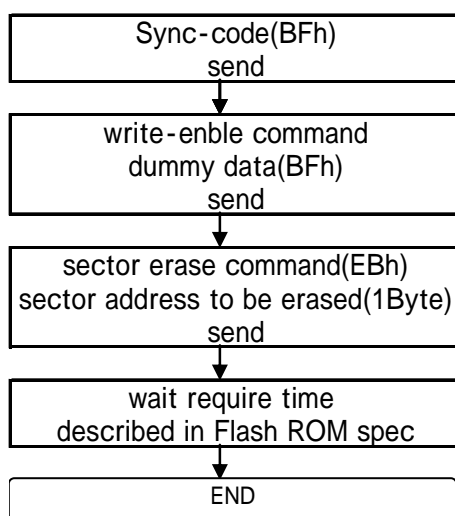   The procedure of status-register, see Chapt13-4.

```
┌─────────────────────────────┐
│      Sync-code(BFh)          │
│         send                 │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│    write-enble command       │
│     dummy data(BFh)          │
│         send                 │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│  sector erase command(EBh)   │
│ sector address to be erased(1Byte)│
│         send                 │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│     wait require time        │
│  described in Flash ROM spec │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│            END               │
└─────────────────────────────┘
```

Figure13-6b.   **Sector-erase-sequence**

13.7. Deep power down of external Flash ROM and restoring from Deep power down

This command   is setting deep power down mode (and restoring deep power down mode) into external Flash ROM. See Flash ROM manual which is provided by the Flash ROM manufactures for details.

Noted that SST Flash ROM does not support Deep Power down mode.

Deep Power Down

(1) Sending Sync-code (BFh).
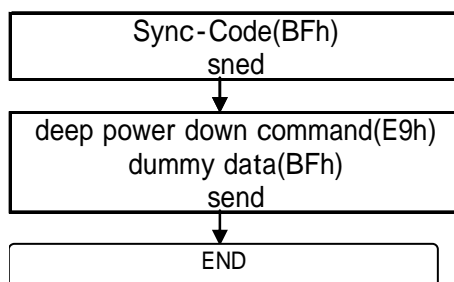
(2) Sending deep power down command(E9h, BFh).

```
┌─────────────────────────────┐
│      Sync-Code(BFh)         │
│          sned               │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│  deep power down command(E9h)│
│      dummy data(BFh)        │
│          send               │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│            END              │
└─────────────────────────────┘
```

Figure 13-7a.   Deep Power down sequence

Restoring Deep Power Down

(1) Sending Sync-Code (BFh).

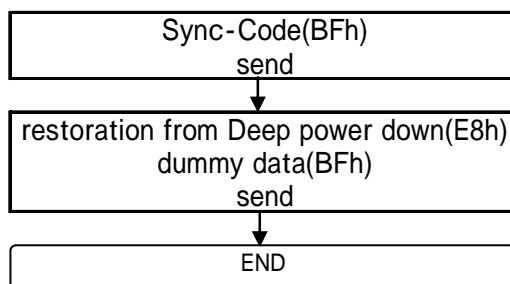(2) Sending restoration command from deep power down(E8h, BFh)

```
┌─────────────────────────────┐
│      Sync-Code(BFh)         │
│          send               │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────────┐
│ restoration from Deep power down(E8h)│
│      dummy data(BFh)            │
│          send                   │
└─────────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│            END              │
└─────────────────────────────┘
```

Figure13-7b.   Sequence for restoring deep power down

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13.8. ROM Address Control command

This command is used for SPI intarafce Flash/EEPROM whose address is controlled by 2 bytes, and valid only for playback. The default setting of the chip after Reset is 3 bytes address mode, so need to set 2 bytes address mode by SIO before playback tunes when ROM is 2bytes-mode.

Use hardware reset (RESETB='L') when reset address mode. Software reset command is not valid.

When 2bytes address mode, serial Flash control commands are all invalid. So when update Flash ROM/EEPROM, re-write data at off-line tools like ROM writer.

Followings are the commands;

(1) Sending Sync-code (BFh).
(2) Sending ROM address control command(EFh, BFh).

```
        +-----------------------------+
        |      Sync-Code(BFh)         |
        |          send               |
        +-----------------------------+
                      |
                      v
        +-----------------------------+
        |   ROM Address control(EFh)  |
        |      dummy data(BFh)        |
        |          send               |
        +-----------------------------+
                      |
                      v
        +-----------------------------+
        |            END              |
        +-----------------------------+
```
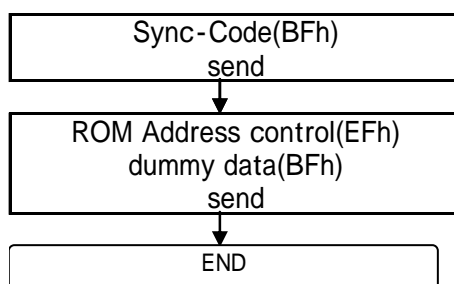
Figure 13-8.   ROM Address control sequence

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13.9. Available Serial Flash ROM

Following Serial Flash ROM is available. Others are not guaranteed.

SST

SST25VF512B(512kbit)
SST25VF040B   4Mbit
SST25VF080B   8Mbit
SST25VF016B   16Mbit
SST25VF032B   32Mbit

SPANSHION

S25FL004A   4Mbit
S25FL008A   8Mbit
S25FL016A   16Mbit
S25FL032A   32Mbit

ST Micro

M25P40   4Mbit
M25P80   8Mbit
M25P16   16Mbit
M25P32   32Mbit

*)   These Flash ROMs have not been tested, but some of the family products are tested.
Therefore, these flash ROMs should be working correctly.

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14. Sequencer

Control of sequencer and addition/clear of tune in a sequencer mode are done by play command and tune-selection command respectively. Each track has a sequencer independently. The maximum numbers of tunes registered to sequencer are 16. The example of sequencer is shown below;

Track 0 sequencer

Command 0 = selection command (Mode=1,Tune=3,ChSel=0)   add tune
Command 1 = selection command (Mode=1,Tune=15,ChSel=0)   add tune
Command 2 = selection command (Mode=1,Tune=9,ChSel=0)   add tune
Command 3 = selection command (Mode=2,Tune=255,ChSel=0)   add tune
Command 4 = selection command (Mode=1,ChSel=0)   execute

Playback order

| Tune number 3 |
| Tune number 15 |
| Tune number 9 |
| Tune number 255 |
| Blank |
| Blank |
| Blank |
| Blank |

Sequencer is executed at the time command is executed.

The order of playback is from tune number3 , 15, 9, 255.

Tune number 15 is started to play at the point when playback of tune number3 is ended.

Figure14-1. Example of sequencer

- Addition of a tune to sequencer
It is done by selection command .
When sequencer is stopped by stop command while sequencer is running, or when additional command is issued after execution of sequencer is finished, a tune is added at the end of sequencer list.

- Sequencer clear
Clear of sequencer is done by sequence clear command . When sequencer clear is issued, all tunes in the list are cleared shown in figure 14-1. For changing the order of tunes, it is necessary to clear sequencer once, and add tune by tune-selection command. Clear command during sequencer is running is ignored.

-tune add command after 16 tunes are already registered in a sequencer
Tune add command is discarded when 16 tunes are already registered in a sequencer. Noted that BFULLB is not active in a sequencer mode

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15. Loop playback

The order of playback when sequencer is running with LOOP mode is from tune number
3　15　9　255　3　15　9　　　　　as described in Figure 15-1.
Also, when disabling LOOP command is issued while LOOP is on, sequencer is stopped at the end of next tune of the tune currently running.
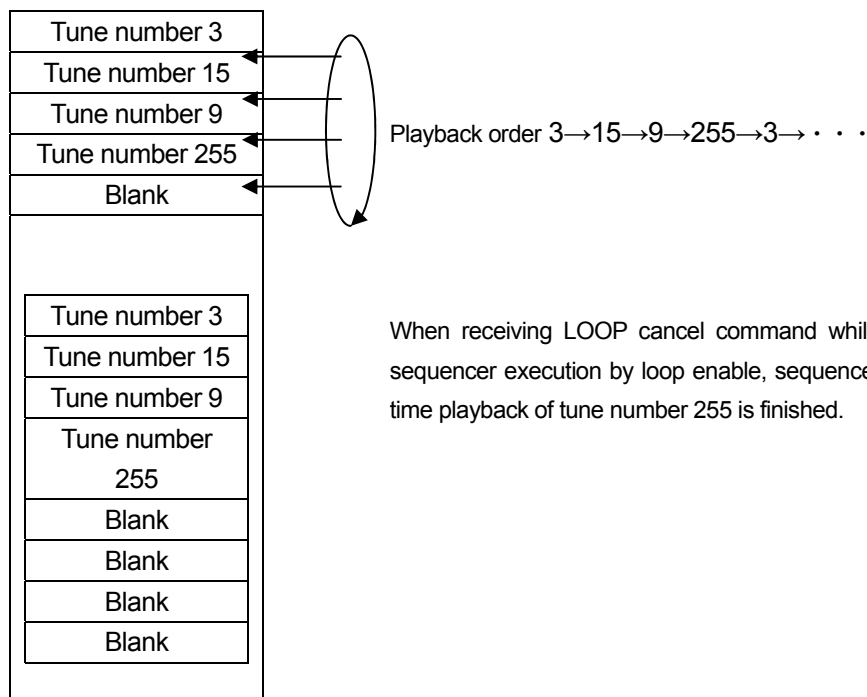
| Tune number 3 |
| Tune number 15 |
| Tune number 9 |
| Tune number 255 |
| Blank |

Playback order 3→15→9→255→3→

| Tune number 3 |
| Tune number 15 |
| Tune number 9 |
| Tune number 255 |
| Blank |
| Blank |
| Blank |
| Blank |

When receiving LOOP cancel command while playing tune number 9 at sequencer execution by loop enable, sequencer execution is finished at the time playback of tune number 255 is finished.

Figure15-1. Loop processing by the sequencer

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16. Fade

BU6940FV supports the function of fade in/out.

The example of fade in is described below.

1. Fade volume initial value command (ChSel=0,Vol=0)
2. Fade interval time command (ChSel=0,Time=10)
3. Volume command (Fade=1,Master=0,ChSel=0,Vol=31) ---Fade in is executed when this command is

issued.
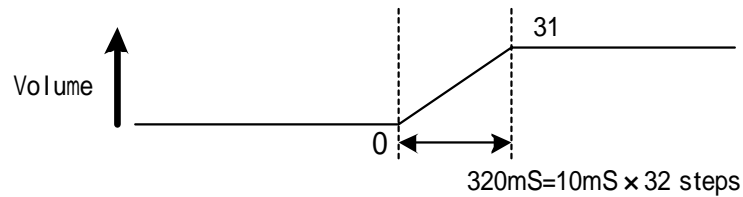
In this example, volume is increased from 0 to 31 in the period of 320 ms.

In the case that volume value of initial value command is bigger than the volume set by volume command, fade out is executed.

17. Direct Pin Input mode

When SIO_ENABLE="L", command input is not from SIO, but from PIN direct.

This mode has very high advantage for simple system without CPU.

At PIN direct mode, just set tunes from #1 to #31 and volume (High or Low) by "VSEL" pin for tune playback.

17-1. timing chart at direct pin input

Select a tune by VSEL[4:0] pins. When level of pins is more than Trh, a tune is playback after 2ms.

-when tune#1~27 is selected, a tune is playback only once. When stop, set VSEL[4:0]=5'b00000.

- When tune#28~31 is selected, a tune is playback with loop. When stop, set VSEL[4:0]=5'b00000.

-noted that VSEL[4:0]=5'b00000 is "stop" command, not tune#0.

(1) In the case that tune#23 is selected to be played
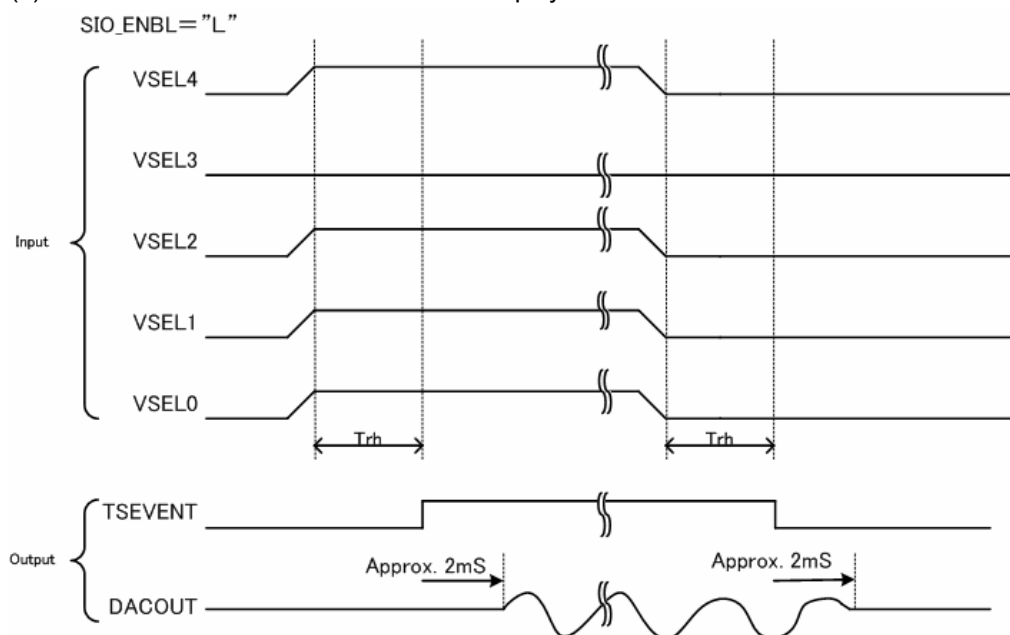
Figure 17-1a.   Direct Pin input timing chart

Table 17-1   Direct pin input timing chart

Item	Symbol	Min	standard	Max	Unit
VSEL Hold time	Trh	20	-	-	mS

-20ms is not related to the input clock frequency.

- the input which does not hold the value more than 20ms is discarded.

(2) In the case that #7 and #6 of tune are selected to play in sequentially
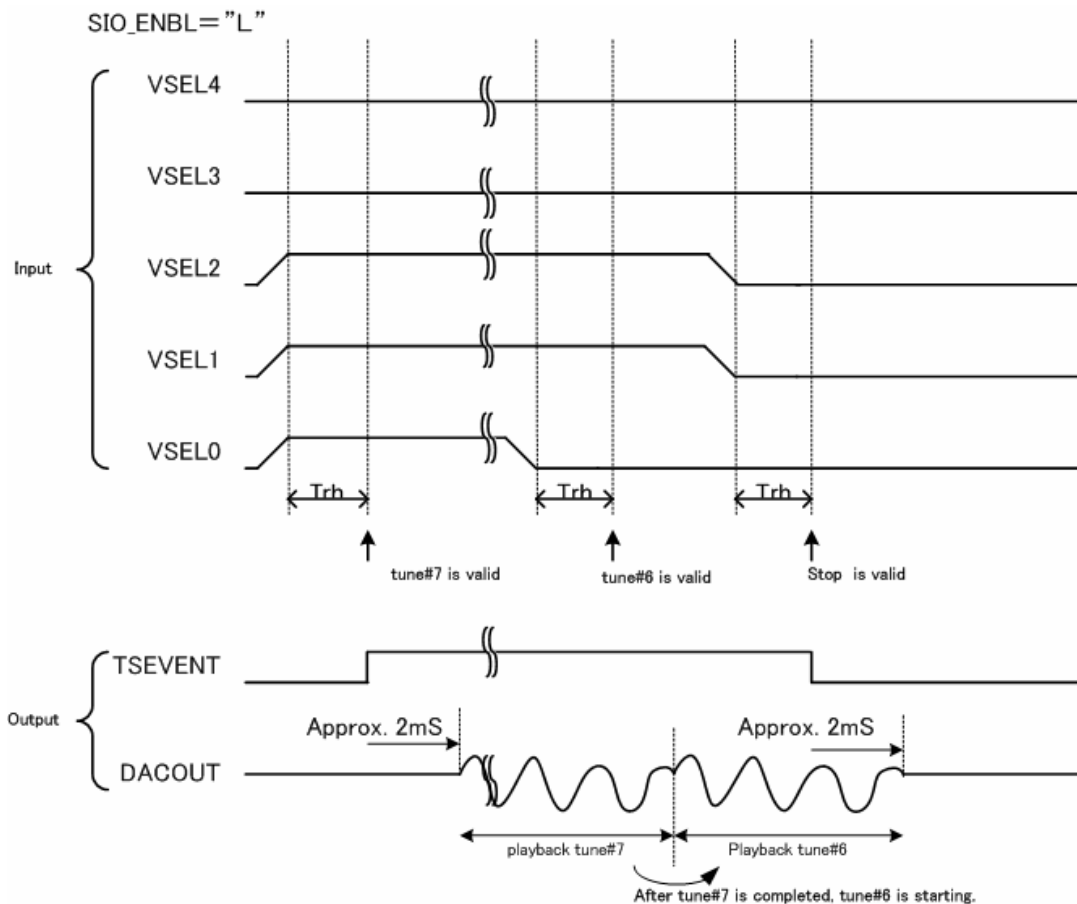
Figure.17-1b.　2 tunes sequential play timing chart

Maximum 16 tunes are enable to buffering, and playback sequentially.
When you send STOP command, all clear in tune Buffer
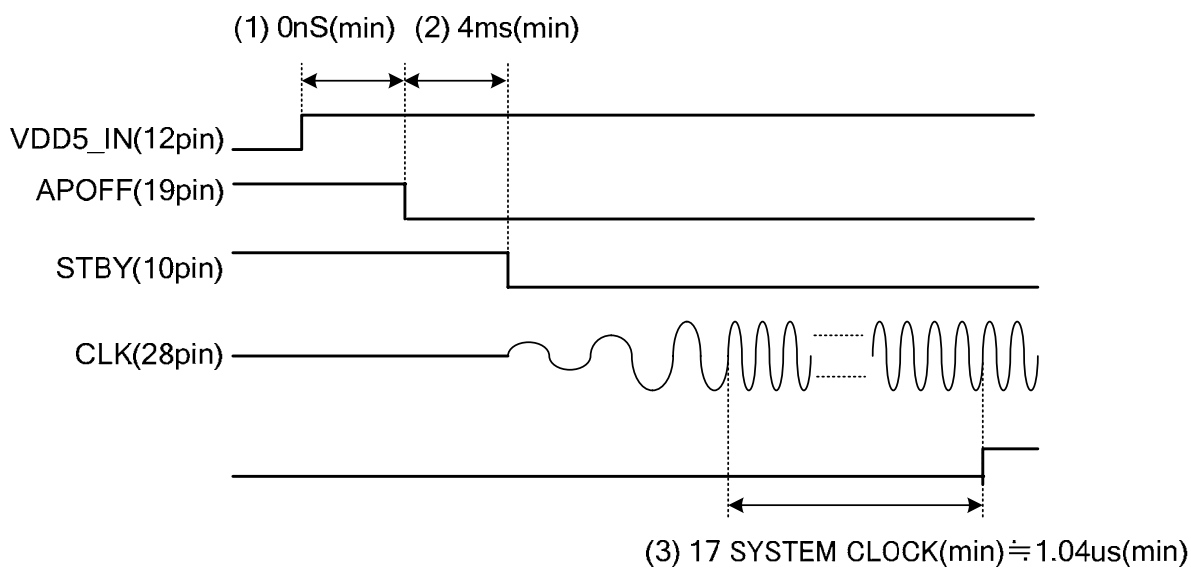
18.RESETsequence and AP OFF pin and STBY pin

Please follow the below steps at initial sequence.

Internal regulator and DAC start working by setting APOFF to "L".

Clock is oscillated by STBY signal setting to "L". Reset is not invoked automatically.

When initial, Reset procedure shall be done as follows;

1.Set APOFF pin to "L".

2.Set STBY signal to "L" (Clock is oscillated).

3.input 17 clock or more after RESETB is "L"

4.Set RESETB signal to "H."

(1) 0nS(min) (2) 4ms(min)

VDD5_IN(12pin)

APOFF(19pin)

STBY(10pin)

CLK(28pin)

(3) 17 SYSTEM CLOCK(min)≒1.04us(min)

When invoke APOFF (setting to "H"), STBY shall be "H" first.

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19. Example of system block diagram using BU6940FV and example of command setting

Examples of system block diagram using BU6940FV is shown in Fugure19-1, and also example of command setting is listed below
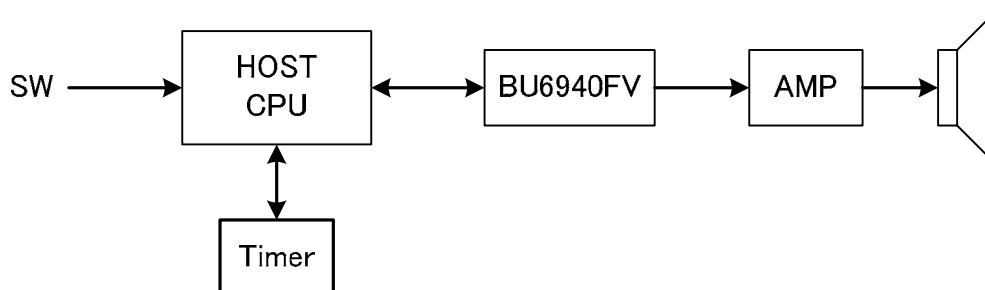
Example of HOST-BU6940 connection
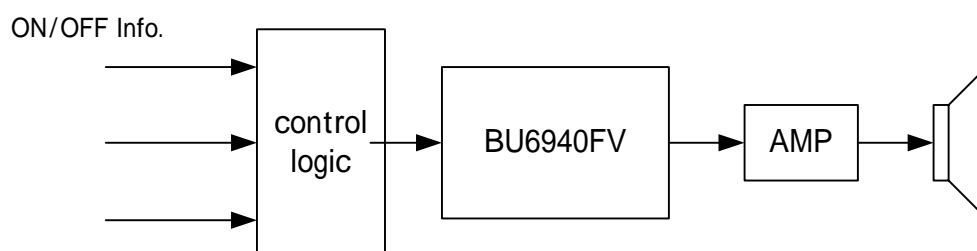
Example of direct-pin　connection

Figure 19-1. System Example

Example of command setting

The example shows the case when playing 2 tracks simultaneously and executing fade out at the end of the sequence. For the tune number to play, channel 0 loop from 0th to 5th tune, and channel 1 repeats 10th tune.

Table 19-1 Command setting example

Proce-dure	Operation	Command setting value		Content
		1st byte	2nd byte	
1	**Synchronization command issue**	BFh	—	**Synchronization command is established.**
2	System setting command issue	05h	—	changes from NOP to 2 cannel mode
3	Selection command issue	D4h	00h	adding time #0into sequence buffer on channel 0
		D4h	05h	adding time #5 into sequence buffer on channel 0
		D1h	0Ah	The 10th tune is added to cannel 1.
4	Volume setting command	90h	0Fh	The volume of cannel 0 is set to 15.
		91h	0Fh	The volume of cannel 1 is set to 15.
5	Fade volume initial setting	A0h	0Fh	Initial value of cannel 0 is set to 15.
		A1h	0Fh	Initial value of cannel 1 is set to 15
6	Fade time setting	A4h	70h	Channel 0 is set at 127ms intervals.
		A5h	70h	Channel 1 is set at 127ms intervals.
7	Play	2Ch	—	Channel 0 is played with sequencer and loop. 0 5 0 5------
		25h	—	Channel 1 is played without sequencer and with loop. 10 10 10 10------
8	Volume command setting	98h 99h	00h 00h	Volume of cannel 0 is set to "0". Start fade out for cannel 0. Volume of cannel 1 is set to "0". Start fade out for cannel 0.
9	Stop command	40h	—	Channel 0 stop
		41h	—	Channel 1 stop

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20. Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the ICs power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Others

In case of use this LSI, please peruse some other detail documents(Technical note, Application note and so on).

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