

Two-stage, single-output, opto-coupled gate driver evaluation board

The SGDR600P1 is an opto-isolated, two-stage gate driver with a single output. The driver is optimized for high-speed, hard switching of SemiSouth's SJEP120R050 and SJEP120R063 normally-off SiC VJFETs. With a small modification effort (parts included in the evaluation kit) it can also be used to drive the SJEP120R100, SJDP120R085, or SJDP120R045. The SGDR600P1 gate driver provides a peak output current of +6/-3 A for fast turn-on transients yielding record-low switching energy losses.

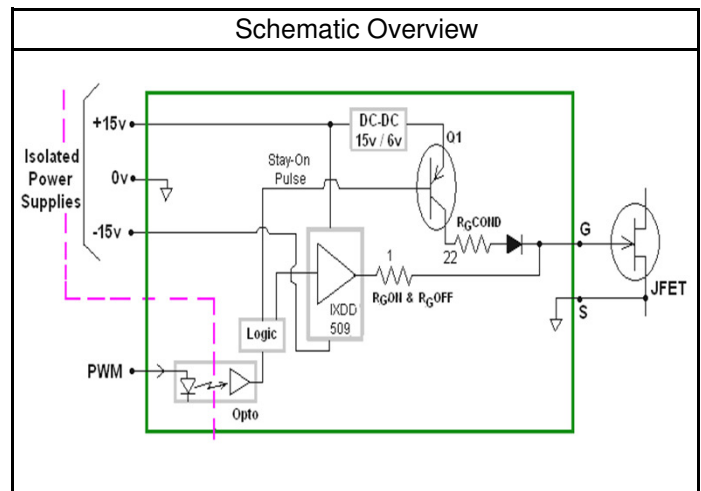
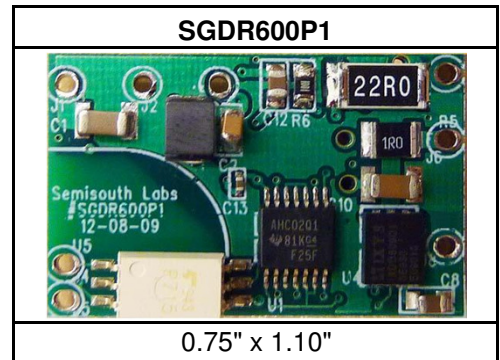
Features:

- Suitable for driving SJEP120R063 or SJEP120R050
- Two-stage driver: switching & conduction
- Peak gate current of +6/-3 A
- Switching frequency
- Duty cycle: 0 to 100 %
- Low BOM cost
- Can be modified to drive SJEP120R100, SJDP120R085, or SJDP120R045. See AN-SS3 Rev 2 for instructions. Parts included in the evaluation kit.

Applications:

- Hard Switched Bridge Topologies
- Inverters/Converters
- IT/Telecom Power Supplies
- Product Evaluation
- Research

Product Summary		
V_{DD}/V_{SS}	+15/-15	V
I_{PK}	+6/-3	A
$F_{SW(MAX)}$	250	kHz
Duty Cycle	0-100	%



MAXIMUM RATINGS

Parameter	Symbol	Conditions	Value	Unit
Positive supply voltage	V_{CC}	to GND	+ 15	V
Negative supply voltage	V_{EE}	to GND	-15	V
Input current logic HIGH	$I_{F(ON)}$		10	mA
Peak output current	I_O	Not connected to the JFET, output shorted to GND or pure capacitive load	+ 9	A
			- 9	
Operating temperature	T_{OP}		+ 85	°C
Storage temperature	T_{ST}		+ 100	°C

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	

External Power Supplies

Positive supply voltage	V_{CC}	to GND	+ 8		+15	V
Positive supply current	I_{CC}	$V_{CC} = +15\text{ V}$, $f = 50\text{ kHz}$, $D = 100\%$		130		mA
Negative supply voltage	V_{EE}	to GND	- 8		-15	V
Negative supply current	I_{EE}	$V_{EE} = -15\text{ V}$, $f = 50\text{ kHz}$, $D = 100\%$		- 30		mA

Input

Input forward voltage	V_F	$I_F = 5\text{ mA}$, $T_A = 2\text{ }^\circ\text{C}$	1.4	1.60	1.70	V
Input voltage, OFF	$V_{F(OFF)}$		0	-	0.8	V
Input current, ON	$I_{F(ON)}$		4.5	-	10	mA
Input capacitance	C_{in}	$V = 0\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25\text{ }^\circ\text{C}$	-	45	-	pF

Timing Characteristics

Delay time input to output	$t_{d(ON)}$		-	130	-	ns
	$t_{d(OFF)}$		-	130	-	ns

Output

Output voltage	V_O	Peak positive voltage clamped by JFET gate-source diode	$V_{EE} + 1$	-	+ 5V	V
Peak output current ⁽¹⁾	I_O	$V_{CC} = 15\text{ V}$, $R_{GON} = 1\ \Omega$	-	+ 6		A
		$V_{EE} = -15\text{ V}$, $R_{GOFF} = 1\ \Omega$		- 3	-	
Steady-state output current	I_{ODC}	limited by R_{GCOND}	-	140		mA
Output voltage rise time	t_{ro}		-	-	20	ns
Output voltage fall time	t_{fo}		-	-	20	ns

Electrical Isolation

Creep path input-output			7	-	-	mm
Max $\Delta V/\Delta t$ at $\Delta V = \text{TBD}$		10 kV used at 1000 Vp-p		TBD		kV/ μs

Operating Conditions

Operating Temperature	T_{OP}		0	-	+ 85	$^\circ\text{C}$
Storage Temperature	T_{ST}		0	-	+ 100	$^\circ\text{C}$

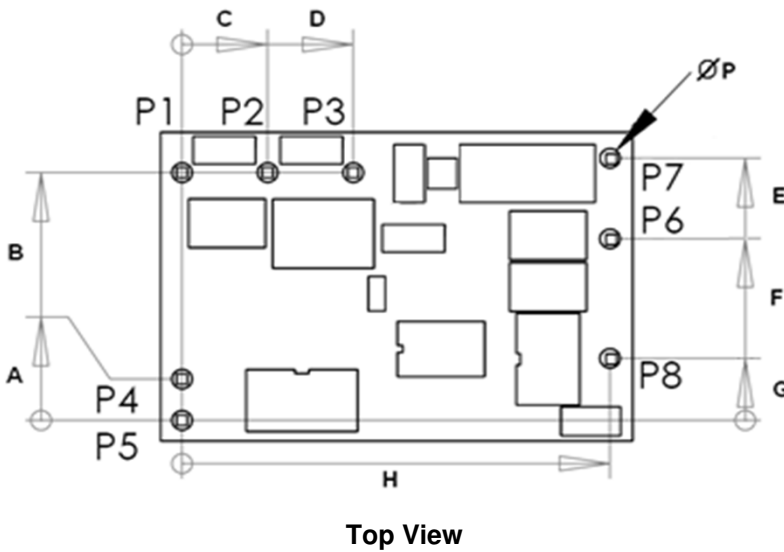
Notes:

- (1) I_{PK} is limited by the JFET gate-source voltage (V_{GS}) and gate resistor (R_G). Pulse width is fixed at 100 ns. Connected to SJEP120R063 or SJEP120R050.

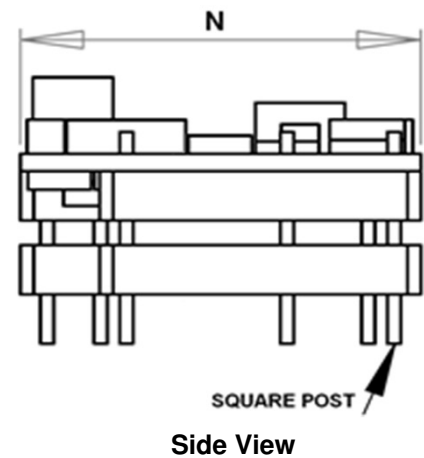
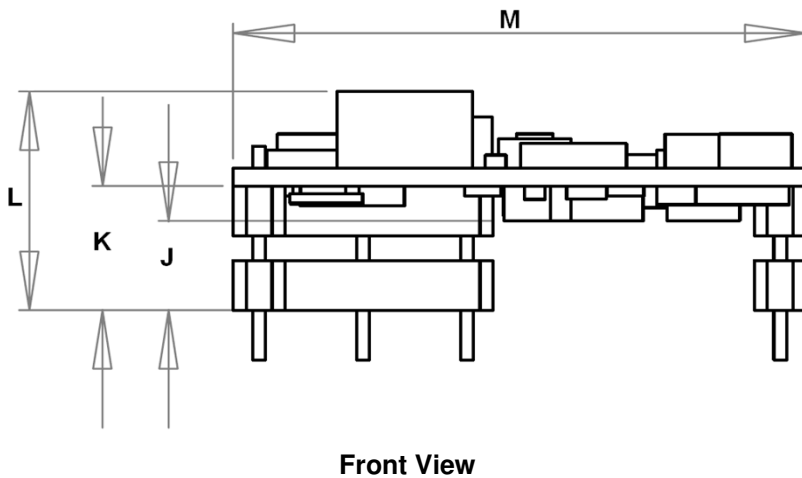
Package Pinout

Pin Descriptions						
1	VCC	Positive supply		5	VIN-	Input control signal negative terminal
2	GND	Ground		6	Vo	Output to gate
3	VEE	Negative supply		7	GND	Ground
4	VIN+	Input control signal positive terminal		8	Vs	Source connection

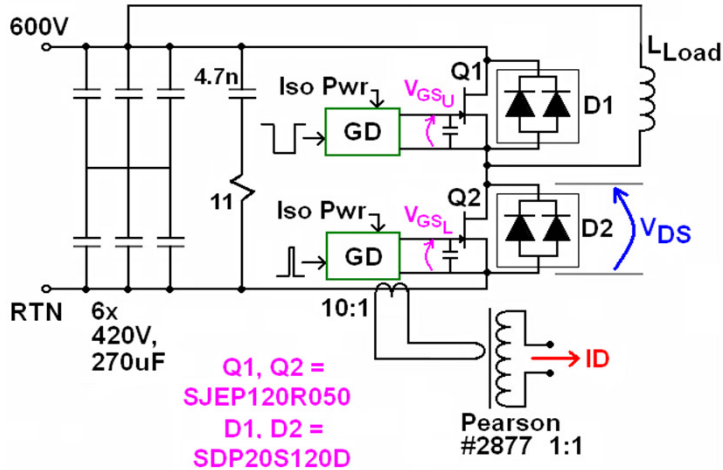
Package Dimensions



	in.	mm
A	0.100	2.54
B	0.500	12.70
C	0.200	5.08
D	0.200	5.08
E	0.200	5.08
F	0.300	7.62
G	0.150	3.81
H	1.000	25.40
ØP	0.047	1.20
J	0.180	4.57
K	0.250	6.35
L	0.440	11.19
M	1.102	28.00
N	0.748	19.00
ØR	0.025	0.64



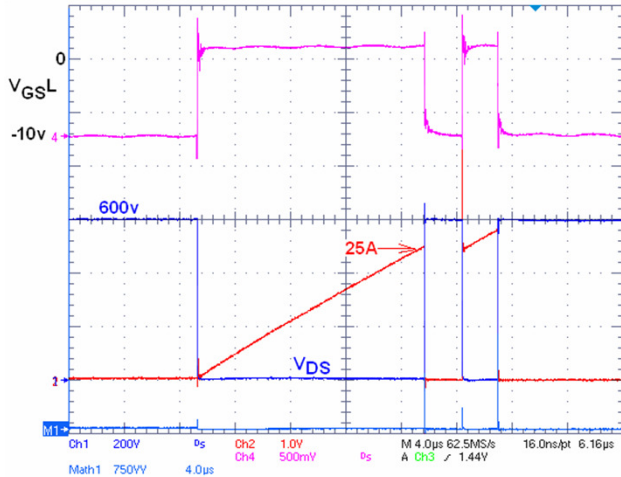
Application Test Circuit



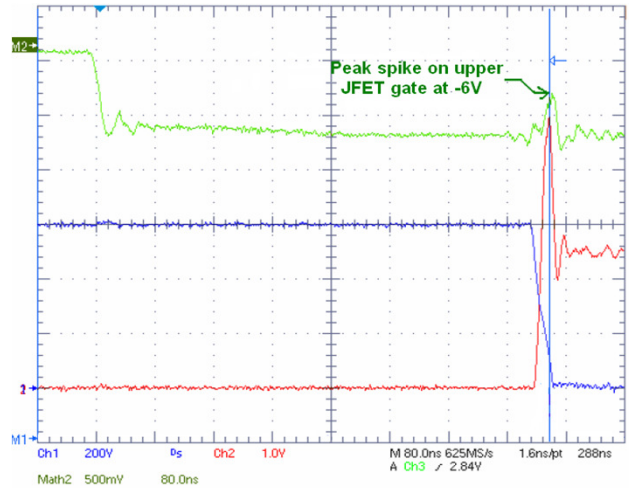
Test Conditions

1. Results for SJEP120R050
2. Phase-leg configuration
3. $V_{DC} = 600\text{ V}$; $I_{LPK} = 25\text{ A}$, $T_A = 25\text{ }^\circ\text{C}$
4. RC snubber equal to $11\text{ }\Omega$ and 4.7 nF
5. $400\mu\text{H}$ load inductance
6. Each device driven by separate SGDR600P1
7. Gate driver power supplies of $\pm 15\text{ V}$
8. Gate driver approx. 5 mm from gate terminal
9. 3.3 nF gate-source capacitive clamp

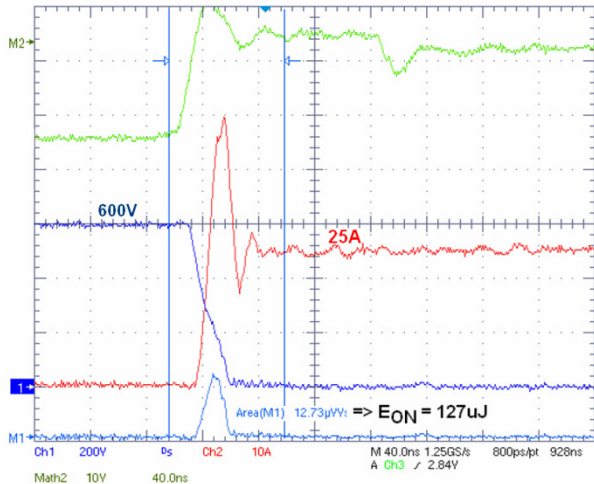
Switching Waveforms



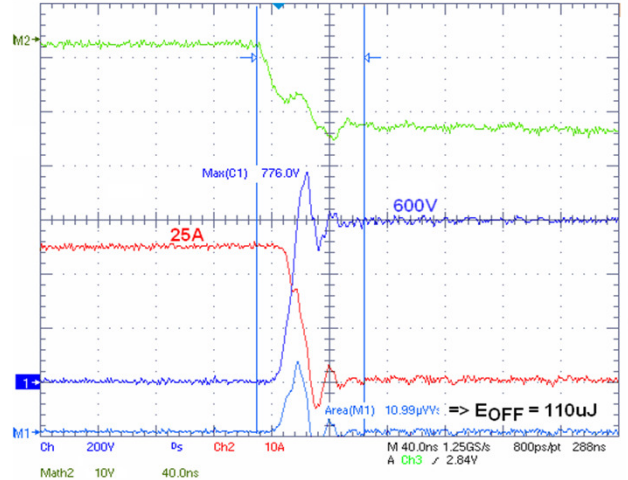
Upper JFET Gate Waveform in the OFF Condition



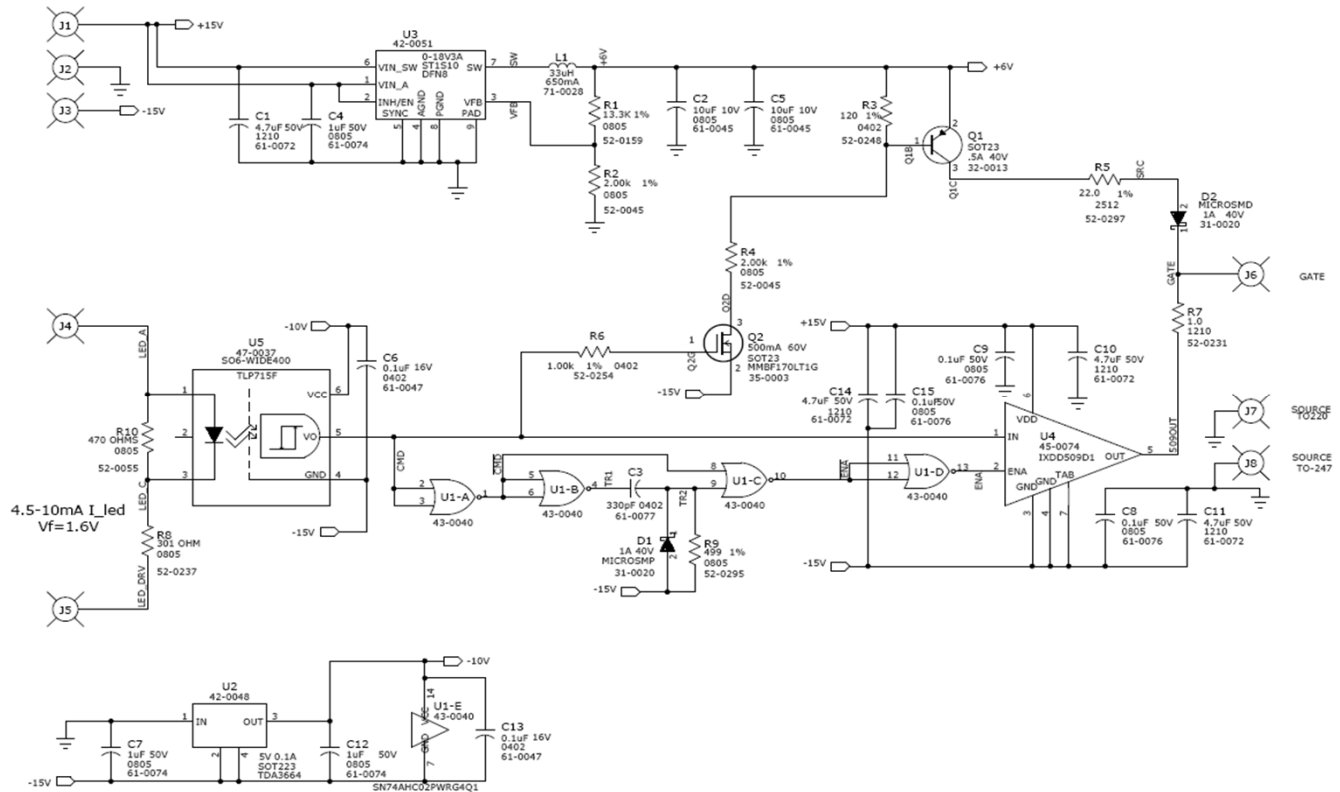
Lower JFET Turn-on Waveforms



Lower JFET Turn-off Waveforms



Detailed Schematic



Functional Description

TLP715F: This reference design uses a Toshiba high-speed opto-coupler (U5) enabling fast switching speeds while allowing layout spacing to meet safety isolation requirements.

IXDD509: This IXYS high-speed driver (U4) is used to provide a high-current turn-on and turn-off gate pulse through $R_{G(on/off)}$ for fast switching and low switching losses.

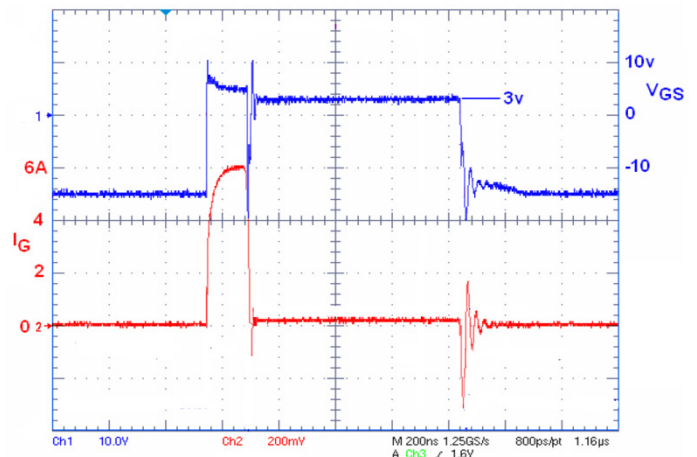
PBSS5140: Q1 is a small PNP transistor used to provide the ON-state gate current of 140 mA to maintain a low $R_{DS(on)}$ during the conduction period.

ST1S10: This 15 V to 6 V (80% eff) step down DC/DC converter IC (U3) is used as the power source for Q1 and enables a reduction in gate power loss during the conduction period.

Timing Logic: The logic / timing gates (U1) generates the required timing signal for the IXDD509 gate Driver and Q1. The timing is set to achieve a 100 ns turn-on high-current pulse and then maintain the 140 mA conduction pulse.

UA78L05AC: The TI 5 V regulator (U5) is used to generate an internal voltage supply for the secondary side of the opto-coupler and logic gates.

Typical Gate Voltage and Gate Current Waveforms



Application Recommendations

External +15 V and -15 V power supplies - The required power supplies must be sufficiently isolated from any source voltage that is accessible to human touch. This isolation requirement will depend upon the bus voltage used and the requirements set by the applicable regulatory agency. Here are some additional considerations:

1. Minimize the lead length between the output of these isolated power supplies and the input to the gate drive circuit.
2. The voltage differential between the +15 V and -15 V must not exceed 30 V in order to protect the driver IC.
3. The +15 V supply must be constrained at or above +8 V to ensure operation of the internal DC/DC converter. The -15 V supply must be constrained at or below -8 V for the internal 5 V regulator for the logic and optocoupler to have enough head room.
4. If two gate driver circuits are used in a half-bridge configuration, the stray capacitance between the two sets of isolated outputs must be low (<10 pF). Bench-top power supplies should not be used.
5. If a switching power supply is used to generate the supplies for both the upper and lower JFETs, the transformer should be segment-wound to minimize stray capacitance.

Adjusting the gate current for R_{ds} during conduction

The gate current required by the JFET during its ON state is set by the resistor R5 in the schematic of page 5. In this reference design the value of R5 was set for a gate current of 140 mA which is the recommendation for the SJEP120R063 JFET to maintain a low $R_{DS(ON)}$ over temperature while keeping the gate power loss to a reasonably low level. If a different JFET is being used, the values of R5 can be adjusted to reach the desired gate current. The designer should refer to the JFET data sheet for picking the proper gate current.

EMI issues and adjusting turn on and turn off switching speeds

- The turn-on and turn-off speeds are set by the combination of the value of the +/-15 V power supplies and the value of R7 (1 Ω) in the schematic on page 5. The default values are for minimum switching energies for the SJEP120R063 and SJEP120R050. If this default switching results in excessive EMI or ringing, then there are two options to reduce the switching speeds which can be used individually or together:

1. Decrease the +/- 15 V power supplies from +/- 15 V to as low as +/- 8 V.
2. Add a non-inductive resistor in the range of 1 to 10 Ω in series between the board's gate output terminal and the JFET's gate terminal.

Techniques for reducing gate ringing - Excessive ringing on the gate voltage waveform can be caused by the leakage inductance in either the main power circuit and/or in the gate circuit itself. Hence, the loop area composed of the JFET + freewheel diode + bus caps must be minimized and the physical distance from the gate driver to the JFET must be minimized. The use of a ferrite bead can also significantly reduce the ringing at the expense of slower turn on.

Recommendation for using a snubber across the DC Bus - Further reductions in ringing can sometimes be achieved by the addition of a low power series R-C snubber circuit, as shown in the test circuit of page 4.

Eliminating shoot-through in bridge configurations In bridge configurations, the action of turning on one of the JFETs often results in the a corresponding miller effect "glitch" on the gate of the other JFET such that it can be transiently turned on as well resulting in excessive switching losses in both devices. Due to the very fast switching performance of the JFET, this reference design requires a negative 15 V power supply to suppress this phenomenon. Additionally to add more safety margin, a small (1 – 5 nF) capacitor placed across each JFET's gate & source can be used.

Cooling of the driver board - The heat dissipated by the board will become significant when:

1. The JFET's duty cycle is closer to 100 %.
2. The power supplies are at or near their max rated +/- 15 V values.
3. The PWM frequency is higher than 25 kHz.

When one or more of the above conditions is met, care must be taken to ensure that none of the components on the PCB have surface temperature in excess of 100 °C. Options to improve cooling include reducing the ambient temperature in the vicinity of the driver board, increasing airflow, and sinking some of the heat from the board by soldering the board's mounting pins to a suitable copper plane of another PCB.

Additional information on the JFET and drive recommendations can be found in SemiSouth White Paper WP-SS2 and "how to use" applications note AN-SS1. For modification instructions for using the SGDR600P1 to drive other enhancement-mode or depletion-mode SiC JFETs please see applications note AN-SS3 Rev 2.

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