**Freescale Semiconductor**
Data Sheet: Technical Data

Document Number: P1013EC
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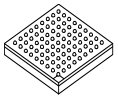
# P1013

# P1013 QorIQ Integrated Processor Hardware Specifications



WB-TePBGA II—689
31 mm x 31 mm

The following list provides an overview of the P1013 feature set:

- One high-performance 32-bit e500v2 core that implements the Power Architecture® technology:
- 36-bit physical addressing
  - Double-precision floating-point support
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache for each core
  - 400-MHz to 1067-MHz clock frequency
- 256-Kbyte L2 cache with ECC. Also configurable as SRAM and stashing memory.
- e500 coherency module (ECM) manages core and intrasystem transactions
- Integrated security engine (SEC)
  - Protocol support includes ARC4, 3DES, AES, RSA/ECC, RNG, single-pass SSL/TLS
  - XOR acceleration
- 64-bit DDR2/DDR3 SDRAM memory controller with ECC support
  - 32/64 bit data interface
  - DDR2/3 supported for data rate up to 667 MHz
  - Four banks of memory supported, each up to 8 Gbytes
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- Dual $I^2C$ controllers
- Enhanced secure digital host controller (SD/MMC)
- Enhanced Serial peripheral interface (eSPI)
- Enhanced local bus controller (eLBC)
- Display interface unit (DIU)
- I2S interface supported through synchronous serial interface (SSI)
- DUART
- Two High-Speed USB controller (USB 2.0)
  - Host and device support
  - Enhanced host controller interface (EHCI)
  - ULPI interface to PHY
- Two enhanced three-speed Ethernet controllers (eTSECs)
  - TCP/IP acceleration, quality of service, and classification capabilities
  - IEEE Std 1588™ support
  - Lossless flow control
  - RGMII, RMII, SGMII
- Two four-channel DMA controllers
- 87 general-purpose I/O signals
- Three PCI Express controllers
- Dual serial ATA (SATA) controllers
- TDM Interface
- Power management
- System performance monitor
- System access port
- IEEE Std 1149.1™- compatible, JTAG boundary scan
- Operating junction temperature ($T_j$) range: 0–105°C and –40–125°C (industrial specification)
- 31 × 31 mm 689-pin WB-TePBGA II (wire bond temperature-enhanced plastic BGA)

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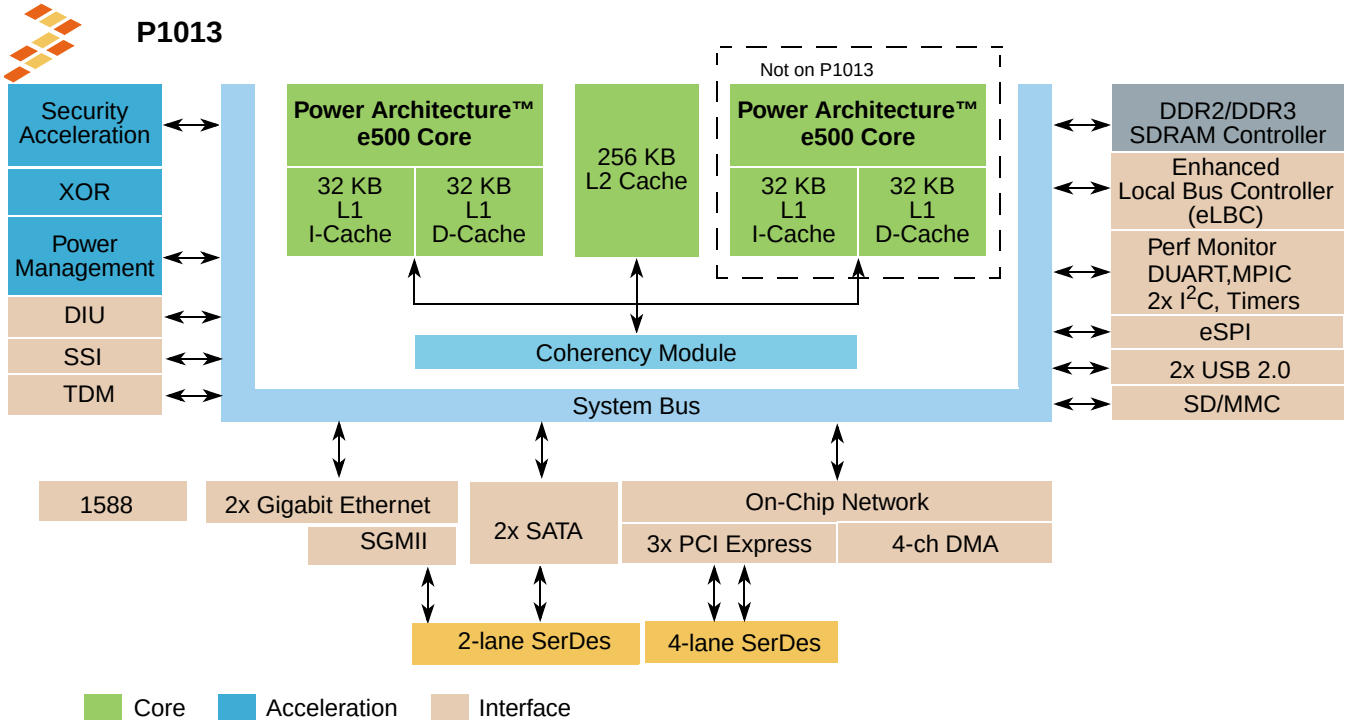



**Figure 1. P1013 Block Diagram**

# 1 Pin Assignments and Reset States

## 1.1 Ball Layout Diagrams

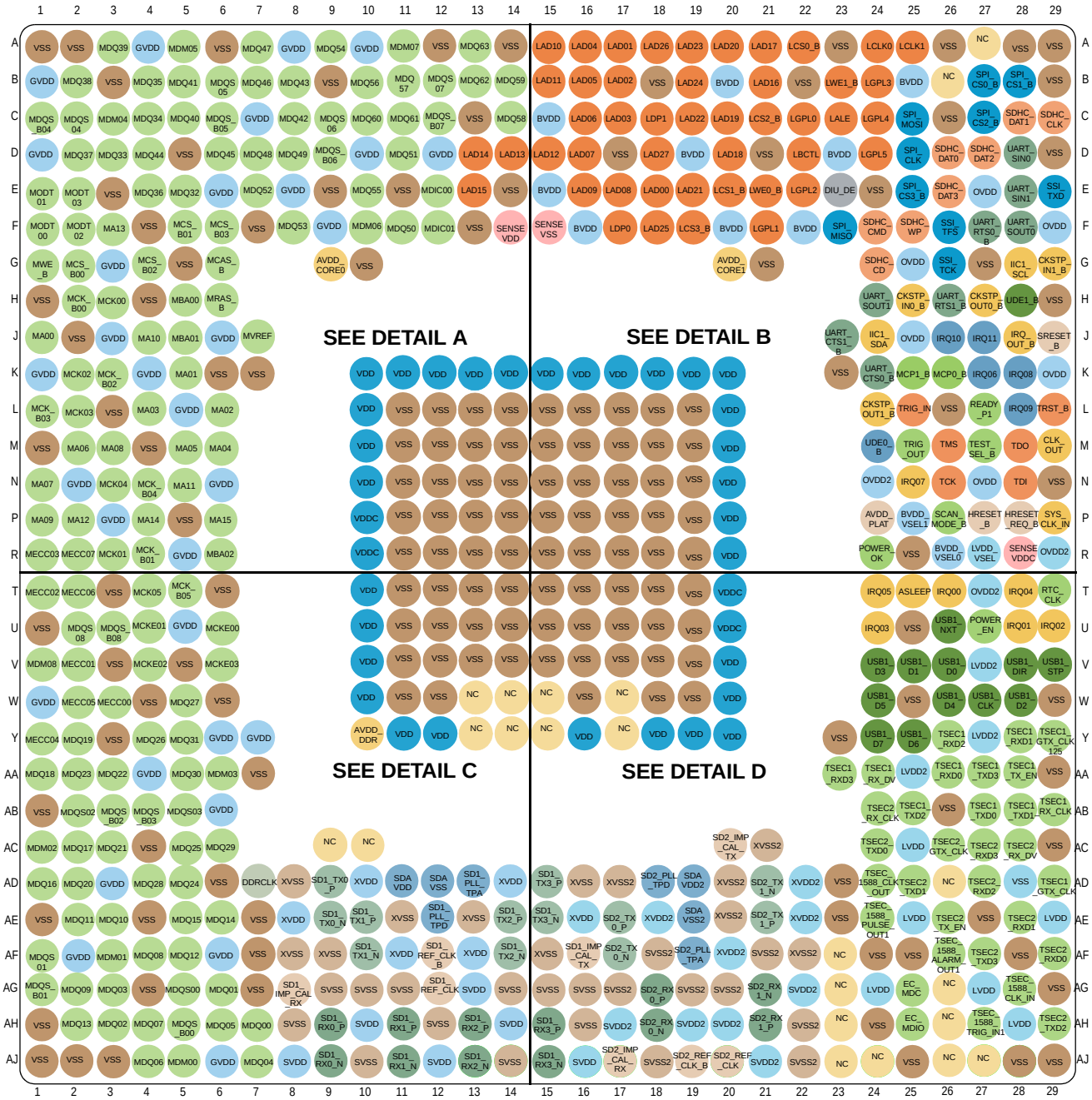



**Figure 2. P1013 Top View Ball Map**

**DETAIL A**

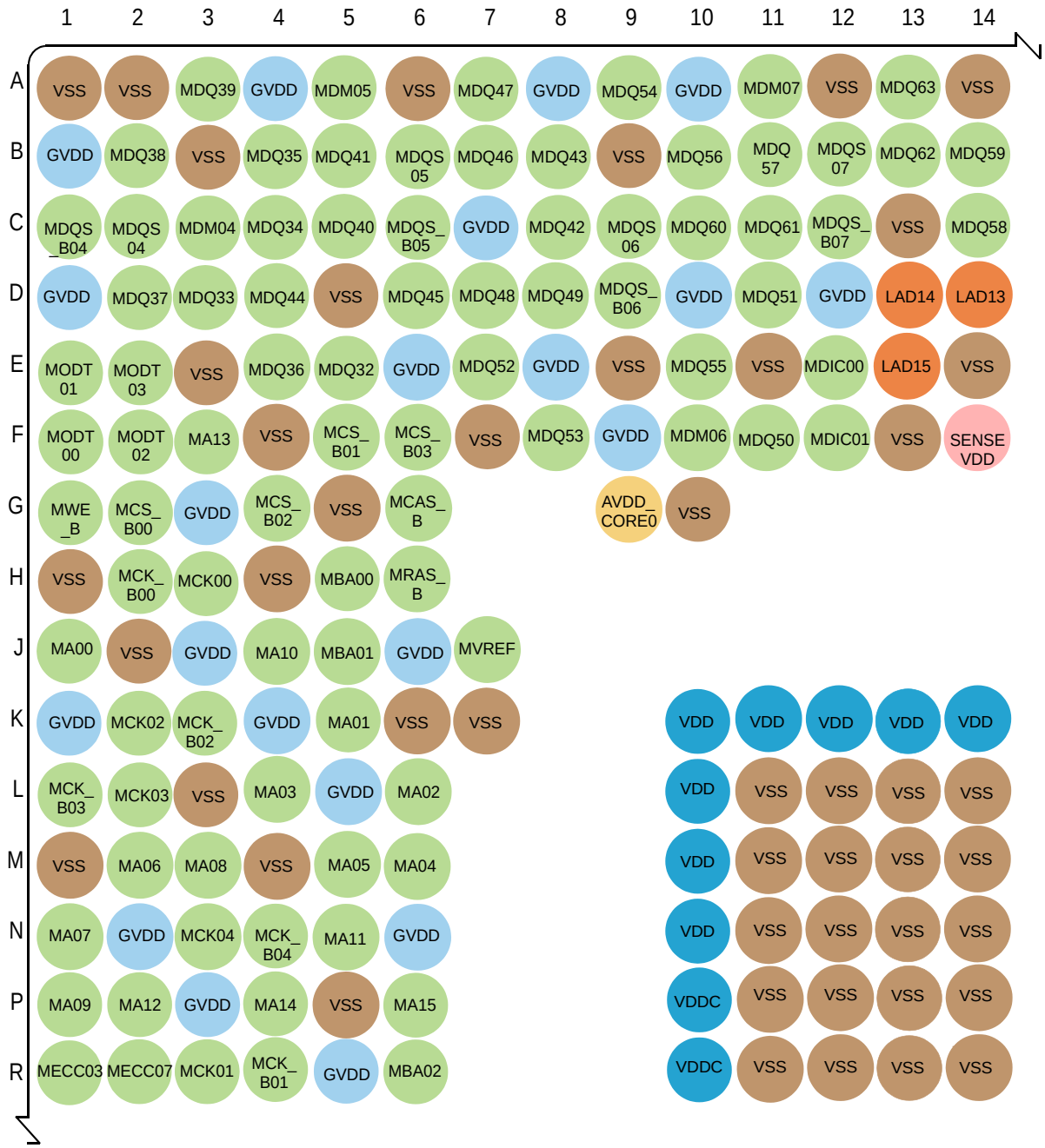



**Figure 3. P1013 Detail A Ball Map**

## DETAIL B

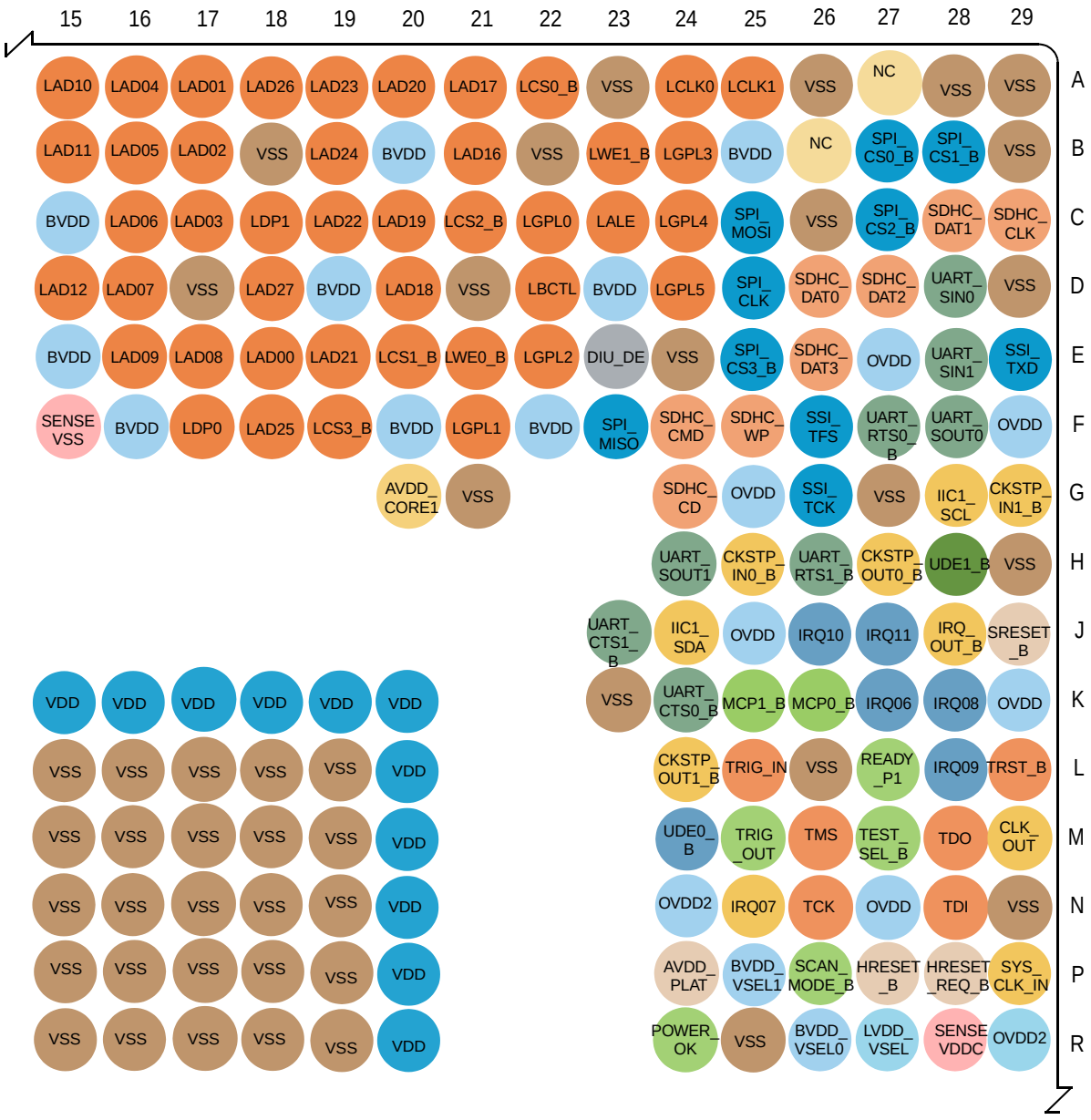



**Figure 4. P1013 Detail B Ball Map**

DETAIL C

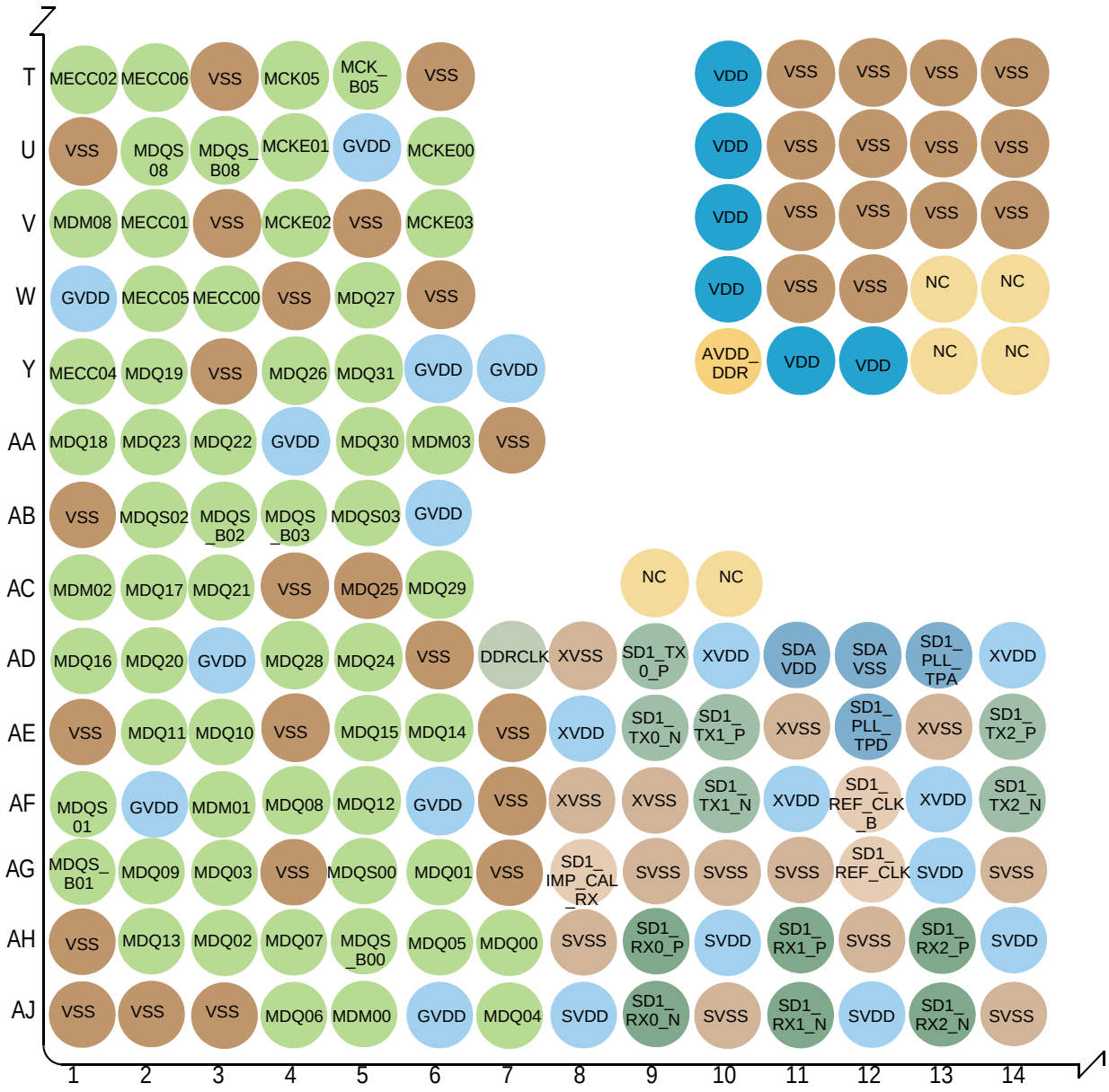



**Figure 5. P1013 Detail C Ball Map**

**DETAIL D**

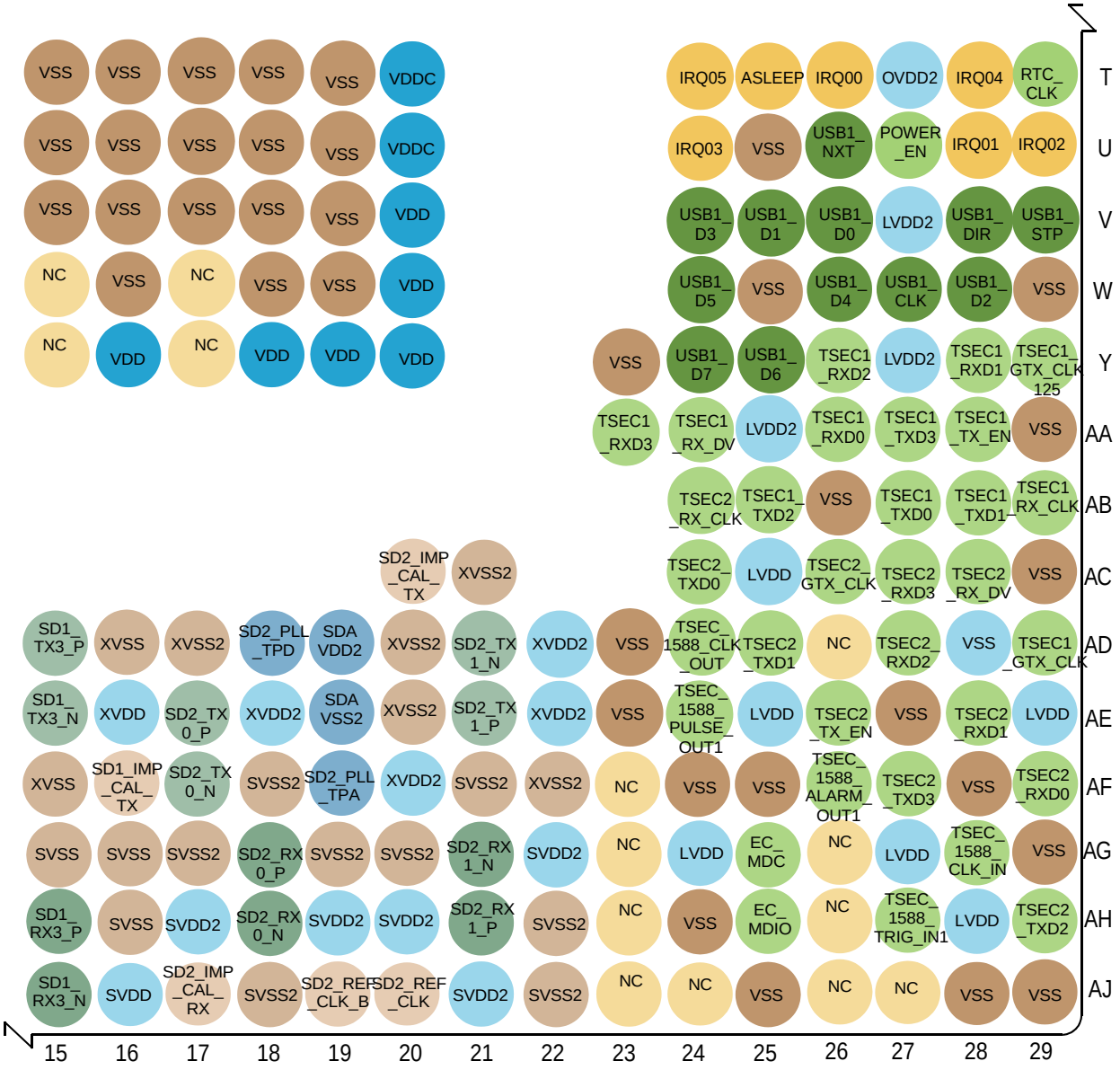



**Figure 6. P1013 Detail C Ball Map**

## 1.2 Pinout Assignments

**Table 1. P1013 Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| **DDR SDRAM Memory Interface** | | | | |
| MA00 | J1 | O | $GV_{DD}$ | — |
| MA01 | K5 | O | $GV_{DD}$ | — |
| MA02 | L6 | O | $GV_{DD}$ | — |
| MA03 | L4 | O | $GV_{DD}$ | — |
| MA04 | M6 | O | $GV_{DD}$ | — |
| MA05 | M5 | O | $GV_{DD}$ | — |
| MA06 | M2 | O | $GV_{DD}$ | — |
| MA07 | N1 | O | $GV_{DD}$ | — |
| MA08 | M3 | O | $GV_{DD}$ | — |
| MA09 | P1 | O | $GV_{DD}$ | — |
| MA10 | J4 | O | $GV_{DD}$ | — |
| MA11 | N5 | O | $GV_{DD}$ | — |
| MA12 | P2 | O | $GV_{DD}$ | — |
| MA13 | F3 | O | $GV_{DD}$ | — |
| MA14 | P4 | O | $GV_{DD}$ | — |
| MA15 | P6 | O | $GV_{DD}$ | — |
| MDQ00 | AH7 | I/O | $GV_{DD}$ | — |
| MDQ01 | AG6 | I/O | $GV_{DD}$ | — |
| MDQ02 | AH3 | I/O | $GV_{DD}$ | — |
| MDQ03 | AG3 | I/O | $GV_{DD}$ | — |
| MDQ04 | AJ7 | I/O | $GV_{DD}$ | — |
| MDQ05 | AH6 | I/O | $GV_{DD}$ | — |
| MDQ06 | AJ4 | I/O | $GV_{DD}$ | — |
| MDQ07 | AH4 | I/O | $GV_{DD}$ | — |
| MDQ08 | AF4 | I/O | $GV_{DD}$ | — |
| MDQ09 | AG2 | I/O | $GV_{DD}$ | — |
| MDQ10 | AE3 | I/O | $GV_{DD}$ | — |
| MDQ11 | AE2 | I/O | $GV_{DD}$ | — |
| MDQ12 | AF5 | I/O | $GV_{DD}$ | — |
| MDQ13 | AH2 | I/O | $GV_{DD}$ | — |
| MDQ14 | AE6 | I/O | $GV_{DD}$ | — |
| MDQ15 | AE5 | I/O | $GV_{DD}$ | — |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| MDQ16 | AD1 | I/O | $GV_{DD}$ | — |
| MDQ17 | AC2 | I/O | $GV_{DD}$ | — |
| MDQ18 | AA1 | I/O | $GV_{DD}$ | — |
| MDQ19 | Y2 | I/O | $GV_{DD}$ | — |
| MDQ20 | AD2 | I/O | $GV_{DD}$ | — |
| MDQ21 | AC3 | I/O | $GV_{DD}$ | — |
| MDQ22 | AA3 | I/O | $GV_{DD}$ | — |
| MDQ23 | AA2 | I/O | $GV_{DD}$ | — |
| MDQ24 | AD5 | I/O | $GV_{DD}$ | — |
| MDQ25 | AC5 | I/O | $GV_{DD}$ | — |
| MDQ26 | Y4 | I/O | $GV_{DD}$ | — |
| MDQ27 | W5 | I/O | $GV_{DD}$ | — |
| MDQ28 | AD4 | I/O | $GV_{DD}$ | — |
| MDQ29 | AC6 | I/O | $GV_{DD}$ | — |
| MDQ30 | AA5 | I/O | $GV_{DD}$ | — |
| MDQ31 | Y5 | I/O | $GV_{DD}$ | — |
| MDQ32 | E5 | I/O | $GV_{DD}$ | — |
| MDQ33 | D3 | I/O | $GV_{DD}$ | — |
| MDQ34 | C4 | I/O | $GV_{DD}$ | — |
| MDQ35 | B4 | I/O | $GV_{DD}$ | — |
| MDQ36 | E4 | I/O | $GV_{DD}$ | — |
| MDQ37 | D2 | I/O | $GV_{DD}$ | — |
| MDQ38 | B2 | I/O | $GV_{DD}$ | — |
| MDQ39 | A3 | I/O | $GV_{DD}$ | — |
| MDQ40 | C5 | I/O | $GV_{DD}$ | — |
| MDQ41 | B5 | I/O | $GV_{DD}$ | — |
| MDQ42 | C8 | I/O | $GV_{DD}$ | — |
| MDQ43 | B8 | I/O | $GV_{DD}$ | — |
| MDQ44 | D4 | I/O | $GV_{DD}$ | — |
| MDQ45 | D6 | I/O | $GV_{DD}$ | — |
| MDQ46 | B7 | I/O | $GV_{DD}$ | — |
| MDQ47 | A7 | I/O | $GV_{DD}$ | — |
| MDQ48 | D7 | I/O | $GV_{DD}$ | — |
| MDQ49 | D8 | I/O | $GV_{DD}$ | — |
| MDQ50 | F11 | I/O | $GV_{DD}$ | — |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| MDQ51 | D11 | I/O | $GV_{DD}$ | — |
| MDQ52 | E7 | I/O | $GV_{DD}$ | — |
| MDQ53 | F8 | I/O | $GV_{DD}$ | — |
| MDQ54 | A9 | I/O | $GV_{DD}$ | — |
| MDQ55 | E10 | I/O | $GV_{DD}$ | — |
| MDQ56 | B10 | I/O | $GV_{DD}$ | — |
| MDQ57 | B11 | I/O | $GV_{DD}$ | — |
| MDQ58 | C14 | I/O | $GV_{DD}$ | — |
| MDQ59 | B14 | I/O | $GV_{DD}$ | — |
| MDQ60 | C10 | I/O | $GV_{DD}$ | — |
| MDQ61 | C11 | I/O | $GV_{DD}$ | — |
| MDQ62 | B13 | I/O | $GV_{DD}$ | — |
| MDQ63 | A13 | I/O | $GV_{DD}$ | — |
| MBA0 | H5 | O | $GV_{DD}$ | — |
| MBA1 | J5 | O | $GV_{DD}$ | — |
| MBA2 | R6 | O | $GV_{DD}$ | — |
| MDQS0 | AG5 | I/O | $GV_{DD}$ | — |
| MDQS1 | AF1 | I/O | $GV_{DD}$ | — |
| MDQS2 | AB2 | I/O | $GV_{DD}$ | — |
| MDQS3 | AB5 | I/O | $GV_{DD}$ | — |
| MDQS4 | C2 | I/O | $GV_{DD}$ | — |
| MDQS5 | B6 | I/O | $GV_{DD}$ | — |
| MDQS6 | C9 | I/O | $GV_{DD}$ | — |
| MDQS7 | B12 | I/O | $GV_{DD}$ | — |
| MDQS0_B | AH5 | I/O | $GV_{DD}$ | — |
| MDQS1_B | AG1 | I/O | $GV_{DD}$ | — |
| MDQS2_B | AB3 | I/O | $GV_{DD}$ | — |
| MDQS3_B | AB4 | I/O | $GV_{DD}$ | — |
| MDQS4_B | C1 | I/O | $GV_{DD}$ | — |
| MDQS5_B | C6 | I/O | $GV_{DD}$ | — |
| MDQS6_B | D9 | I/O | $GV_{DD}$ | — |
| MDQS7_B | C12 | I/O | $GV_{DD}$ | — |
| MDM0 | AJ5 | O | $GV_{DD}$ | — |
| MDM1 | AF3 | O | $GV_{DD}$ | — |
| MDM2 | AC1 | O | $GV_{DD}$ | — |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| MDM3 | AA6 | O | $GV_{DD}$ | — |
| MDM4 | C3 | O | $GV_{DD}$ | — |
| MDM5 | A5 | O | $GV_{DD}$ | — |
| MDM6 | F10 | O | $GV_{DD}$ | — |
| MDM7 | A11 | O | $GV_{DD}$ | — |
| MDM8 | V1 | O | $GV_{DD}$ | — |
| MCS0_B | G2 | O | $GV_{DD}$ | — |
| MCS1_B | F5 | O | $GV_{DD}$ | — |
| MCS2_B | G4 | O | $GV_{DD}$ | — |
| MCS3_B | F6 | O | $GV_{DD}$ | — |
| MRAS_B | H6 | O | $GV_{DD}$ | — |
| MCAS_B | G6 | O | $GV_{DD}$ | — |
| MWE_B | G1 | O | $GV_{DD}$ | — |
| MCKE0 | U6 | O | $GV_{DD}$ | 17 |
| MCKE1 | U4 | O | $GV_{DD}$ | 17 |
| MCKE2 | V4 | O | $GV_{DD}$ | 17 |
| MCKE3 | V6 | O | $GV_{DD}$ | 17 |
| MCK0 | H3 | O | $GV_{DD}$ | 10 |
| MCK1 | R3 | O | $GV_{DD}$ | 10 |
| MCK2 | K2 | O | $GV_{DD}$ | 10 |
| MCK3 | L2 | O | $GV_{DD}$ | 10 |
| MCK4 | N3 | O | $GV_{DD}$ | 10 |
| MCK5 | T4 | O | $GV_{DD}$ | 10 |
| MCK0_B | H2 | O | $GV_{DD}$ | 10 |
| MCK1_B | R4 | O | $GV_{DD}$ | 10 |
| MCK2_B | K3 | O | $GV_{DD}$ | 10 |
| MCK3_B | L1 | O | $GV_{DD}$ | 10 |
| MCK4_B | N4 | O | $GV_{DD}$ | 10 |
| MCK5_B | T5 | O | $GV_{DD}$ | 10 |
| MODT0 | F1 | O | $GV_{DD}$ | — |
| MODT1 | E1 | O | $GV_{DD}$ | — |
| MODT2 | F2 | O | $GV_{DD}$ | — |
| MODT3 | E2 | O | $GV_{DD}$ | — |
| MDIC0 | E12 | I/O | $GV_{DD}$ | 5 |
| MDIC1 | F12 | I/O | $GV_{DD}$ | 5 |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| MECC0 | W3 | I/O | $GV_{DD}$ | — |
| MECC1 | V2 | I/O | $GV_{DD}$ | — |
| MECC2 | T1 | I/O | $GV_{DD}$ | — |
| MECC3 | R1 | I/O | $GV_{DD}$ | — |
| MECC4 | Y1 | I/O | $GV_{DD}$ | — |
| MECC5 | W2 | I/O | $GV_{DD}$ | — |
| MECC6 | T2 | I/O | $GV_{DD}$ | — |
| MECC7 | R2 | I/O | $GV_{DD}$ | — |
| MDQS8 | U2 | I/O | $GV_{DD}$ | — |
| MDQS8_B | U3 | I/O | $GV_{DD}$ | — |
| MVREF | J7 | I | $GV_{DD}$ | — |
| **eLBC Controller Interface/DIU** | | | | |
| LAD00 | E18 | I/O | $BV_{DD}$ | — |
| LAD01 | A17 | I/O | $BV_{DD}$ | — |
| LAD02 | B17 | I/O | $BV_{DD}$ | — |
| LAD03 | C17 | I/O | $BV_{DD}$ | — |
| LAD04 | A16 | I/O | $BV_{DD}$ | — |
| LAD05 | B16 | I/O | $BV_{DD}$ | — |
| LAD06 | C16 | I/O | $BV_{DD}$ | — |
| LAD07 | D16 | I/O | $BV_{DD}$ | — |
| LAD08/DIU_R0 | E17 | I/O | $BV_{DD}$ | — |
| LAD09/DIU_R1 | E16 | I/O | $BV_{DD}$ | 21 |
| LAD10/DIU_R2 | A15 | I/O | $BV_{DD}$ | — |
| LAD11/DIU_R3 | B15 | I/O | $BV_{DD}$ | 21 |
| LAD12/DIU_R4 | D15 | I/O | $BV_{DD}$ | 14 |
| LAD13/DIU_R5 | D14 | I/O | $BV_{DD}$ | 21 |
| LAD14/DIU_R6 | D13 | I/O | $BV_{DD}$ | — |
| LAD15/DIU_R7 | E13 | I/O | $BV_{DD}$ | 21 |
| LDP0/DIU_HSYNC | F17 | I/O | $BV_{DD}$ | 16, 24 |
| LDP1/DIU_VSYNC | C18 | I/O | $BV_{DD}$ | 16, 21 |
| LAD16/DIU_G0 | B21 | I/O | $BV_{DD}$ | 27 |
| LAD17/DIU_G1 | A21 | I/O | $BV_{DD}$ | 21 |
| LAD18/DIU_G2 | D20 | I/O | $BV_{DD}$ | — |
| LAD19/DIU_G3 | C20 | I/O | $BV_{DD}$ | — |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| LAD20/DIU_G4 | A20 | I/O | $BV_{DD}$ | — |
| LAD21/DIU_G5 | E19 | I/O | $BV_{DD}$ | — |
| LAD22/DIU_G6 | C19 | I/O | $BV_{DD}$ | — |
| LAD23/DIU_G7 | A19 | I/O | $BV_{DD}$ | 27 |
| LAD24/DIU_B0/LCS7_B | B19 | I/O | $BV_{DD}$ | 27 |
| LAD25/DIU_B1/LCS6_B | F18 | I/O | $BV_{DD}$ | 27 |
| LAD26/DIU_B2/LCS5_B | A18 | I/O | $BV_{DD}$ | 27 |
| LAD27/DIU_B3/LCS4_B | D18 | I/O | $BV_{DD}$ | 27 |
| LCS0_B | A22 | O | $BV_{DD}$ | 16 |
| LCS1_B | E20 | O | $BV_{DD}$ | 16 |
| LCS2_B/DIU_B5 | C21 | O | $BV_{DD}$ | 16 |
| LCS3_B/DIU_B4/LDP3 | F19 | I/O | $BV_{DD}$ | 16 |
| LWE0_B | E21 | O | $BV_{DD}$ | 15 |
| LWE1_B/DIU_B6 | B23 | O | $BV_{DD}$ | — |
| LBCTL/DIU_B7 | D22 | O | $BV_{DD}$ | 15 |
| LALE | C23 | O | $BV_{DD}$ | 15 |
| LGPL0 | C22 | O | $BV_{DD}$ | |
| LGPL1 | F21 | O | $BV_{DD}$ | 14 |
| LGPL2 | E22 | O | $BV_{DD}$ | 15 |
| LGPL3 | B24 | O | $BV_{DD}$ | — |
| LGPL4 | C24 | I/O | $BV_{DD}$ | 9 |
| LGPL5/DIU_CLKOUT | D24 | O | $BV_{DD}$ | — |
| LCLK0 | A24 | O | $BV_{DD}$ | — |
| LCLK1 | A25 | O | $BV_{DD}$ | — |
| DIU_DE | E23 | O | $BV_{DD}$ | 14 |
| **USB1 Interface** | | | | |
| USB1_NXT/GPIO2_0 | U26 | I/O | $LV_{DD2}$ | — |
| USB1_STP/GPIO2_1 | V29 | I/O | $LV_{DD2}$ | 21 |
| USB1_CLK/GPIO2_2 | W27 | I/O | $LV_{DD2}$ | — |
| USB1_DIR/GPIO2_3 | V28 | I/O | $LV_{DD2}$ | — |
| USB1_D7/GPIO2_4 | Y24 | I/O | $LV_{DD2}$ | — |
| USB1_D6/GPIO2_5 | Y25 | I/O | $LV_{DD2}$ | — |
| USB1_D5/GPIO2_6 | W24 | I/O | $LV_{DD2}$ | — |
| USB1_D4/GPIO2_7 | W26 | I/O | $LV_{DD2}$ | — |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| USB1_D3/GPIO2_8 | V24 | I/O | $LV_{DD2}$ | — |
| USB1_D2/GPIO2_9 | W28 | I/O | $LV_{DD2}$ | — |
| USB1_D1/GPIO2_10 | V25 | I/O | $LV_{DD2}$ | — |
| USB1_D0/GPIO2_11 | V26 | I/O | $LV_{DD2}$ | — |
| **Ethernet 1 Interface (RGMII/RMII)** | | | | |
| TSEC1_TX_EN/GPIO2_12 | AA28 | O | $LV_{DD2}$ | 22 |
| TSEC1_TXD0/GPIO2_13 | AB27 | O | $LV_{DD2}$ | 27 |
| TSEC1_TXD1/GPIO2_14 | AB28 | O | $LV_{DD2}$ | — |
| TSEC1_TXD2/GPIO2_15 | AB25 | O | $LV_{DD2}$ | 27 |
| TSEC1_TXD3/GPIO2_16 | AA27 | O | $LV_{DD2}$ | 21 |
| TSEC1_GTX_CLK/ TSEC1_TX_CLK/GPIO2_17 | AD29 | I/O | $LV_{DD2}$ | — |
| TSEC1_RX_DV/GPIO2_18 | AA24 | I/O | $LV_{DD2}$ | — |
| TSEC1_RX_CLK/GPIO2_19 | AB29 | I/O | $LV_{DD2}$ | — |
| TSEC1_RXD0/GPIO2_20 | AA26 | I/O | $LV_{DD2}$ | — |
| TSEC1_RXD1/GPIO2_21 | Y28 | I/O | $LV_{DD2}$ | — |
| TSEC1_RXD2/GPIO2_22 | Y26 | I/O | $LV_{DD2}$ | — |
| TSEC1_RXD3/GPIO2_23 | AA23 | I/O | $LV_{DD2}$ | — |
| TSEC1_GTX_CLK125/GPIO2_24 | Y29 | I/O | $LV_{DD2}$ | — |
| **Ethernet 2 Interface (RGMII/RMII)/USB2** | | | | |
| GPIO1_0/TSEC2_TX_EN/ USB2_STP | AE26 | I/O | $LV_{DD}$ | 22 |
| GPIO1_1/TSEC2_TXD0/USB2_D4 | AC24 | I/O | $LV_{DD}$ | — |
| GPIO1_2/TSEC2_TXD1/USB2_D5 | AD25 | I/O | $LV_{DD}$ | — |
| GPIO1_3/TSEC2_TXD2/USB2_D6 | AH29 | I/O | $LV_{DD}$ | — |
| GPIO1_4/TSEC2_TXD3/USB2_D7 | AF27 | I/O | $LV_{DD}$ | — |
| GPIO1_5/TSEC2_GTX_CLK/ TSEC2_TX_CLK/USB2_CLK | AC26 | I/O | $LV_{DD}$ | — |
| GPIO1_6/TSEC2_RX_DV/ USB2_NXT | AC28 | I/O | $LV_{DD}$ | — |
| GPIO1_7/TSEC2_RX_CLK/ USB2_DIR | AB24 | I/O | $LV_{DD}$ | — |
| GPIO1_8/TSEC2_RXD0/USB2_D0 | AF29 | I/O | $LV_{DD}$ | — |
| GPIO1_9/TSEC2_RXD1/USB2_D1 | AE28 | I/O | $LV_{DD}$ | — |
| GPIO1_10/TSEC2_RXD2/USB2_D2 | AD27 | I/O | $LV_{DD}$ | — |
| GPIO1_11/TSEC2_RXD3/USB2_D3 | AC27 | I/O | $LV_{DD}$ | — |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| **Ethernet MI** | | | | |
| EC_MDC | AG25 | O | $LV_{DD}$ | — |
| EC_MDIO | AH25 | I/O | $LV_{DD}$ | — |
| **1588** | | | | |
| TSEC_1588_CLK_IN/ USB1_PWRFAULT/GPIO1_12 | AG28 | I/O | $LV_{DD}$ | — |
| TSEC_1588_TRIG_IN1/ TSEC2_GTX_CLK125/ USB2_PWRFAULT/GPIO1_13 | AH27 | I/O | $LV_{DD}$ | — |
| TSEC_1588_ALARM_OUT1/GPIO1_14 | AF26 | O | $LV_{DD}$ | — |
| TSEC_1588_CLK_OUT/GPIO1_15 | AD24 | O | $LV_{DD}$ | 21 |
| TSEC_1588_PULSE_OUT1/GPIO1_16 | AE24 | O | $LV_{DD}$ | 24 |
| **eSPI/eSDHC** | | | | |
| SPI_MOSI/LWE2_B/GPIO1_17 | C25 | I/O | $BV_{DD}$ | 1 |
| SPI_MISO/LWE3_B/GPIO1_18 | F23 | I/O | $BV_{DD}$ | 1 |
| SPI_CLK/LDP2/GPIO1_19 | D25 | I/O | $BV_{DD}$ | 1 |
| SPI_CS0_B/SDHC_DAT4/ LAD28/GPIO1_20 | B27 | I/O | $BV_{DD}$ | 1 |
| SPI_CS1_B/SDHC_DAT5/ LAD29/GPIO1_21 | B28 | I/O | $BV_{DD}$ | 1 |
| SPI_CS2_B/SDHC_DAT6/ LAD30/GPIO1_22 | C27 | I/O | $BV_{DD}$ | 1 |
| SPI_CS3_B/SDHC_DAT7/ LAD31/GPIO1_23 | E25 | I/O | $BV_{DD}$ | 1 |
| SDHC_CMD/GPIO1_24 | F24 | I/O | $OV_{DD}$ | — |
| SDHC_DAT0/GPIO1_25 | D26 | I/O | $OV_{DD}$ | — |
| SDHC_DAT1 | C28 | I/O | $OV_{DD}$ | — |
| SDHC_DAT2 | D27 | I/O | $OV_{DD}$ | — |
| SDHC_DAT3/GPIO1_26 | E26 | I/O | $OV_{DD}$ | 28 |
| SDHC_CLK/GPIO1_27 | C29 | I/O | $OV_{DD}$ | — |
| SDHC_CD/GPIO1_28 | G24 | I/O | $OV_{DD}$ | — |
| SDHC_WP/GPIO1_29 | F25 | I/O | $OV_{DD}$ | — |
| **DUART/$I^2C$/SSI** | | | | |
| UART_SOUT0/DMA_DACK0_B/ GPIO1_30 | F28 | O | $OV_{DD}$ | — |
| UART_SIN0/DMA_DREQ0_B/ GPIO1_31 | D28 | I/O | $OV_{DD}$ | — |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| UART_CTS0_B/SSI_RCK/ TDM_RCLK/GPIO3_0 | K24 | I/O | $OV_{DD}$ | — |
| UART_RTS0_B/DMA_DDONE0_B/ GPIO3_1 | F27 | O | $OV_{DD}$ | 24 |
| IIC1_SDA/SSI_RXD/TDM_RXD | J24 | I/O | $OV_{DD}$ | 13, 20 |
| IIC1_SCL/SSI_RFS/TDM_RFS | G28 | I/O | $OV_{DD}$ | 13, 20 |
| UART_SOUT1/GPIO3_2 | H24 | O | $OV_{DD}$ | 15 |
| UART_SIN1/GPIO3_3 | E28 | I/O | $OV_{DD}$ | — |
| UART_CTS1_B/IIC2_SCL/GPIO3_4 | J23 | I/O | $OV_{DD}$ | 13, 20 |
| UART_RTS1_B/IIC2_SDA/GPIO3_5 | H26 | I/O | $OV_{DD}$ | 13, 20 |
| SSI_TCK/DMA_DACK1_B/ TDM_TCK/GPIO3_6 | G26 | I/O | $OV_{DD}$ | — |
| SSI_TFS/DMA_DDONE1_B/ TDM_TFS/GPIO3_7 | F26 | I/O | $OV_{DD}$ | — |
| SSI_TXD/DMA_DREQ1_B/ TDM_TXD/GPIO3_8 | E29 | I/O | $OV_{DD}$ | — |
| **Reset/System Control** | | | | |
| HRESET_B | P27 | I | $OV_{DD2}$ | — |
| HRESET_REQ_B | P28 | O | $OV_{DD2}$ | 21 |
| SRESET_B | J29 | I | $OV_{DD}$ | — |
| CKSTP_IN0_B | H25 | I | $OV_{DD}$ | 11 |
| CKSTP_IN1_B | G29 | I | $OV_{DD}$ | 11 |
| CKSTP_OUT0_B | H27 | O | $OV_{DD}$ | 11,13 |
| CKSTP_OUT1_B | L24 | O | $OV_{DD}$ | 11,13 |
| **Clocks** | | | | |
| SYS_CLK_IN | P29 | I | $OV_{DD2}$ | 7 |
| RTC_CLK | T29 | I | $OV_{DD2}$ | — |
| DDRCLK | AD7 | I | $OV_{DD2}$ | 25 |
| **Interrupts** | | | | |
| IRQ00/DMA_DREQ2_B/GPIO2_25 | T26 | I/O | $OV_{DD2}$ | — |
| IRQ01/DMA_DACK2_B/GPIO2_26 | U28 | I/O | $OV_{DD2}$ | — |
| IRQ02/DMA_DDONE2_B/GPIO2_27 | U29 | I/O | $OV_{DD2}$ | — |
| IRQ03/DMA_DREQ3_B/GPIO2_28 | U24 | I/O | $OV_{DD2}$ | — |
| IRQ04/DMA_DACK3_B/GPIO2_29 | T28 | I/O | $OV_{DD2}$ | — |
| IRQ05/DMA_DDONE3_B/GPIO2_30 | T24 | I/O | $OV_{DD2}$ | — |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| IRQ06/MSRCID0/LB_MSRCID0/ GPIO2_31 | K27 | I/O | $OV_{DD}$ | — |
| IRQ07/MSRCID1/LB_MSRCID1/ GPIO3_9 | N25 | I/O | $OV_{DD}$ | — |
| IRQ08/MSRCID2/LB_MSRCID2/ GPIO3_10 | K28 | I/O | $OV_{DD}$ | — |
| IRQ09/MSRCID3/LB_MSRCID3/ GPIO3_11 | L28 | I/O | $OV_{DD}$ | — |
| IRQ10/MSRCID4/LB_MSRCID4/ GPIO3_12 | J26 | I/O | $OV_{DD}$ | — |
| IRQ11/MDVAL/LB_MDVAL/ GPIO3_13 | J27 | I/O | $OV_{DD}$ | — |
| MCP0_B/GPIO3_14 | K26 | I/O | $OV_{DD}$ | — |
| MCP1_B/GPIO3_15 | K25 | I/O | $OV_{DD}$ | — |
| UDE0_B/GPIO3_16 | M24 | I/O | $OV_{DD}$ | — |
| UDE1_B/GPIO3_17 | H28 | I/O | $OV_{DD}$ | — |
| IRQ_OUT_B/GPIO3_18 | J28 | O | $OV_{DD}$ | 12, 13, 21 |
| **I/O VSEL** | | | | |
| $LV_{DD}$_VSEL | R27 | I | $OV_{DD2}$ | 26 |
| $BV_{DD}$_VSEL0 | R26 | I | $OV_{DD2}$ | 26 |
| $BV_{DD}$_VSEL1 | P25 | I | $OV_{DD2}$ | 26 |
| **JTAG** | | | | |
| TCK | N26 | I | $OV_{DD2}$ | — |
| TDI | N28 | I | $OV_{DD2}$ | 18 |
| TDO | M28 | O | $OV_{DD2}$ | 17 |
| TMS | M26 | I | $OV_{DD2}$ | 18 |
| TRST_B | L29 | I | $OV_{DD2}$ | 18 |
| **Misc Debug/Power Management/DFT** | | | | |
| SCAN_MODE_B | P26 | I | $OV_{DD2}$ | 29 |
| TEST_SEL | M27 | I | $OV_{DD2}$ | 2 |
| ASLEEP | T25 | O | $OV_{DD2}$ | 27 |
| POWER_EN | U27 | O | $OV_{DD2}$ | — |
| POWER_OK/GPIO3_19 | R24 | I/O | $OV_{DD2}$ | — |
| TRIG_IN/GPIO3_20 | L25 | I/O | $OV_{DD}$ | — |
| TRIG_OUT/READY_P0/GPIO3_21 | M25 | O | $OV_{DD2}$ | — |
| READY_P1/GPIO3_22 | L27 | O | $OV_{DD2}$ | 15 |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| CLK_OUT | M29 | O | $OV_{DD}$ | — |
| **SerDes 1(x4)** | | | | |
| SD1_TX0_P | AD9 | O | $XV_{DD}$ | — |
| SD1_TX1_P | AE10 | O | $XV_{DD}$ | — |
| SD1_TX2_P | AE14 | O | $XV_{DD}$ | — |
| SD1_TX3_P | AD15 | O | $XV_{DD}$ | — |
| SD1_TX0_N | AE9 | O | $XV_{DD}$ | — |
| SD1_TX1_N | AF10 | O | $XV_{DD}$ | — |
| SD1_TX2_N | AF14 | O | $XV_{DD}$ | — |
| SD1_TX3_N | AE15 | O | $XV_{DD}$ | — |
| SD1_RX0_P | AH9 | I | $SV_{DD}$ | — |
| SD1_RX1_P | AH11 | I | $SV_{DD}$ | — |
| SD1_RX2_P | AH13 | I | $SV_{DD}$ | — |
| SD1_RX3_P | AH15 | I | $SV_{DD}$ | — |
| SD1_RX0_N | AJ9 | I | $SV_{DD}$ | — |
| SD1_RX1_N | AJ11 | I | $SV_{DD}$ | — |
| SD1_RX2_N | AJ13 | I | $SV_{DD}$ | — |
| SD1_RX3_N | AJ15 | I | $SV_{DD}$ | — |
| SD1_REF_CLK | AG12 | I | $XV_{DD}$ | — |
| SD1_REF_CLK_B | AF12 | I | $XV_{DD}$ | — |
| SD1_PLL_TPD | AE12 | O | $XV_{DD}$ | — |
| SD1_IMP_CAL_TX | AF16 | I | $XV_{DD}$ | 3 |
| SD1_IMP_CAL_RX | AG8 | I | $XV_{DD}$ | 4 |
| SD1_PLL_TPA | AD13 | O | $XV_{DD}$ | — |
| **SerDes 2(x2)** | | | | |
| SD2_TX0_P | AE17 | O | $XV_{DD2}$ | — |
| SD2_TX1_P | AE21 | O | $XV_{DD2}$ | — |
| SD2_TX0_N | AF17 | O | $XV_{DD2}$ | — |
| SD2_TX1_N | AD21 | O | $XV_{DD2}$ | — |
| SD2_RX0_P | AG18 | I | $SV_{DD2}$ | — |
| SD2_RX1_P | AH21 | I | $SV_{DD2}$ | — |
| SD2_RX0_N | AH18 | I | $SV_{DD2}$ | — |
| SD2_RX1_N | AG21 | I | $SV_{DD2}$ | — |
| SD2_REF_CLK | AJ20 | I | $XV_{DD2}$ | — |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| SD2_REF_CLK_B | AJ19 | I | $XV_{DD2}$ | — |
| SD2_PLL_TPD | AD18 | O | $XV_{DD2}$ | — |
| SD2_IMP_CAL_TX | AC20 | I | $XV_{DD2}$ | 3 |
| SD2_IMP_CAL_RX | AJ17 | I | $XV_{DD2}$ | 4 |
| SD2_PLL_TPA | AF19 | O | $XV_{DD2}$ | — |
| **Voltage Sense/Process** | | | | |
| SENSEVDD | F14 | I/O | — | 6 |
| SENSEVDDC | R28 | I/O | — | 6 |
| SENSEVSS | F15 | I/O | — | 6 |
| **Power** | | | | |
| $AV_{DD}$_CORE1 | G20 | I | — | 19 |
| $AV_{DD}$_DDR | Y10 | I | — | 19 |
| $AV_{DD}$_PLAT | P24 | I | — | 19 |
| $GV_{DD}$ | A10, A4, A8, AA4, AB6, AD3, AF2, AF6, AJ6, B1, C7, D1, D10, D12, E6, E8, F9, G3, J3, J6, K1, K4, L5, N2, N6, P3, R5, U5, W1, Y6, Y7 | I | — | — |
| $BV_{DD}$ | B20, B25, C15, D19, D23, E15, F16, F20, F22 | I | — | — |
| $OV_{DD}$ | E27, F29, G25, J25, K29, N27 | I | — | 8 |
| $OV_{DD2}$ | N24, R29, T27 | I | — | 8 |
| $LV_{DD}$ | AC25, AE25, AE29, AG24, AG27, AH28 | I | — | 8 |
| $LV_{DD2}$ | AA25, V27, Y27 | I | — | 8 |
| $SV_{DD}$ | AG13, AH10, AH14, AJ12, AJ16, AJ8 | I | — | — |
| $SV_{DD2}$ | AG22, AH17, AH19, AH20, AJ21 | I | — | — |
| $SDAV_{DD}$ | AD11 | I | — | — |
| $SDAV_{DD2}$ | AD19 | I | — | — |
| $XV_{DD}$ | AD10, AD14, AE16, AE8, AF11, AF13 | I | — | — |
| $XV_{DD2}$ | AD22, AE18, AE22, AF20 | I | — | — |
| VDDC | P10, R10, T20, U20 | I | — | 8 |
| VDD | K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, K20, L10, L20, M10, M20, N10, N20, P20, R20, T10, U10, V10, V20, W10, W20, Y11, Y12, Y16, Y18, Y19, Y20, G9 | I | — | 8 |
| **Ground** | | | | |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| VSS | A1, A2, A6, A12, A14, A23, A26, A28, A29, AA29, AA7, AB1, AB26, AC4, AC29, AD6, AD23, AE1, AE4, AE23, AE27, AF7, AF24, AF25, AF28, AG4, AG7, AG29, AH1, AH24, AJ1, AJ2, AJ3, AJ25, AJ28, AJ29, B3, B9, B18, B22, B29, C13, C26, D5, D17, D21, D29, E3, E9, E11, E14, E24, F4, F7, F13, G5, G10, G21, G27, H1, H4, H29, J2, K6, K7, K23, L3, L11, L12, L13, L14, L15, L16, L17, L18, L19, L26, M1, M4, M11, M12, M13, M14, M15, M16, M17, M18, M19, N11, N12, N13, N14, N15, N16, N17, N18, N19, N29, P5, P11, P12, P13, P14, P15, P16, P17, P18, P19, R11, R12, R13, R14, R15, R16, R17, R18, R19, R25, T3, T6, T11, T12, T13, T14, T15, T16, T17, T18, T19, U1, U11, U12, U13, U14, U15, U16, U17, U18, U19, U25, V3, V5, V11, V12, V13, V14, V15, V16, V17, V18, V19, W4, W6, W11, W12, W16, W18, W19, W25, W29, Y3, Y23, AE7, AD28 | I | — | — |
| SDAVSS | AD12 | I | — | — |
| SDAVSS2 | AE19 | I | — | — |
| $XV_{SS}$ | AD16, AD8, AE11, AE13, AF15, AF8, AF9 | I | — | — |
| $XV_{SS2}$ | AC21, AD17, AD20, AE20, AF22 | I | — | — |
| SVSS | AG9, AG10, AG11, AG14, AG15, AG16, AH8, AH12, AH16, AJ10, AJ14, | I | — | — |
| SVSS2 | AF18, AF21, AG17, AG19, AG20, AH22, AJ18, AJ22 | I | — | — |
| **Not Connected** | | | | |
| NC | AC10, AC9, AF23, AG23, AG26, AH23, AH26, AJ23, AJ24, AJ26, AJ27, W13, W14, W15, W17, Y13, Y14, Y15, Y17, AD26, B26, A27 | NC | — | — |

**Table 1. P1013 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|

**Note:**

1. For eSDHC (8-bit), $BV_{DD}$ has to be 3.3V
2. This pin should be pulled down
3. Connect with 100ohm (±1%) to GND
4. Connect with 200ohm (±1%) to GND
5. In DDR2 mode, connect MDIC[0] to GND and MDIC[1] to GVDD through 18.2Ω (full strength mode) or 36.4Ω (half strength mode) precision 1% resistors. In DDR3 mode these resistors should be 20x (full strength mode) or 40x (half strength mode). These pins are used for automatic hardware calibration of DDR I/Os.
6. These pins can be left unconnected if they are not used.
7. Also referred to as SYSCLK in this document. This is the main system clock of the device.
8. Switchable supplies should be derived from their continuos counterparts as shown in Section "External Power Supply Requirements" in the *P1022 QorIQ Integrated Processor Reference Manual*.
9. For systems which boot from Local Bus (GPCM)-controller NOR flash or (FCM)-controlled NAND flash, a pull up on LGPL4 is required.
10. Disable the clocks that are not used via the DDRCLKDR register. By default, all clocks are enabled, but all clock signals might not be used in an application. DDRCLKDR is in Section "Global Utilities" in the *P1022 QorIQ Integrated Processor Reference Manual*.
11. It is recommended that a weak pull-up resistor (2-10kΩ) be placed on these pins to $OV_{DD}$.
12. If this pin is configured as IRQ_OUT, it is recommended that a weak pull-up resistor (2-10kΩ) be placed on this pin to $OV_{DD}$.
13. These pins CKSTP_OUT0_B, CKSTP_OUT1_B, IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL are open drain signals. Further GPIO pins may be programmed to operate as open-drain signals.
14. The value of DIU_DE, LAD[12] and LGPL[1] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7kΩ pull-up or pull-down resistors. See *P1022 QorIQ Integrated Processor Reference Manual* for clock ratio settings.
15. The value of LBCTL, LALE, LGPL[02], LWE[00], UART_SOUT[01], and READY_P1, at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7kΩ pull-up or pull-down resistors. See *P1022 QorIQ Integrated Processor Reference Manual* for clock ratio settings.
16. If these pins are configured for local bus controller use, it is recommend that a weak pull-up resistor (2-10kΩ) be placed on these pins to BVDD, to ensure that there is no random chip select assertion due to possible noise etc.
17. These outputs are actively driven during reset rather than being tristated during reset.
18. These JTAG pins have weak internal pull-ups that are always enabled.
19. Independent supplies derived from board $V_{DD}$.
20. When used as $I^2C$, it is recommended that an appropriate pull-up resistor be placed on these pins to $OV_{DD}$.
21. These pins must NOT be pulled down by a resistor or the component they are connected to during power-on reset. When pulled low during POR, the device behavior may be undefined.
22. When eTSEC1 and eTSEC2 are used as parallel interfaces, pins TSEC1_TX_EN and TSEC2_TX_EN require an external 4.7kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
23. The value of UART_RTS0, 1588_PULSE_OUT1 and LDP0, at reset set the DDR controller Clock PLL ratio. These pins require 4.7kΩ pull-up or pull-down resistors. See *P1022 QorIQ Integrated Processor Reference Manual* for clock ratio settings.
24. DDRCLK input is only required when the P1013 DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via reset configuration setting cfg_ddr_pll[0:2]= 111, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode. See the *P1022 QorIQ Integrated Processor Reference Manual* for more details.
25. Incorrect settings can lead to irreversible device damage.
26. These pins are all reset configuration pins. See the Chapter "Reset Configuration" in the *P1022 QorIQ Integrated Processor Reference Manual* for details on what configuration is done by these pins. These pins require a 4.7kΩ pull-up or pull-down resistor.
27. 100kΩ pull-down needed if SDHC_DAT3 signal used as CD pin for SD cards. This pull down is not needed for MMC cards.
28. This pin requires a 1 kΩ pull-up to $OV_{DD2}$

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the P1013 device. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

## 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

### 2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

**Table 2. Absolute Maximum Ratings[1]**

| Characteristic | | Symbol | Max Value | Unit | Note |
|---|---|---|---|---|---|
| Supply voltage for DDR, eTSEC, ECM, and COP | | $V_{DDC}$ | -0.3 to 1.05 | V | — |
| Cores and Platform supply voltage (except the ones mentioned above) | | $V_{DD}$ | –0.3 to 1.05 | V | — |
| PLL supply voltages | | $AV_{DD}$_CORE0, $AV_{DD}$_CORE1, $AV_{DD}$_DDR, $AV_{DD}$_PLAT | –0.3 to 1.05 | V | 2 |
| SerDes Transceivers | Core power supply | $SV_{DD}$, $SV_{DD2}$ | –0.3 to 1.05 | V | — |
| | Pad power supply | $XV_{DD}$, $XV_{DD2}$ | –0.3 to 1.05 | V | — |
| | PLL Power Supply | $SDAV_{DD}$, $SDAV_{DD2}$ | -0.3 to 1.05 | | — |
| DDR2/3 DRAM I/O voltage | | $GV_{DD}$ | –0.3 to 1.98<br>–0.3 to 1.65 | V | — |
| Three-speed Ethernet I/O, MII management voltage, USB | | $LV_{DD}$<br>$LV_{DD2}$ | –0.3 to 3.63<br>–0.3 to 2.75 | V | — |
| DUART, $I^2C$, SSI, eSDHC, system control and power management, and JTAG I/O voltage | | $OV_{DD}$, $OV_{DD2}$ | –0.3 to 3.63 | V | — |
| eSPI, eSDHC, DIU, and eLBC I/O voltage | | $BV_{DD}$ | –0.3 to 3.63<br>–0.3 to 2.75<br>–0.3 to 1.98 | V | — |
| Input voltage | DDR2/DDR3 DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 3, 6 |
| | DDR2/DDR3 DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$/2 + 0.3) | V | 6 |
| | USB and Three-speed Ethernet signals | $LV_{IN}$ | –0.3 to ($LV_{DD}$ + 0.3) | V | 5, 6 |
| | eSPI, eSDHC, DIU, and eLBC signals | $BV_{IN}$ | –0.3 to ($BV_{DD}$ + 0.3) | — | 7 |
| | DUART, SYSCLK, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 4, 6 |
| | SerDes signals | $XV_{IN}$ | -0.3 to ($XV_{DD}$ + 0.3) | | 8 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | °C | — |

**Table 2. Absolute Maximum Ratings[1] (continued)**

| Characteristic | Symbol | Max Value | Unit | Note |
|---|---|---|---|---|

**Note:**

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. $AV_{DD}$_CORE0, $AV_{DD}$_CORE1, $AV_{DD}$_PLAT and $AV_{DD}$_DDR are measured at the input to the filter (as shown in AN4343) and not at the pin of the device.
3. **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** $OV_{IN}$ must not exceed $OV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** $LV_{IN}$ must not exceed $LV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. (M,L,O)$V_{IN}$ and $MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.
7. **Caution:** $BV_{IN}$ must not exceed $BV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. **Caution:** $XV_{IN}$ must not exceed $XV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

## 2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

**Table 3. Recommended Operating Conditions**

| Characteristic | | Symbol | Recommended Value | Unit | Note |
|---|---|---|---|---|---|
| Supply voltage for DDR, eTSEC, ECM and COP | | $V_{DDC}$ | 1.0 ± 50 mV | V | 1 |
| Cores and Platform supply voltage | | $V_{DD}$ | 1.0 ± 50 mV | V | 1 |
| PLL supply voltages | | $AV_{DD}$_CORE0<br>$AV_{DD}$_CORE1<br>$AV_{DD}$_DDR<br>$AV_{DD}$_PLAT | 1.0 ± 50 mV | V | — |
| SerDes Transceivers | Core power supply | $SV_{DD}$<br>$SV_{DD2}$ | 1.0 ± 50 mV | V | — |
| | Pad power supply | $XV_{DD}$<br>$XV_{DD2}$ | 1.0 ± 50 mV | V | — |
| | PLL Power Supply | $SDAV_{DD}$<br>$SDAV_{DD2}$ | 1.0 ± 50 mV | — | — |
| DDR2/3 DRAM I/O voltage | | $GV_{DD}$ | 1.8 V ± 100 mV<br>1.5 V ± 75 mV | V | 2 |
| Three-speed Ethernet I/O, MII management voltage, USB | | $LV_{DD}$<br>$LV_{DD2}$ | 3.3 V ± 165 mV<br>2.5 V ± 125 mV | — | 2 |
| DUART, $I^2C$, SSI, eSDHC, system control and power management and JTAG I/O voltage | | $OV_{DD}$<br>$OV_{DD2}$ | 3.3 V ± 165 mV | V | 2 |
| eSPI, eSDHC, DIU, and eLBC I/O voltage | | $BV_{DD}$ | 3.3 V ± 165 mV<br>2.5 V ± 125 mV<br>1.8 V ± 90 mV | V | 2 |

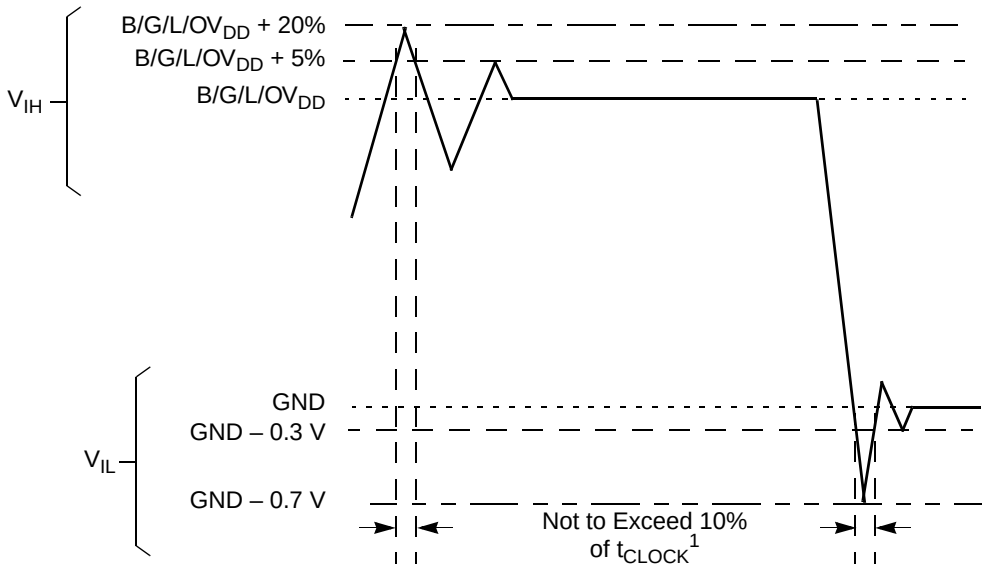
**Table 3. Recommended Operating Conditions (continued)**

| Characteristic | | Symbol | Recommended Value | Unit | Note |
|---|---|---|---|---|---|
| Input voltage | DDR2/DDR3 DRAM signals | $MV_{IN}$ | GND to $GV_{DD}$ | V | — |
| | DDR3 DRAM reference | $MV_{REF}$ | $GV_{DD}/2$ ± 2% | V | — |
| | DDR2 DRAM reference | $MV_{REF}$ | $GV_{DD}/2$ ± 2% | V | — |
| | Three-speed Ethernet signals and USB | $LV_{IN}$ | GND to $LV_{DD}$ | V | — |
| | eSPI, eSDHC, DIU, and eLBC signals | $BV_{IN}$ | GND to $BV_{DD}$ | V | — |
| | DUART, SYSCLK, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | GND to $OV_{DD}$ | V | — |
| | SerDes signals | $XV_{IN}$ | GND to $XV_{DD}$ | V | — |
| Junction Temperature range | | $T_A/T_J$ | 0 to 105 Commercial<br>–40 to 125 Industrial | °C | 3 |

**Note:**

1. **Caution:** Until $V_{DD}$ reaches its recommended operating voltage, $V_{DD}$ may exceed $L/B/G/OV_{DD}$ by up to 0.7 V. If 0.7 V is exceeded, extra current will be drawn by the device.
2. **Caution:** Until $V_{DD}$ reaches its recommended operating voltage, if $L/B/G/OV_{DD}$ exceeds $V_{DD}$ extra current may be drawn by the device.
3. Min temp is specified with $T_A$; Max temp is specified with $T_J$.
4. All I/O pins should be interfaced with peripheral devices operating at the same voltage level.
5. In deep sleep power saving mode all switchable power supplies must be switched off to prevent damage to the device.

This figure shows the undershoot and overshoot voltages at the interfaces of the device.




**Note:**

1. $t_{CLOCK}$ refers to the clock period associated with the respective interface:
   For $I^2C$ and JTAG, $t_{CLOCK}$ references SYSCLK.
   For DDR, $t_{CLOCK}$ references MCLK.
   For eTSEC, $t_{CLOCK}$ references EC_GTX_CLK125.
   For eLBC, $t_{CLOCK}$ references LCLK.

**Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}$**

The core voltage must always be provided at nominal rated VDD (see Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. $OV_{DD}$ and $LV_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2/3 SDRAM interface uses a differential receiver referenced the externally supplied $MV_{REF}$ signal (nominally set to $GV_{DD}/2$).

### 2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

**Table 4. Output Drive Capability**

| Driver Type | Output Impedance (Ω) | Supply Voltage | Note |
|---|---|---|---|
| eSPI, eSDHC, DIU, and eLBC interface | 45<br>45<br>45 | $BV_{DD}$ = 3.3 V<br>$BV_{DD}$ = 2.5 V<br>$BV_{DD}$ = 1.8 V | 2 |
| DDR2/3 signal (Programmable) | 16<br>32 (half strength mode) | $GV_{DD}$ = 1.8 V DDR2<br>$GV_{DD}$ = 1.5 V DDR3 | 1 |
| USB and eTSEC signals | 45 | $LV_{DD}$ = 2.5/3.3 V<br>$LV_{DD2}$ = 2.5/3.3 V | 2 |
| DUART, $I^2C$, SSI, eSDHC, system control, JTAG | 45 | $OV_{DD}$ = 3.3 V<br>$OV_{DD2}$ = 3.3. V | 2 |

**Note:**

1. The drive strength of the DDR2/3 interface in half-strength mode is at $T_j$ = 105°C and at $GV_{DD}$ (min)
2. For GPIOs multiplexed with pins on these power supplies the drive capabilities are similar to those of the primary functions of the pins.

## 2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up when POWER_EN is not used to control switchable supplies:

1. $V_{DDC}$, $V_{DD}$, $AV_{DD}$_PLAT, $AV_{DD}$_DDR, $LV_{DD2}$, $OV_{DD2}$, $AV_{DD}$_CORE0, $AV_{DD}$_CORE1, $BV_{DD}$, $LV_{DD}$, $OV_{DD}$, $SV_{DD}$, $SV_{DD2}$, $XV_{DD}$, $XV_{DD2}$, $SDAV_{DD}$, $SDAV_{DD2}$
2. $GV_{DD}$

The requirements are as follows for power up when POWER_EN is used to control switchable supplies:

1. Always ON core supply: $V_{DDC}$, $AV_{DD}$_PLAT, $AV_{DD}$_DDR
2. Always ON I/O supply: $LV_{DD2}$, $OV_{DD2}$, $GV_{DD}$
   – Wait for POWER_EN to assert
3. Switchable core supply: $V_{DD}$, $AV_{DD}$_CORE0, $AV_{DD}$_CORE1
4. Switchable I/O supply: $BV_{DD}$, $LV_{DD}$, $OV_{DD}$, $SV_{DD}$, $SV_{DD2}$, $XV_{DD}$, $XV_{DD2}$, $SDAV_{DD}$ and $SDAV_{DD2}$

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for $GV_{DD}$ is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for $GV_{DD}$ is not required.

**NOTE**

From a system standpoint, if any of the I/O power supplies ramp prior to the VDD core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

## 2.3 Power Down Requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

## 2.4 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table provides the RESET initialization AC timing specifications.

**Table 5. RESET Initialization Timing Specifications**

| Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ | 25 | — | μs | 1, 2 |
| Minimum assertion time of $\overline{\text{TRESET}}$ simultaneous to HRESET assertion | 25 | — | ns | 3 |
| Maximum rise/fall time of $\overline{\text{HRESET}}$ | — | 1 | $t_{SYSCLK}$ | — |
| Minimum assertion time for $\overline{\text{SRESET}}$ | 3 | — | $t_{SYSCLK}$ | 4 |
| PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation | 100 | — | μs | — |
| Input setup time for POR configurations (other than PLL configuration) with respect to negation of $\overline{\text{HRESET}}$ | 4 | — | $t_{SYSCLK}$ | 4 |
| Input hold time for all POR configurations (including PLL configuration) with respect to negation of $\overline{\text{HRESET}}$ | 8 | — | $t_{SYSCLK}$ | 4 |
| Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{HRESET}}$ | — | 12 | $t_{SYSCLK}$ | 4 |

**Note:**

1. There may be some extra current leakage when driving signals high during this time.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.
3. TRST is an asynchronous level sensitive signal. For guidance on how this requirement can be met, refer to the JTAG signal termination guidelines in Section 2.24, “JTAG Controller.”
4. SYSCLK is the primary clock input for the device. It must be ensured that SYSCLK is stable during $\overline{\text{HRESET}}$ assertion.

This table provides the PLL lock times.

**Table 6. PLL Lock Times**

| Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|
| PLL lock times | — | 100 | μs | — |

## 2.5 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

**Table 7. Power Supply Ramp Rate**

| Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|
| Required ramp rate for all voltage supplies (including $OV_{DD}/OV_{DD2}$ $GV_{DD}/BV_{DD}/SV_{DD}/LV_{DD}/LV_{DD2}$, All $V_{DD}$ supplies, MVREF and all $AV_{DD}$ supplies.) | — | 36000 | Volts/s | 1, 2 |

**Note:**

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (e.g. exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

## 2.6 Power Characteristics

During deep sleep, the maximum power consumption of the device is expected to be below 300mW. This includes 260mW consumed by core as shown in the table below and ~40mW by I/Os on $GV_{DD}$, $OV_{DD2}$ and $LV_{DD2}$ power supplies.

This table hows the power dissipations of the VDD, VDDC, and SVDD supply for various operating platform clock frequencies versus the core and DDR clock frequencies.

**Table 8. P1013 Core Power Dissipation**

| Core Frequency (MHz) | Platform Frequency (MHz) | DDR Data Rate (MHz) | $V_{DD}$, $V_{DDC}$, $S_{VDD}$ (V) | Junction Temp (°C) | Power Mode | Power (W) | | | Total Core and Platform Power (W)[1] | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | VDD[12] | VDDC | SVDD[12] | | |
| 1067 | 533 | 667 | 1.0 | 65 | Typical | 1.89 | 0.57 | 0.19 | 2.65 | 2, 3 |
| | | | | 105 | Thermal | 2.80 | 0.84 | 0.19 | 3.83 | 5, 7 |
| | | | | | Maximum | 3.06 | 0.91 | 0.19 | 4.17 | 4, 6, 7 |
| | | | | 125 | Thermal | 3.34 | 1.00 | 0.20 | 4.53 | 5, 7 |
| | | | | | Maximum | 3.48 | 1.04 | 0.20 | 4.72 | 4, 6, 7 |
| | | | | 65 | Doze | 1.54 | 0.64 | 0.19 | 2.36 | 8, 11 |
| | | | | | Nap | 1.37 | 0.67 | 0.19 | 2.22 | 8, 11 |
| | | | | | Sleep | 1.18 | 0.63 | 0.08 | 1.89 | 8, 11 |
| | | | | 35 | Deep Sleep | 0.00 | 0.26 | 0.00 | 0.26 | 8, 9, 10 |

**Table 8. P1013 Core Power Dissipation (continued)**

| Core Frequency (MHz) | Platform Frequency (MHz) | DDR Data Rate (MHz) | $V_{DD}$, $V_{DDC}$, $S_{VDD}$ (V) | Junction Temp (°C) | Power Mode | Power (W) | | | Total Core and Platform Power (W)[1] | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | VDD[12] | VDDC | SVDD[12] | | |
| 800 | 400 | 667 | 1.0 | 65 | Typical | 1.66 | 0.50 | 0.19 | 2.34 | 2, 3 |
| | | | | 105 | Thermal | 2.56 | 0.77 | 0.19 | 3.52 | 5, 7 |
| | | | | | Maximum | 2.62 | 0.78 | 0.19 | 3.60 | 4, 6, 7 |
| | | | | 125 | Thermal | 2.90 | 0.83 | 0.20 | 3.93 | 5, 7 |
| | | | | | Maximum | 2.99 | 0.89 | 0.20 | 4.08 | 4, 6, 7 |
| | | | | 65 | Doze | 1.44 | 0.58 | 0.19 | 2.21 | 8, 11 |
| | | | | | Nap | 1.33 | 0.61 | 0.19 | 2.13 | 8, 11 |
| | | | | | Sleep | 1.16 | 0.56 | 0.08 | 1.80 | 8, 11 |
| | | | | 35 | Deep Sleep | 0.00 | 0.26 | 0.00 | 0.26 | 8, 9, 10 |
| 600 | 400 | 667 | 1.0 | 65 | Typical | 1.54 | 0.46 | 0.19 | 2.19 | 2, 3 |
| | | | | 105 | Thermal | 2.45 | 0.73 | 0.19 | 3.37 | 5, 7 |
| | | | | | Maximum | 2.66 | 0.80 | 0.19 | 3.65 | 4, 6, 7 |
| | | | | 125 | Thermal | 2.84 | 0.83 | 0.20 | 3.87 | 5, 7 |
| | | | | | Maximum | 2.933 | 0.89 | 0.20 | 4.02 | 4, 6, 7 |
| | | | | 65 | Doze | 1.37 | 0.55 | 0.19 | 2.10 | 8, 11 |
| | | | | | Nap | 1.28 | 0.57 | 0.19 | 2.03 | 8, 11 |
| | | | | | Sleep | 1.16 | 0.54 | 0.08 | 1.78 | 8, 11 |
| | | | | 35 | Deep Sleep | 0.00 | 0.26 | 0.00 | 0.26 | 8, 9, 10 |

**Note:**

1. Combined power of VDDC, VDD and SVDDx with DDR Controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform with 90% activity factor.
3. Typical power is based on nominal processed device.
4. Maximum power assumes Multicore Dhrystone activity factor at 100% and executing DMA on the platform at 100% activity factor.
5. Thermal power assumes Multicore Dhrystone activity factor of 80% and executing DMA on the platform with 90% activity factor.
6. Maximum power is provided for power supply design sizing.
7. Thermal and Maximum power are based on worst case processed device.
8. All low power mode numbers are based on worst case processed device.
9. Deep Sleep power is the maximum number measured with USB1, eTSEC1 and DDR blocks enabled. It is characterized at $105^0$C.
10. Deep Sleep power is measured with DDR PLL disabled using DSCR[DDR_pll_disable].
11. These values specify the power consumption at nominal voltage and are meant for reference only.
12. VDD and SVDD are switchable core supplies.

## 2.6.1 I/O DC Power Supply Recommendation

This table provides estimated I/O power numbers for each block: DDR, PCI Express, eLBC, eTSEC, SGMII, eSDHC, USB, eSPI, DUART, $I^2C$, DIU, SSI, SATA, and GPIO.

**Table 9. I/O Power Supply Estimated Values**

| Interface | Parameter | Symbol | Typical[1] | Maximum[7] | Deep Sleep | Unit | Note |
|---|---|---|---|---|---|---|---|
| DDR2 | 400MHz data rate | $GV_{DD}$ (1.8 V) | 0.700 | 1.000 | — | W | 2, 6 |
| DDR3 | 600 MHz data rate | $GV_{DD}$ (1.5 V) | 0.600 | 1.050 | 0.003 | W | 2, 6, 8 |
| | 667 MHz data rate | $GV_{DD}$ (1.5 V) | 0.700 | 1.100 | 0.003 | W | 2, 6, 8 |
| PCI Express | ×1, 2.5 G-baud | $XV_{DD}$ (1.0 V) | 0.020 | 0.020 | — | W | — |
| | ×2, 2.5 G-baud | $XV_{DD}$ (1.0 V) | 0.037 | 0.037 | — | W | — |
| | ×4, 2.5 G-baud | $XV_{DD}$ (1.0 V) | 0.075 | 0.075 | — | W | — |
| SGMII | ×1, 1.25G-baud | $XV_{DD}$ (1.0 V) | 0.014 | 0.014 | — | W | — |
| SATA | 3.0G-baud | $XV_{DD2}$ (1.0 V) | 0.022 | 0.022 | — | W | — |
| eLBC | 32-bit, 83MHz | $BV_{DD}$ (1.8 V) | 0.040 | 0.100 | — | W | 3 |
| | | $BV_{DD}$ (2.5 V) | 0.060 | 0.160 | — | W | 3 |
| | | $BV_{DD}$ (3.3 V) | 0.100 | 0.230 | — | W | 3 |
| eLBC | 16-bit, 83MHz | $BV_{DD}$ (1.8 V) | 0.017 | 0.025 | — | W | 3 |
| | | $BV_{DD}$ (2.5 V) | 0.030 | 0.038 | — | W | 3 |
| | | $BV_{DD}$ (3.3 V) | 0.047 | 0.063 | — | W | 3 |
| eTSEC1 | RGMII | $LV_{DD2}$ (2.5 V) | 0.075 | 0.100 | 0.015 | W | 3 |
| | | $LV_{DD2}$ (3.3 V) | 0.124 | 0.150 | — | W | 3 |
| eTSEC2 | RGMII | $LV_{DD}$ (2.5 V) | 0.075 | 0.100 | — | W | 3 |
| | | $LV_{DD}$ (3.3 V) | 0.124 | 0.150 | — | W | 3 |
| eSDHC | — | $O/BV_{DD}$ (3.3 V) | 0.014 | 0.018 | — | W | 3 |
| USB1 | — | $LV_{DD2}$ (3.3 V) | 0.012 | 0.015 | — | W | 3 |
| | | $LV_{DD2}$ (2.5 V) | 0.008 | 0.010 | 0.005 | W | 3 |
| USB2 | — | $LV_{DD}$ (3.3 V) | 0.012 | 0.015 | — | W | 3 |
| | | $LV_{DD}$ (2.5 V) | 0.008 | 0.010 | — | W | 3 |
| eSPI | — | $BV_{DD}$ (1.8 V) | 0.004 | 0.005 | — | W | 3 |
| | | $BV_{DD}$ (2.5 V) | 0.006 | 0.008 | — | W | 3 |
| | | $BV_{DD}$ (3.3 V) | 0.010 | 0.013 | — | W | 3 |
| DIU | — | $BV_{DD}$ (3.3 V) | 0.180 | 0.225 | — | W | 3 |
| $I^2C$ | — | $OV_{DD}$ (3.3 V) | 0.002 | 0.003 | — | W | 3 |
| DUART | — | $OV_{DD}$ (3.3 V) | 0.006 | 0.008 | — | W | 3 |
| SSI | — | $OV_{DD}$ (3.3 V) | 0.005 | 0.006 | — | W | 3 |
| TDM | — | $OV_{DD}$ (3.3 V) | 0.004 | 0.005 | — | W | 3 |

**Table 9. I/O Power Supply Estimated Values (continued)**

| Interface | Parameter | Symbol | Typical[1] | Maximum[7] | Deep Sleep | Unit | Note |
|---|---|---|---|---|---|---|---|
| IEEE1588 | — | $LV_{DD}$ (2.5 V) | 0.004 | 0.005 | — | W | 3 |
| | | $LV_{DD}$ (3.3 V) | 0.007 | 0.009 | — | W | 3 |
| GPIO | x8 | 3.3 V | 0.009 | 0.011 | — | W | 3, 5 |
| | x8 | 2.5 V | 0.007 | 0.009 | — | W | 3, 5 |
| | x8 | 1.8 V | 0.005 | 0.006 | — | W | 3, 5 |
| Others (Reset, System Clock, JTAG and Misc) | — | $OV_{DD2}$ (3.3 V) | 0.030 | 0.036 | 0.015 | W | 3, 5 |

**Note:**

1. Typical values are estimates based on simulations at 65°C
2. Typical DDR power numbers are based on 1Rank DIMM with 40% utilization.
3. Assuming 15 pF total capacitance load per pin.
4. GPIOs are supported on $OV_{DD2}$, $OV_{DD}$, $LV_{DD}$, $LV_{DD2}$ and $BV_{DD}$ power rails.
5. Maximum DDR power numbers are based on 2 Rank DIMM with 75% utilization.
6. Maximum values are estimates based on simulations at 105 °C.
7. Assuming DDR I/Os tristated in deep sleep.

## 2.7 Input Clocks

This table provides the system clock (SYSCLK) and DDR clock (DDRCLK) DC specifications for the device.

**Table 10. SYSCLK/DDRCLK DC Electrical Characteristics ($OV_{DD2}$ = 3.3 V ± 165 mV)**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2.0 | — | — | V | 1 |
| Low-level input voltage | $V_{IL}$ | — | — | 0.8 | V | 1 |
| Input Capacitance | $C_{IN}$ | — | 7 | 15 | pf | — |
| Input current ($V_{IN}$= 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | — | ±50 | μA | 2 |

**Note:**

1. The max $V_{IH}$, and min $V_{IL}$ values can be found in Table 3.
2. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 3.

This table provides the system clock (SYSCLK) and DDR clock (DDRCLK) AC timing specifications for the device.

**Table 11. SYSCLK/DDRCLK AC Timing Specifications**

At recommended operating conditions (see Table 3) with $OV_{DD2}$ = 3.3 V ± 165 mV.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SYSCLK frequency | $f_{SYSCLK}$ | 66 | — | 133 | MHz | 1, 2 |
| SYSCLK cycle time | $t_{SYSCLK}$ | 7.5 | — | 15 | ns | 1, 2 |
| DDRCLK frequency | $f_{DDRCLK}$ | 66 | — | 133 | MHz | 1, 2 |
| DDRCLK cycle time | $t_{DDRCLK}$ | 7.5 | — | 15 | ns | 1, 2 |

**Table 11. SYSCLK/DDRCLK AC Timing Specifications (continued)**

At recommended operating conditions (see Table 3) with $OV_{DD2}$ = 3.3 V ± 165 mV.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SYSCLK/DDRCLK duty cycle | $t_{KHK}$/ $t_{SYSCLK/DDRCLK}$ | 40 | — | 60 | % | 2 |
| SYSCLK/DDRCLK slew rate | — | 1 | — | 4 | V/ns | 3 |
| SYSCLK/DDRCLK peak period jitter | — | — | — | ± 150 | ps | — |
| SYSCLK/DDRCLK jitter phase noise at – 56dBc | — | — | — | 500 | KHz | 4 |
| AC Input Swing Limits at 3.3 V $OV_{DD2}$ | $\Delta V_{AC}$ | 1.9 | — | — | V | — |

**Note:**

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK/DDRCLK frequency, do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD2}$/2.
3. Slew rate as measured from ±0.3 $\Delta V_{AC}$ at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

## 2.7.1 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 11 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet P1013's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and P1013 is compatible with spread spectrum sources if the recommendations listed in Table 11 are observed.

**Table 12. Spread Spectrum Clock Source Recommendations**

At recommended operating conditions (see Table 3) with $OV_{DD2}$ = 3.3 V ± 165 mV.

| Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|
| Frequency modulation | — | 60 | kHz | — |
| Frequency spread | — | 1.0 | % | 1, 2 |

**Note:**

1. SYSCLK frequencies resulting from frequency spreading, and the resulting core frequency, must meet the minimum and maximum specifications given in Table 11.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device

**CAUTION**

The processor's minimum and maximum SYSCLK/DDRCLK and core/DDR memory frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/DDR memory frequency should avoid violating the stated limits by using down-spreading only.

## 2.7.2 Real Time Clock Timing

The real time clock timing (RTC_CLK) input is sampled by the core complex bus clock (CCB_clk). The output of the sampling latch is then used as an input to the counters of the PIC and the time base unit of the e500; there is no need for jitter specification. The minimum pulse width of RTC_CLK should be greater than 16x of the CCB clock. That is minimum clock high time is $16 \times t_{CCB\_clk}$, and minimum clock low time is $16 \times t_{CCB\_clk}$. There is no minimum RTC_CLK frequency; RTC_CLK may be grounded if not needed. If used the edge rate for RTC_CLK should be within 10ns ± 2%.

## 2.7.3 eTSEC Gigabit Reference Clock Timing

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the device.

**Table 13. EC_GTX_CLK125 AC Timing Specifications**

At recommended operating conditions with LVDD = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| EC_GTX_CLK125 frequency | $t_{G125}$ | — | 125 | — | MHz | — |
| EC_GTX_CLK125 cycle time | $t_{G125}$ | — | 8 | — | ns | — |
| EC_GTX_CLK125 rise and fall time<br>$LV_{DD}$ = 2.5 V<br>$LV_{DD}$ = 3.3 V | $t_{G125R}/t_{G125F}$ | — | — | <br>0.75<br>1.0 | ns | 1 |
| EC_GTX_CLK125 duty cycle | $t_{G125H}/t_{G125L}$ | 47 | — | 53 | % | 2 |
| EC_GTX_CLK125 total jitter | — | — | — | ±150 | ps | 2 |

**Note:**

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for $LV_{DD}$ = 2.5 V, and from 0.6 and 2.7 V for $LV_{DD}$ = 3.3 V
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Table 34 for duty cycle for 10Base-T and 100Base-T reference clock.

## 2.7.4 Other Input Clocks

A description of the overall clocking of this device is available in the *P1022 QorIQ Integrated Processor Reference Manual* in the form of a Clock Subsystem Block Diagram. For information on the input clock requirements of functional blocks sourced external of the device, such as SerDes, Ethernet Management, eSDHC, enhanced Local Bus, see the specific interface section.

# 2.8 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the device. Note that the required $GV_{DD}$(typ) voltage is 1.8V or 1.5V when interfacing to DDR2 or DDR3 SDRAM respectively.

## 2.8.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM Controller of the device when interfacing to DDR2 SDRAM.

**Table 14. DDR2 SDRAM Interface DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V[1]**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| I/O reference voltage | MVREFn | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V | 2, 3, 4 |

**Table 14. DDR2 SDRAM Interface DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V[1] (continued)**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | MVREFn + 0.125 | — | V | 5 |
| Input low voltage | $V_{IL}$ | — | MVREFn – 0.125 | V | 5 |
| I/O leakage current | $I_{OZ}$ | –50 | 50 | μA | 8 |
| Output high current ($V_{OUT}$ = 1.370 V) | $I_{OH}$ | — | –13.4 | mA | 6, 7 |
| Output low current ($V_{OUT}$ = 0.330 V) | $I_{OL}$ | 13.4 | — | mA | 6, 7 |

**Note:**

1. $GV_{DD}$ is expected to be within 50 mV of the DRAM's voltage supply at all times.The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREFn is expected to be equal to 0.5 × $GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MVREFn may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREFn *with min value of* MVREFn – 0.04, and max value of MVREFn + 0.04. This rail should track variations in the DC level of MVREFn.
4. The voltage regulator for MVREFn must meet the specifications stated in Table 17.
5. Input capacitance load for DQ, DQS and $\overline{DQS}$ are available in the IBIS models,
6. IOH and IOL are measured at GVDD = 1.7 V
7. Refer to the IBIS model for the complete output IV curve characteristics.
8. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$

This table provides the recommended operating conditions for the DDR SDRAM Controller of the device when interfacing to DDR3 SDRAM.

**Table 15. DDR3 SDRAM Interface DC Electrical Characteristics for $GV_{DD}$(typ) = 1.5 V[1]**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| I/O reference voltage | MVREFn | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 2, 3, 4 |
| Input high voltage | $V_{IH}$ | MVREFn + 0.100 | $GV_{DD}$ | V | 5 |
| Input low voltage | $V_{IL}$ | GND | MVREFn – 0.100 | V | 5 |
| I/O leakage current | $I_{OZ}$ | –50 | 50 | μA | 6 |

**Note:**

1. $GV_{DD}$ is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREFn is expected to be equal to 0.5 × $GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MVREFn may not exceed ±1% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREFn *with min value of* MVREFn – 0.04, and max value of MVREFn + 0.04. This rail should track variations in the DC level of MVREFn.
4. The voltage regulator for MVREFn must meet the specifications stated in Table 17.
5. Input capacitance load for DQ, DQS and $\overline{DQS}$ are available in the IBIS models
6. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$.

This table provides the DDR Controller interface capacitance for DDR2 and DDR3.

**Table 16. DDR2/DDR3 SDRAM Capacitance for $GV_{DD}$(typ) = 1.8 V and 1.5 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{IO}$ | 6 | 8 | pF | 1, 2 |
| Delta input/output capacitance: DQ, DQS, $\overline{DQS}$ | $C_{DIO}$ | — | 0.5 | pF | 1, 2 |

**Note:**
1. This parameter is sampled. $GV_{DD}$ = 1.8 V ± 0.1 V (for DDR2), f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.2 V.
2. This parameter is sampled. $GV_{DD}$ = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = $GV_{DD}$/2, $V_{OUT}$ (peak-to-peak) = 0.150V.

This table provides the current draw characteristics for MVREFn.

**Table 17. Current Draw Characteristics for MVREFn**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Current draw for DDR2 SDRAM for MVREFn | MVREFn | — | 1500 | μA | — |
| Current draw for DDR3 SDRAM for MVREFn | MVREFn | — | 1250 | μA | |

## 2.8.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM Controller interface. The DDR controller supports both DDR2 and DDR3 memories.

## 2.8.3 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 SDRAM.

**Table 18. DDR2 SDRAM Interface Input AC Timing Specifications**

**At recommended operating conditions with GVDD of 1.8 V ± 5%**

| Parameter | | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| AC input low voltage | > 533 MHz data rate | $V_{ILAC}$ | — | MVREFn – 0.20 | V | — |
| | ≤ 533 MHz data rate | | — | MVREFn – 0.25 | | |
| AC input high voltage | > 533 MHz data rate | $V_{IHAC}$ | MVREFn + 0.20 | — | V | — |
| | ≤ 533 MHz data rate | | MVREFn + 0.25 | — | | |

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

**Table 19. DDR3 SDRAM Interface Input AC Timing Specifications**

**At recommended operating conditions with GVDD of 1.5 V ± 5%**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| AC input low voltage | $V_{ILAC}$ | — | MVREFn – 0.175 | V | — |
| AC input high voltage | $V_{IHAC}$ | MVREFn + 0.175 | — | V | — |

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

**Table 20. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Controller Skew for MDQS—MDQ/MECC | $t_{CISKEW}$ | — | — | ps | 1 |
| 667 MHz data rate | | –390 | 390 | — | — |
| Tolerated Skew for MDQS—MDQ/MECC | $t_{DISKEW}$ | — | — | ps | 2 |
| 667 MHz data rate | | –360 | 360 | — | — |

**Note:**

1. $t_{CISKEW}$ represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called tDISKEW.This can be determined by the following equation: tDISKEW = ±(T/4 – abs(tCISKEW)) where T is the clock period and abs(tCISKEW) is the absolute value of tCISKEW.

This figure shows the DDR2 and DDR3 SDRAM interface input timing diagram.

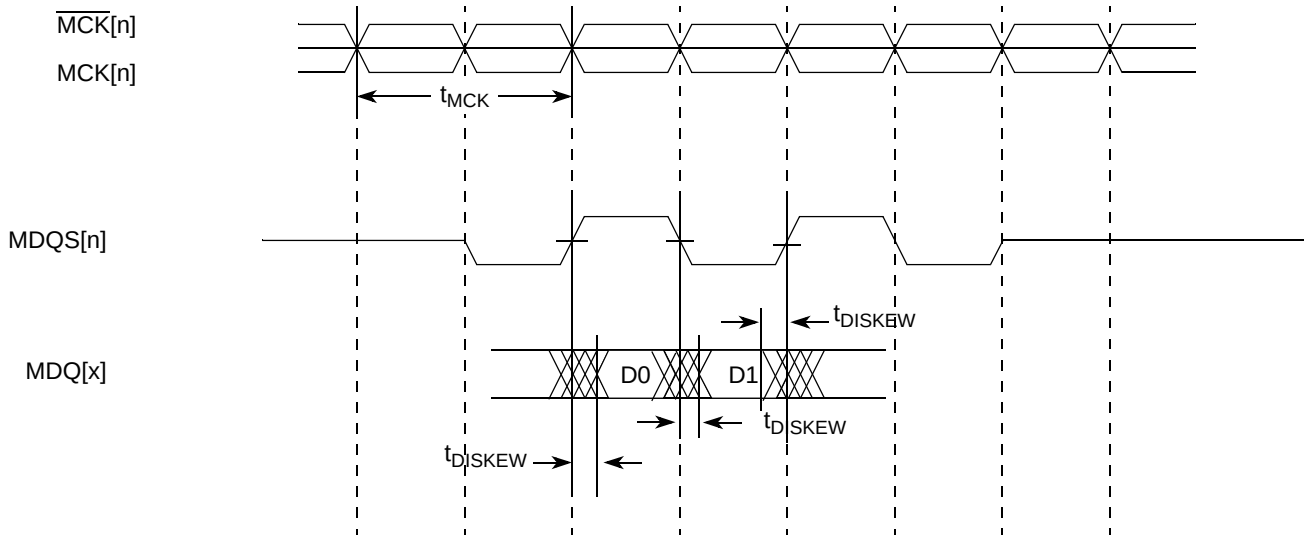



**Figure 8. DDR SDRAM Interface Input Timing Diagram**

## 2.8.4 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

This table contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

**Table 21. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

| Parameter | Symbol [1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| MCK[n] cycle time | $t_{MCK}$ | 3 | 5 | ns | 2 |
| ADDR/CMD output setup with respect to MCK<br>667 MHz data rate | $t_{DDKHAS}$ | <br>0.95 | <br>— | ns | 3 |
| ADDR/CMD output hold with respect to MCK<br>667 MHz data rate | $t_{DDKHAX}$ | <br>0.95 | <br>— | ns | 3 |
| $\overline{MCS}$[n] output setup with respect to MCK<br>667 MHz data rate | $t_{DDKHCS}$ | <br>0.95 | <br>— | ns | 3 |
| $\overline{MCS}$[n] output hold with respect to MCK<br>667 MHz data rate | $t_{DDKHCX}$ | <br>0.95 | <br>— | ns | 3 |
| MCK to MDQS Skew<br>667 MHz data rate | $t_{DDKHMH}$ | <br>–0.6 | <br>0.6 | ns | 4 |
| MDQ/MECC/MDM output setup with respect to MDQS<br>667 MHz data rate | $t_{DDKHDS}$, $t_{DDKLDS}$ | <br>325 | <br>— | ps | 5 |
| MDQ/MECC/MDM output hold with respect to MDQS<br>667 MHz data rate | $t_{DDKHDX}$, $t_{DDKLDX}$ | <br>325 | <br>— | ps | 5 |
| MDQS preamble | $t_{DDKHMP}$ | $0.9 \times t_{MCK}$ | — | ns | |
| MDQS postamble | $t_{DDKHME}$ | $0.4 \times t_{MCK}$ | $0.6 \times t_{MCK}$ | ns | |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This will typically be set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *P1022 QorIQ Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

**NOTE**

For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

This figure shows the DDR2 and DDR3 SDRAM Interface output timing for the MCK to MDQS skew measurement ($t_{DDKHMH}$).

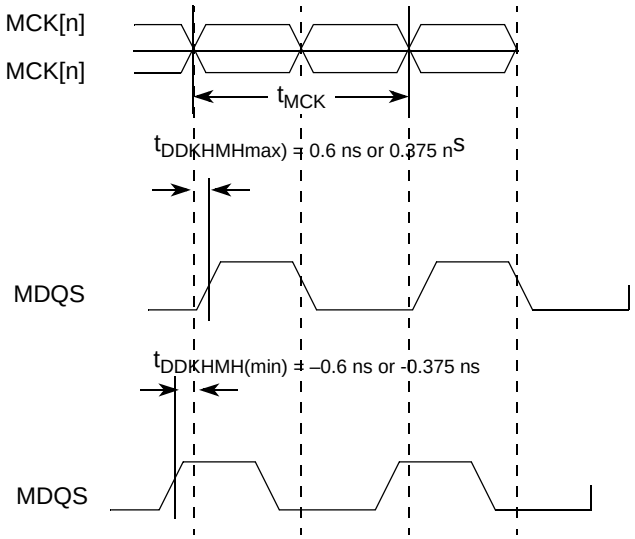



**Figure 9. Timing Diagram for $t_{DDKHMH}$**

This figure shows the DDR2 and DDR3 SDRAM output timing diagram.

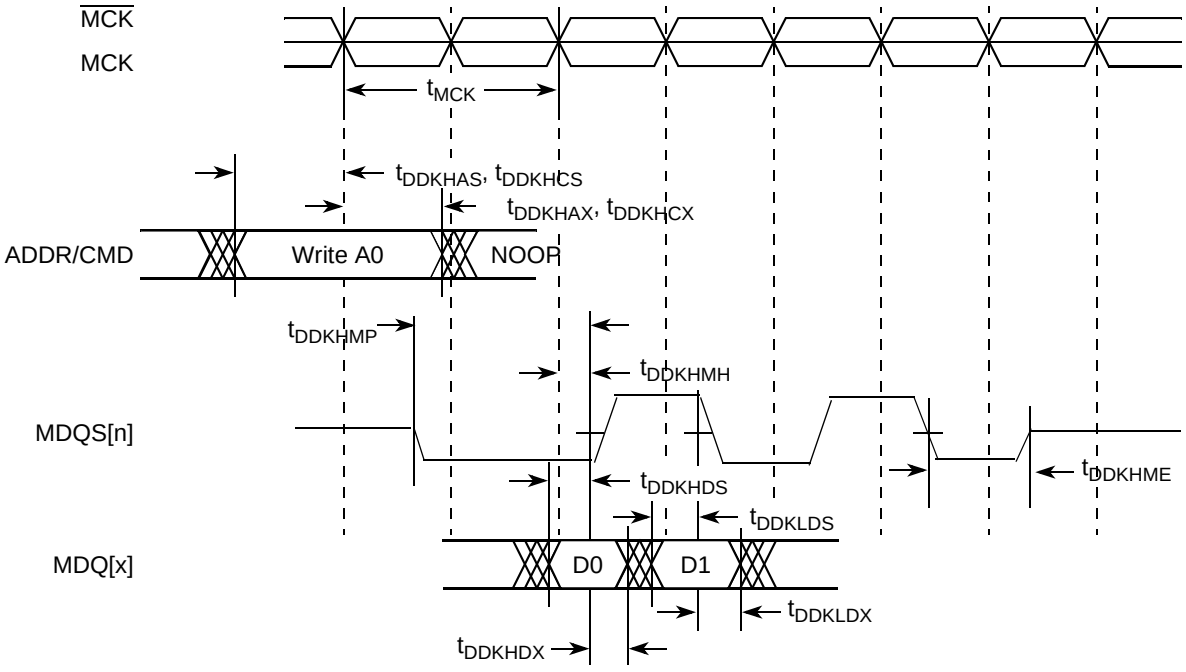



**Figure 10. DDR2 and DDR3 SDRAM Output Timing Diagram**

This figure provides the AC test load for the DDR2 and DDR3 Controller bus.

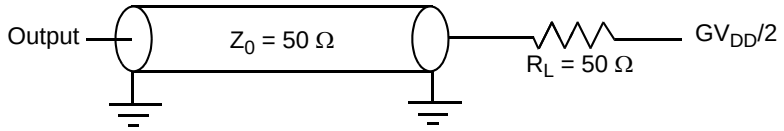



**Figure 11. DDR2 and DDR3 Controller bus AC Test Load**

## 2.8.5 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential electrical specifications for the DDR2 and DDR3SDRAM controller interface of the device.

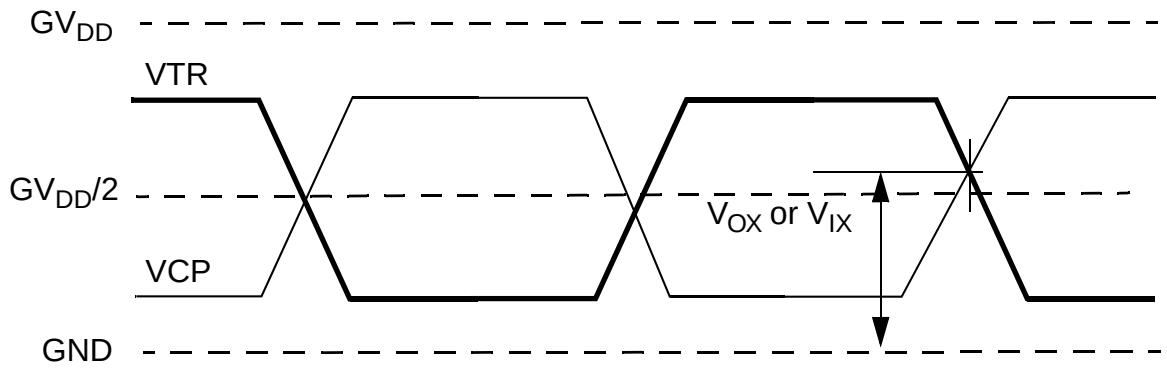



**Figure 12. DDR2 and DDR3 SDRAM Differential Timing Specifications**

### NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

This table provides the differential specifications for P1013 differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$ in DDR2 mode.

**Table 22. DDR2 SDRAM Differential Electrical Characteristics**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input AC Differential Cross-point Voltage | $V_{IXAC}$ | $0.5 \times GV_{DD} - 0.175$ | $0.5 \times GV_{DD} + 0.175$ | V | 1 |
| Output AC Differential Cross-point Voltage | $V_{OXAC}$ | $0.5 \times GV_{DD} - 0.125$ | $0.5 \times GV_{DD} - 0.125$ | V | 1 |

**Note:**

1. I/O drivers are calibrated before making measurements.

This table provides the differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$ in DDR3 mode.

**Table 23. DDR3 SDRAM Differential Electrical Characteristics**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input AC Differential Cross-point Voltage | $V_{IXAC}$ | $0.5 \times GV_{DD} - 0.150$ | $0.5 \times GV_{DD} + 0.150$ | V | 1 |
| Output AC Differential Cross-point Voltage | $V_{OXAC}$ | $0.5 \times GV_{DD} - 0.115$ | $0.5 \times GV_{DD} - 0.115$ | V | 1 |

**Table 23. DDR3 SDRAM Differential Electrical Characteristics (continued)**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|

**Note:**
1. I/O drivers are calibrated before making measurements.

## 2.9 eSPI

This section describes the DC and AC electrical specifications for the eSPI of the device.

### 2.9.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at 3.3 V.

**Table 24. eSPI DC Electrical Characteristics (3.3 V)**

| Characteristic | Symbol | Condition | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.0 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | — | 0.8 | V | 1 |
| Input current | $I_{IN}$ | $V_{IN}$ = 0V or $V_{IN}$ = $BV_{DD}$ | – | ±40 | μA | 2 |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –2.0 mA | 2.4 | — | V | — |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 2.0 mA | — | 0.4 | V | — |

**Note:**
1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $BV_{DD}$ values found in Table 2.
2. The symbol $V_{IN}$, represents $BV_{DD}$ referenced in Table 2.

This table provides the DC electrical characteristics for the eSPI interface operating at 2.5 V.

**Table 25. eSPI DC Electrical Characteristics (2.5 V)**

| Characteristic | Symbol | Condition | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 1.7 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | — | 0.7 | V | 1 |
| Input current | $I_{IN}$ | $V_{IN}$ = 0V or $V_{IN}$ = $BV_{DD}$ | – | ±40 | μA | 2 |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –1.0 mA | 2.0 | — | V | — |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.0 mA | — | 0.4 | V | — |

**Note:**
1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $BV_{DD}$ values found in Table 2.
2. The symbol $V_{IN}$, represents $BV_{DD}$ referenced in Table 2.

This table provides the DC electrical characteristics for the eSPI interface operating at 1.8 V.

**Table 26. eSPI DC Electrical Characteristics (1.8 V)**

| Characteristic | Symbol | Condition | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 1.25 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | — | 0.6 | V | 1 |

**Table 26. eSPI DC Electrical Characteristics (1.8 V) (continued)**

| Characteristic | Symbol | Condition | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Input current | $I_{IN}$ | $V_{IN}$ = 0V or $V_{IN}$ = $BV_{DD}$ | – | ±40 | μA | 2 |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –0.5 mA | 1.35 | — | V | — |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 0.5 mA | — | 0.4 | V | — |

**Note:**

1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $BV_{DD}$ values found in Table 2.
2. The symbol $V_{IN}$, represents $BV_{DD}$ referenced in Table 2.

## 2.9.2 eSPI AC Timing Specifications

This table and provide the eSPI input and output AC timing specifications.

**Table 27. eSPI AC Timing Specifications[1]**

| Characteristic | Symbol [2] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| SPI_MOSI output—Master data (internal clock) hold time | $t_{NIKHOX}$ | 0.5+($t_{PLATFORM\_CLK}$ *SPMODE[HO_ADJ]) | — | ns | 1, 3 |
| SPI_MOSI output—Master data (internal clock) delay | $t_{NIKHOV}$ | — | 5.5+($t_{PLATFORM\_CLK}$ *SPMODE[HO_ADJ]) | ns | 1, 3 |
| SPI_CS outputs—Master data (internal clock) hold time | $t_{NIKHOX2}$ | 0 | — | ns | 1 |
| SPI_CS outputs—Master data (internal clock) delay | $t_{NIKHOV2}$ | — | 5.5 | ns | 1 |
| SPI inputs—Master data (internal clock) input setup time | $t_{NIIVKH}$ | 5 | — | ns | — |
| SPI inputs—Master data (internal clock) input hold time | $t_{NIIXKH}$ | 0 | — | ns | — |

**Note:**

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{NIKHOV}$ symbolizes the NMSI outputs internal timing (NI) for the time $t_{SPI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
3. See *P1022 QorIQ Integrated Processor Reference Manual* for detail about the register SPMODE.

This figure provides the AC test load for the eSPI.

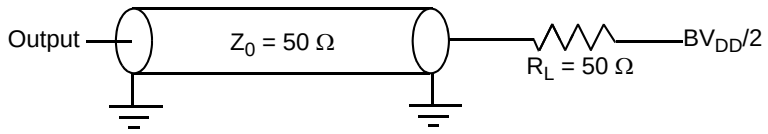
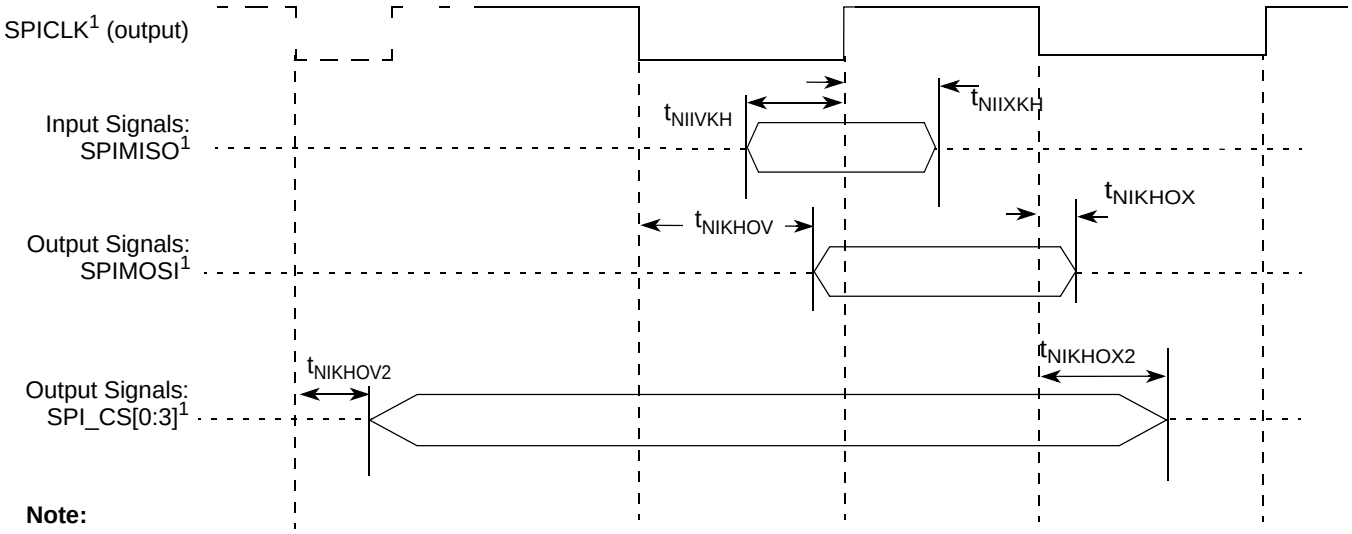



**Figure 13. eSPI AC Test Load**

This figure represents the AC timing from Table 27 in master mode (internal clock). (It apply when SPMODEx[CIx] = 0, SPMODEx[CPx] = 0.) Note that the clock edge is selectable on SPI.




**Note:**
1. SPICLK appears on the interface only after CS assertion.

**Figure 14. SPI AC Timing in Master Mode (Internal Clock) Diagram**

## 2.10 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the device.

### 2.10.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

**Table 28. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | — | V | 1 |
| Low-level input voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($OV_{IN}$ = 0 V or $OV_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**
1. The min $V_{IL}$and max $V_{IH}$ values are based on the min and max $OV_{IN}$ respective values found in Table 3.
2. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 3.

## 2.10.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

**Table 29. DUART AC Timing Specifications**

| Parameter | Value | Unit | Note |
|---|---|---|---|
| Minimum baud rate | $f_{CCB}$/1,048,576 | baud | 1 |
| Maximum baud rate | $f_{CCB}$/16 | baud | 1, 2 |
| Oversample rate | 16 | — | 3 |

**Note:**

1. $f_{CCB}$ refers to the internal platform clock.
2. Actual attainable baud rate will be limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8$^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16$^{th}$ sample.

# 2.11 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed Ethernet controller and the MII management interface.

## 2.11.1 RMII/RGMII DC Electrical Characteristics

All RMII/RGMII drivers and receivers comply with the DC parametric attributes specified in Table 30 and Table 31.

**Table 30. RMII DC Electrical Characteristics @ $LV_{DD}$ = 3.3 V**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Supply voltage, 3.3 V | $LV_{DD}$ | 3.13 | 3.47 | V | — |
| Output high voltage ($LV_{DD}$ = min, $I_{OH}$ = –4.0 mA) | $V_{OH}$ | 2.1 | $LV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}$ = min, $I_{OL}$ = 4.0 mA) | $V_{OL}$ | GND | 0.50 | V | — |
| Input high voltage RMII | $V_{IH}$ | 2.0 | — | V | — |
| Input low voltage | $V_{IL}$ | — | 0.90 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$) | $I_{IH}$ | — | 40 | μA | 1 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –600 | — | μA | 1 |

**Note:**

1. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbols referenced iin Table 2 and Table 3.

**Table 31. RMII/RGMII DC Electrical Characteristics @ $LV_{DD}$ = 2.5 V**

| Parameters | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Supply voltage, 2.5 V | $LV_{DD}$ | 2.37 | 2.63 | V | 1 |
| Output high voltage ($LV_{DD}$ = min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.00 | $LV_{DD}$ + 0.3 | V | — |
| Output low voltage ($LV_{DD}$= min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | GND – 0.3 | 0.40 | V | — |
| Input high voltage | $V_{IH}$ | 1.70 | — | V | — |

**Table 31. RMII/RGMII DC Electrical Characteristics (continued)@ $LV_{DD}$ = 2.5 V**

| Parameters | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | — | 0.70 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$) | $I_{IH}$ | — | 10 | μA | — |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –15 | — | μA | 1 |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbols referenced in Table 2 and Table 3.

## 2.11.2 RMII/RGMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications and then the RGMII AC timing specifications

### 2.11.2.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in this table.

**Table 32. RMII Transmit AC Timing Specifications**

For recommended operating conditions, ses Table 3.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSEC*n*_TX_CLK clock period | $t_{RMT}$ | — | 20.0 | — | ns |
| TSEC*n*_TX_CLK duty cycle | $t_{RMTH}$ | 35 | — | 65 | % |
| TSEC*n*_TX_CLK peak-to-peak jitter | $t_{RMTJ}$ | — | — | 250 | ps |
| Rise time TSEC*n*_TX_CLK (20%–80%) | $t_{RMTR}$ | 1.0 | — | 5.0 | ns |
| Fall time TSEC*n*_TX_CLK (80%–20%) | $t_{RMTF}$ | 1.0 | — | 5.0 | ns |
| TSEC*n*_TX_CLK to RMII data TXD[1:0], TX_EN delay | $t_{RMTDX}$ | 2.0 | — | 10.0 | ns |

This figure shows the RMII transmit AC timing diagram.

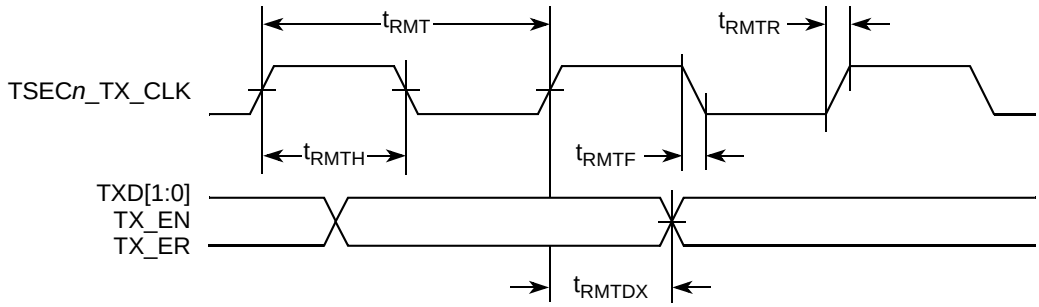



**Figure 15. RMII Transmit AC Timing Diagram**

### 2.11.2.2 RMII Receive AC Timing Specifications

This table lists the RMII receive AC timing specifications. In RMII mode the reference clock should be fed to TSEC*n*_TX_CLK. The reference clock is used for both transmit and receive.

**Table 33. RMII Receive AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TSEC*n*_TX_CLK clock period | $t_{RMR}$ | — | 20.0 | — | ns |
| TSEC*n*_TX_CLK duty cycle | $t_{RMRH}$ | 35 | — | 65 | % |
| TSEC*n*_TX_CLK peak-to-peak jitter | $t_{RMRJ}$ | — | — | 250 | ps |
| Rise time TSEC*n*_TX_CLK (20%–80%) | $t_{RMRR}$ | 1.0 | — | 5.0 | ns |
| Fall time TSEC*n*_TX_CLK (80%–20%) | $t_{RMRF}$ | 1.0 | — | 5.0 | ns |
| RXD[1:0], CRS_DV, RX_ER setup time to TSEC*n*_TX_CLK rising edge | $t_{RMRDV}$ | 4.0 | — | — | ns |
| RXD[1:0], CRS_DV, RX_ER hold time to TSEC*n*_TX_CLK rising edge | $t_{RMRDX}$ | 2.0 | — | — | ns |

This figure provides the AC test load for eTSEC.

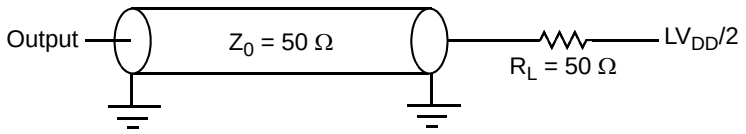



**Figure 16. eTSEC AC Test Load**

This figure shows the RMII receive AC timing diagram.

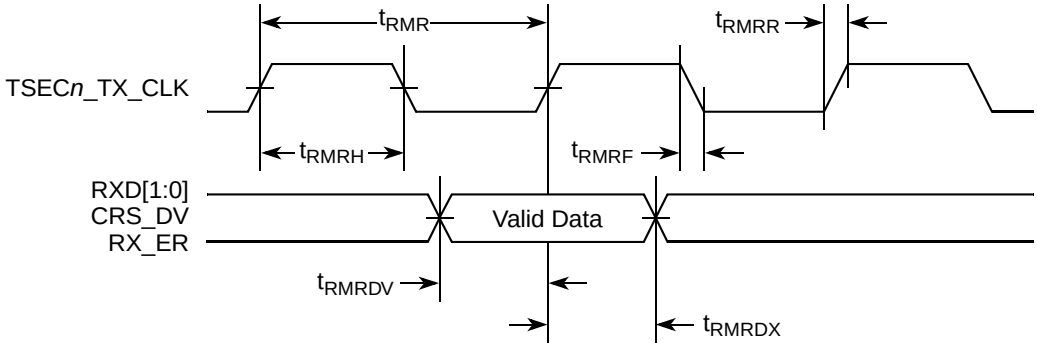



**Figure 17. RMII Receive AC Timing Diagram**

### 2.11.2.3 RGMII AC Timing Specifications

This table presents the RGMII AC timing specifications.

**Table 34. RGMII AC Timing Specification**

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT\_TX}$ | –500 | 0 | 500 | ps | 5 |
| Data to clock input skew (at receiver) | $t_{SKRGT\_RX}$ | 1.0 | — | 2.8 | ns | 2 |
| Clock period duration | $t_{RGT}$ | 7.2 | 8.0 | 8.8 | ns | 3 |

**Table 34. RGMII AC Timing Specification (continued)**

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Duty cycle for 10BASE-T and 100BASE-TX | $t_{RGTH}/t_{RGT}$ | 40 | 50 | 60 | % | 3, 4 |
| Duty cycle for Gigabit | $t_{RGTH}/t_{RGT}$ | 45 | 50 | 55 | % | — |
| Rise time (20%–80%) | $t_{RGTR}$ | — | — | 0.75 | ns | — |
| Fall time (20%–80%) | $t_{RGTF}$ | — | — | 0.75 | ns | — |

**Note:**

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. For example, the subscript of $t_{RGT}$ represents the receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of GTX_CLK125 by more than 300 ppm.

This figure shows the RGMII AC timing and multiplexing diagrams.

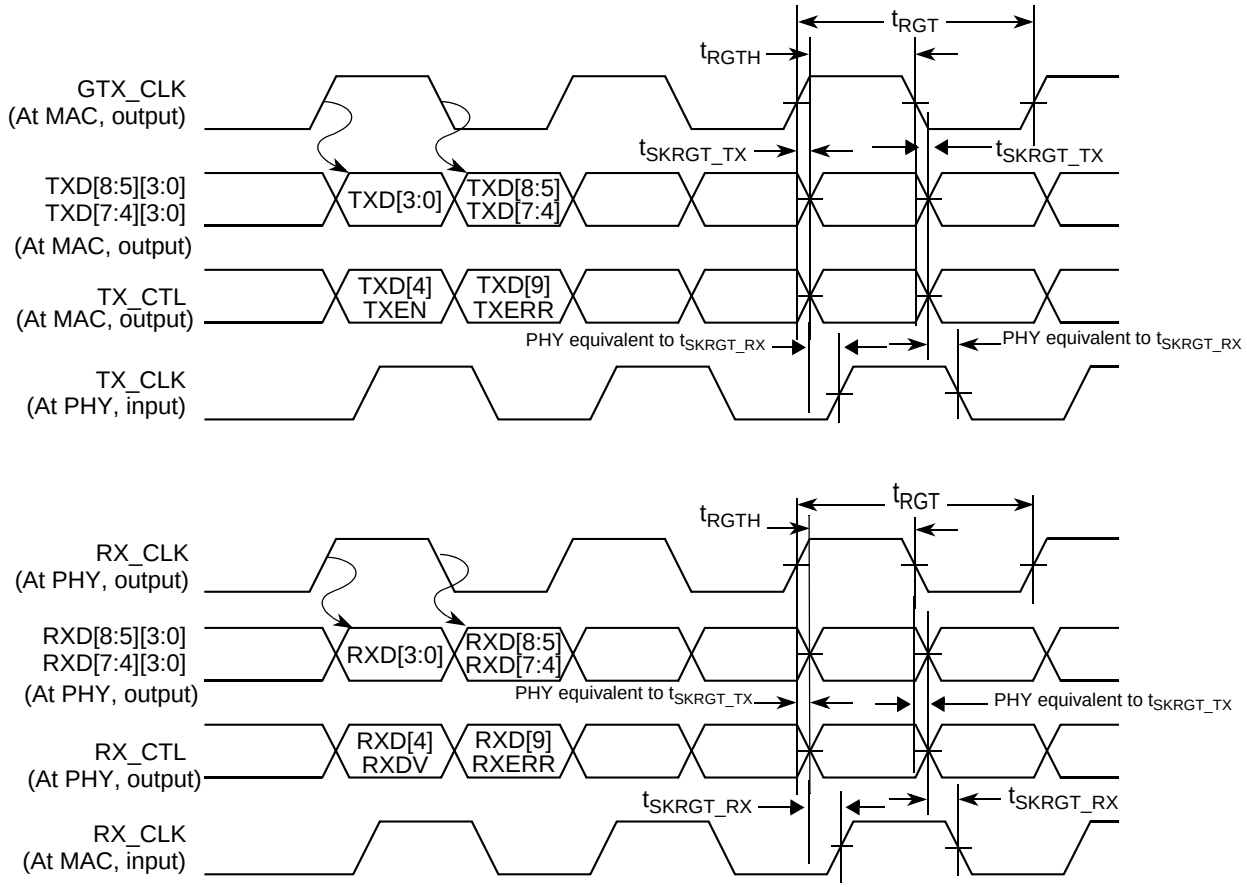



**Figure 18. RGMII AC Timing and Multiplexing Diagrams**

**WARNING**

Freescale guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

## 2.11.3 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

**Table 35. MII Management DC Electrical Characteristics ($LV_{DD}$= 3.3V)**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2.0 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.90 | V | 1 |
| Input high current ($LV_{DD}$ = Max, $V_{IN}$ = 2.1 V) | $I_{IH}$ | — | 40 | μA | 2 |
| Input low current ($LV_{DD}$ = Max, $V_{IN}$ = 0.5 V) | $I_{IL}$ | –600 | — | μA | — |
| Output high voltage ($LV_{DD}$ = Min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.10 | — | V | — |
| Output low voltage ($LV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | — | 0.50 | V | — |

**Note:**
1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $LV_{IN}$ values found in Table 3.
2. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 2.

The MDC and MDIO are defined to operate at a supply voltage of 2.5 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

**Table 36. MII Management DC Electrical Characteristics ($LV_{DD}$ = 2.5V)**

| Parameters | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 1.70 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.70 | V | 1 |
| Input high current ($V_{IN}$ = $LV_{DD}$,) | $I_{IH}$ | — | 10 | μA | 2 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –15 | — | μA | — |
| Output high voltage ($LV_{DD}$ = Min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.00 | — | V | — |
| Output low voltage ($LV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | — | 0.40 | V | — |

**Note:**
1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $LV_{IN}$ values found in Table 3.
2. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 2.

## 2.11.4 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

**Table 37. MII Management AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ is 3.3 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| MDC frequency | $f_{MDC}$ | — | 2.5 | — | MHz | 2 |

**Table 37. MII Management AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}$ is 3.3 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| MDC period | $t_{MDC}$ | — | 400 | — | ns | — |
| MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| MDC to MDIO delay | $t_{MDKHDX}$ | $(16 \times t_{plb\_clk}) - 3$ | — | $(16 \times t_{plb\_clk}) + 3$ | ns | 3, 4 |
| MDIO to MDC setup time | $t_{MDDVKH}$ | 6 | — | — | ns | — |
| MDIO to MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |
| MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | — |
| MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | — |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns).
4. $t_{plb\_clk}$ is the platform (CCB) clock.

This figure shows the MII management interface timing diagram.

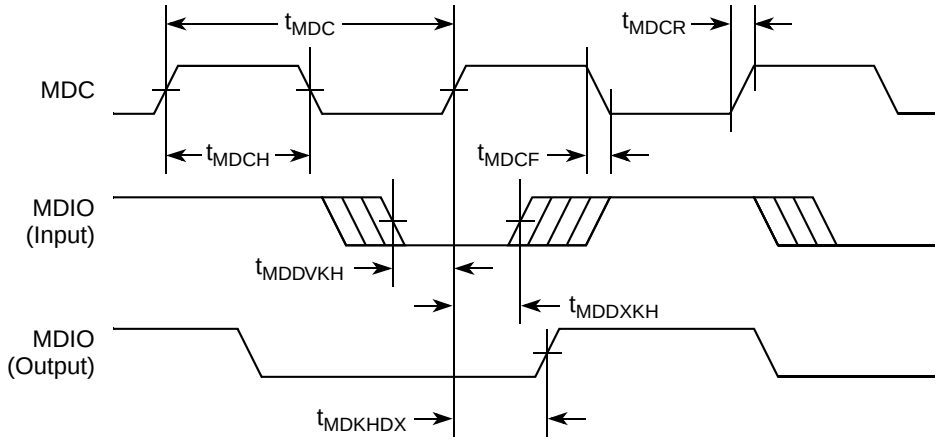
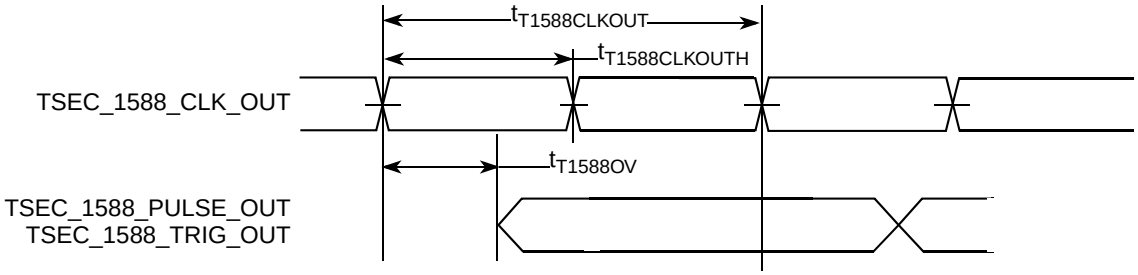



**Figure 19. MII Management Interface Timing Diagram**

## 2.11.5 eTSEC IEEE Std 1588™ Timing Specifications

Table 38 provides the IEEE 1588 AC timing specifications.

This figure shows the data and command output AC timing diagram.




**Note:** The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is noninverting. Otherwise, it is counted starting at the falling edge.

**Figure 20. eTSEC IEEE 1588 Output AC Timing**

This figure shows the data and command input AC timing diagram.

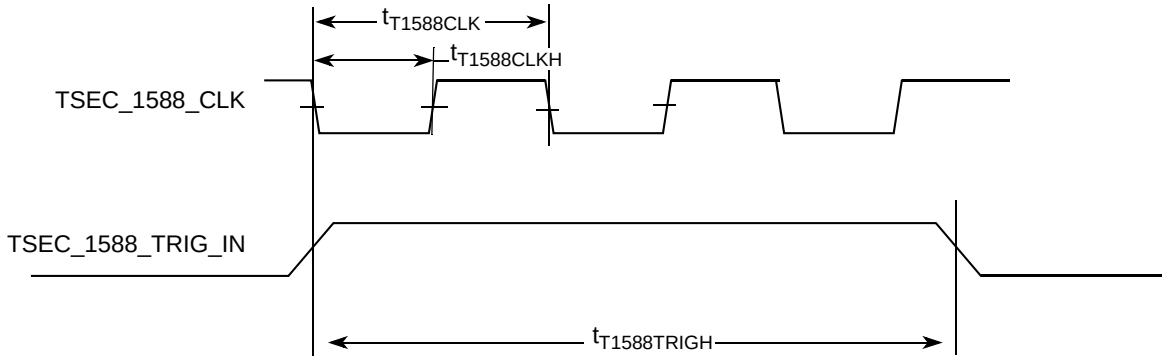



**Figure 21. eTSEC IEEE 1588 Input AC Timing**

### 2.11.5.1 eTSEC IEEE Std 1588 AC Electrical Characteristics

This table provides the IEEE 1588 AC timing specifications.

**Table 38. eTSEC IEEE 1588 AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TSEC_1588_CLK clock period | $t_{T1588CLK}$ | 3.3 | — | $T_{RX\_CLK} \times 7$ | ns | 1, 2, 3, 4 |
| TSEC_1588_CLK duty cycle | $t_{T1588CLKH}/t_{T1588CLK}$ | 40 | 50 | 60 | % | — |
| TSEC_1588_CLK peak-to-peak jitter | $t_{T1588CLKINJ}$ | — | — | 250 | ps | — |
| Rise time eTSEC_1588_CLK (20%–80%) | $t_{T1588CLKINR}$ | 1.0 | — | 2.0 | ns | — |
| Fall time eTSEC_1588_CLK (80%–20%) | $t_{T1588CLKINF}$ | 1.0 | — | 2.0 | ns | — |
| TSEC_1588_CLK_OUT clock period | $t_{T1588CLKOUT}$ | $2 \times t_{T1588CLK}$ | — | — | ns | — |
| TSEC_1588_CLK_OUT duty cycle | $t_{T1588CLKOTH}/t_{T1588CLKOUT}$ | 30 | 50 | 70 | % | — |

**Table 38. eTSEC IEEE 1588 AC Timing Specifications (continued)**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TSEC_1588_PULSE_OUT | $t_{T1588OV}$ | 0.5 | — | 3.0 | ns | — |
| TSEC_1588_TRIG_IN pulse width | $t_{T1588TRIGH}$ | $2 \times t_{T1588CLK\_MAX}$ | — | — | ns | 2 |

**Note:**

1. $T_{RX\_CLK}$ is the maximum clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *P1022 QorIQ Integrated Processor Reference Manual,* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *P1022 QorIQ Integrated Processor Reference Manual,* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of $T_{RX\_CLK}$, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns, respectively.
4. It needs to be greater than half of the platform (CCB) clock period. This places a higher minimum value of the $t_{T1588CLK}$ when operating at higher platform frequencies.

## 2.11.5.2 eTSEC IEEE Std 1588 DC Electrical Characteristics

This table shows eTSEC IEEE Std 1588 DC electrical characteristics when operating at $LV_{DD}$ = 3.3 V supply.

**Table 39. eTSEC IEEE 1588 DC Electrical Characteristics ($LV_{DD}$ = 3.3 V)**

For recommended operating conditions with $LV_{DD}$ = 3.3 V.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2.0 | — | V | 2 |
| Input low voltage | $V_{IL}$ | — | 0.9 | V | 2 |
| Input high current ($LV_{DD}$ = Max, $V_{IN}$ = 2.1 V) | $I_{IH}$ | — | 40 | μA | 1 |
| Input low current ($LV_{DD}$ = Max, $V_{IN}$ = 0.5 V) | $I_{IL}$ | –600 | — | μA | 1 |
| Output high voltage ($LV_{DD}$ = Min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Output low voltage ($LV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**

1. Note that the symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 2 and Table 3.
2. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective $LV_{IN}$ values found in Table 3.

This table shows the IEEE 1588 DC electrical characteristics when operating at $LV_{DD}$ = 2.5 V supply.

**Table 40. eTSEC IEEE 1588 DC Electrical Characteristics ($LV_{DD}$ = 2.5 V)**

**For recommended operating conditions with** $LV_{DD}$ = 2.5 V

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 1.70 | — | V | — |
| Input low voltage | $V_{IL}$ | — | 0.70 | V | — |
| Input current ($LV_{IN}$ = 0 V or $LV_{IN}$ = $LV_{DD}$) | $I_{IH}$ | — | ±40 | μA | 2 |
| Output high voltage ($LV_{DD}$ = min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.00 | — | V | — |
| Output low voltage ($LV_{DD}$ = min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | — | 0.40 | V | — |

**Note:**

1. The min $V_{IL}$and max $V_{IH}$ values are based on the respective min and max $LV_{IN}$ values found in Table 3.
2. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbols referenced in Table 2 and Table 3.

## 2.11.6 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the SerDes interface of the P1013, as shown in Figure 22, where $C_{TX}$ is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to the ground. The reference circuit of the SerDes transmitter and receiver is shown in Figure 50.

### 2.11.6.1 DC Requirements for SGMII SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.21.3, "DC Level Requirement for SerDes Reference Clocks."

### 2.11.6.2 AC Requirements for SGMII SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$

Note that the SGMII clock requirements for SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 2.21.3.1, "AC Requirements for SerDes Reference Clocks."

### 2.11.6.3 SGMII Transmitter Electrical Characteristics

This section contains the following subsections:

- Section 2.11.6.3.1, "SGMII Transmit DC Timing Specifications"
- Section 2.11.6.3.2, "SGMII Transmit AC Timing Specifications"

#### 2.11.6.3.1 SGMII Transmit DC Timing Specifications

Table 41 and Table 43 describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX[n] and $\overline{\text{SD}n\text{\_TX}}$[n]) as shown in Figure 23.

**Table 41. SGMII DC Transmitter Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | — | — | $XV_{DD}$-Typ/2 + $\lvert V_{OD}\rvert$-max/2 | mV | 1 |
| Output low voltage | $V_{OL}$ | $XV_{DD}$-Typ/2 – $\lvert V_{OD}\rvert$-max/2 | — | — | mV | 1 |
| Output differential voltage[2, 3, 4] ($XV_{DD}$-Typ at 1.0V) | $\lvert V_{OD}\rvert$ | 320 | 500 | 725 | mV | Equalization setting: 1.0x. |
| | | 294 | 459 | 665 | | Equalization setting: 1.09x |
| | | 267 | 417 | 604 | | Equalization setting: 1.2x |
| | | 241 | 376 | 545 | | Equalization setting: 1.33x |
| | | 213 | 333 | 483 | | Equalization setting: 1.5x |
| | | 187 | 292 | 424 | | Equalization setting: 1.71x |
| | | 160 | 250 | 362 | | Equalization setting: 2.0x |
| Output impedance (single-ended) | $R_O$ | 40 | 50 | 60 | Ω | — |

**Table 41. SGMII DC Transmitter Electrical Characteristics (continued)**

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|

**Note:**

1. This does not align to DC-coupled SGMII.
2. $|V_{OD}| = |V_{SDn\_TXn} - V_{\overline{SDn\_TXn}}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*|V_{OD}|$.
3. The $|V_{OD}|$ value shown in the table assumes the following transmit equalization setting in the TXEQ0, TXEQ1 (for SerDes lanes 0 and 1) or TXEQ2, TXEQ3 (for SerDes lanes 2 and 3) bit field of P1013SerDes 0,1control register:
   - The LSB (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. The $|V_{OD}|$ value shown in the Typ column is based on the condition of $XV_{DD}$-Typ = 1.0V, no common mode offset variation, SerDes transmitter is terminated with 100-Ω differential load between SD_TX[n] and $\overline{SD\_TX[n]}$.

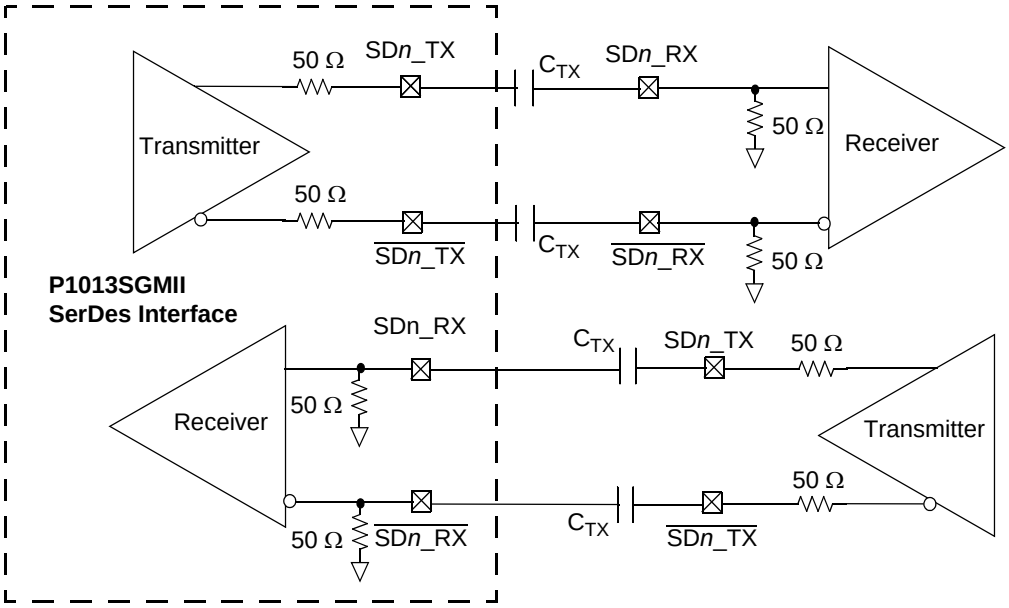



**Figure 22. 4-Wire AC-Coupled SGMII Serial Link Connection Example**

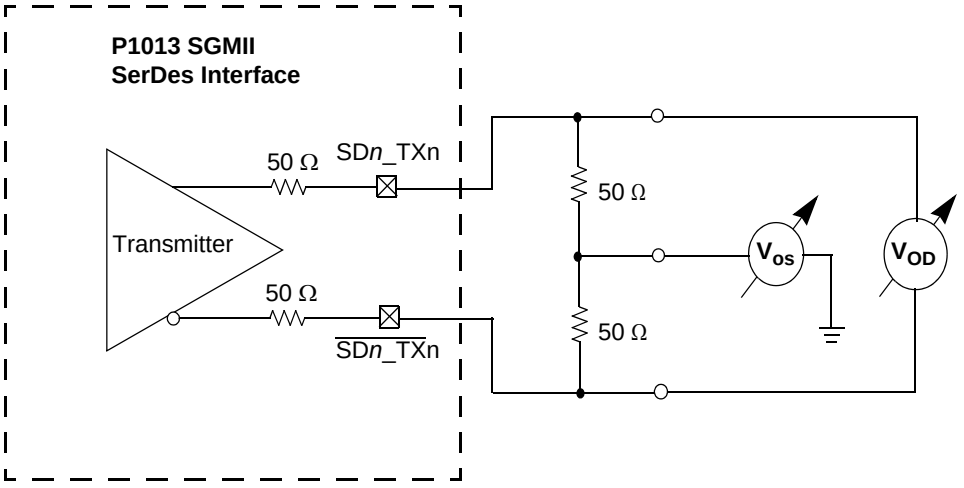



**Figure 23. SGMII Transmitter DC Measurement Circuit**

### 2.11.6.3.2 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

**Table 42. SGMII Transmit AC Timing Specifications**

At recommended operating conditions with $XV_{DD}$ = 1.0 V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Deterministic Jitter | JD | — | — | 0.17 | UI p-p | — |
| Total Jitter | JT | — | — | 0.35 | UI p-p | 2 |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | 1 |
| AC coupling capacitor | $C_{TX}$ | 5 | 100 | 200 | nF | 3 |

**Note:**

1. Each UI is 800 ps ± 100 ppm.
2. See Figure 25 for single frequency sinusoidal jitter limits.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

### 2.11.6.4 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX[n] and $\overline{\text{SD\_TX}}$[n]) or at the receiver inputs (SD_RX[n] and $\overline{\text{SD\_RX}}$[n]) as depicted in this figure, respectively.

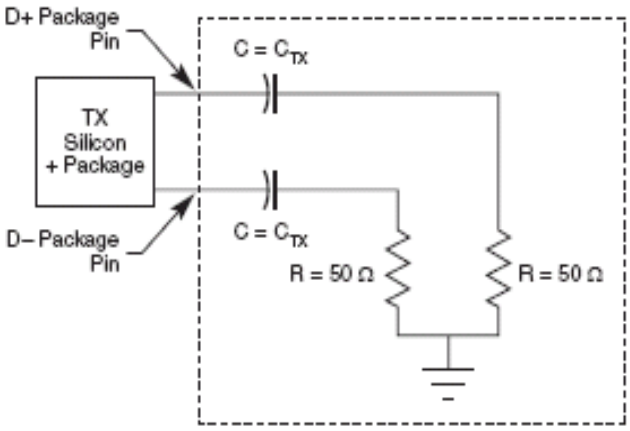



**Figure 24. SGMII AC Test/Measurement Load**

## 2.11.7 SGMII Receiver Timing Specifications

Table 43 and Table 44 provide the SGMII receive DC and AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data.

### 2.11.7.1 SGMII DC Receiver Timing Specification

This table lists the SGMII DC receiver electrical characteristics.

**Table 43. SGMII DC Receiver Electrical Characteristics[5]**

| Parameter | | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| DC Input voltage range | | — | N/A | | | — | 1 |
| Input differential voltage | LSTS = 0 | $V_{RX\_DIFFp-p}$ | 100 | — | 1200 | mV | 2, 4 |
| | LSTS = 1 | | 175 | — | | | |
| Loss of signal threshold | LSTS = 0 | VLOS | 30 | — | 100 | mV | 3, 4 |
| | LSTS = 1 | | 65 | — | 175 | | |
| Receiver differential input impedance | | $Z_{RX\_DIFF}$ | 80 | — | 120 | Ω | — |

**Note:**

1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The LSTS shown in the table refers to the LSTS**AB** or LSTS**EF** bit field of P1013's SerDes Control Register.
5. The supply voltage is 1.0 V.

### 2.11.7.2 SGMII Receiver AC Timing Specification

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. ource synchronous clocking is not supported. Clock is recovered from the data.

**Table 44. SGMII Receive AC Timing Specifications**

At recommended operating conditions with $XV_{DD}$ = 1.0 V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Deterministic Jitter Tolerance | JD | 0.37 | — | — | UI p-p | 1, 3 |
| Combined Deterministic and Random Jitter Tolerance | JDR | 0.55 | — | — | UI p-p | 1, 3 |
| Total Jitter Tolerance | JT | 0.65 | — | — | UI p-p | 1,3 |
| Bit Error Ratio | BER | — | — | $10^{-12}$ | — | — |
| Unit Interval | UI | 799.92 | 800.00 | 800.08 | ps | 2 |

**Note:**

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

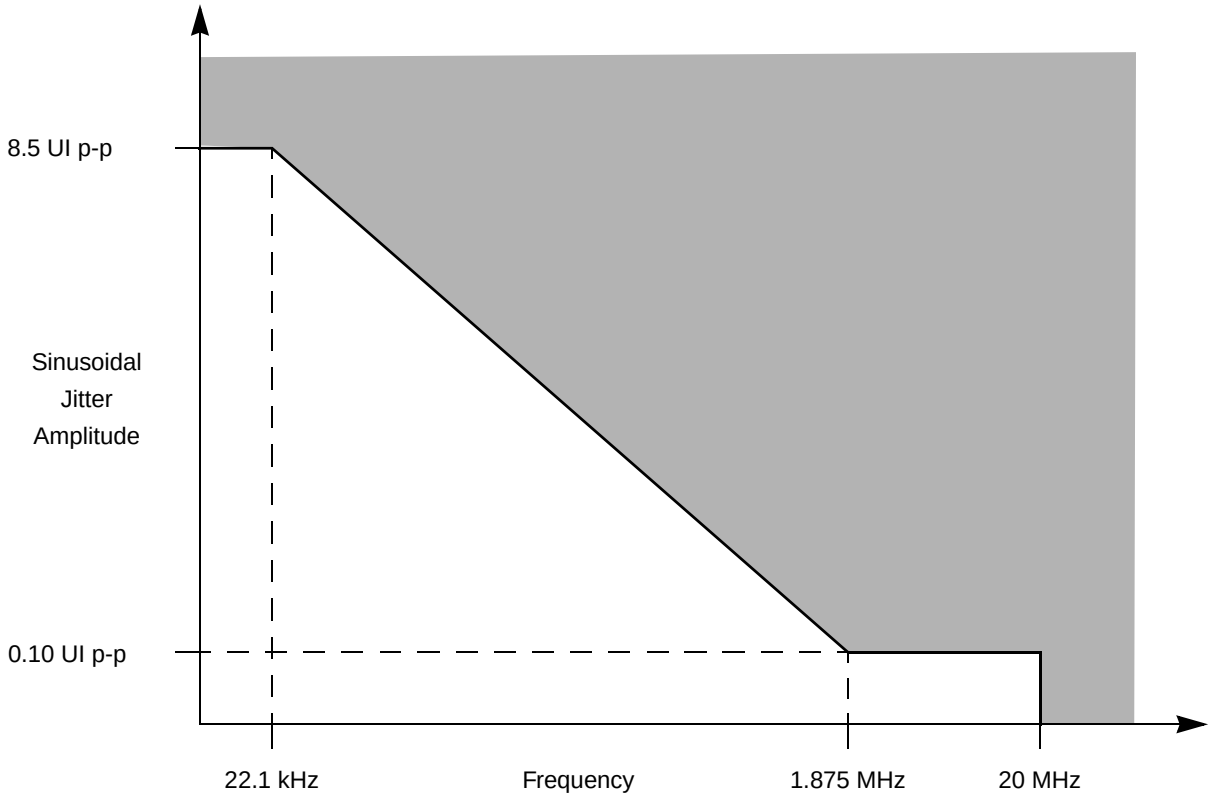



**Figure 25. Single Frequency Sinusoidal Jitter Limits**

## 2.12 USB

This section provides the AC and DC electrical specifications for the USB interfaces of the device.

This table provides the DC electrical characteristics for the ULPI interface when operating at 3.3 V.

**Table 45. USB DC Electrical Characteristics (3.3 V)**

For recommended operating conditions refer to Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($V_{IN}$ = 0 V or $V_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| Output high voltage ($LV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.8 | — | V | — |
| Output low voltage ($LV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.3 | V | — |

**Note:**

1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $LV_{IN}$ values found in Table 3.
2. The symbol $LV_{IN}$ represents the input voltage of the supply, and is referenced in Table 3.

This table provides the DC electrical characteristics for the ULPI interface when operating at 2.5 V.

**Table 46. USB DC Electrical Characteristics (2.5 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 1.7 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.7 | V | 1 |
| Input current ($V_{IN}$ = 0 V or $V_{IN}$ = $LV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| Output high voltage ($LV_{DD}$ = min, $I_{OH}$ = –1 mA) | $V_{OH}$ | 2.0 | — | V | — |
| Output low voltage ($OV_{DD}$ = min, $I_{OL}$ = 1 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**

1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $LV_{IN}$ values found in Table 3.
2. The symbol $LV_{IN}$ represents the input voltage of the supply, and is referenced in Table 3.

## 2.12.1 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

**Table 47. USB General Timing Parameters**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| USB clock cycle time | $t_{USCK}$ | 15 | — | ns | 2, 3, 4, 5 |
| Input setup to USB clock—all inputs | $t_{USIVKH}$ | 4 | — | ns | 2, 3, 4, 5 |
| input hold to USB clock—all inputs | $t_{USIXKH}$ | 1 | — | ns | 2, 3, 4, 5 |
| USB clock to output valid— all outputs | $t_{USKHOV}$ | — | 7 | ns | 2, 3, 4, 5 |
| Output hold from USB clock—all outputs | $t_{USKHOX}$ | 2 | — | ns | 2, 3, 4, 5 |

**Note:**

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{USIXKH}$ symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, $t_{USKHOX}$ symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $LV_{DD}/2$ of the rising edge of the USB clock to 0.4 × $LV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.
6. When switching the data pins from outputs to inputs using the USBn_DIR pin, the output timings will be violated on that cycle because the output buffers are tristated asynchronously. This should not be a problem, because the PHY should not be functionally looking at these signals on that cycle as per ULPI specifications.

The following two figures provide the AC test load and signals for the USB.

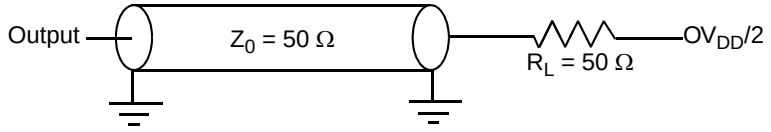



**Figure 26. USB AC Test Load**

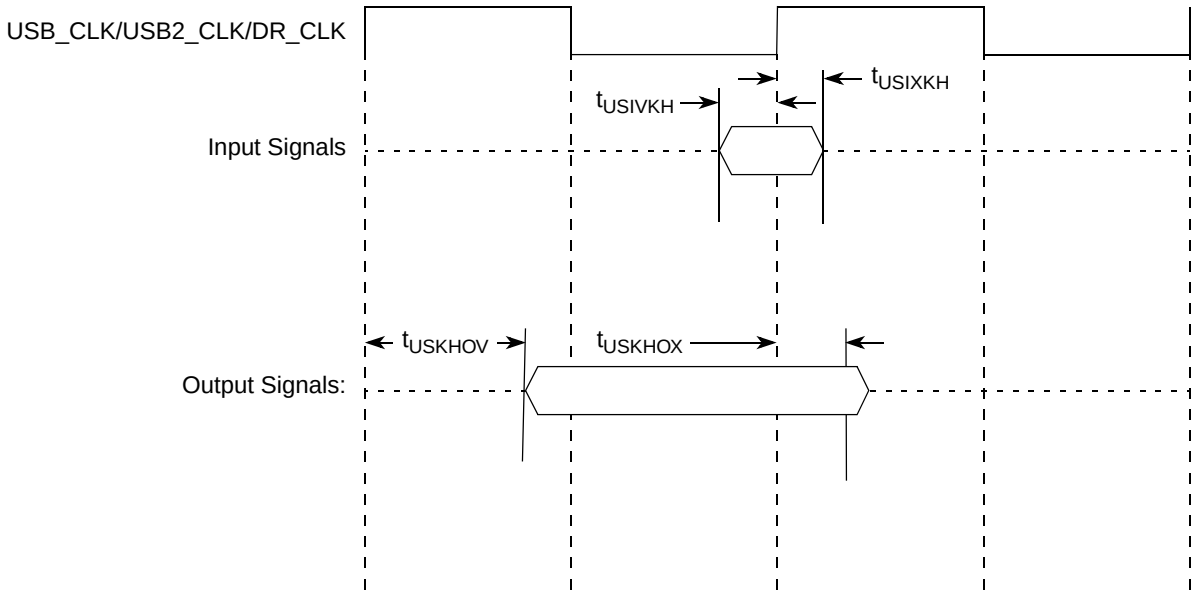



**Figure 27. USB Signals**

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

**Table 48. USB_CLK_IN AC Timing Specifications**

| Parameter | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency range | Steady state | $f_{USB\_CLK\_IN}$ | 59.97 | 60 | 60.03 | MHz |
| Clock frequency tolerance | — | $t_{CLK\_TOL}$ | –0.05 | 0 | 0.05 | % |
| Reference clock duty cycle | Measured at 1.6 V | $t_{CLK\_DUTY}$ | 40 | 50 | 60 | % |
| Total input jitter/time interval error | Peak-to-peak value measured with a second-order, high-pass filter of 500 kHz bandwidth | $t_{CLK\_PJ}$ | — | — | 200 | ps |

## 2.13 Enhanced Local Bus Interface

This section describes the DC and AC electrical specifications for the eLBC interface of the device.

### 2.13.1 Enhanced Local Bus DC Electrical Specifications

This table provides the DC electrical characteristics for the eLBC interface operating at $BV_{DD}$ = 3.3 V DC.

**Table 49. Enhanced Local Bus DC Electrical Specifications (3.3 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | — | V |
| Low-level input voltage | $V_{IL}$ | — | 0.8 | V |
| Input current ($V_{IN}$ = 0 V or $V_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±40 | μA |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V |

**Table 49. Enhanced Local Bus DC Electrical Specifications (3.3 V DC) (continued)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V |

This table provides the DC electrical characteristics for the eLBC interface operating at $BV_{DD}$ = 2.5 V DC.

**Table 50. Enhanced Local Bus DC Electrical Specifications (2.5 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 1.7 | — | V |
| Low-level input voltage | $V_{IL}$ | — | 0.7 | V |
| Input current ($V_{IN}$ = 0 V or $V_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±40 | μA |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –1 mA) | $V_{OH}$ | 2.0 | — | V |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 1 mA) | $V_{OL}$ | — | 0.4 | V |

This table provides the DC electrical characteristics for the eLBC interface operating at $BV_{DD}$ = 1.8 V DC.

**Table 51. Enhanced Local Bus DC Electrical Specifications (1.8 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 1.25 | — | V |
| Low-level input voltage | $V_{IL}$ | — | 0.6 | V |
| Input current ($V_{IN}$ = 0 V or $V_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±40 | μA |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –0.5 mA) | $V_{OH}$ | 1.35 | — | V |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 0.5 mA) | $V_{OL}$ | — | 0.4 | V |

## 2.13.2 Enhanced Local Bus AC Electrical Specifications

## 2.13.3 Test Condition

This figure provides the AC test load for the enhanced local bus.

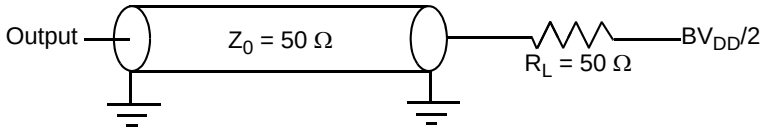



**Figure 28. Enhanced Local Bus AC Test Load**

## 2.13.4 Local Bus AC Electrical Specification

All the output signal timings are relative to the falling edge of any LCLKs for PLL bypass mode. The external circuit must use the rising edge of the LCLKs to latch the data.

All the input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

This table describes the timing parameters of the local bus interface.

**Table 52. Enhanced Local Bus Timing Parameters ($BV_{DD}$ = 3.3V, 2.5V and 1.8V)**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 12 | — | ns | — |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 45 | 55 | % | — |
| LCLK[n] skew to LCLK[m] | $t_{LBKSKEW}$ | — | 150 | ps | 2 |
| Input setup (except LGTA/LUPWAIT/LFRB) | $t_{LBIVKH}$ | 6 | — | ns | — |
| Input hold (except LGTA/LUPWAIT/LFRB) | $t_{LBIXKH}$ | 1 | — | ns | — |
| Input setup (for LGTA/LUPWAIT/LFRB) | $t_{LBIVKL}$ | 6 | — | ns | — |
| Input hold (for LGTA/LUPWAIT/LFRB) | $t_{LBIXKL}$ | 1 | — | ns | — |
| Output delay (Except LALE) | $t_{LBKLOV}$ | — | 1.5 | ns | — |
| Output hold (Except LALE) | $t_{LBKLOX}$ | -3.5 | — | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKLOZ}$ | — | 2 | ns | 3 |
| LALE output negation to LAD/LDP output transition (LATCH hold time) | $t_{LBONOT}$ | 1/2 (LBCR[AHD]=1) | 1 (LBCR[AHD] = 0) | eLBC controller clock | 4 |

**Note:**

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question
2. Skew measured between complementary signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. $t_{LBONOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBONOT}$ is determined by LBCR[AHD]. The unit is the eLBC controller clock. The ratio between the platform clock and eLBC controller clock is **1:1**. After power on reset, LBCR[AHD] defaults to 0, eLBC runs at maximum hold time.
5. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.

This figure shows the AC timing diagram.

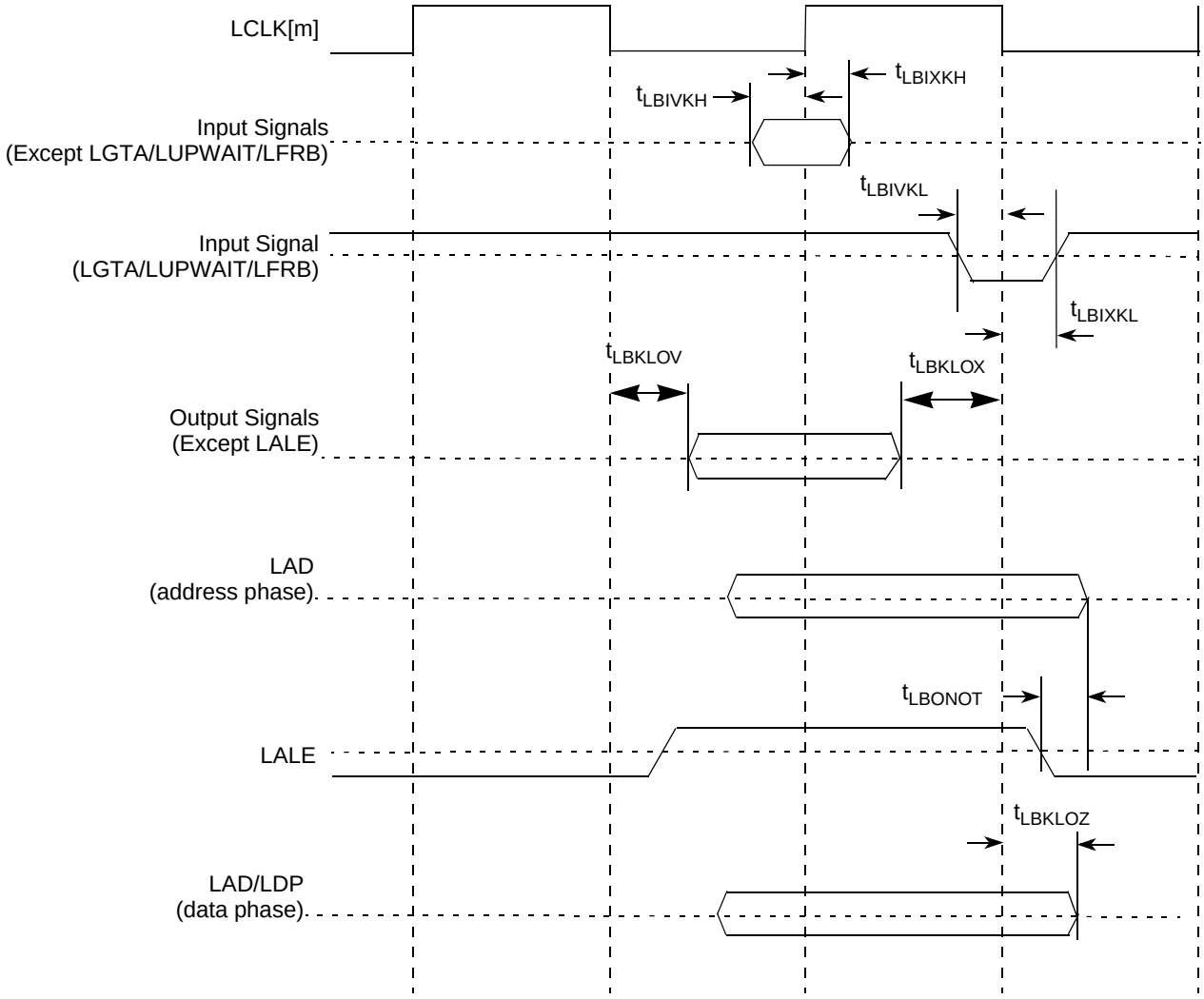



**Figure 29. Enhanced Local Bus Signals**

Figure 29 AC timing diagram applies to all three controllers that eLBC supports: GPCM, UPM and FCM. For input signals, the AC timings data are used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the timing of the signals.The final signal delay value for output signals will be the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by $t_{acs}$ (0, 1/4, 1/2, 1, 1+1/4, 1+1/2, 2, 3 cycles), so the final delay will be $t_{acs}$ + $t_{LBKLOV}$.

This figure shows how the AC timing diagram applies to GPCM in PLL bypass mode. Same principle applies to UPM and FCM.

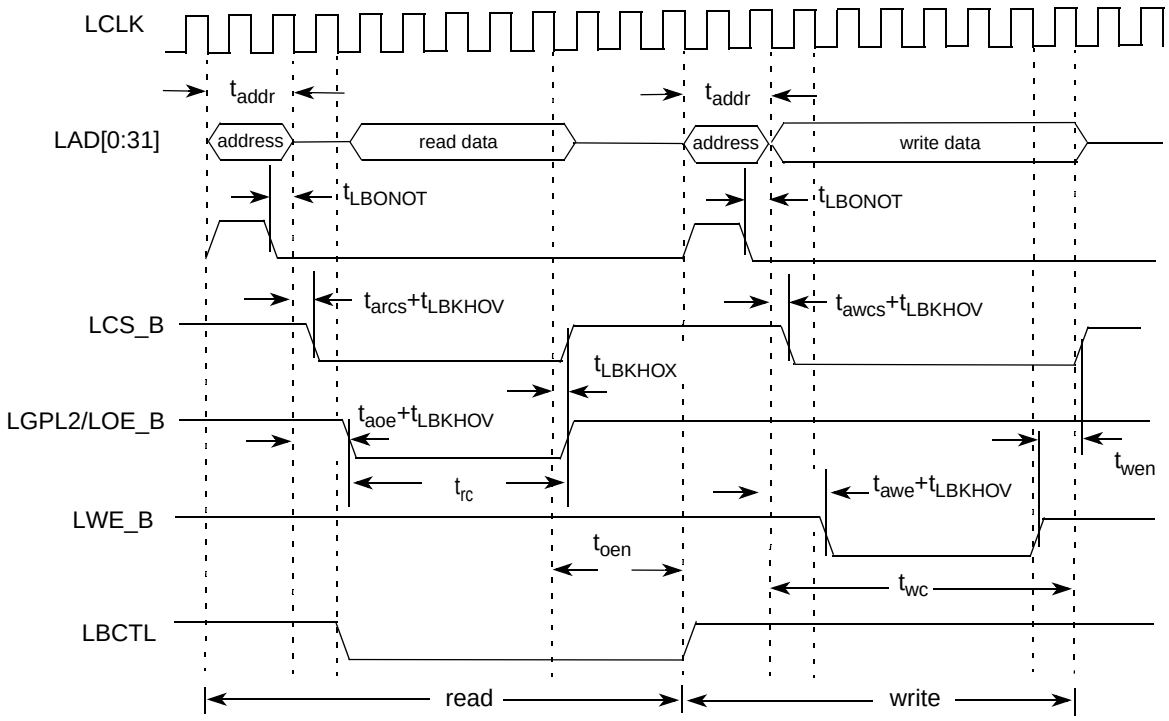



**Figure 30. GPCM Timing Diagram**

1 $t_{addr}$ is programmable and determined by LCRR[EADC] and ORx[EAD].

2 $t_{arcs}$, $t_{awcs}$, $t_{aoe}$, $t_{rc}$, $t_{oen}$, $t_{awe}$, $t_{wc}$, $t_{wen}$ are determined by ORx. See the *P1022 QorIQ Integrated Processor Reference Manual*.

## 2.14 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC (SDIO) interface of the device.

### 2.14.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface of the device.

**Table 53. eSDHC interface DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 0.625 × $OV_{DD}$ | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | — | 0.25 × $OV_{DD}$ | V | 1 |
| Input/Output leakage current | $I_{IN}/I_{OZ}$ | — | –50 | 50 | uA | — |

**Table 53. eSDHC interface DC Electrical Characteristics (continued)**

| Characteristic | Symbol | Condition | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -100 uA @$OV_{DD}$min | 0.75 × $OV_{DD}$ | — | V | — |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 100uA @$OV_{DD}$min | — | 0.125 × $OV_{DD}$ | V | — |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –100 uA | $OV_{DD}$ – 0.2 | — | V | 2 |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 2 mA | — | 0.3 | V | 2 |

**Note:**

1. Note that the min $V_{IL}$and max $V_{IH}$ values are based on the respective min and max $OV_{IN}$ values found in Figure 3.
2. Open drain mode for MMC cards only.

## 2.14.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in Figure 31 and Figure 32.

**Table 54. eSDHC AC Timing Specifications**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| SD_CLK clock frequency:<br>SD/SDIO Full speed/high speed mode<br>MMC Full speed/high speed mode | $f_{SHSCK}$ | <br>0 | <br>25/50<br>20/52 | MHz | 2, 4 |
| SD_CLK clock low time - High speed/Full speed mode | $t_{SHSCKL}$ | 7/10 | — | ns | 4 |
| SD_CLK clock high time - High speed/Full speed mode | $t_{SHSCKH}$ | 7/10 | — | ns | 4 |
| SD_CLK clock rise and fall times | $t_{SHSCKR}$/ $t_{SHSCKF}$ | — | 3 | ns | 4 |
| Input setup time: SD_CMD, SD_DATx, SD_CD to SD_CLK | $t_{SHSIVKH}$ | 5 | — | ns | 4 |
| Input hold time: SD_CMD, SD_DATx, SD_CD to SD_CLK | $t_{SHSIXKH}$ | 2.5 | — | ns | 3,4 |
| Output delay time: SD_CLK to SD_CMD, SD_DATx valid | $t_{SHSKHOV}$ | –3 | 3 | ns | 4 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0 - 25 MHz for a SD/SDIO card and 0 - 20 MHz for a MMC card. In high speed mode, clock frequency value can be 0 - 50 MHz for a SD/SDIO card and 0 - 52MHz for a MMC card.
3. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2ns.
4. $C_{CARD} \leq$10 pF, (1 card), and $C_L = C_{BUS} + C_{HOST}+C_{CARD} \leq 40$ pF

This figure provides the eSDHC clock input timing diagram.

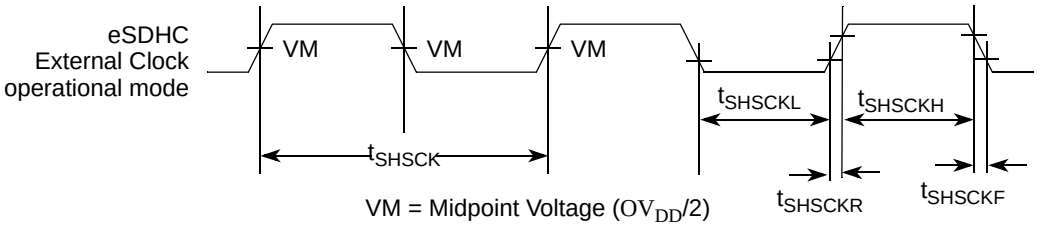



**Figure 31. eSDHC Clock Input Timing Diagram**

This figure provides the data and command input/output timing diagram.

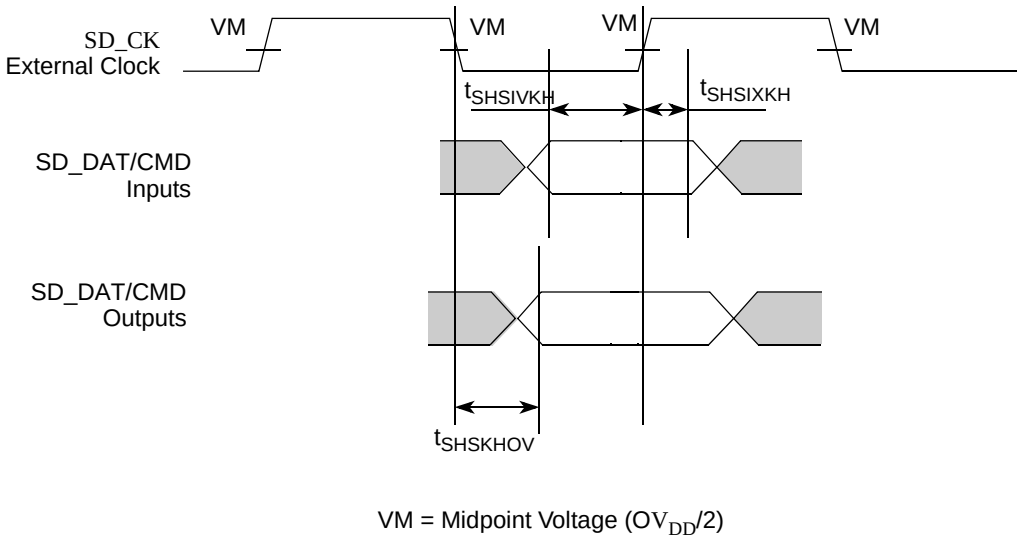



**Figure 32. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock**

## 2.15 Display Interface Unit

This section describes the DIU DC and AC electrical specifications.

### 2.15.1 DIU DC Electrical Characteristics

This table provides the DIU DC electrical characteristics.

**Table 55. DIU DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | — | V |
| Low-level input voltage | $V_{IL}$ | — | 0.8 | V |
| Input current ($V_{IN}$[1] = 0 V or $V_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±40 | μA |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –100 μA) | $V_{OH}$ | $BV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 100 μA) | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 2 and Table 3.

## 2.15.2 DIU AC Timing Specifications

This figure depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the DIU_CLK_OUT signal and active-high polarity of the DIU_HSYNC, DIU_VSYNC, and DIU_DE signals. By default, all control signals and the display data are generated at the rising edge of the internal pixel clock, and the DIU_CLK_OUT output to drive the panel has the same polarity with the internal pixel clock. User can select the polarity of the DIU_HSYNC and DIU_VSYNC signal (via the SYN_POL register), whether active-high or active-low, the default is active-high. The DIU_DE signal is always active-high.

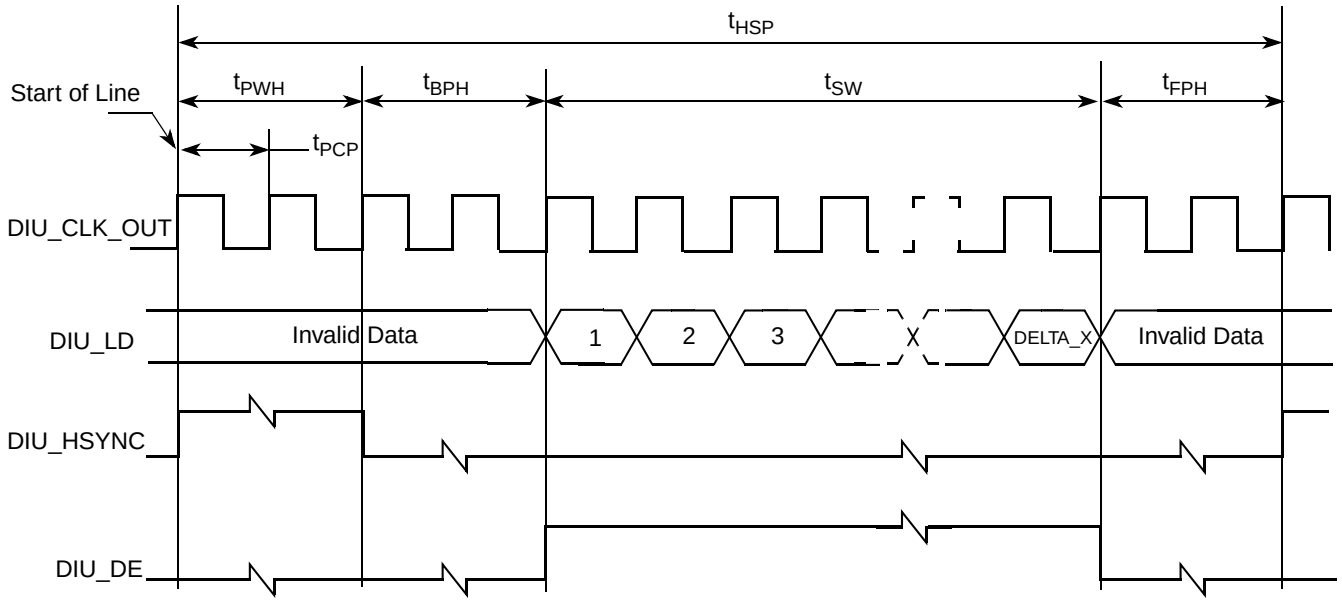



**Figure 33. TFT DIU/LCD Interface Timing Diagram—Horizontal Sync Pulse**

This figure depicts the vertical timing (timing of one frame), including both the vertical sync pulse and the data. All parameters shown in the diagram are programmable.

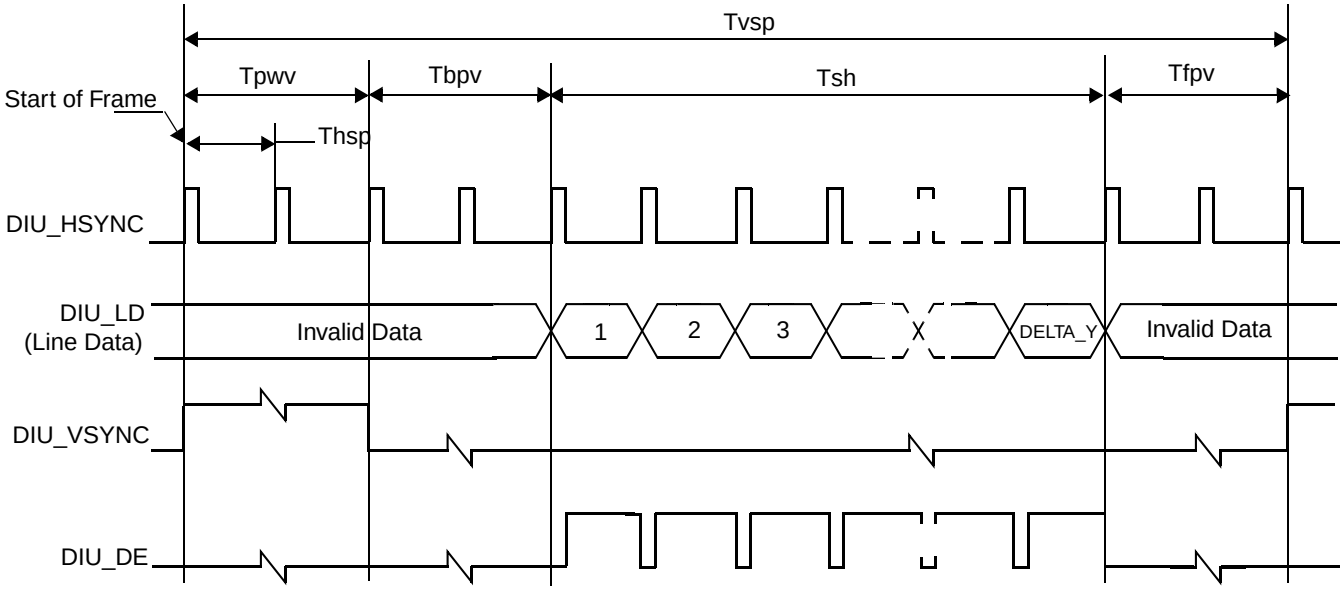



**Figure 34. TFT DIU/LCD Interface Timing Diagram—Vertical Sync Pulse**

This table shows timing parameters of signals presented in Figure 33 and Figure 34.

**Table 56. DIU Interface AC Timing Parameters—Pixel Level**

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| Display pixel clock period | $t_{PCP}$ | 7.5 (minimum) | ns | 1 |
| | | | | — |
| HSYNC width | $t_{PWH}$ | PW_H × $t_{PCP}$ | ns | — |
| HSYNC back porch width | $t_{BPH}$ | BP_H × $t_{PCP}$ | ns | — |
| HSYNC front porch width | $t_{FPH}$ | FP_H × $t_{PCP}$ | ns | — |
| Screen width | $t_{SW}$ | DELTA_X × $t_{PCP}$ | ns | — |
| HSYNC (line) period | $t_{HSP}$ | (PW_H + BP_H + DELTA_X + FP_H) × $t_{PCP}$ | ns | — |
| | | | | — |
| VSYNC width | $t_{PWV}$ | PW_V × $t_{HSP}$ | ns | — |
| VSYNC back porch width | $t_{BPV}$ | BP_V × $t_{HSP}$ | ns | — |
| VSYNC front porch width | $t_{FPV}$ | FP_V × $t_{HSP}$ | ns | — |
| Screen height | $t_{SH}$ | DELTA_Y × $t_{HSP}$ | ns | — |
| VSYNC (frame) period | $t_{VSP}$ | (PW_V + BP_V + DELTA_Y + FP_H) × $t_{HSP}$ | ns | — |

**Note:**

1. Display pixel clock frequency must also be less than or equal to 1/3 of the platform clock

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H, and FP_H parameters are programmed via the HSYN_PARA register; and the PW_V, BP_V, and FP_V parameters are programmed via the VSYN_PARA register.

This figure depicts the synchronous display interface timing for access level, and Table 57 lists the timing parameters.

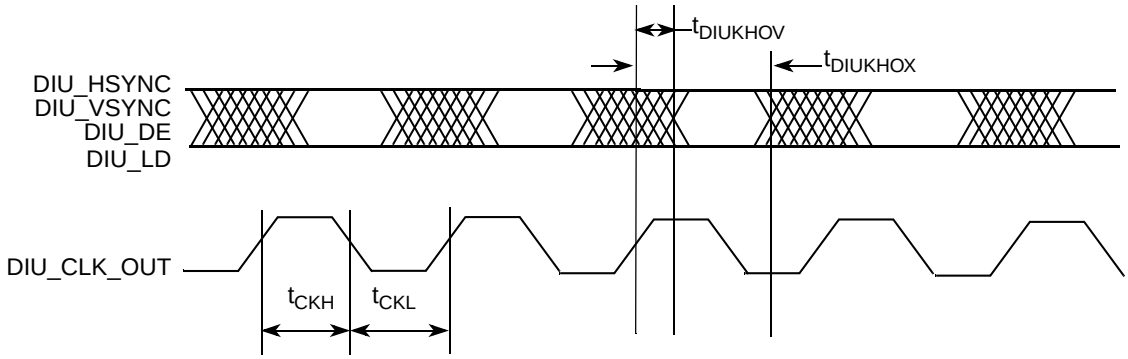



**Figure 35. LCD Interface Timing Diagram—Access Level**

## NOTE

The DIU_OUT_CLK edge and phase delay is selectable via the Global Utilities CLKDVDR register.

**Table 57. LCD Interface Timing Parameters—Access Level**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LCD interface pixel clock high time | $t_{CKH}$ | 0.35 × $t_{PCP}$ | 0.5 × $t_{PCP}$ | 0.65 × $t_{PCP}$ | ns |
| LCD interface pixel clock low time | $t_{CKL}$ | 0.35 × $t_{PCP}$ | 0.5 × $t_{PCP}$ | 0.65 × $t_{PCP}$ | ns |
| LCD interface pixel clock to output valid | $t_{DIUKHOV}$ | — | — | 2 | ns |
| LCD interface output hold from pixel clock | $t_{DIUKHOX}$ | $t_{PCP}$ – 2 | — | — | ns |

## 2.16 Synchronous Serial Interface (SSI)

This section describes the DC and AC electrical specifications for the SSI interface of the device.

### 2.16.1 SSI DC Electrical Characteristics

The following table provides SSI DC electrical characteristics.

**Table 58. SSI DC Electrical Characteristics**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | — | V | 1 |
| Low-level input voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($OV_{IN}$[1] = 0 V or $OV_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**

1. The min $V_{IL}$and max $V_{IH}$ values are based on the respective min and max $OV_{IN}$ values found in Table 3.
2. The symbol $OV_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.

### 2.16.2 SSI AC Timing Specifications

All timings for the SSI are given:

- for a noninverted serial clock polarity (STCR[TSCKP] = 0, SRCR[RSCKP] = 1) and
- for a noninverted frame sync (STCR[TFSI], SRCR[RFSI] = 1).

If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK, SRCK and/or the frame sync STFS, SRFS shown in the following tables and figures. See the *P1022 QorIQ Integrated Processor Reference Manual* for more information.

#### 2.16.2.1 SSI Transmitter Timing

This table provides the transmitter timing parameters.

**Table 59. SSI Transmitter Timing Parameters**

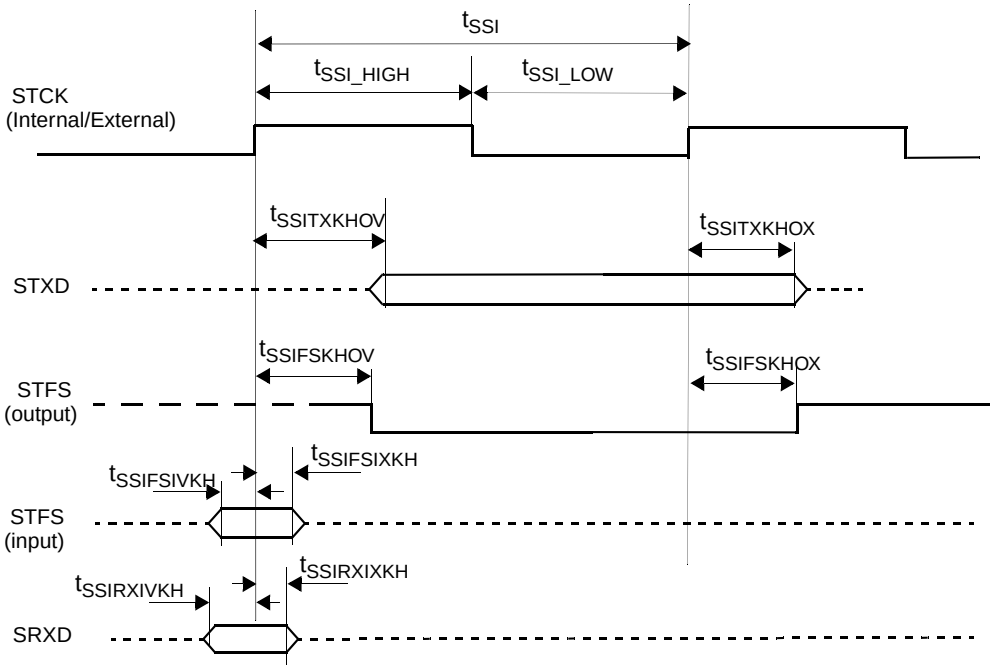
| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| STCK clock period | $t_{SSI}$ | 81.4 | — | ns | — |

**Table 59. SSI Transmitter Timing Parameters (continued)**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| STCK clock high period | $t_{SSI\_HIGH}$ | 36.0 | — | ns | — |
| STCK clock rise time | $t_{SSIKH}$ | — | 6.0 | ns | — |
| STCK clock low period | $t_{SSI\_LOW}$ | 36.0 | — | ns | — |
| STCK clock fall time | $t_{SSIKL}$ | — | 6.0 | ns | — |
| STCK high to STFS valid | $t_{SSIFSKHOV}$ | — | 12.0 | ns | 1 |
| STFS hold time | $t_{SSIFSKHOX}$ | -3.0 | -- | ns | 1 |
| STCK high to STXD valid from high impedance | $t_{SSITXKHOV}$ | — | 12.0 | ns | 1 |
| STXD hold time | $t_{SSITXKHOX}$ | -3.0 | | ns | 1 |
| STFS input setup time | $t_{SSIFSIVKH}$ | 10.0 | | ns | — |
| STFS input hold time | $t_{SSIFSIXKH}$ | 15.0 | | ns | — |
| **Synchronous Clock Operation** | | | | | — |
| SRXD setup time | $t_{SSIRXIVKH}$ | 10.0 | — | ns | — |
| SRXD hold time | $t_{SSIRXIXKH}$ | 2.0 | — | ns | — |

**Note:**
1. Output values are based on 25pF capacitive load.

This figure shows the SSI transmit signal timing.




**Note:**
1) All timings shown are with respect to STCK
2) SRXD input shown for synchronous mode

**Figure 36. SSI Transmitter Timing Diagram**

### 2.16.2.2 SSI Receiver Timing

This table provides the receiver timing parameters.

**Table 60. SSI Receiver Timing Parameters**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| SRCK clock period | $t_{SSI}$ | 81.4 | — | ns | — |
| SRCK clock high period | $t_{SSI\_HIGH}$ | 36.0 | — | ns | — |
| SRCK clock rise time | $t_{SSIKH}$ | — | 6.0 | ns | — |
| SRCK clock low period | $t_{SSI\_LOW}$ | 36.0 | — | ns | — |
| SRCK clock fall time | $t_{SSIKL}$ | — | 6.0 | ns | — |
| SRCK high to SRFS valid | $t_{SSIFSKHOV}$ | — | 12.0 | ns | 1 |
| SRFS hold time | $t_{SSIFSKHOX}$ | -3.0 | | ns | 1 |
| SRXD setup time | $t_{SSIRXIVKH}$ | 10.0 | — | ns | — |
| SRXD hold time | $t_{SSIRXIXKH}$ | 2.0 | — | ns | — |
| SRFS input setup time | $t_{SSIFSIVKH}$ | 10.0 | — | ns | — |
| SRFS input hold time | $t_{SSIFSIXKH}$ | 15.0 | — | ns | — |

**Note:**
1. Output values are based on 25pF capacitive load.

This figure shows the SSI receiver timing.

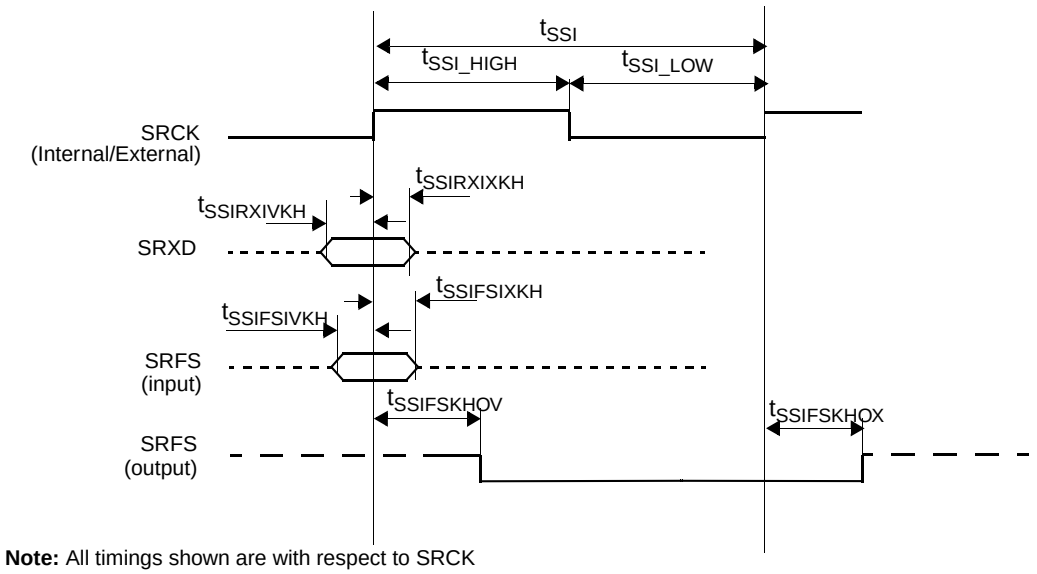



**Figure 37. SSI Receiver Timing Diagram**

# 2.17 Programmable Interrupt Controller (PIC) Specifications

This section describes the DC and AC electrical specifications for PIC on the device.

## 2.17.1 PIC DC specifications

This table provides the DC electrical characteristics for the PIC interface.

**Table 61. PIC DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | — | V | 1 |
| Low-level input voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($OV_{IN}$ = 0 V or $OV_{IN}$ = $OV_{DD}$/$OV_{DD2}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| High-level output voltage ($OV_{DD}$/$OV_{DD2}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**

1. The min $V_{IL}$and max $V_{IH}$ values are based on the min and max $OV_{IN}$ respective values found in Table 2.
2. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 3.

## 2.17.2 PIC AC Timing Specifications

This table provides the PIC input and output AC timing specifications.

**Table 62. PIC Input AC Timing Specifications**

| Characteristic | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| PIC inputs—minimum pulse width | $t_{PIWID}$ | 3 | — | SYSCLKs | 1 |

**Note:**

1. PIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least $t_{PIWID}$ ns to ensure proper operation when working in edge triggered mode

# 2.18 $I^2C$

This section describes the DC and AC electrical characteristics for the $I^2C$ interfaces of the device.

## 2.18.1 $I^2C$ DC Electrical Characteristics

This table provides the DC electrical characteristics for the $I^2C$ interfaces.

**Table 63. $I^2C$ DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | — | V | 1 |
| Low-level input voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | 0 | 0.4 | V | 2 |

**Table 63. I²C DC Electrical Characteristics (continued)**

| | | | | | |
|---|---|---|---|---|---|
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 3 |
| Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max) | $I_I$ | –10 | 10 | μA | 4 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | — |

**Note:**
1. Note that the min $V_{IL}$ and max $V_{IH}$ values are based on the min and max $OV_{IN}$ respective values found in Table 2.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the *P1022 QorIQ Integrated Processor Reference Manual* for information on the digital filter used.
4. I/O pins will obstruct the SDA and SCL lines if $OV_{DD}$ is switched off.

## 2.18.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interfaces.

**Table 64. I²C AC Electrical Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%. All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 63)

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{I2C}$ | 0 | 400 | kHz[4] |
| Low period of the SCL clock | $t_{I2CL}$ | 1.3 | — | μs |
| High period of the SCL clock | $t_{I2CH}$ | 0.6 | — | μs |
| Setup time for a repeated START condition | $t_{I2SVKH}$ | 0.6 | — | μs |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ | 0.6 | — | μs |
| Data setup time | $t_{I2DVKH}$ | 100 | — | ns |
| Data input hold time:<br>CBUS compatible masters<br>I²C bus devices | $t_{I2DXKL}$ | <br>—<br>0[2] | <br>—<br>— | μs |
| Data output delay time | $t_{I2OVKL}$ | — | 0.9[3] | μs |
| Setup time for STOP condition | $t_{I2PVKH}$ | 0.6 | — | μs |
| Bus free time between a STOP and START condition | $t_{I2KHDX}$ | 1.3 | — | μs |
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{NL}$ | $0.1 \times OV_{DD}$ | — | V |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | $0.2 \times OV_{DD}$ | — | V |
| Capacitive load for each bus line | Cb | — | 400 | pF |

**Table 64. $I^2C$ AC Electrical Specifications (continued)**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%. All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 63)

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|

**Note:**

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes $I^2C$ timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes $I^2C$ timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes $I^2C$ timing (I2) for the time that the data with respect to the STOP condition (P) reaching the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time.
2. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to the $V_{IH}$min of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP condition. When the device acts as the $I^2C$ bus master while transmitting, the device drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device would not cause unintended generation of START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the device as transmitter, application note AN2919 referred to in note 4 below is recommended.
3. The maximum $t_{I2OVKL}$ has only to be met if the device does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.
4. The requirements for $I^2C$ frequency calculation must be followed. Refer to Freescale application note AN2919, *Determining the $I^2C$ Frequency Divider Ratio for SCL*.

This figure provides the AC test load for the $I^2C$.

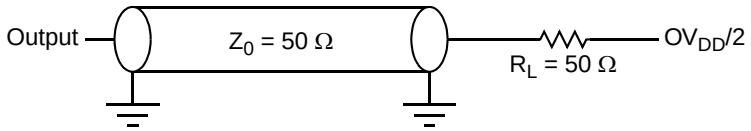



**Figure 38. $I^2C$ AC Test Load**

This figure shows the AC timing diagram for the $I^2C$ bus.

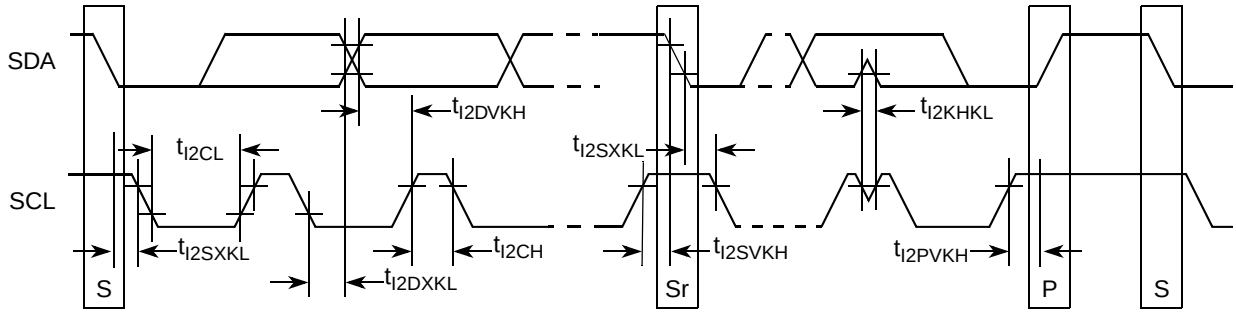



**Figure 39. $I^2C$ Bus AC Timing Diagram**

## 2.19 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface of the device. There are GPIO pins on various power supplies in this device. For the rest of this section, $BV_{IN}$ and $BV_{DD}$ would stand in for any power supply that the GPIO is running off.

## 2.19.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface when operating from a 3.3 V supply.

**Table 65. GPIO DC Electrical Characteristics (3.3 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($BV_{IN}$ = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| Output high voltage ($BV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Output low voltage ($BV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**
1. The min $V_{IL}$ and max $V_{IH}$ values are based on the min and max $BV_{IN}$ respective values found in Table 3.
2. The symbol $BV_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the GPIO interface when operating from a 2.5 V supply.

**Table 66. GPIO DC Electrical Characteristics (2.5 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 1.7 | — | V | 1 |
| Low-level input voltage | $V_{IL}$ | — | 0.7 | V | 1 |
| Input current ($V_{IN}$ = 0 V or $V_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 1.7 | — | V | — |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.7 | V | — |

**Note:**
1. The min $V_{IL}$ and max $V_{IH}$ values are based on the min and max $BV_{IN}$ respective values found in Table 3.
2. The symbol $BV_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the GPIO interface when operating from a 1.8 V supply.

**Table 67. GPIO DC Electrical Characteristics (1.8 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 1.2 | — | V | 1 |
| Low-level input voltage | $V_{IL}$ | — | 0.6 | V | 1 |
| Input current ($BV_{IN}$ = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –0.5 mA) | $V_{OH}$ | 1.35 | — | V | — |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 0.5 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**
1. The min $V_{IL}$ and max $V_{IH}$ values are based on the min and max $BV_{IN}$ respective values found in Table 3.
2. The symbol $BV_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.

## 2.19.2 GPIO AC Electrical Specifications

This table provides the GPIO input and output AC timing specifications.

**Table 68. GPIO Input AC Timing Specifications**

| Parameter | Symbol | Min | Unit | Note |
|---|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 20 | ns | 1 |

**Note:**

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least $t_{PIWID}$ to ensure proper operation.

This figure provides the AC test load for the GPIO.

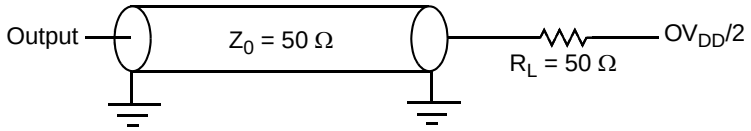



**Figure 40. AC test load for GPIO**

## 2.20 TDM

This section describes the DC and AC electrical specifications for the TDM of the device.

## 2.20.1 TDM DC Timing Specifications

This table provides the DC electrical characteristics for the TDM interface.

**Table 69. TDM DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | — | V | 1 |
| Low-level input voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($OV_{IN}$ = 0 V or $OV_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**

1. Note that the min $V_{IL}$and max $V_{IH}$ values are based on the min and max $OV_{IN}$ respective values found in Table 2.
2. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 3.

## 2.20.2 TDM AC Timing Specifications

This table provides the input and output AC timing specifications for the TDM interface.

**Table 70. TDM AC Timing Specifications**

| Characteristic | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| TDMxRCK/TDMxTCK | $t_{DM}$ | 62.5 | — | ns | 5 |

**Table 70. TDM AC Timing Specifications (continued)**

| Characteristic | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| TDMxRCK/TDMxTCK high pulse width | $t_{DM\_HIGH}$ | 8.0 | — | ns | — |
| TDMxRCK/TDMxTCK low pulse width | $t_{DM\_LOW}$ | 8.0 | — | ns | — |
| TDM all input setup time | $t_{DMIVKH}$ | 3.0 | — | ns | — |
| TDMxRD hold time | $t_{DMRDIXKH}$ | 3.5 | — | ns | — |
| TDMxTFS/TDMxRFS input hold time | $t_{DMFSIXKH}$ | 2.0 | — | ns | — |
| TDMxTCK High to TDMxTD output active | $t_{DM\_OUTAC}$ | 4.0 | — | ns | — |
| TDMxTCK High to TDMxTD output valid | $t_{DMTKHOV}$ | — | 14.0 | ns | — |
| TDMxTD hold time | $t_{DMTKHOX}$ | 2.0 | | ns | — |
| TDMxTCK High to TDMxTD output high impedance | $t_{DM\_OUTHI}$ | — | 10.0 | ns | — |
| TDMxTFS/TDMxRFS output valid | $t_{DMFSKHOV}$ | — | 13.5 | ns | — |
| TDMxTFS/TDMxRFS output hold time | $t_{DMFSKHOX}$ | 2.5 | — | ns | — |

**Note:**

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{HIKHOX}$ symbolizes the outputs internal timing (HI) for the time $t_{serial}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output values are based on 30 pF capacitive load.
3. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. TDMxTCK and TDMxRCK are shown using the rising edge.
4. All values are based on a maximum TDM interface frequency of 50 MHz.
5. The rise / fall time on TDM clock inputs should not exceed 5ns. Rise time refers to signal transitions from 10% to 90% of Vcc; fall time refers to transitions from 90% to 10% of Vcc.

This figure shows the TDM receive signal timing.

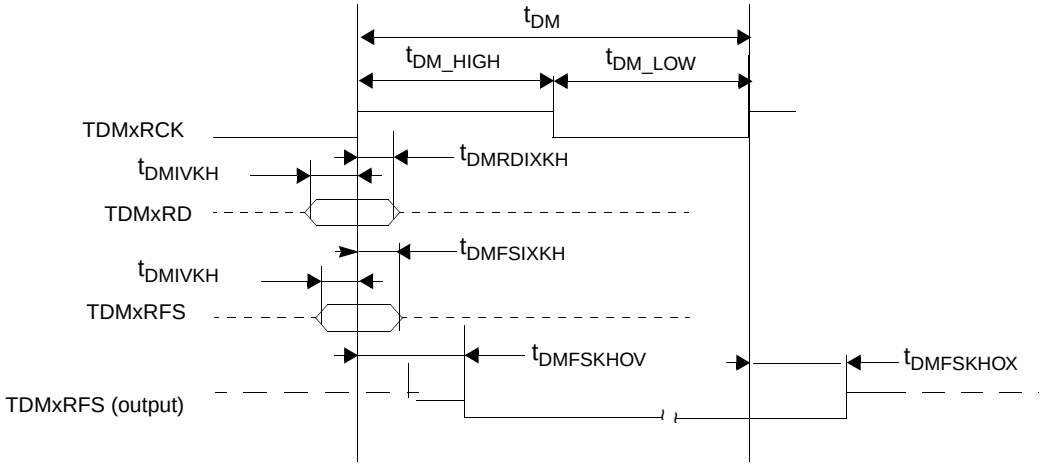



**Figure 41. TDM Receive Signals**

This figure shows the TDM transmit signal timing.

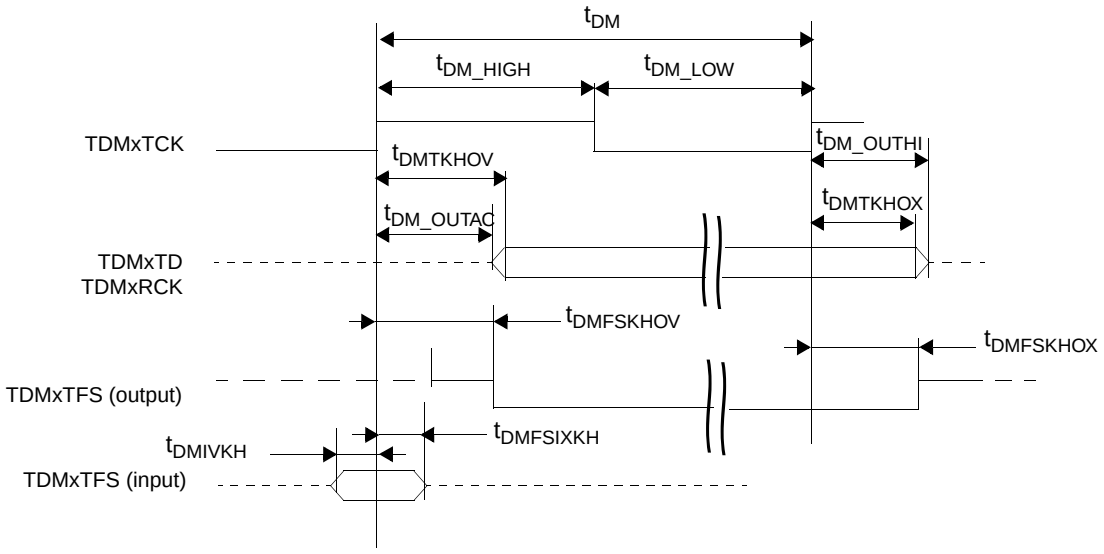



**Figure 42. TDM Transmit Signals**

## 2.21 High-Speed Serial Interfaces (HSSI)

The device features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The two SerDes can be configured as various combinations of PCI Express, SATA and SGMII.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

### 2.21.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 43 shows how the signals are defined. For illustration purposes, only one SerDes lane is used for description. Figure 43 shows the waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify the illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

1. **Single-Ended Swing:** The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{\_TX}}$, SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.
2. **Differential Output Voltage, $V_{OD}$** (or **Differential Output Swing**): The Differential Output Voltage (or Swing) of the transmitter, $V_{OD}$, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The $V_{OD}$ value can be either positive or negative.
3. **Differential Input Voltage, $V_{ID}$** (or **Differential Input Swing**): The Differential Input Voltage (or Swing) of the receiver, $V_{ID}$, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The $V_{ID}$ value can be either positive or negative.
4. **Differential Peak Voltage**, **$V_{DIFFp}$:** The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$:** Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.
6. **Differential Waveform:** The differential waveform is constructed by subtracting the inverting signal ($\overline{SDn\_TX}$, for example) from the non-inverting signal (SD*n*_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 43 as an example for differential waveform.
7. **Common Mode Voltage $V_{cm}$:** The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SDn\_TX} + V_{\overline{SDn\_TX}})/2 = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

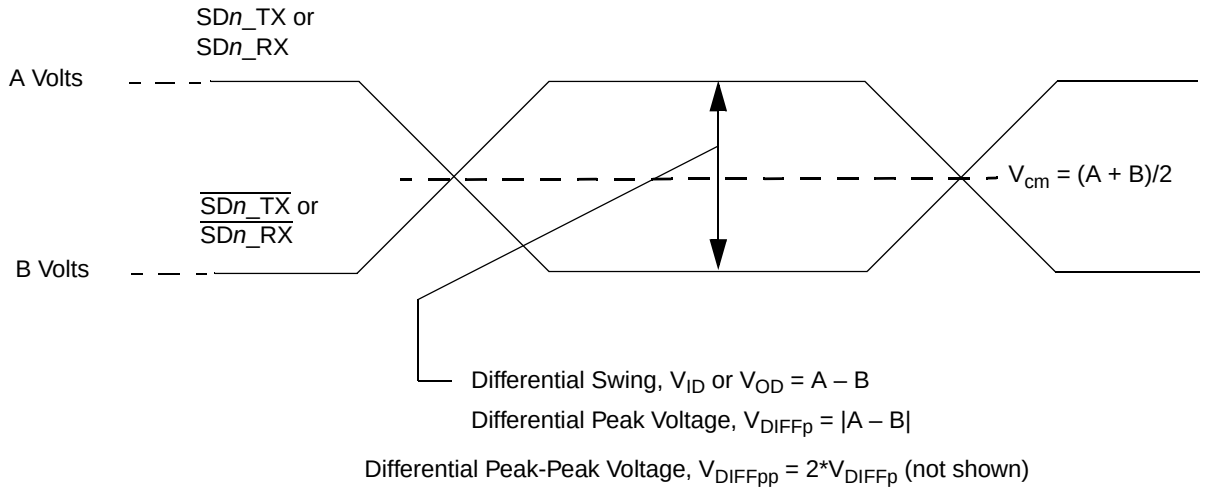



**Figure 43. Differential Voltage Definitions for Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. In this example, because the differential signaling environment is fully symmetrical, the transmitter output's differential swing ($V_{OD}$) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, $V_{OD}$ is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage ($V_{DIFFp}$) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

## 2.21.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SD1_REF_CLK and SD2_REF_CLK for the two SerDes on P1013. These can be configured to be used by PCI Express, SATA the SGMII interface. See the *P1022 QorIQ Integrated Processor Reference Manual* for configuration details.

The following sections describe the SerDes reference clock requirements and some application information.

### 2.21.2.1 SerDes Reference Clock Receiver Characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

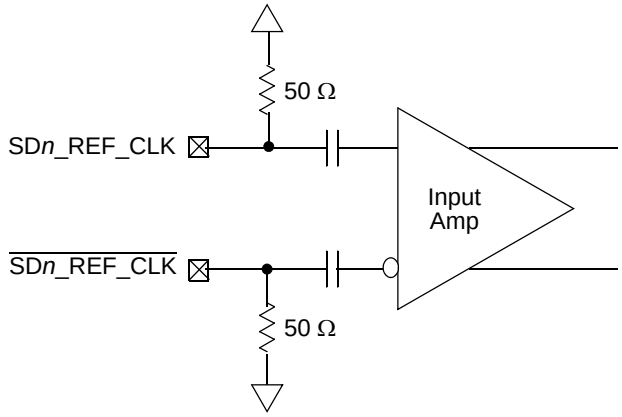



**Figure 44. Receiver of SerDes Reference Clocks**

The characteristics are as follows:

- The supply voltage requirements for $XV_{DD}$ and $XV_{DD2}$ are specified in Table 2 and Table 3.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 44. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{\_REF\_CLK}}$) has on-chip 50-Ω termination to $SV_{SS}n$ followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above $SV_{SS}n$. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to $SV_{SS}n$ DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement is as follows:
  - This requirement is described in detail in the following sections.

## 2.21.3 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the P1013 SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below:

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have

a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For **external DC-coupled** connection, as described in Section 2.21.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 45 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to $SV_{SS}n$. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage ($SV_{SS}n$). Figure 46 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- **Single-ended Mode**

— The reference clock can also be single-ended. The SD*n*_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from $V_{MIN}$ to $V_{MAX}$) with $\overline{\text{SD}n\text{\_REF\_CLK}}$ either left unconnected or tied to ground.

— The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 47 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD}n\text{\_REF\_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

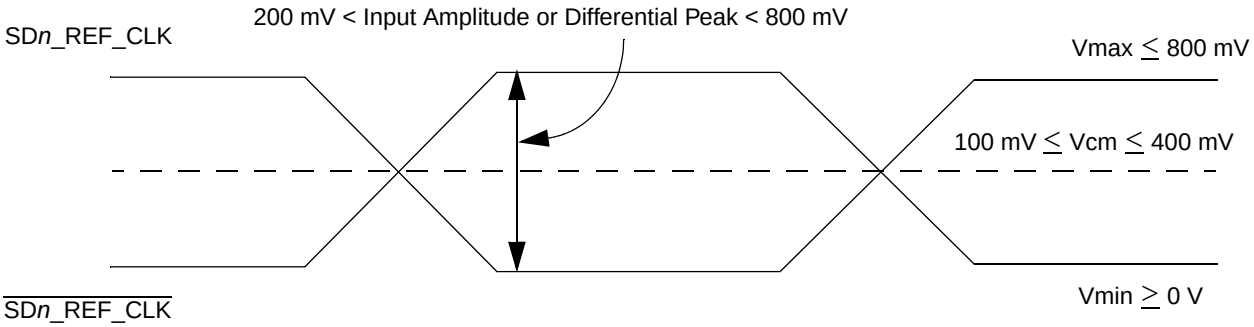



**Figure 45. Differential Reference Clock Input DC Requirements (External DC-Coupled)**

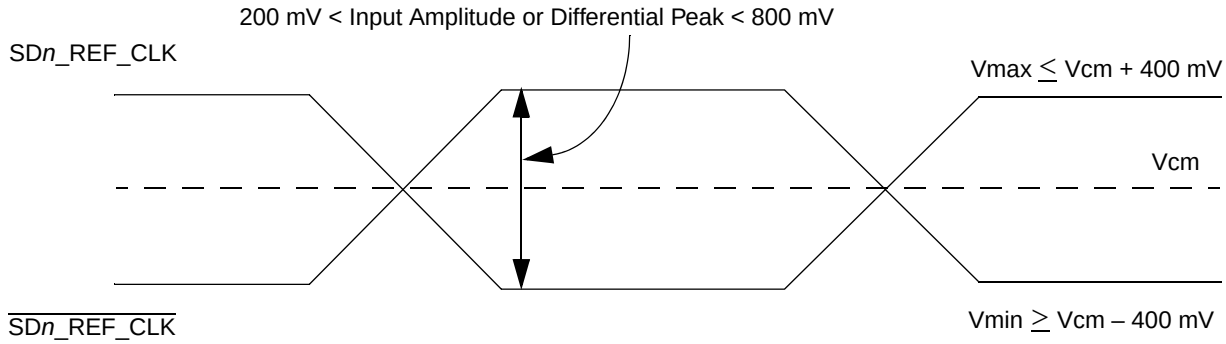



**Figure 46. Differential Reference Clock Input DC Requirements (External AC-Coupled)**

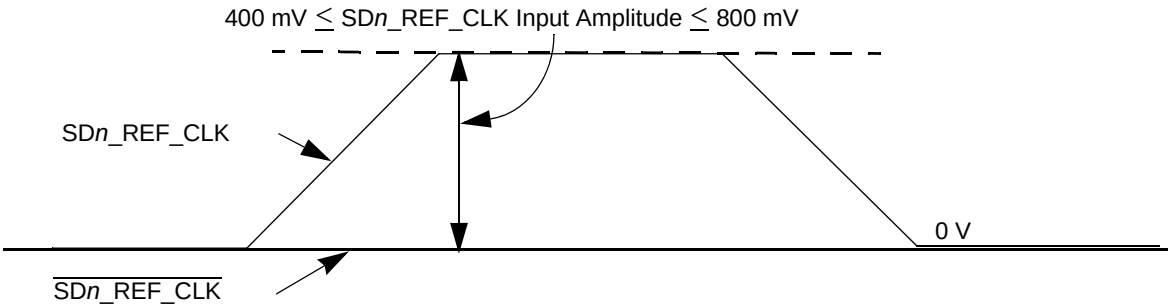



**Figure 47. Single-Ended Reference Clock Input DC Requirements**

### 2.21.3.1 AC Requirements for SerDes Reference Clocks

This table lists AC requirements for the PCI Express and SGMII SerDes reference clocks to be guaranteed by the customer's application design.

**Table 71. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ frequency range | $t_{CLK\_REF}$ | — | 100/125 | — | MHz | 1 |
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance | $t_{CLK\_TOL}$ | –350 | — | +350 | ppm | — |
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle | $t_{CLK\_DUTY}$ | 40 | 50 | 60 | % | 4 |
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak Jitter at $10^{-6}$ BER | $t_{CLK\_DJ}$ | — | — | 42 | ps | — |
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at $10^{-6}$ BER (Peak-to-peak jitter at refClk input) | $t_{CLK\_TJ}$ | — | — | 86 | ps | 2 |
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate | $t_{CLKRR}/t_{CLKFR}$ | 1 | — | 4 | V/ns | 3 |

**Note:**

1. Only 100/125 have been tested, other in between values will not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 48.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 49.

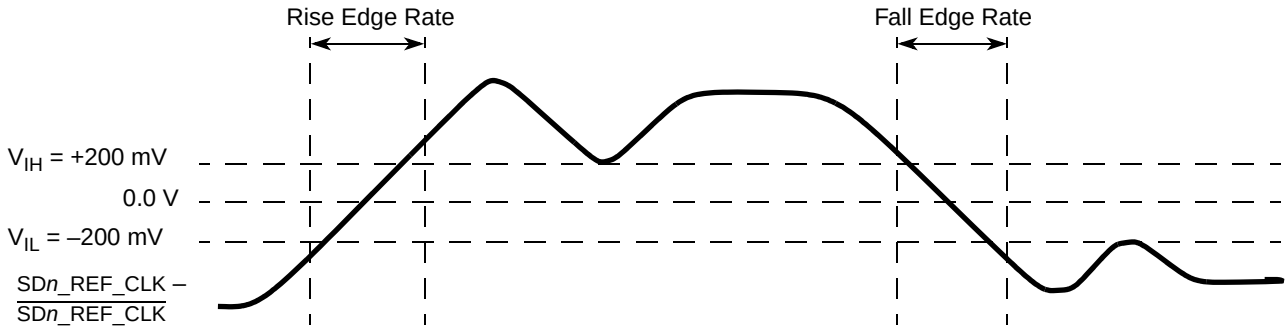



**Figure 48. Differential Measurement Points for Rise and Fall Time**

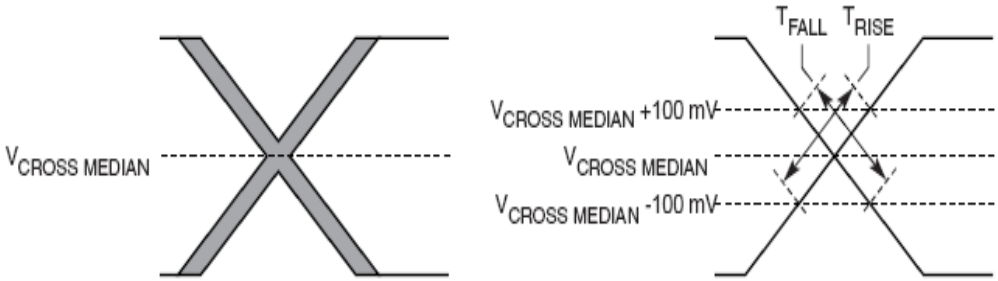



**Figure 49. Single-Ended Measurement Points for Rise and Fall Time Matching**

## 2.21.4 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

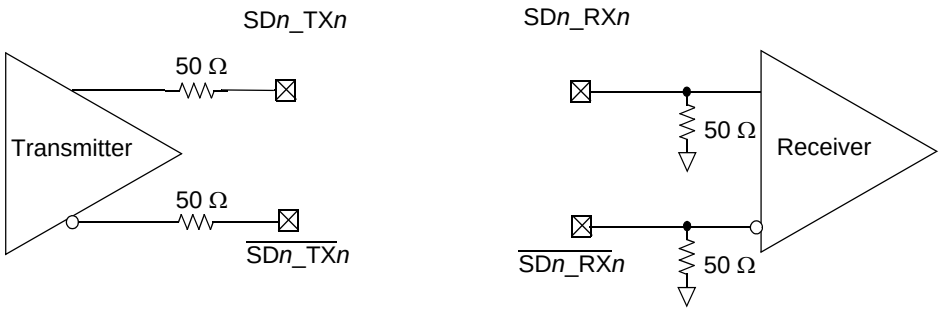



**Figure 50. SerDes Transmitter and Receiver Reference Circuits**

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, SGMII and SATA) in this document based on the application usage:

- Section 2.11.6, "SGMII Interface Electrical Characteristics"
- Section 2.22, "PCI Express"
- Section 2.23, "Serial ATA (SATA)"

Note that external AC Coupling capacitor is required for the above three serial transmission protocols per the protocol's standard requirements.

### 2.21.5 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

## 2.22 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the device.

### 2.22.1 DC Requirements for PCI Express SerDes Reference Clocks

For more information, see Section 2.21.3, "DC Level Requirement for SerDes Reference Clocks."

### 2.22.2 AC Requirements for PCI Express SerDes Reference Clocks

For more information, see Section 2.21.3.1, "AC Requirements for SerDes Reference Clocks."

#### 2.22.2.1 PCI Express Physical Layer Transmitter Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device.

##### 2.22.2.1.1 PCI Express (2.5Gb/s) Differential Transmitter (TX) Output

This table defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

**Table 72. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications**

| Symbol | Parameter | Min | Typical | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{TX\text{-}DIFFp\text{-}p}$ | Differential Peak-to-Peak Output Voltage | 800 | 1000 | 1200 | mV | $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 1. |
| $V_{TX\text{-}DE\text{-}RATIO}$ | De- Emphasized Differential Output Voltage (Ratio) | 3.0 | 3.5 | 4.0 | dB | Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 1. |
| $Z_{TX\text{-}DIFF\text{-}DC}$ | DC Differential TX Impedance | 80 | 100 | 120 | Ω | TX DC Differential mode Low Impedance |
| $Z_{TX\text{-}DC}$ | Transmitter DC Impedance | 40 | 50 | 60 | Ω | Required TX D+ as well as D- DC Impedance during all states |

**Note:**

1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 51 and measured over any 250 consecutive TX UIs.

This table defines the PCI Express (2.5Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

**Table 73. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications**

| Symbol | Parameter | Min | Typical | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| UI | Unit Interval | 399.88 | 400.00 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1. |
| $T_{TX-EYE}$ | Minimum TX Eye Width | 0.70 | — | — | UI | The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 - $T_{TX-EYE}$= 0.3 UI. See Notes 2 and 3. |
| $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.15 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3. |
| $C_{TX}$ | AC Coupling Capacitor | 75 | — | 200 | nF | All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4. |

**Note:**

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 51 and measured over any 250 consecutive TX UIs.
3. A $T_{TX-EYE}$ = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. P1013 SerDes transmitter does not have CTX built-in. An external AC Coupling capacitor is required.

## 2.22.3 PCI Express Physical Layer Receiver Specifications

This section contains the following subsections:

- Section 2.22.3.1, "PCI Express (2.5 Gb/s) Differential Receiver (RX) Input Specifications"
- Section 2.22.4, "Compliance Test and Measurement Load"

### 2.22.3.1 PCI Express (2.5 Gb/s) Differential Receiver (RX) Input Specifications

This table defines the DC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins.

**Table 74. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications**

| Symbol | Parameter | Min | Typical | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{RX-DIFFp-p}$ | Differential Input Peak-to-Peak Voltage | 235 | — | 1200 | mV | $V_{RX-DIFFp-p}$ = 2*\|$V_{RX-D+}$ – $V_{RX-D-}$\| See Note 1. |
| $Z_{RX-DIFF-DC}$ | DC Differential Input Impedance | 80 | 100 | 120 | Ω | RX DC Differential mode impedance. See Note 2 |

**Table 74. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications (continued)**

| Symbol | Parameter | Min | Typical | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $Z_{RX-DC}$ | DC Input Impedance | 40 | 50 | 60 | Ω | Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2. |
| $Z_{RX-HIGH-IMP-DC}$ | Powered Down DC Input Impedance | 50 k | — | — | Ω | Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 3. |
| $V_{RX-IDLE-DET-DIFFp-p}$ | Electrical Idle Detect Threshold | 65 | — | 235 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the Receiver |

**Note:**

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 51 should be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
3. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

This table defines the AC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

**Table 75. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications**

| Symbol | Parameter | Min | Typical | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| UI | Unit Interval | 399.88 | 400.00 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1. |
| $T_{RX-EYE}$ | Minimum Receiver Eye Width | 0.4 | — | — | UI | The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3. |
| $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.3 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 4. |

**Table 75. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications (continued)**

| Symbol | Parameter | Min | Typical | Max | Unit | Comments |
|---|---|---|---|---|---|---|

**Note:**

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 51 should be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

## 2.22.4 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 51.

**NOTE**

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

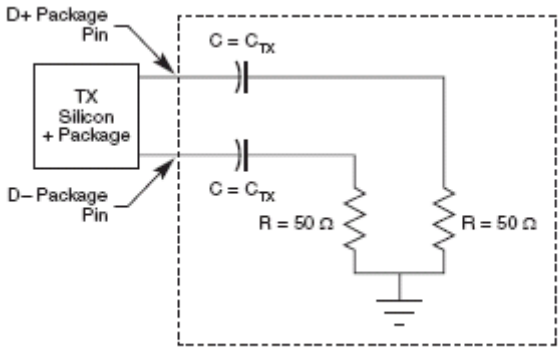



**Figure 51. Compliance Test/Measurement Load**

# 2.23 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the device. External cabled applications or long backplane applications (Gen1x & Gen2x) are not supported for the device.

## 2.23.1 AC Requirements for SATA Reference Clock

The AC requirements for the SATA reference clock are listed in the Table 76 to be guaranteed by the customer's application design.

**Table 76. SATA Reference Clock Input Requirements**

| Parameter | Symbol | Conditions | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ frequency range | $t_{CLK\_REF}$ | — | — | 100/125 | — | MHz | 1 |
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance | $t_{CLK\_TOL}$ | — | –350 | — | +350 | ppm | — |
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle | $t_{CLK\_DUTY}$ | Measured at 1.6 V | 40 | 50 | 60 | % | — |
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ cycle to cycle Clock jitter (period jitter) | $t_{CLK\_CJ}$ | Cycle to cycle at RefClk input | — | — | 100 | ps | — |
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter, phase jitter (peak-peak) | $t_{CLK\_PJ}$ | Peak-to-peak jitter at refClk input | –50 | — | +50 | ps | 2, 3 |

**Note:**

1. Only 100/125 MHz have been tested; other in-between values do not work correctly with the rest of the system.
2. In a frequency band from 150 kHz to 15 MHz at BER of $10^{-12}$
3. Total peak to peak Deterministic Jitter "DJ" should be less than or equal to 50ps.

## 2.23.2 Transmitter (TX) Output Characteristics

## 2.23.3 Gen1i/1.5G Transmitter (TX) Specifications

This table provides the DC differential transmitter (TX) output DC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

**Table 77. Gen1i/1.5G Transmitter (TX) DC Specifications**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TX Diff Output Voltage | $V_{SATA\_TXDIFF}$ | 400 | 500 | 600 | mV p-p | 1 |
| TX Differential pair impedance | $Z_{SATA\_TXDIFFIM}$ | 85 | 100 | 115 | Ω | 2 |

**Note:**

1. Terminated by 50 Ω load.
2. DC Impedance

This table provides the differential transmitter (TX) output AC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

**Table 78. Gen1i/1.5G Transmitter (TX) AC Specifications**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Channel Speed | $t_{CH\_SPEED}$ | — | 1.5 | — | Gbps | — |
| Unit Interval | $T_{UI}$ | 666.4333 | 666.6667 | 670.2333 | ps | — |
| Total Jitter Data-Data 5UI | $U_{SATA\_TXTJ5UI}$ | — | — | 0.355 | UI p-p | 1 |
| Total Jitter, Data-Data 250UI | $U_{SATA\_TXTJ250UI}$ | — | — | 0.47 | UI p-p | 1 |

**Table 78. Gen1i/1.5G Transmitter (TX) AC Specifications**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Deterministic jitter, Data-Data 5UI | $U_{SATA\_TXDJ5UI}$ | — | — | 0.175 | UI p-p | 1 |
| Deterministic jitter, Data-Data 250UI | $U_{SATA\_TXDJ250UI}$ | — | — | 0.22 | UI p-p | 1 |

**Note:**
1. Measured at Tx output pins peak to peak phase variation, Random data pattern

## 2.23.4 Gen2i/3G Transmitter (TX) Specifications

This table provides the differential transmitter (TX) output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

**Table 79. Gen 2i/3G Transmitter (TX) DC Specifications**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TX Diff Output Voltage | $V_{SATA\_TXDIFF}$ | 400 | 550 | 700 | mV p-p | 1 |
| TX Differential pair impedance | $Z_{SATA\_TXDIFFIM}$ | 85 | 100 | 115 | Ω | — |

**Note:**
1. Terminated by 50 Ω load.

This table provides the differential transmitter (TX) output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

**Table 80. Gen 2i/3G Transmitter (TX) AC Specifications**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Channel Speed | $t_{CH\_SPEED}$ | — | 3.0 | — | Gbps | — |
| Unit Interval | $T_{UI}$ | 333.2167 | 333.3333 | 335.1167 | ps | — |
| Total Jitter fC3dB=fBAUD/10 | $U_{SATA\_TXTJfB/10}$ | — | — | 0.3 | UI p-p | 1 |
| Total Jitter fC3dB=fBAUD/500 | $U_{SATA\_TXTJfB/500}$ | — | — | 0.37 | UI p-p | 1 |
| Total Jitter fC3dB=fBAUD/1667 | $U_{SATA\_TXTJfB/1667}$ | — | — | 0.55 | UI p-p | 1 |
| Deterministic jitter, fC3dB=fBAUD/10 | $U_{SATA\_TXDJfB/10}$ | — | — | 0.17 | UI p-p | 1 |
| Deterministic jitter, fC3dB=fBAUD/500 | $U_{SATA\_TXDJfB/500}$ | — | — | 0.19 | UI p-p | 1 |
| Deterministic jitter, fC3dB=fBAUD/1667 | $U_{SATA\_TXDJfB/1667}$ | — | — | 0.35 | UI p-p | 1 |

**Note:**
1. Measured at Tx output pins peak to peak phase variation, Random data pattern

## 2.23.5 Differential Receiver (RX) Input Characteristics

### 2.23.5.1 Gen1i/1.5G Receiver (RX) Specifications

This table provides the Gen1i or 1.5Gbits/s differential receiver (RX) input DC characteristics for the SATA interface.

**Table 81. Gen1i/1.5G Receiver (RX) Input DC Specifications**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Differential Input Voltage | $V_{SATA\_RXDIFF}$ | 240 | 500 | 600 | mV p-p | 1 |
| Differential RX Input impedance | $Z_{SATA\_RXSEIM}$ | 85 | 100 | 115 | Ω | — |
| OOB Signal Detection Threshold | $V_{SATA\_OOB}$ | 50 | 120 | 240 | mV p-p | — |

**Note:**
1. Voltage relative to common of either signal comprising a differential pair

This table provides the Gen1i or 1.5 Gbits/s differential receiver (RX) input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

**Table 82. Gen 1i/1.5G Receiver (RX) AC Specifications**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Unit Interval | $T_{UI}$ | 666.4333 | 666.6667 | 670.2333 | ps | — |
| Total Jitter Data-Data 5UI | $U_{SATA\_TXTJ5UI}$ | — | — | 0.43 | UI p-p | 1 |
| Total Jitter, Data-Data 250UI | $U_{SATA\_TXTJ250UI}$ | — | — | 0.60 | UI p-p | 1 |
| Deterministic jitter, Data-Data 5UI | $U_{SATA\_TXDJ5UI}$ | — | — | 0.25 | UI p-p | 1 |
| Deterministic jitter, Data-Data 250UI | $U_{SATA\_TXDJ250UI}$ | — | — | 0.35 | UI p-p | 1 |

**Note:**
1. Measured at Receiver

## 2.23.5.2 Gen2i/3G Receiver (RX) Specifications

This table provides the Gen2i or 3Gbits/s differential receiver (RX) input DC characteristics for the SATA interface.

**Table 83. Gen2i/3G Receiver (RX) Input DC Specifications**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Differential Input Voltage | $V_{SATA\_RXDIFF}$ | 275 | 500 | 750 | mV p-p | 1 |
| Differential RX Input impedance | $Z_{SATA\_RXSEIM}$ | 85 | 100 | 115 | ohm | 2 |
| OOB Signal Detection Threshold | $V_{SATA\_OOB}$ | 75 | 120 | 275 | mV p-p | 3 |

**Note:**
1. Voltage relative to common of either signal comprising a differential pair
2. DC Impedance
3. Measured at package pins of the receiver

This table provides the differential receiver (RX) input AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

**Table 84. Gen 2i/3G Receiver (RX) AC Specifications**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Unit Interval | $T_{UI}$ | 333.2167 | 333.3333 | 335.1167 | ps | — |
| Total Jitter fC3dB=fBAUD/10 | $U_{SATA\_TXTJfB/10}$ | — | — | 0.46 | UI p-p | 1 |

**Table 84. Gen 2i/3G Receiver (RX) AC Specifications (continued)**

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Total Jitter fC3dB=fBAUD/500 | $U_{SATA\_TXTJfB/500}$ | — | — | 0.60 | UI p-p | 1 |
| Total Jitter fC3dB=fBAUD/1667 | $U_{SATA\_TXTJfB/1667}$ | — | — | 0.65 | UI p-p | 1 |
| Deterministic jitter, fC3dB=fBAUD/10 | $U_{SATA\_TXDJfB/10}$ | — | — | 0.35 | UI p-p | 1 |
| Deterministic jitter, fC3dB=fBAUD/500 | $U_{SATA\_TXDJfB/500}$ | — | — | 0.42 | UI p-p | 1 |
| Deterministic jitter, fC3dB=fBAUD/1667 | $U_{SATA\_TXDJfB/1667}$ | — | — | 0.35 | UI p-p | 1 |

**Note:**
1. Measured at Receiver

## 2.24 JTAG Controller

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device. Table 86 provides the JTAG AC timing specifications as defined in Figure 52 through Figure 55.

### 2.24.1 JTAG DC Electrical Characteristics

This table provides the JTAG DC electrical characteristics.

**Table 85. JTAG DC Electrical Characteristics**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($OV_{IN}$ = 0V or $OV_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| Output high voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Output low voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**
1. Note that the min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $OV_{IN}$ values found in Table 3.
2. Note that the symbol $OV_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.

### 2.24.2 JTAG AC Timing Specifications

This table provides the JTAG AC timing specifications as defined in Figure 52 through Figure 55.

**Table 86. JTAG AC Timing Specifications [1]**

At recommended operating conditions (see Table 3).

| Parameter | Symbol[2] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | — |

**Table 86. JTAG AC Timing Specifications (continued)[1]**

At recommended operating conditions (see Table 3).

| Parameter | Symbol[2] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $\overline{\text{TRST}}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times | $t_{JTDVKH}$ | 4 | — | ns | — |
| Input hold times | $t_{JTDXKH}$ | 10 | — | ns | — |
| Output valid times | $t_{JTKLDV}$ | — | 10 | ns | 1 |
| Output hold times | $t_{JTKLDX}$ | 0 | — | ns | 1 |

**Note:**

1. All outputs are measured from the midpoint voltage of the falling edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

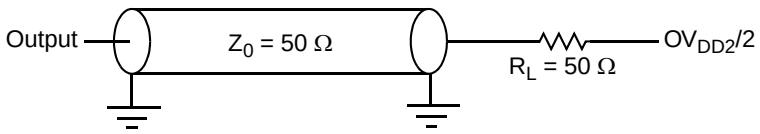



**Figure 52. AC Test Load for the JTAG Interface**

This figure provides the JTAG clock input timing diagram.

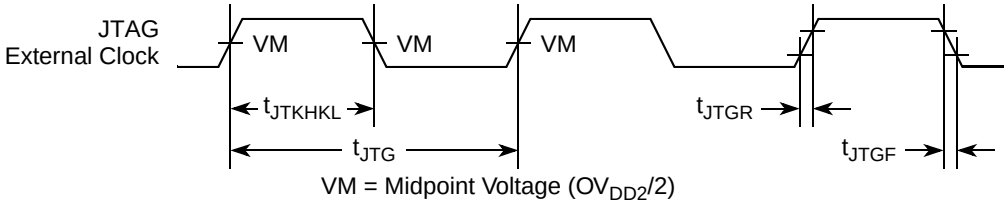



**Figure 53. JTAG Clock Input Timing Diagram**

This figure provides the $\overline{\text{TRST}}$ timing diagram.

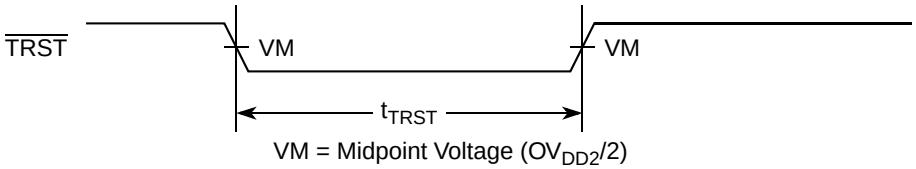
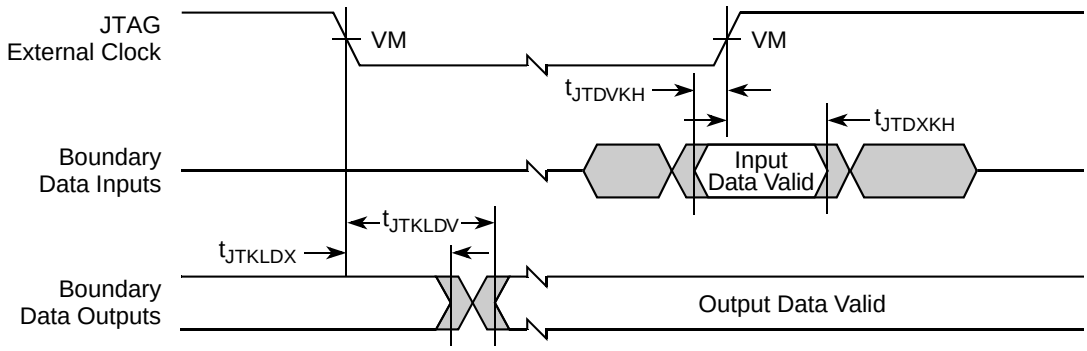



**Figure 54. $\overline{\text{TRST}}$ Timing Diagram**

This figure provides the boundary-scan timing diagram.




VM = Midpoint Voltage ($OV_{DD2}$/2)

**Figure 55. Boundary-Scan Timing Diagram**

# 3 Thermal

This section describes the thermal specifications of the device.

## 3.1 Thermal Characteristics

This table provides the package thermal characteristics.

**Table 87. Package Thermal Characteristics**

| Characteristic | JEDEC Board | Symbol | Value | Unit | Note |
|---|---|---|---|---|---|
| Junction-to-ambient Natural Convection | Single layer board (1s) | $R_{\theta JA}$ | 22 | °C/W | 1, 2 |
| Junction-to-ambient Natural Convection | Four layer board (2s2p) | $R_{\theta JA}$ | 17 | °C/W | 1, 2, 3 |
| Junction-to-ambient (at 200 ft/min) | Single layer board (1s) | $R_{\theta JA}$ | 16 | °C/W | 1, 3 |
| Junction-to-ambient (at 200 ft/min) | Four layer board (2s2p) | $R_{\theta JA}$ | 13 | °C/W | 1, 3 |
| Junction-to-board thermal | — | $R_{\theta JB}$ | 9 | °C/W | 4 |
| Junction-to-case thermal | — | $R_{\theta JC}$ | 6 | °C/W | 5 |
| Junction-to-package top thermal | Natural Convection | $\Psi_{JT}$ | 6 | °C/W | 6 |

**Note:**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

This table provides the thermal resistance with heat sink in open flow.

**Table 88. Thermal Resistance with Heat Sink in Open Flow**

| Heat Sink with Thermal Grease | Air Flow | Thermal Resistance (°C/W) |
|---|---|---|
| Wakefield 53 × 53 × 25 mm Pin Fin | Natural Convection | 10.3 |
| | 0.5 m/s | 8.3 |
| | 1 m/s | 7.4 |
| | 2 m/s | 7.0 |
| | 4 m/s | 6.7 |
| Aavid 35 × 31 × 23 mm Pin Fin | Natural Convection | 11.7 |
| | 0.5 m/s | 9.1 |
| | 1 m/s | 8.3 |
| | 2 m/s | 7.8 |
| | 4 m/s | 7.4 |
| Aavid 30 × 30 × 9.4 mm Pin Fin | Natural Convection | 13.7 |
| | 0.5 m/s | 11.2 |
| | 1 m/s | 9.9 |
| | 2 m/s | 8.8 |
| | 4 m/s | 8.1 |
| Aavid 43 × 41 × 16.5 mm Pin Fin | Natural Convection | 12.0 |
| | 0.5 m/s | 9.6 |
| | 1 m/s | 8.4 |
| | 2 m/s | 7.6 |
| | 4 m/s | 7.1 |

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. A power value of 4.5 W was used for the heat sink simulations.The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.

Simulation Details:

The 1/8 symmetry model included the following package parameters:
Four layer Substrate
Substrate solder mask thickness: 0.030 mm
Substrate metal thicknesses: 0.030mm, 0.064mm, 0.064mm, 0.030 mm
Substrate core thickness: 0.115mm, 0.100mm, 0.115 mm
Core via I.D: 0.118 mm, Core via plating 0.016 mm
Flag: trace style with ground balls under the die connected to the flag
Die Attach: 0.033 mm conductive die attach, k = 1.5 W/m K
Mold Compound: generic mold compound, k = 0.9 W/m K

# 4 Package Information

This section provides the package parameters and ordering information.

## 4.1 Package Parameters for the P1013WB-TePBGA II

The package parameters are provided in the following list. The package type is 31 mm × 31 mm, 689 plastic ball grid array (WB-TePBGA).

| | |
|---|---|
| Package outline | 31 mm × 31 mm |
| Interconnects | 689 |
| Pitch | 1.00 mm |
| Module height (typical) | 2.0 mm to 2.46 mm (Maximum) |
| Solder Balls | 3.5% Ag, 96.5% Sn |
| Ball diameter (typical) | 0.60 mm |

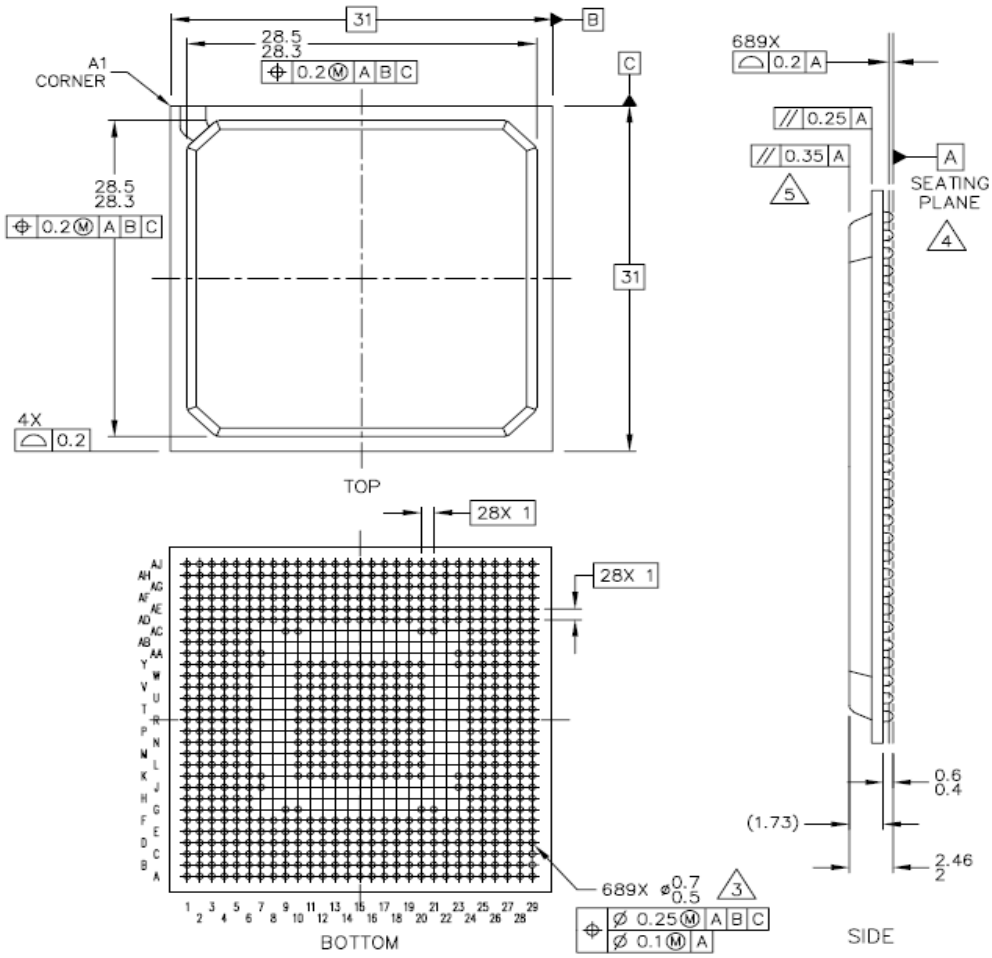



**Figure 56. P1013 Package**

**Notes:**

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M-1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

## 4.2 Ordering Information

This table provides the Freescale part numbering nomenclature for the P1013. Each part number also contains a revision code which refers to the die mask revision number.

**Table 89. P1013 Part Numbers**

| P | 1 | 01 | 3 | q | t | e | n | dd | r |
|---|---|---|---|---|---|---|---|---|---|
| **Generation** | **Platform** | **Number of Cores** | **Derivative** | **Qualification Status** | **Temperature Range** | **Encryption** | **Package Type** | **CPU/CCB/DDR Frequency (MHz)** | **Silicon Revision** |
| P = 45nm | 1–5 | 01 = Single Core<br>02 = Dual Core | 0–9 | P = Prototype<br>N = Qualified to industrial tier<br>S= Special | S = Std temp<br>X = Ext temp | E = SEC present<br>N = SEC Not present | 2 = TEPBGAII<br>Pbfree | EF=600/400/667<br>HF=800/400/667<br>LF=1067/533/667 | A = 1.0<br>B = 1.1 |

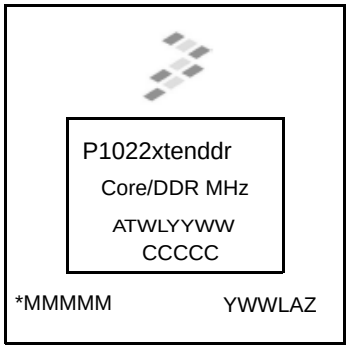
**Note:**

1. See Section 4, “Package Information,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

3) Extended Temperature range only supported for DDR3

## 4.3 Part Marking

Parts are marked as the example shown in this figure.




WB-TePBGA

**Notes:**

P1022xtenddr is the orderable part number
*MMMMM is the mask number
YWWLAZ is the assembly traceability code.
CCCCC is the country code
ATWLYYWW is the standard assembly, test, year, and work week codes.

**Figure 57. Part Marking for WB-TePBGA II Device**

# 5 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

The following documents are required for a complete description of the device and are needed to design properly with the part:

- *P1022 QorIQ Integrated Processor Reference Manual* (document number P1022RM)
- *e500 PowerPC Core Family Reference Manua*l (E500CORERM)

# 6 Revision History

This table summarizes a revision history for this document.

**Table 90. Revision History**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 0 | 11/2011 | Initial release |

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