

Crystal Clock Oscillator Module Evaluation Board Manual for NBX Family in 6 Pin CLCC 5mm X 7mm Package

Generic Evaluation Board: XOCLCC6EVB
Devices: NBXxxxx
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Description

This Evaluation Board manual (XOCLCC6EVB/D) is a guide for using the XOCLCC6EVB Evaluation Board to provide a convenient platform for quickly evaluating, characterizing and verify performance and operation of a device in the NBXxxxx family of Clock Oscillator Modules packaged in the 6 pin CLCC, 5mm by 7 mm, CASE 848AB (see Appendix).

This family of devices offer an internal crystal and PLL IC. This Evaluation Board Manual and Evaluation Board should be used in conjunction with a specific device data sheet, which contains full technical details on specifications and operation.

An NBXxxxx Clock Oscillator Module device may be directly solder mounted onto the available evaluation board footprint; or multiple units may be inserted and tested by solder mounting a separate insertion socket (P/N AM0393-320R from SER Electronics) onto the available footprint.

Evaluation Board Features

- 6 pin CLCC solder footprint for solder mounting a device or test socket
 - Incorporates jumper headers to conveniently and manually control the levels for the 'Output Enable' (Pin 1) and 'Frequency Select' (Pin 2) pins.
 - Enable single or split-power supply operation.
- LVPECL differential outputs are accessed via SMA connectors offering different output load configurations.

Evaluation Board Manual Document Features

- Information on the XOCLCC6EVB Evaluation Board
- Appropriate Lab Setup and Procedures
- Board build Bill of Materials (Table 5)
- Evaluation Board schematic (Figure 7)
- Evaluation Board Lamination Stackup (Figure 8)
- Evaluation Board Fabrication Notes
- Appendix:
 - MECHANICAL CASE OUTLINE
 - GENERIC MARKING DIAGRAM
 - SOLDERING FOOTPRINT

What measurements can you expect to make?

With this evaluation board, the following measurements could be performed in single-ended or differential modes of operation.

- DC Characteristics
- Frequency Performance
- Output Rise and Fall Time
- Phase Noise
- Jitter

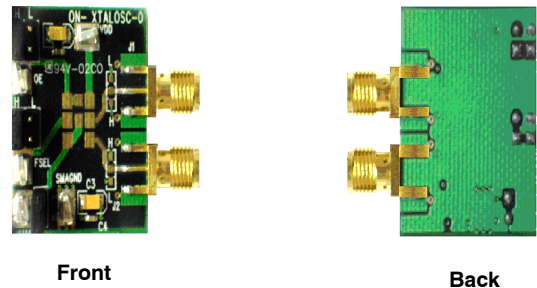


Figure 1. Evaluation Board Images (Front and Back)

XOCLCC6EVB

EVALUATION BOARD MAP

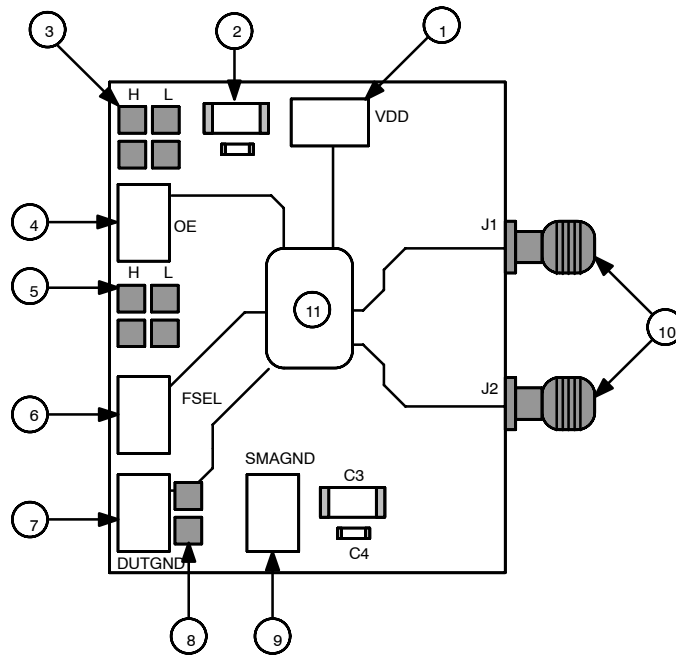
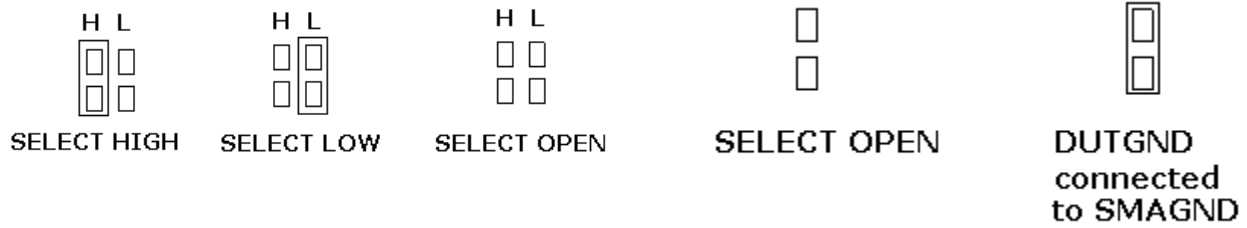


Figure 2. Evaluation Board Layout

Table 1. EVALUATION BOARD MAP DESCRIPTION

Number	Description
1	DUT PIN6 Positive supply connection anvil and test point.
2	Decoupling capacitors. See BOM/board schematic for details.
3	DUT PIN 4 OE jumper header to force logic HIGH (Active) or LOW (Outputs Disabled to High Impedance). Leave open or use jumper to force HIGH (OE Pin defaults HIGH when left floating) (see Figure 3 below)
4	OE connection anvil and test point.
5	DUT PIN 2 FSEL jumper header to force logic HIGH or LOW. FSEL Pin defaults HIGH when left floating. (see Figure 3 below)
6	FSEL connection anvil and test point.
7	Device ground (DUTGND) connection anvil and test point.
8	DUT PIN 3 GND/SMAGND jumper header to force DUTGND connection to SMAGND. (see Figure 3 below)
9	SMAGND connection anvil and test point.
10	SMA outputs (CLK/ $\overline{\text{CLK}}$).
11	6 pin CLCC 5mmX7mm DUT (Device under test).

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Evaluation Board Jumper Headers on OE (Pin 4), FSEL (Pin 5)

Evaluation Board Jumper Header on DUTGND (Pin 3)

Figure 3. Select Positions for Evaluation Board Jumper Headers on OE (Pin 4), FSEL (Pin 5), and DUTGND (Pin 3)

TIME DOMAIN MEASUREMENTS

Equipment

Table 2 indicates the recommended equipment for making characterization and performance measurements.

Table 2. BASIC EQUIPMENT

Description	Example Equipment	Qty
Power Supply with 4 outputs	HP6624A or similar	1
Real-Time Oscilloscope	DPO70804 or similar	1
Matched High Speed Cables with SMA Connectors	Storm, Semflex, or similar	2
Power supply cables		4

Setup

The following steps should be followed for proper equipment setup.

Step 1: Connect Power (split power supply mode)

Three power levels must be provided to the board: V_{DD} , DUTGND, and SMAGND via the test point anvils at the edges of the board. Bypass capacitors are installed from V_{DD} to SMAGND and DUTGND to SMAGND near the test points (see BOM). Devices may be tested in one of three supply modes (see Table 3):

A). Single (Positive) +3.3 V Setup

No offset to supplies or output levels

B). Split 3.3 V Setup

Offsets the V_{DD} , DUTGND, and output voltage levels by -1.3 V and avoids an additional, separate V_{TT} supply and allows a direct connection to test equipment such as an oscilloscope or counter with 50Ω impedance to GND inputs. $SMAGND = V_{TT} = V_{DD} - 2.0$ V = 0.0 V.

C). Single (Negative) -3.3 V Setup

Offsets the V_{DD} , DUTGND, and output voltage levels by -3.3 V

Table 3. XOCLCC6EVB POWER SUPPLY CONNECTION VOLTAGES

A). Single Positive +3.3 V Setup	B). Split 3.3 V Setup	C). Single Negative -3.3 V Setup
$V_{DD} = 3.3$ V	$V_{DD} = 2.0$ V	$V_{DD} = 0$ V
$V_{TT} = V_{DD} - 2.0$ V = 1.3 V	$V_{TT} = V_{DD} - 2.0$ V = SMAGND = 0 V	$V_{TT} = V_{DD} - 2.0$ V = -2.0 V SMAGND = $V_{DD} = 0$ V
DUTGND = SMAGND = 0 V	DUTGND = -1.3 V	DUTGND = -3.3 V

NOTE: SMAGND is the SMA cable shield reference for the inputs and outputs only, not to be confused with the device ground pin (DUTGND).

Step 2: Connect Output Signals

Table 4 gives a list of specific LOGIC Levels and their appropriate Power Supply and Typical Lab Setup conditions

LVPECL: The LVPECL outputs have standard, open emitter outputs and must be externally DC loaded and AC terminated. A split power supply technique takes advantage of terminating the LVPECL outputs into 50Ω of an oscilloscope or a frequency counter. Since $V_{TT} = V_{DD} - 2$ V, offsetting V_{DD} to $+2.0$ V yields $V_{TT} = 0$ V or Ground (SMAGND). The V_{TT} terminal connects to the isolated SMAGND connector ground plane, and is not to be confused with the device ground pin (DUTGND). (See Application Note AN8020/D for details on ECL termination).

CML: For CML lab setup and test, operation with negative supply voltage is recommended to enable the 50Ω internal impedance in the oscilloscope to be used as a termination of the CML signals ($V_{DD} = 0.0$ V, SMAGND = 0.0 V, and DUTGND = -3.3 V (See Application Note AN8173/D for details on CML termination).

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LVDS: Driver termination is a 100 Ω resistor across the differential lines located at the receiver input.

Table 4. TYPICAL LAB SETUP

LOGIC Levels	Power Supply	Typical Lab Setup
LVPECL	Split 3.3 V	See Figure 4
CML	Single -3.3 V	See Figure 5
LVDS	Single 3.3 V	See Figure 6

Step 3: Configure FSEL and OE

The FSEL and OE control pins can be controlled from an external source via the appropriate test point, or via the jumper headers located on the evaluation board, as indicated in Figures 2 and 7. Refer to the specific device datasheet for details on the proper settings for these pins.

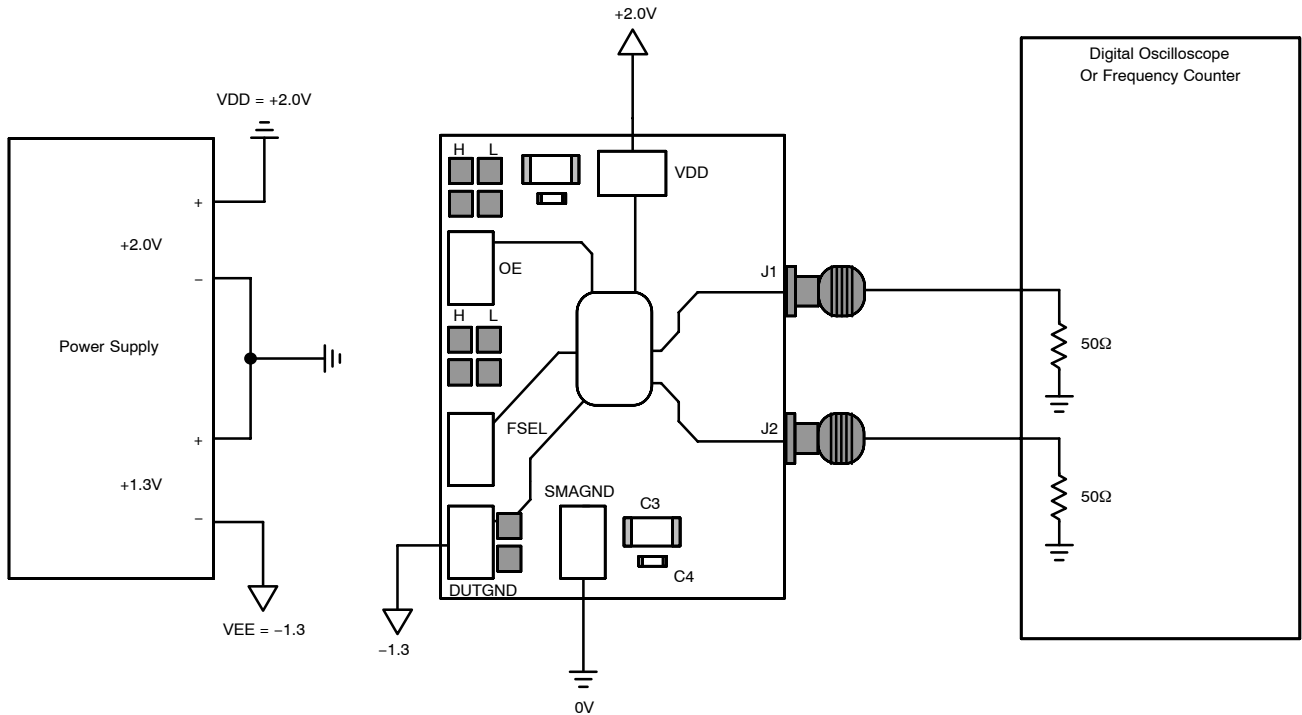
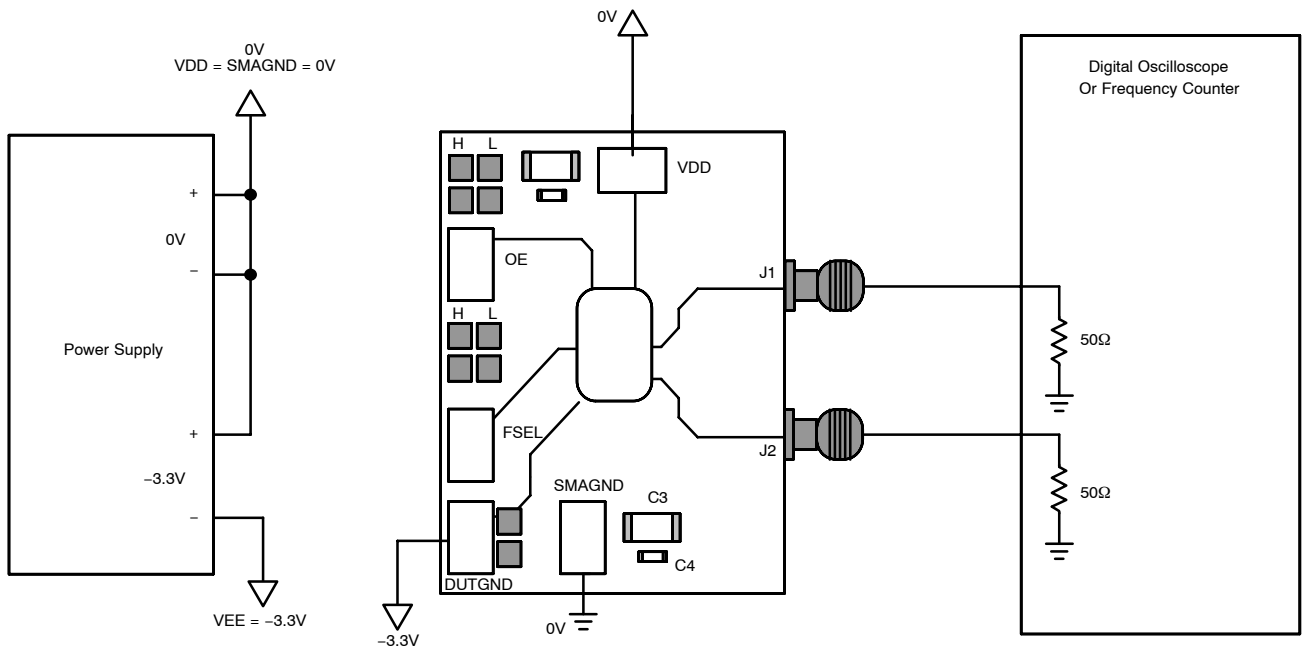


Figure 4. Split Power Supply Lab Setup for LVPECL Outputs (DO NOT JUMPER DUTGND and SMAGND)

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Note: For CML outputs, 50 Ω to V_{DD} is needed for proper termination. See application note AND8173/D.

Figure 5. Typical Lab Setup for CML Outputs (DO NOT JUMPER DUTGND and SMAGND)

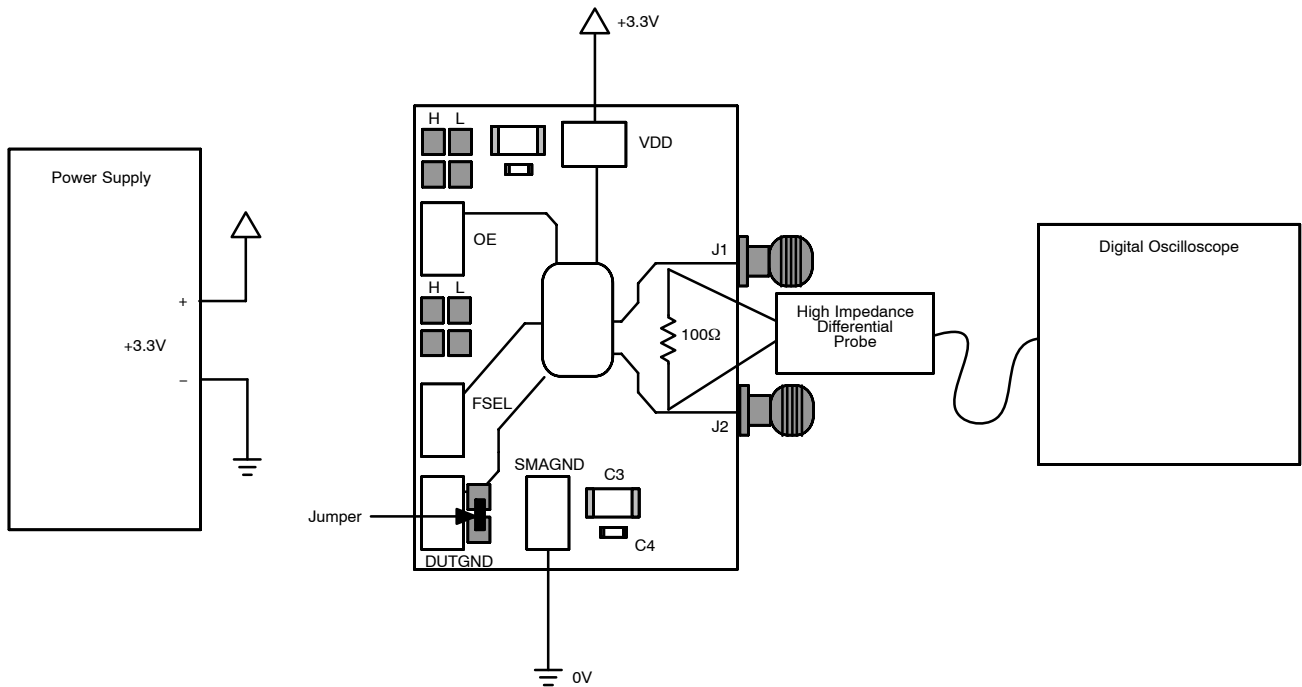


Figure 6. Typical Lab Setup for LVDS Outputs (JUMPER DUTGND and SMAGND)

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Table 5. XOCLCC6EVB EVALUATION BOARD BILL OF MATERIALS

Components	Manufacturer	Description	Part Number	Qty
Jumper Header	Berg	100 mil	In House	5
Test Point	Keystone	Anvil SMD	5016	3
Shunt				
Connector	Johanson	SMA, Edge Mount	142-0711-821	2
Capacitor	Kemet	22 μ F, 10%	T491D22K016AS, Case C or D	2
Capacitor	Kemet	0.1 μ F, 10%	C0603C104K4RAC	2
Socket (Not Supplied)	SER Electronics	Socket - 6-Lead 5mm x 7mm	AM0393-320R	1

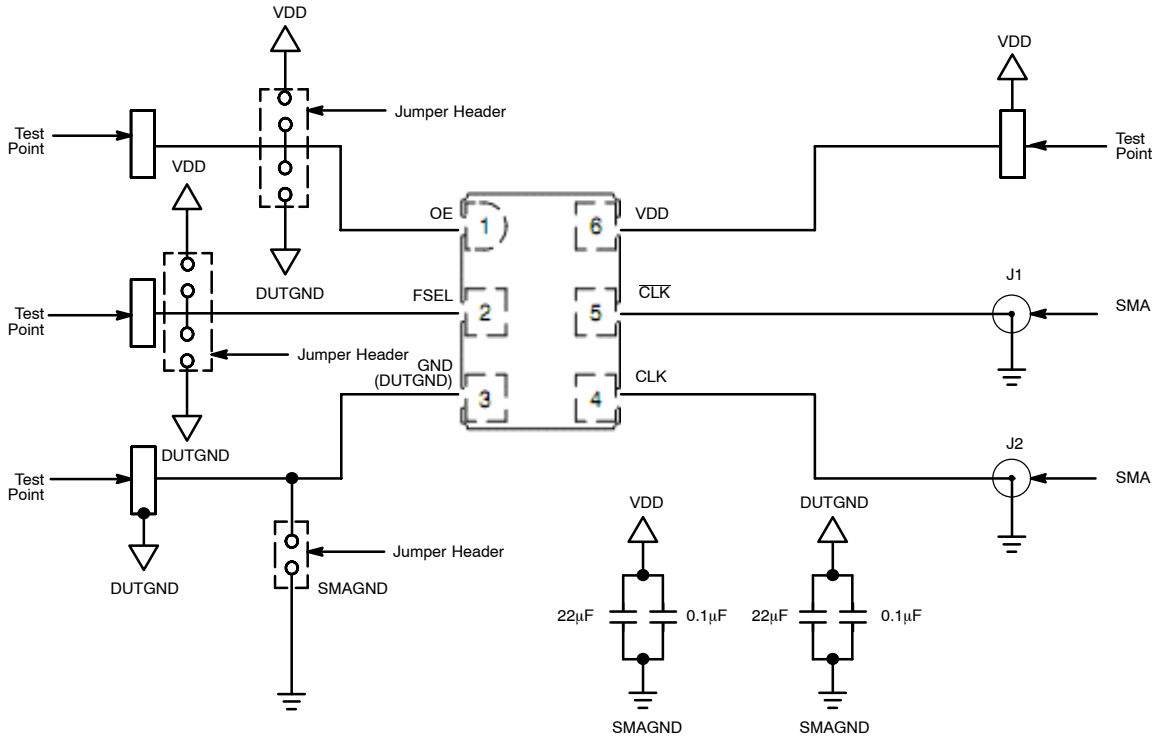


Figure 7. XOCLCC6EVB Evaluation Board Schematic

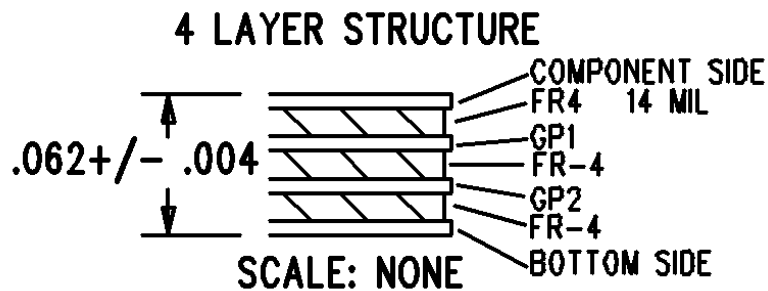


Figure 8. XOCLCC6EVB Evaluation Board Layer Lamination Stackup

XOCLCC6EVB

Evaluation Board Fabrication Notes

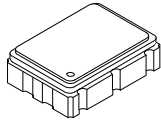
1. MATERIAL: FR-4
2. FINISHED COPPER TO BE 1oz. (0.0014) EXTERNAL LAYERS
3. MINIMUM COPPER PLATING 0.0007" THICK FOR PLATED THRU HOLES ANNULAR RING TO BE 0.0002" MINIMUM
4. LPI SOLDERMASK GREEN
5. SOLDERMASK REGISTRATION ± 0.002 " N/A
6. ALL EXPOSED COPPER AREAS TO BE GOLD PLATED (0.000030" GOLD OVER 0.000100" NICKEL)
7. IF SPECIFIED, SILKSCREEN IS TO BE WHITE EPOXY INK.
8. HOLE DIAMETER TOLERANCE IS ± 0.002 ", MAXIMUM LAYER TO LAYER MISREGISTRATION SHALL BE 0.004", MEASUREMENT METHOD MUST COMPLY WITH MIL-P-55110D, FIGURE 1.
9. FINISHED CONDUCTOR WIDTH SHALL NOT VARY MORE THAN ± 0.001 " FROM ARTWORK MASTER
50 Ω TRACES ARE 0.024" WIDE.
10. WARP AND TWIST OF SINGLE SIDED BOARDS SHALL NOT EXCEED 0.002" PER INCH, WARP AND TWIST OF MULTI-LAYER BOARDS SHALL NOT EXCEED 0.010" PER INCH.
11. ALL DIMENTIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES. XX ± 0.010 " XXX ± 0.004 ".
12. ACCEPTABILITY REQUIREMENTS PER IPC-A-600E.
13. DRAWING IS VIEWED FROM COMPONENT OR PRIMARY SIDE.
14. THIS IS A 4 LAYER BOARD.
15. ALL HOLES ARE PLATED THRU UNLESS OTHERWISE SPECIFIED.
16. DRILL SIZE UNITS ARE THOUSANDTHS OF AN INCH.
17. TRIM ALL SILKSCREEN WHICH FLOWS OVER VIA HOLES OR SMD PADS.
18. BREAK ALL SHARP EDGES, PCB EDGES SHOULD BE SMOOTH AND EVEN.

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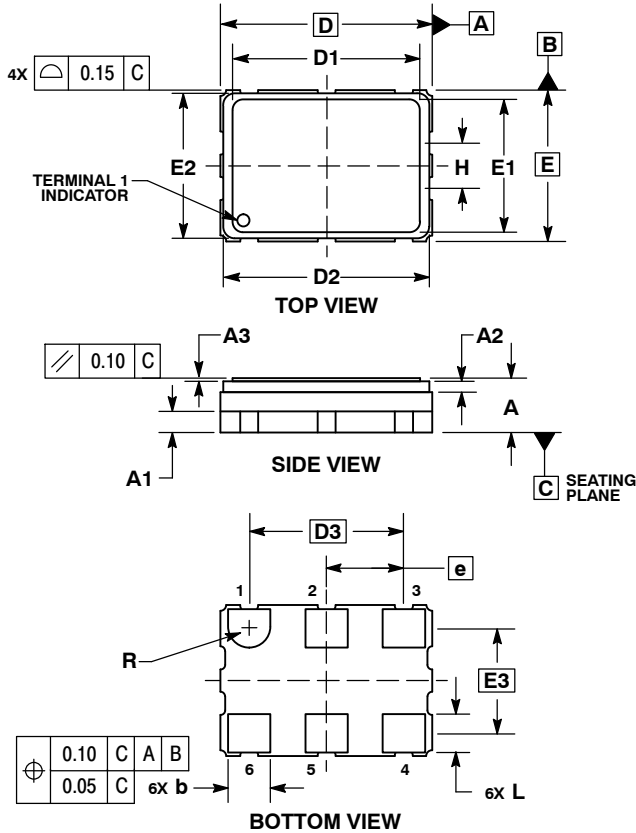
Appendix:

MECHANICAL CASE OUTLINE
 GENERIC MARKING DIAGRAM
 SOLDERING FOOTPRINT

PACKAGE DIMENSIONS



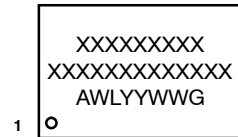
6 PIN CLCC, 7x5, 2.54P
 CASE 848AB-01
 ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.70	1.80	1.90
A1	0.70 REF		
A2	0.36 REF		
A3	0.08	0.10	0.12
b	1.30	1.40	1.50
D	7.00 BSC		
D1	6.17	6.20	6.23
D2	6.66	6.81	6.96
D3	5.08 BSC		
E	5.00 BSC		
E1	4.37	4.40	4.43
E2	4.65	4.80	4.95
E3	3.49 BSC		
e	2.54 BSC		
H	1.80 REF		
L	1.17	1.27	1.37
R	0.70 REF		

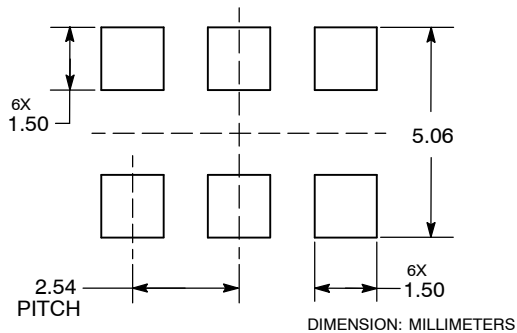
GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package


*This information is generic. Please refer to device data sheet for actual part marking.
 Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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