# Ultralow Power, Low Distortion Fully Differential ADC Driver

Data Sheet

# ADA4940-1/ADA4940-2

## FEATURES

- Small signal bandwidth: 260 MHz
- Ultralow power 1.25mA
- Extremely low harmonic distortion
  - −122 dB THD at 50 kHz
  - −96 dB THD at 1 MHz
- Low input voltage noise: 3.9 nV/√Hz
- 0.35 mV maximum offset voltage
- Differential-to-differential or single-to-differential operation
- Balanced outputs
- Settling time to 0.1%: 34 ns
- Rail-to-rail output: $-V_S$ + 0.1 V to $+V_S$ − 0.1 V
- Adjustable output common-mode voltage
- Flexible power supplies: 3 V to 7 V
- Disable pin to reduce power consumption

## APPLICATIONS

- Low power PulSAR®/SAR ADC drivers
- Single-ended-to-differential conversion
- Differential buffers
- Line drivers
- Medical imaging
- Industrial process controls
- Portable electronics

## GENERAL DESCRIPTION

The ADA4940-1/ADA4940-2 are low noise, low distortion fully differential amplifiers with very low power consumption. They are an ideal choice for driving low power, high resolution, high performance SAR and sigma-delta (Σ-Δ) analog-to-digital converters (ADCs) with resolutions up to 16 bits from dc to 1 MHz on only 1.25 mA of quiescent current. The adjustable level of the output common-mode voltage allows the ADA4940-1/ADA4940-2 to match the input common-mode voltage of multiple ADCs. The internal common-mode feedback loop provides exceptional output balance, as well as suppression of even-order harmonic distortion products.

With the ADA4940-1/ADA4940-2, differential gain configurations are easily realized with a simple external feedback network of four resistors determining the closed-loop gain of the amplifier. The ADA4940-1/ADA4940-2 are fabricated using Analog Devices, Inc., SiGe complementary bipolar process, enabling them to achieve very low levels of distortion with an input voltage noise of only 3.9 nV/√Hz. The low dc offset and excellent dynamic performance of the ADA4940-1/ADA4940-2 make them well suited for a variety of data acquisition and signal processing applications.

## FUNCTIONAL BLOCK DIAGRAMS

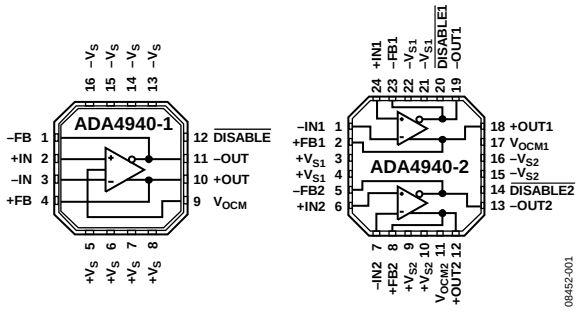


*Figure 1.*

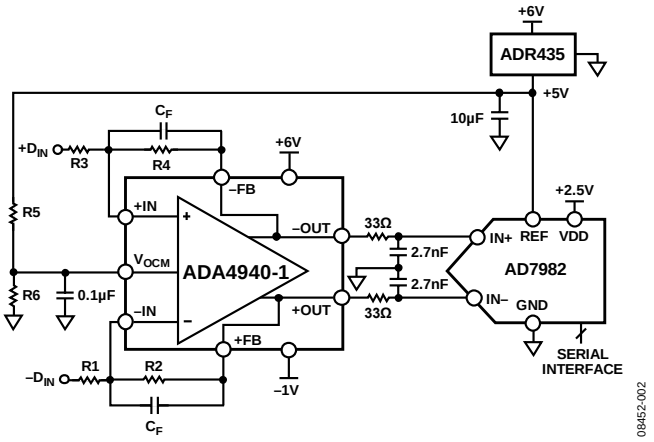


*Figure 2. ADA4940-1 Driving the AD7982 ADC*

The ADA4940-1 is available in a Pb-free, 3 mm × 3 mm, 16-lead LFCSP. The ADA4940-2 is available in a Pb-free, 4 mm × 4 mm, 24-lead LFCSP. The pinout is optimized to facilitate printed circuit board (PCB) layout and minimize distortion. The ADA4940-1/ADA4940-2 are specified to operate over the −40°C to +125°C temperature range.

**Table 1. Similar Products to the ADA4940-1/ADA4940-2**

| Product | Power (mA) | Bandwidth (MHz) | Slew Rate (V/µs) | Noise (nV/√Hz) |
|---|---|---|---|---|
| AD8137 | 3 | 110 | 450 | 8.25 |
| ADA4932-x | 9 | 560 | 2800 | 3.6 |
| ADA4941-1 | 2.2 | 31 | 22 | 5.1 |

**Table 2. Complementary Products to the ADA4940-1/ADA4940-2**

| Product | Power (mW) | Throughput (MSPS) | Resolution (Bits) | SNR (dB) |
|---|---|---|---|---|
| AD7982 | 7.0 | 1 | 18 | 98 |
| AD7984 | 10.5 | 1.333 | 18 | 96.5 |
| AD7621 | 65 | 3 | 16 | 88 |
| AD7623 | 45 | 1.333 | 16 | 88 |

**Rev. A**



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**10/11—Revision 0: Initial Version**

# SPECIFICATIONS

## $V_S$ = ±2.5 V (OR +5 V)

$V_{OCM}$ = 0 V (or +2.5 V), $R_F$ = $R_G$ = 1 kΩ, $R_{L, dm}$ = 1 kΩ, $T_A$ = 25°C, unless otherwise noted. $T_{MIN}$ to $T_{MAX}$ = −40°C to +125°C. (See Figure 53 for the definition of terms.)

### *+$D_{IN}$ or −$D_{IN}$ to $V_{OUT, dm}$ Performance*

**Table 3.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT, dm}$ = 0.1 V p-p, G = 1 | | 260 | | MHz |
| | $V_{OUT, dm}$ = 0.1 V p-p, G = 2 | | 220 | | MHz |
| | $V_{OUT, dm}$ = 0.1 V p-p, G = 5 | | 75 | | MHz |
| −3 dB Large Signal Bandwidth | $V_{OUT, dm}$ = 2 V p-p, G = 1 | | 25 | | MHz |
| | $V_{OUT, dm}$ = 2 V p-p, G = 2 | | 22 | | MHz |
| | $V_{OUT, dm}$ = 2 V p-p, G = 5 | | 19 | | MHz |
| Bandwidth for 0.1 dB Flatness | $V_{OUT, dm}$ = 2 V p-p, G = 1 and G = 2 | | 14.5 | | MHz |
| Slew Rate | $V_{OUT, dm}$ = 2 V step | | 95 | | V/µs |
| Settling Time to 0.1% | $V_{OUT, dm}$ = 2 V step | | 34 | | ns |
| Overdrive Recovery Time | G = 2, $V_{IN, dm}$ = 6 V p-p, triangle wave | | 86 | | ns |
| NOISE/HARMONIC PERFORMANCE | | | | | |
| HD2/HD3 | $V_{OUT, dm}$ = 2 V p-p, $f_C$ = 50 kHz | | −123/−126 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, $f_C$ = 50 kHz, G = 2 | | −117/−124 | | |
| | $V_{OUT, dm}$ = 2 V p-p, $f_C$ = 1 MHz | | −102/−96 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, $f_C$ = 1 MHz, G = 2 | | −92/−100 | | |
| IMD3 | $V_{OUT, dm}$ = 2 V p-p, $f_1$ = 1.9 MHz, $f_2$ = 2.1 MHz | | −99 | | dBc |
| Input Voltage Noise | f = 100 kHz | | 3.9 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 0.81 | | pA/√Hz |
| Crosstalk | $V_{OUT, dm}$ = 2 V p-p, $f_C$ = 1 MHz | | −110 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Offset Voltage | $V_{IP}$ = $V_{IN}$ = $V_{OCM}$ = 0 V | −0.35 | ±0.06 | +0.35 | mV |
| Input Offset Voltage Drift | $T_{MIN}$ to $T_{MAX}$ | | 1.2 | | µV/°C |
| Input Bias Current | | −1.6 | −1.1 | | µA |
| Input Bias Current Drift | $T_{MIN}$ to $T_{MAX}$ | | −4.5 | | nA/°C |
| Input Offset Current | | −200 | ±50 | +200 | nA |
| Input Common-Mode Voltage Range | | | $-V_S$ − 0.2 to $+V_S$ − 1.2 | | V |
| Input Resistance | Differential | | 33 | | kΩ |
| | Common mode | | 50 | | MΩ |
| Input Capacitance | | | 1 | | pF |
| Common-Mode Rejection Ratio (CMRR) | $\Delta V_{OS, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V dc | | −96 | −86 | dB |
| Open-Loop Gain | | 91 | 99 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | Each single-ended output | $-V_S$ + 0.1 to $+V_S$ − 0.1 | $-V_S$ + 0.07 to $+V_S$ − 0.07 | | V |
| Linear Output Current | f = 1 MHz, $R_{L, dm}$ = 22 Ω, SFDR = −60 dBc | | 46 | | mA peak |
| Output Balance Error | f = 1 MHz, $\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$ | | −65 | −60 | dB |

### $V_{OCM}$ to $V_{OUT, cm}$ Performance

**Table 4.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OCM}$ DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT, cm}$ = 0.1 V p-p | | 36 | | MHz |
| −3 dB Large Signal Bandwidth | $V_{OUT, cm}$ = 1 V p-p | | 29 | | MHz |
| Slew Rate | $V_{OUT, cm}$ = 1 V p-p | | 52 | | V/µs |
| Input Voltage Noise | f = 100 kHz | | 83 | | nV/√Hz |
| Gain | $\Delta V_{OUT, cm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±1 V | 0.99 | 1 | 1.01 | V/V |
| $V_{OCM}$ CHARACTERISTICS | | | | | |
| Input Common-Mode Voltage Range | | | $-V_S + 0.8$ to $+V_S - 0.7$ | | V |
| Input Resistance | | | 250 | | kΩ |
| Offset Voltage | $V_{OS, cm} = V_{OUT, cm} - V_{OCM}$; $V_{IP} = V_{IN} = V_{OCM}$ = 0 V | −6 | ±1 | +6 | mV |
| Input Offset Voltage Drift | $T_{MIN}$ to $T_{MAX}$ | | 20 | | µV/°C |
| Input Bias Current | | −7 | +4 | +7 | µA |
| CMRR | $\Delta V_{OS, dm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±1 V, measured using 1% resistors | | −100 | −86 | dB |

### General Performance

**Table 5.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| Operating Range | | 3 | | 7 | V |
| Quiescent Current per Amplifier | Enabled | 1.16 | 1.25 | 1.32 | mA |
| | $T_{MIN}$ to $T_{MAX}$ | | 4.25 | | µA/°C |
| | Disabled | | 13.5 | 25 | µA |
| +PSRR | $\Delta V_{OS, dm}/\Delta V_S$, $\Delta V_S$ = 1 V p-p | | −90 | −80 | dB |
| −PSRR | $\Delta V_{OS, dm}/\Delta V_S$, $\Delta V_S$ = 1 V p-p | | −96 | −80 | dB |
| DISABLE ($\overline{\text{DISABLE}}$ PIN) | | | | | |
| $\overline{\text{DISABLE}}$ Input Voltage | Disabled | | ≤($-V_S$ + 1) | | V |
| | Enabled | | ≥($-V_S$ + 1.8) | | V |
| Turn-Off Time | | | 10 | | µs |
| Turn-On Time | | | 0.6 | | µs |
| $\overline{\text{DISABLE}}$ Pin Bias Current per Amplifier | | | | | |
| Enabled | $\overline{\text{DISABLE}}$ = +2.5 V | | 2 | 5 | µA |
| Disabled | $\overline{\text{DISABLE}}$ = −2.5 V | −10 | −5 | | µA |
| OPERATING TEMPERATURE RANGE | | −40 | | +125 | °C |

## $V_S$ = 3 V

$V_{OCM}$ = 1.5 V, $R_F$ = $R_G$ = 1 kΩ, $R_{L, dm}$ = 1 kΩ, $T_A$ = 25°C, unless otherwise noted. $T_{MIN}$ to $T_{MAX}$ = −40°C to +125°C. (See Figure 53 for the definition of terms.)

### *+$D_{IN}$ or −$D_{IN}$ to $V_{OUT, dm}$ Performance*

**Table 6.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT, dm}$ = 0.1 V p-p | | 240 | | MHz |
| | $V_{OUT, dm}$ = 0.1 V p-p, G = 2 | | 220 | | MHz |
| | $V_{OUT, dm}$ = 0.1 V p-p, G = 5 | | 70 | | MHz |
| −3 dB Large Signal Bandwidth | $V_{OUT, dm}$ = 2 V p-p | | 24 | | MHz |
| | $V_{OUT, dm}$ = 2 V p-p, G = 2 | | 20 | | MHz |
| | $V_{OUT, dm}$ = 2 V p-p, G = 5 | | 17 | | MHz |
| Bandwidth for 0.1 dB Flatness | $V_{OUT, dm}$ = 0.1 V p-p | | 14 | | MHz |
| Slew Rate | $V_{OUT, dm}$ = 2 V step | | 90 | | V/µs |
| Settling Time to 0.1% | $V_{OUT, dm}$ = 2 V step | | 37 | | ns |
| Overdrive Recovery Time | G = 2, $V_{IN, dm}$ = 3.6 V p-p, triangle wave | | 85 | | ns |
| NOISE/HARMONIC PERFORMANCE | | | | | |
| HD2/HD3 | $V_{OUT, dm}$ = 2 V p-p, $f_C$ = 50 kHz (HD2/HD3) | | −115/−121 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, $f_C$ = 1 MHz (HD2/HD3) | | −104/−96 | | dBc |
| IMD3 | $V_{OUT, dm}$ = 2 V p-p, $f_1$ = 1.9 MHz, $f_2$ = 2.1 MHz | | −98 | | dBc |
| Input Voltage Noise | f = 100 kHz | | 3.9 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 0.84 | | pA/√Hz |
| Crosstalk | $V_{OUT, dm}$ = 2 V p-p, $f_C$ = 1 MHz | | −110 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Offset Voltage | $V_{IP}$ = $V_{IN}$ = $V_{OCM}$ = 1.5 V | −0.4 | ±0.06 | +0.4 | mV |
| Input Offset Voltage Drift | $T_{MIN}$ to $T_{MAX}$ | | 1.2 | | µV/°C |
| Input Bias Current | | −1.6 | −1.1 | | µA |
| Input Bias Current Drift | $T_{MIN}$ to $T_{MAX}$ | | −4.5 | | nA/°C |
| Input Offset Current | | −200 | ±50 | +200 | nA |
| Input Common-Mode Voltage Range | | | $-V_S$ − 0.2 to $+V_S$ − 1.2 | | V |
| Input Resistance | Differential | | 33 | | kΩ |
| | Common mode | | 50 | | MΩ |
| Input Capacitance | | | 1 | | pF |
| Common-Mode Rejection Ratio (CMRR) | $\Delta V_{OS, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±0.25 V dc | | −96 | −86 | dB |
| Open-Loop Gain | | 91 | 99 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | Each single-ended output | $-V_S$ + 0.08 to $+V_S$ − 0.08 | $-V_S$ + 0.04 to $+V_S$ − 0.04 | | V |
| Linear Output Current | f = 1 MHz, $R_{L, dm}$ = 26 Ω, SFDR = −60 dBc | | 38 | | mA peak |
| Output Balance Error | f = 1 MHz, $\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$ | | −65 | −60 | dB |

### $V_{OCM}$ to $V_{OUT, cm}$ Performance

**Table 7.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OCM}$ DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT, cm}$ = 0.1 V p-p | | 36 | | MHz |
| −3 dB Large Signal Bandwidth | $V_{OUT, cm}$ = 1 V p-p | | 26 | | MHz |
| Slew Rate | $V_{OUT, cm}$ = 1 V p-p | | 48 | | V/µs |
| Input Voltage Noise | f = 100 kHz | | 92 | | nV/√Hz |
| Gain | $\Delta V_{OUT, cm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±0.25 V | 0.99 | 1 | 1.01 | V/V |
| $V_{OCM}$ CHARACTERISTICS | | | | | |
| Input Common-Mode Voltage Range | | | $-V_S + 0.8$ to $+V_S - 0.7$ | | V |
| Input Resistance | | | 250 | | kΩ |
| Offset Voltage | $V_{OS, cm} = V_{OUT, cm} - V_{OCM}$; $V_{IP} = V_{IN} = V_{OCM}$ = 1.5 V | −7 | ±1 | +7 | mV |
| Input Offset Voltage Drift | $T_{MIN}$ to $T_{MAX}$ | | 20 | | µV/°C |
| Input Bias Current | | −5 | +1 | +5 | µA |
| CMRR | $\Delta V_{OS,dm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±0.25 V, measured using 1% resistors | | −100 | −80 | dB |

### General Performance

**Table 8.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| Operating Range | | 3 | | 7 | V |
| Quiescent Current per Amplifier | Enabled | 1.08 | 1.18 | 1.28 | mA |
| | $T_{MIN}$ to $T_{MAX}$ | | 4.25 | | µA/°C |
| | Disabled | | 7 | 20 | µA |
| +PSRR | $\Delta V_{OS, dm}/\Delta V_S$, $\Delta V_S$ = 0.25 V p-p | | −90 | −80 | dB |
| −PSRR | $\Delta V_{OS, dm}/\Delta V_S$, $\Delta V_S$ = 0.25 V p-p | | −96 | −80 | dB |
| DISABLE ($\overline{\text{DISABLE}}$ PIN) | | | | | |
| $\overline{\text{DISABLE}}$ Input Voltage | Disabled | | $\leq(-V_S + 1)$ | | V |
| | Enabled | | $\geq(-V_S + 1.8)$ | | V |
| Turn-Off Time | | | 16 | | µs |
| Turn-On Time | | | 0.6 | | µs |
| $\overline{\text{DISABLE}}$ Pin Bias Current per Amplifier | | | | | |
| Enabled | $\overline{\text{DISABLE}}$ = +3 V | | 0.3 | 1 | µA |
| Disabled | $\overline{\text{DISABLE}}$ = 0 V | −6 | −3 | | µA |
| OPERATING TEMPERATURE RANGE | | −40 | | +125 | °C |

# ABSOLUTE MAXIMUM RATINGS

**Table 9.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 8 V |
| $V_{OCM}$ | $\pm V_S$ |
| Differential Input Voltage | 1.2 V |
| Operating Temperature Range | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Junction Temperature | 150°C |
| ESD | |
| Field Induced Charged Device Model (FICDM) | 1250 V |
| Human Body Model (HBM) | 2000 V |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, $\theta_{JA}$ is specified for the device soldered on a circuit board in still air.

**Table 10.**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 16-Lead LFCSP (Single)/4-Layer Board | 91.3 | °C/W |
| 24-Lead LFCSP (Dual)/4-Layer Board | 65.1 | °C/W |

## MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4940-1/ADA4940-2 packages is limited by the associated rise in junction temperature ($T_J$) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4940-1/ADA4940-2. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package ($P_D$) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power dissipation is the voltage between the supply pins ($\pm V_S$) times the quiescent current ($I_S$). The load current consists of the differential and common-mode currents flowing to the load, as well as currents flowing through the external feedback networks and internal common-mode feedback loop. The internal resistor tap used in the common-mode feedback loop places a negligible differential load on the output. RMS voltages and currents should be considered when dealing with ac signals.

Airflow reduces $\theta_{JA}$. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the $\theta_{JA}$.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 16-lead LFCSP ($\theta_{JA}$ = 91.3°C/W, single) and 24-lead LFCSP ($\theta_{JA}$ = 65.1°C/W, dual) packages on a JEDEC standard 4-layer board. $\theta_{JA}$ values are approximations.

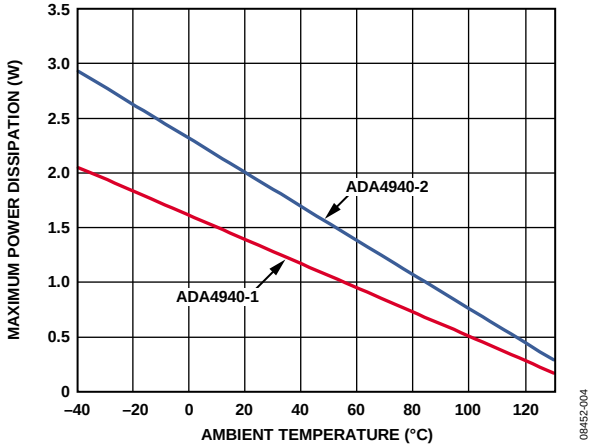


*Figure 3. Maximum Safe Power Dissipation vs. Ambient Temperature*

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

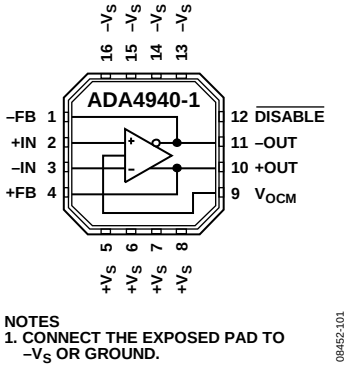


*Figure 4. ADA4940-1 Pin Configuration (16-Lead LFCSP)*

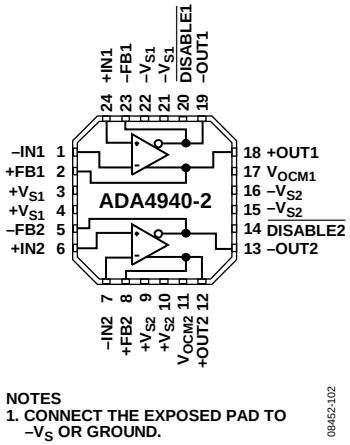


*Figure 5. ADA4940-2 Pin Configuration (24-Lead LFCSP)*

**Table 11. ADA4940-1 Pin Function Descriptions (16-Lead LFCSP)**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | −FB | Negative Output for Feedback Component Connection. |
| 2 | +IN | Positive Input Summing Node. |
| 3 | −IN | Negative Input Summing Node. |
| 4 | +FB | Positive Output for Feedback Component Connection. |
| 5 to 8 | $+V_S$ | Positive Supply Voltage. |
| 9 | $V_{OCM}$ | Output Common-Mode Voltage. |
| 10 | +OUT | Positive Output for Load Connection. |
| 11 | −OUT | Negative Output for Load Connection. |
| 12 | $\overline{\text{DISABLE}}$ | Disable Pin. |
| 13 to 16 | $-V_S$ | Negative Supply Voltage. |
| | Exposed paddle (EPAD) | Connect the exposed pad to $-V_S$ or ground. |

**Table 12. ADA4940-2 Pin Function Descriptions (24-Lead LFCSP)**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | −IN1 | Negative Input Summing Node 1. |
| 2 | +FB1 | Positive Output Feedback Pin 1. |
| 3, 4 | $+V_{S1}$ | Positive Supply Voltage 1. |
| 5 | −FB2 | Negative Output Feedback Pin 2. |
| 6 | +IN2 | Positive Input Summing Node 2. |
| 7 | −IN2 | Negative Input Summing Node 2. |
| 8 | +FB2 | Positive Output Feedback Pin 2. |
| 9, 10 | $+V_{S2}$ | Positive Supply Voltage 2. |
| 11 | $V_{OCM2}$ | Output Common-Mode Voltage 2. |
| 12 | +OUT2 | Positive Output 2. |
| 13 | −OUT2 | Negative Output 2. |
| 14 | $\overline{\text{DISABLE2}}$ | Disable Pin 2. |
| 15, 16 | $-V_{S2}$ | Negative Supply Voltage 2. |
| 17 | $V_{OCM1}$ | Output Common-Mode Voltage 1. |
| 18 | +OUT1 | Positive Output 1. |
| 19 | −OUT1 | Negative Output 1. |
| 20 | $\overline{\text{DISABLE1}}$ | Disable Pin 1. |
| 21, 22 | $-V_{S1}$ | Negative Supply Voltage 1. |
| 23 | −FB1 | Negative Output Feedback Pin 1. |
| 24 | +IN1 | Positive Input Summing Node 1. |
| | Exposed paddle (EPAD) | Connect the exposed pad to $-V_S$ or ground. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $V_S$ = ±2.5 V, G = 1, $R_F$ = $R_G$ = 1 kΩ, $R_T$ = 52.3 Ω (when used), $R_L$ = 1 kΩ, unless otherwise noted. See Figure 51 and Figure 52 for the test circuits.

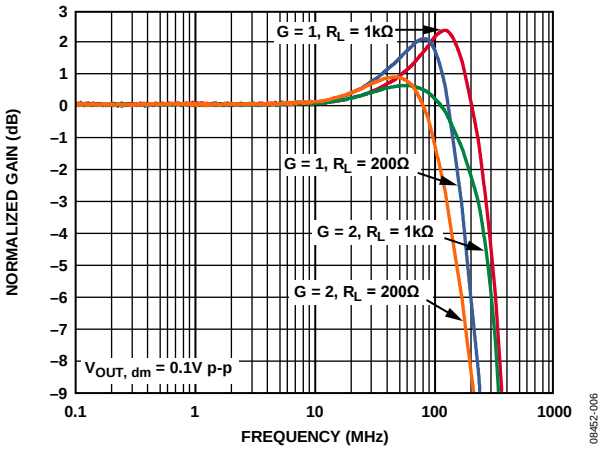


Figure 6. Small Signal Frequency Response for Various Gains and Loads

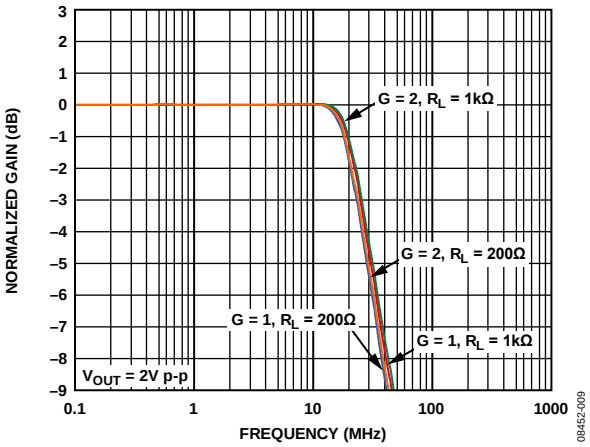


Figure 9. Large Signal Frequency Response for Various Gains and Loads

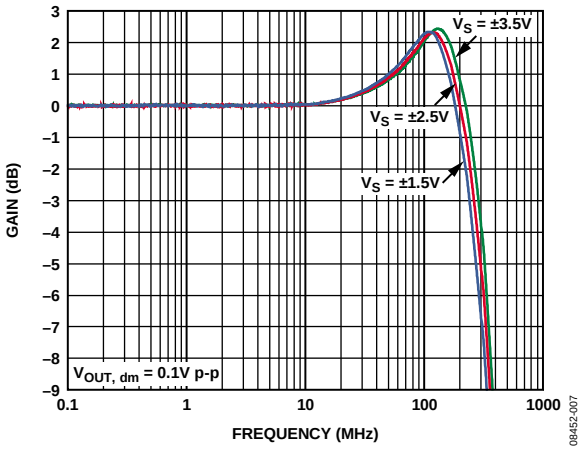


Figure 7. Small Signal Frequency Response for Various Supplies

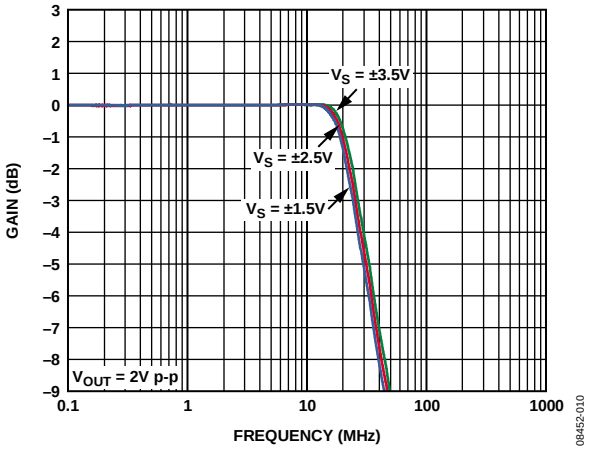


Figure 10. Large Signal Frequency Response for Various Supplies

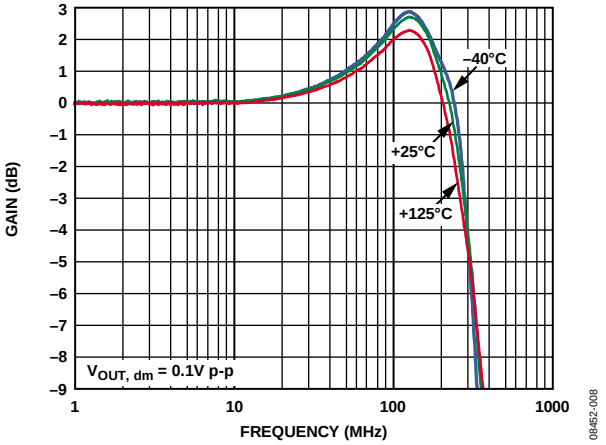


Figure 8. Small Signal Frequency Response for Various Temperatures

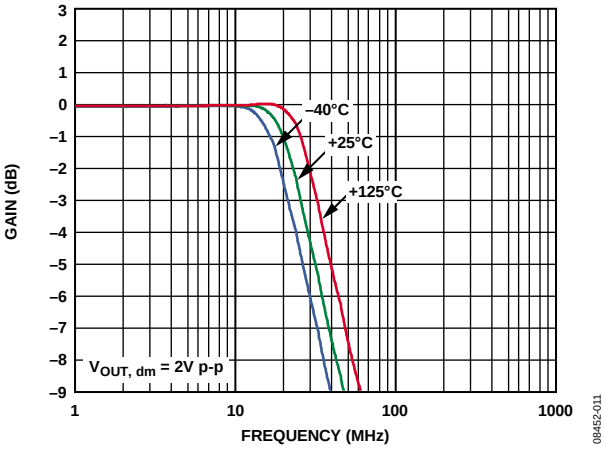


Figure 11. Large Signal Frequency Response for Various Temperatures

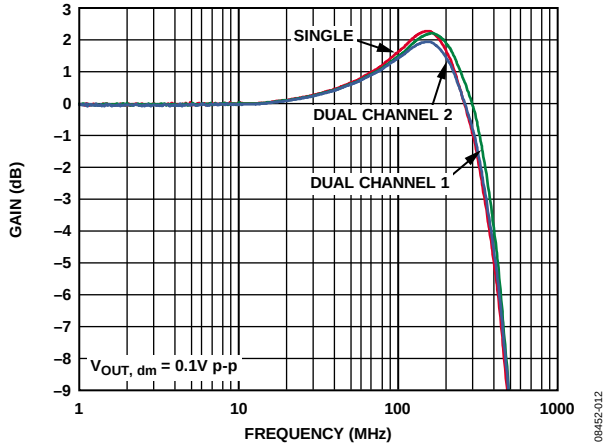


Figure 12. Small Signal Frequency Response for Various Packages

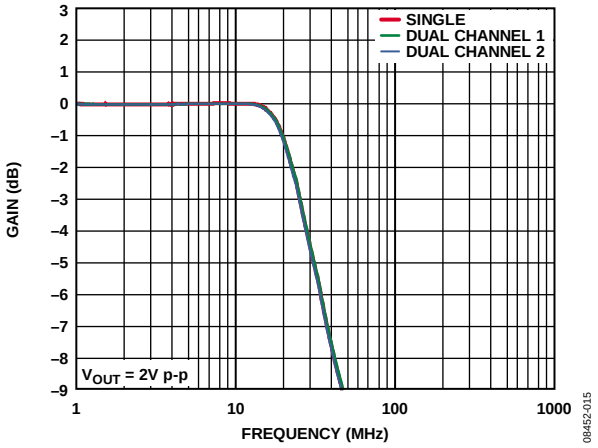


Figure 15. Large Signal Frequency Response for Various Packages

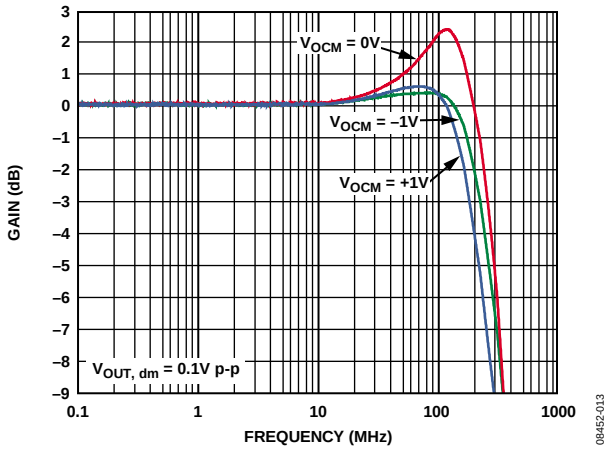


Figure 13. Small Signal Frequency Response at Various $V_{OCM}$ Levels

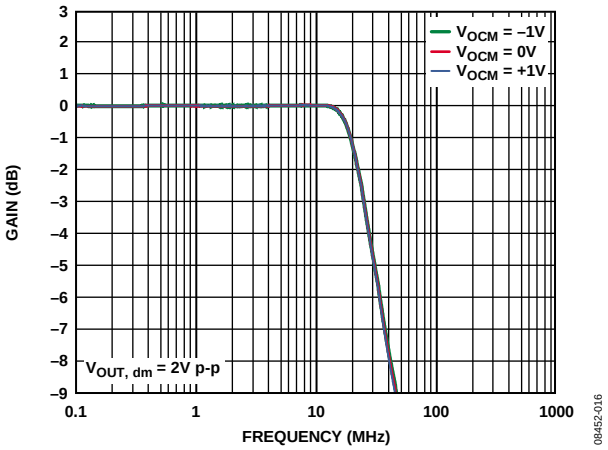


Figure 16. Large Signal Frequency Response at Various $V_{OCM}$ Levels

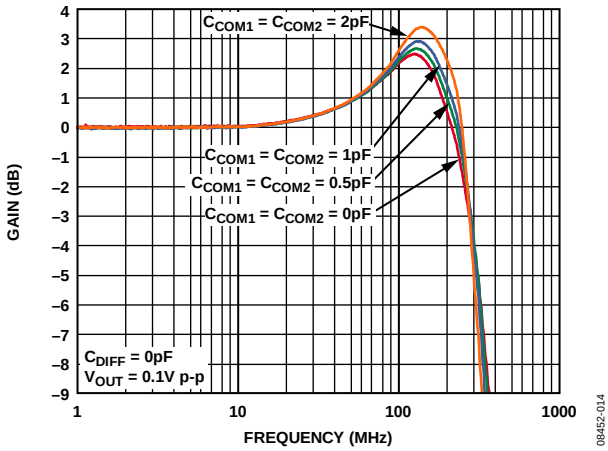


Figure 14. Small Signal Frequency Response for Various Capacitive Loads

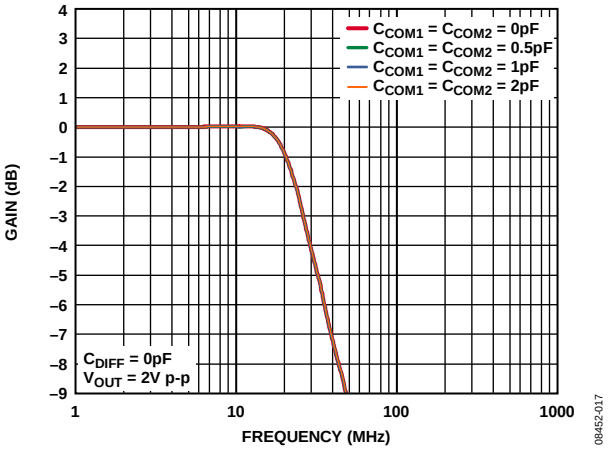


Figure 17. Large Signal Frequency Response for Various Capacitive Loads

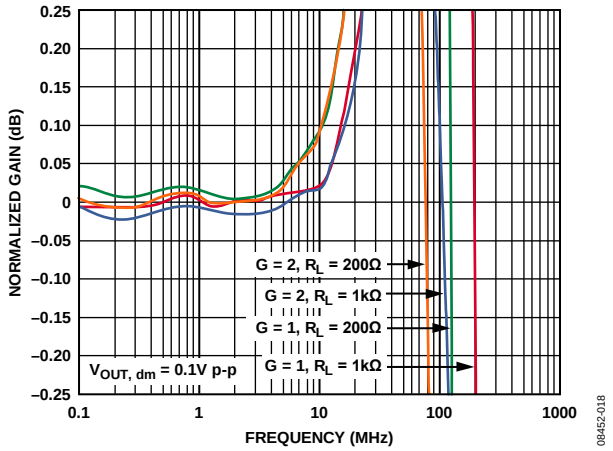


Figure 18. 0.1 dB Flatness Small Signal Frequency Response for Various Gains and Loads

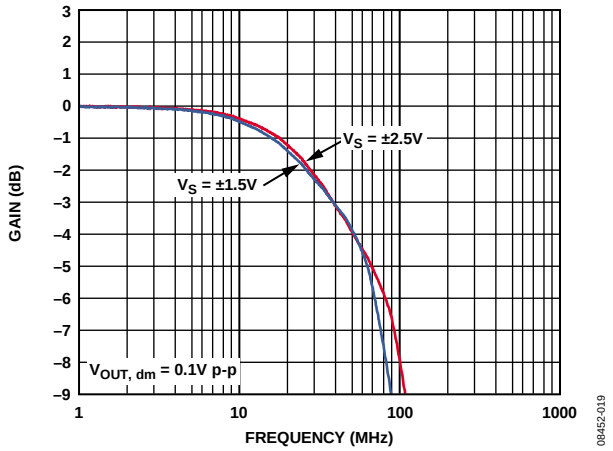


Figure 19. $V_{OCM}$ Small Signal Frequency Response for Various Supplies

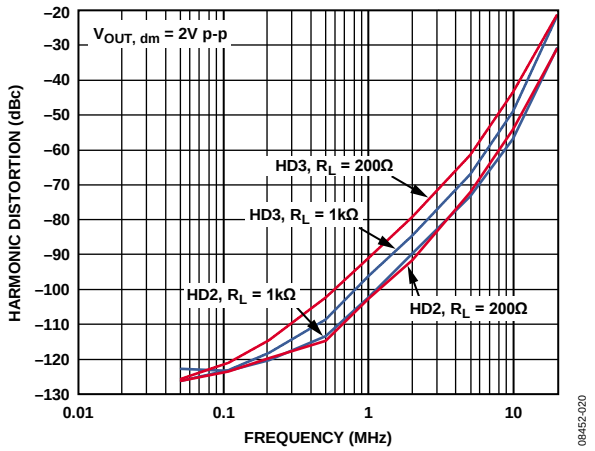


Figure 20. Harmonic Distortion vs. Frequency for Various Loads

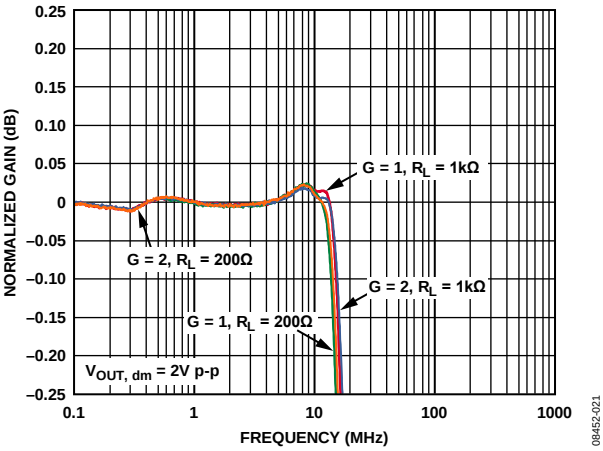


Figure 21. 0.1 dB Flatness Large Signal Frequency Response for Various Gains and Loads

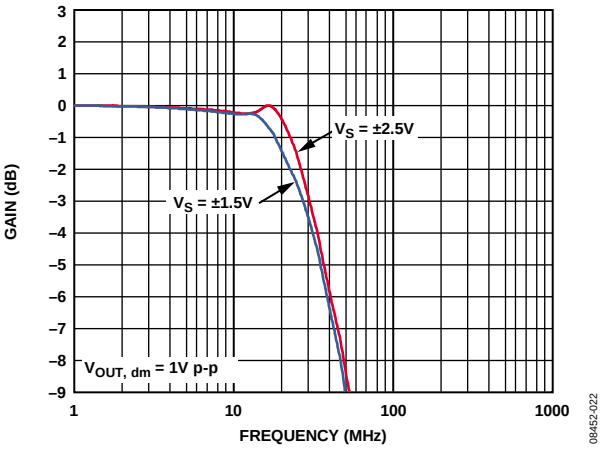


Figure 22. $V_{OCM}$ Large Signal Frequency Response for Various Supplies

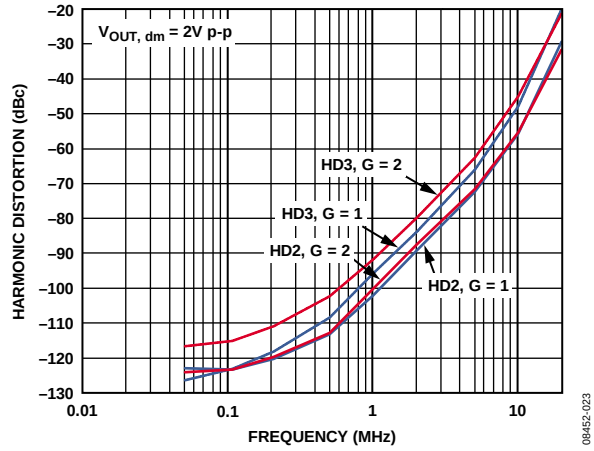


Figure 23. Harmonic Distortion vs. Frequency for Various Gains

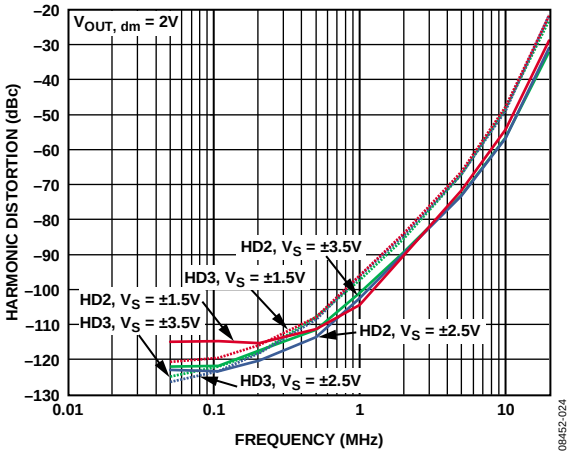


Figure 24. Harmonic Distortion vs. Frequency for Various Supplies

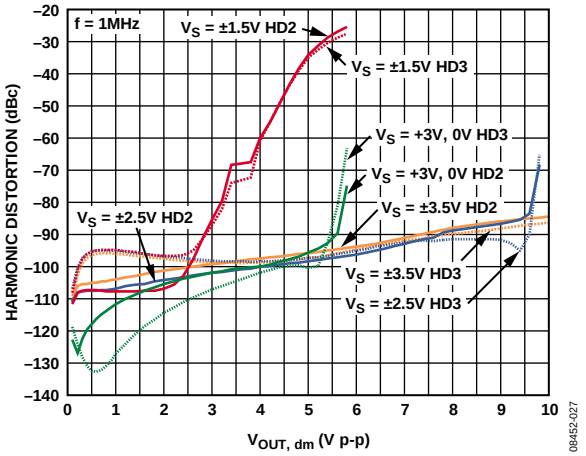


Figure 27. Harmonic Distortion vs. $V_{OUT, dm}$ for Various Supplies, f = 1 MHz

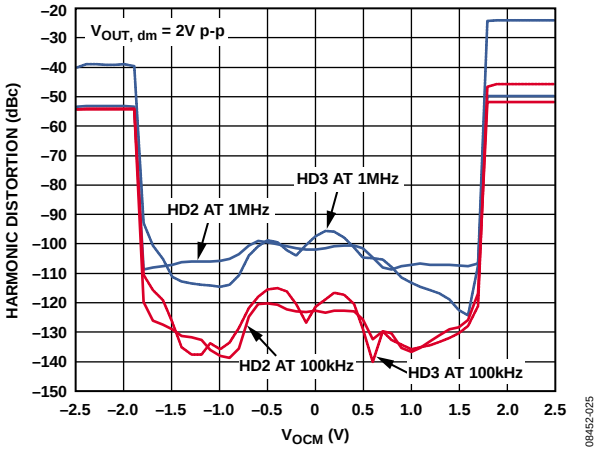


Figure 25. Harmonic Distortion vs. $V_{OCM}$ for 100 kHz and 1 MHz, ±2.5 V Supplies

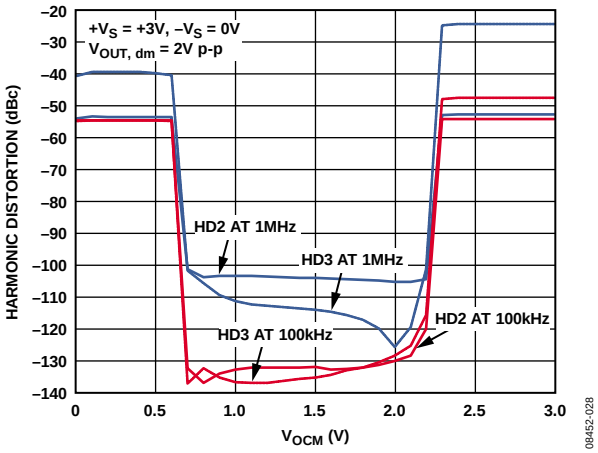


Figure 28. Harmonic Distortion vs. $V_{OCM}$ for 100 kHz and 1 MHz, 3 V Supply

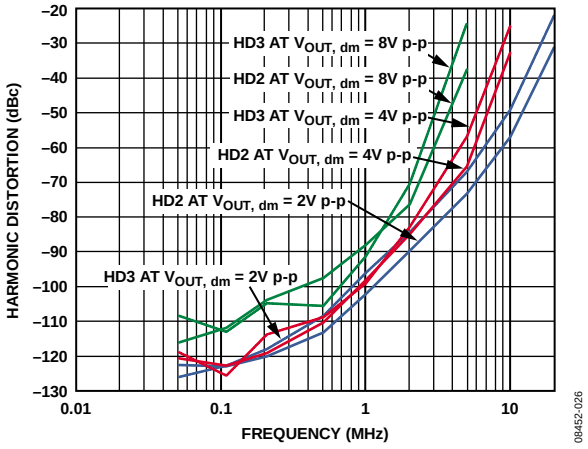


Figure 26. Harmonic Distortion vs. Frequency for Various $V_{OUT, dm}$

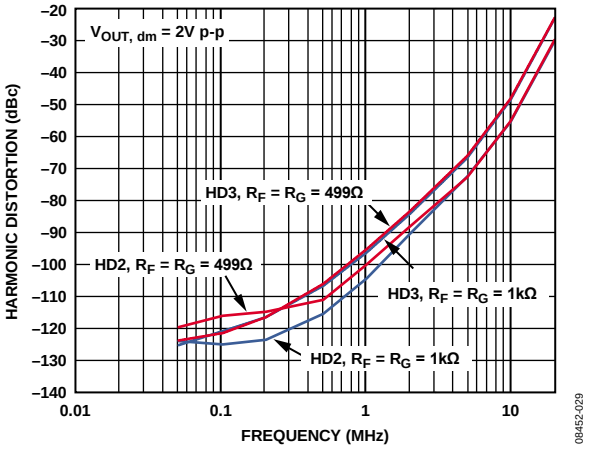


Figure 29. Harmonic Distortion vs. Frequency for Various $R_F$ and $R_G$

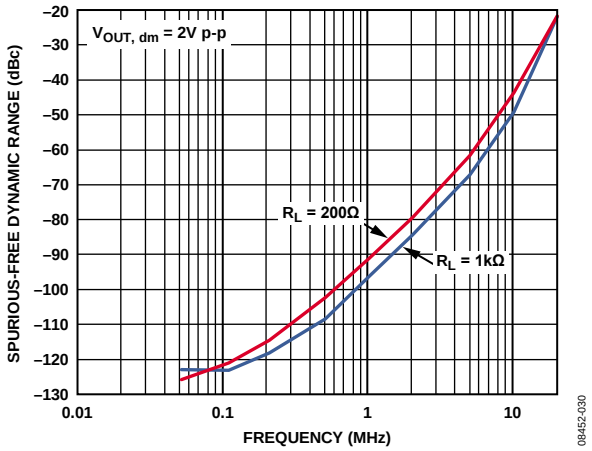


Figure 30. Spurious-Free Dynamic Range vs. Frequency at $R_L$ = 200 Ω and $R_L$ = 1kΩ

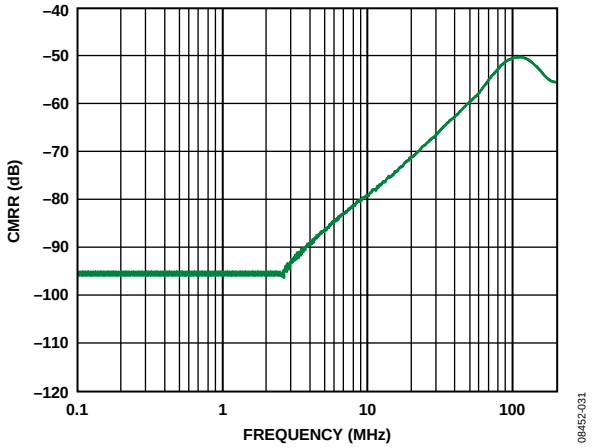


Figure 31. CMRR vs. Frequency

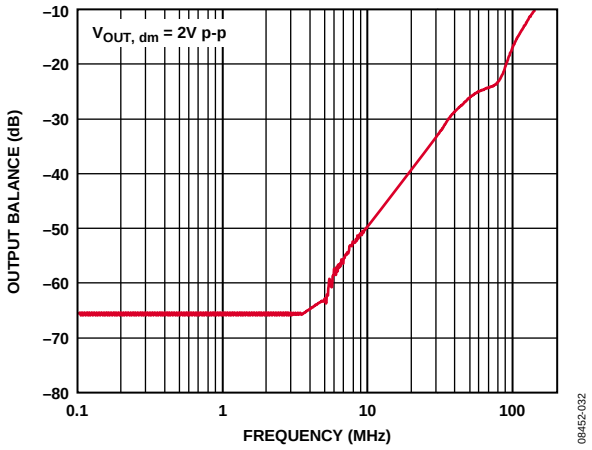


Figure 32. Output Balance vs. Frequency

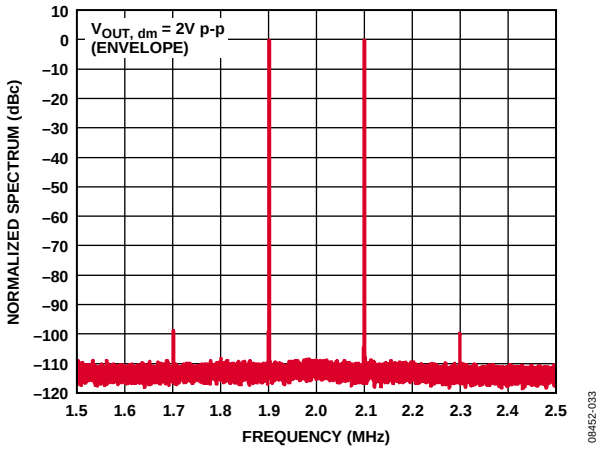


Figure 33. 2 MHz Intermodulation Distortion

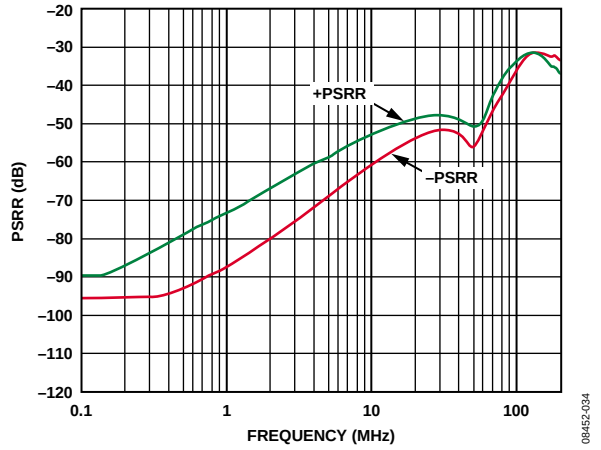


Figure 34. PSRR vs. Frequency

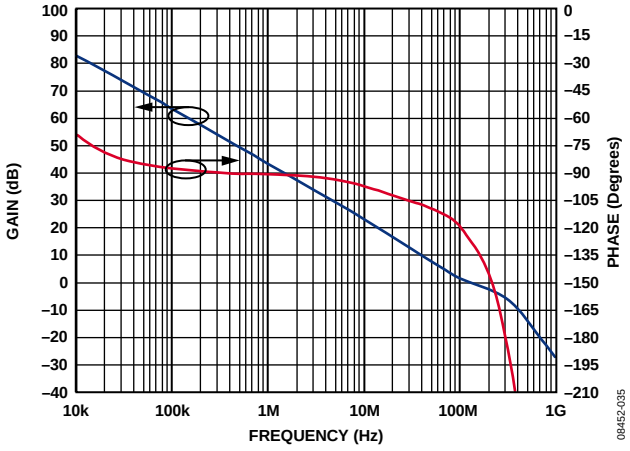


Figure 35. Open-Loop Gain and Phase vs. Frequency

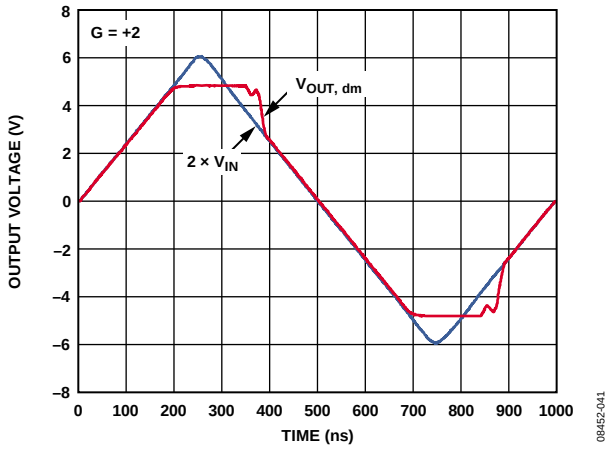


Figure 36. Output Overdrive Recovery, G = 2

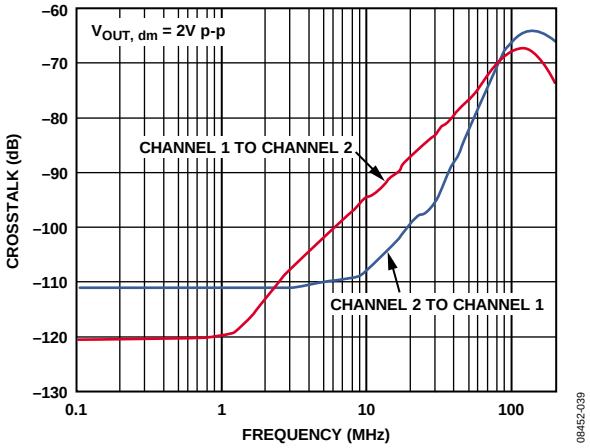


Figure 39. Crosstalk vs. Frequency, ADA4940-2

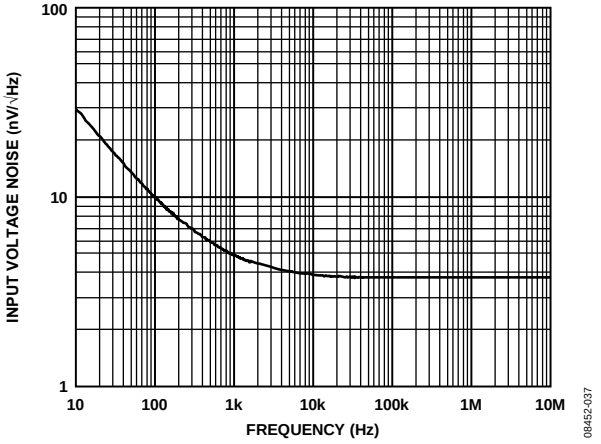


Figure 37. Voltage Noise Spectral Density, Referred to Input

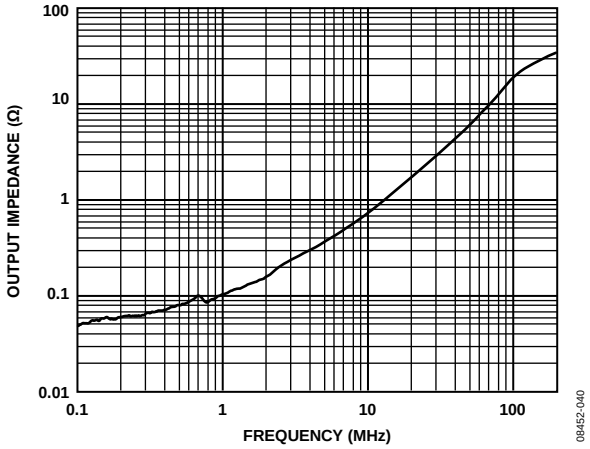


Figure 40. Closed-Loop Output Impedance Magnitude vs. Frequency, G = 1

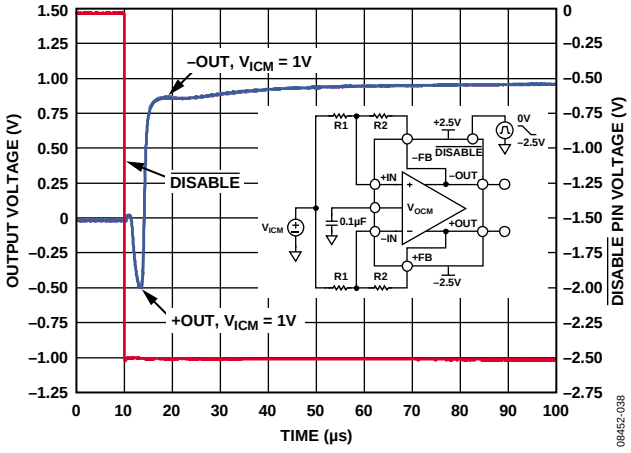


Figure 38. $\overline{DISABLE}$ Pin Turn-Off Time

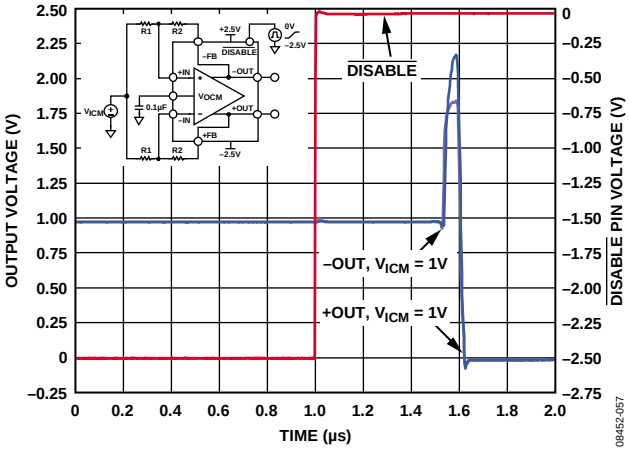


Figure 41. $\overline{DISABLE}$ Pin Turn-On Time

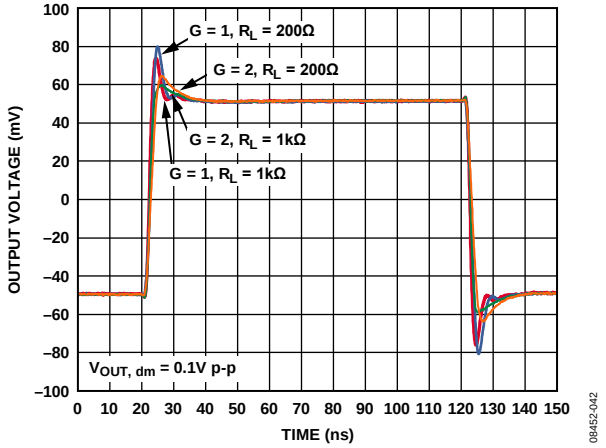


Figure 42. Small Signal Transient Response for Various Gains and Loads

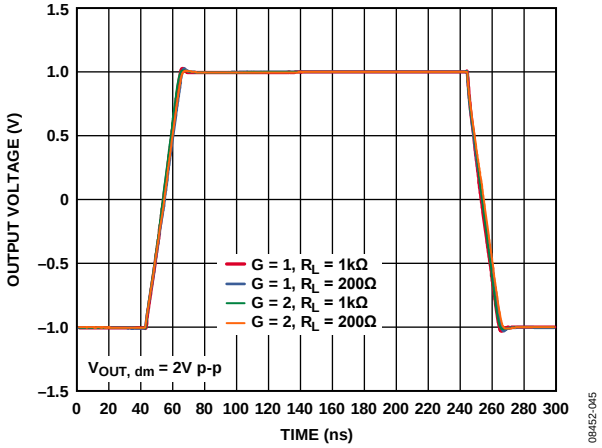


Figure 45. Large Signal Transient Response for Various Gains and Loads

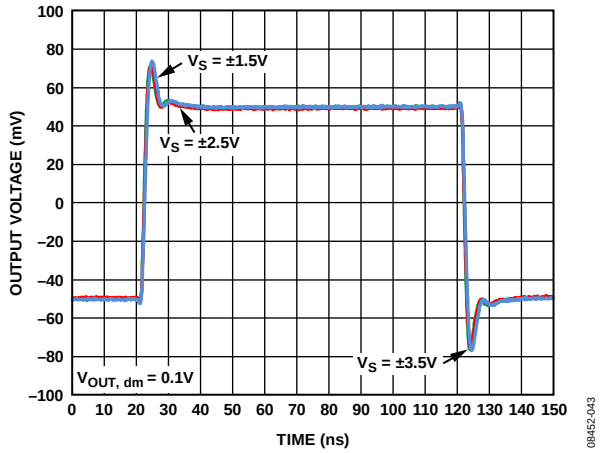


Figure 43. Small Signal Transient Response for Various Supplies

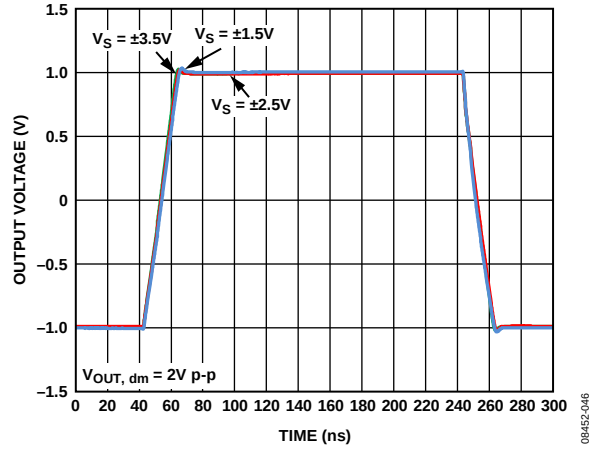


Figure 46. Large Signal Transient Response for Various Supplies

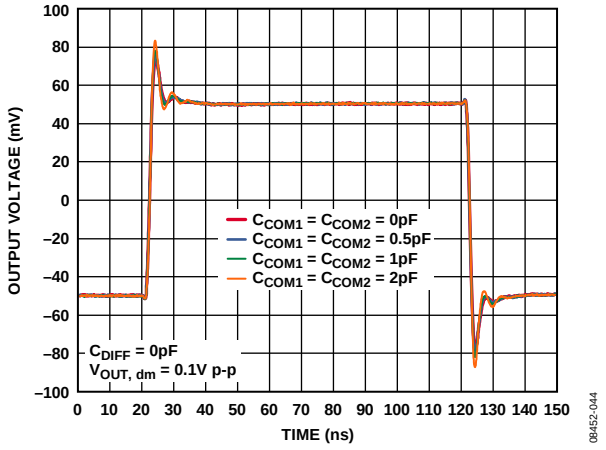


Figure 44. Small Signal Transient Response for Various Capacitive Loads

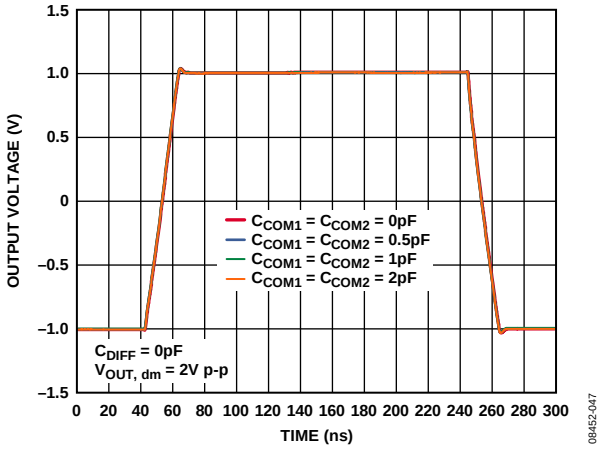


Figure 47. Large Signal Transient Response for Various Capacitive Loads

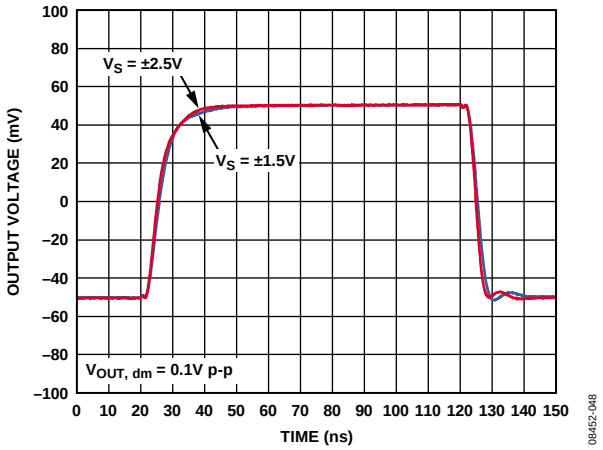


Figure 48. $V_{OCM}$ Small Signal Transient Response

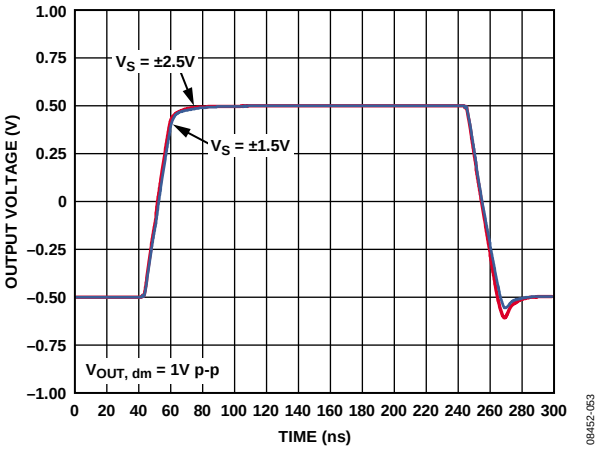


Figure 50. $V_{OCM}$ Large Signal Transient Response

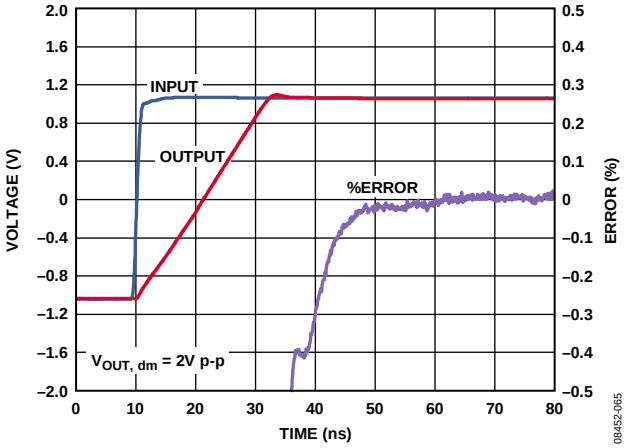


Figure 49. 0.1% Settling Time

# TEST CIRCUITS

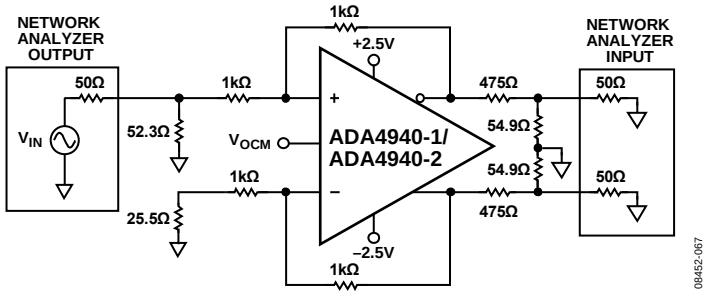


*Figure 51. Equivalent Basic Test Circuit*

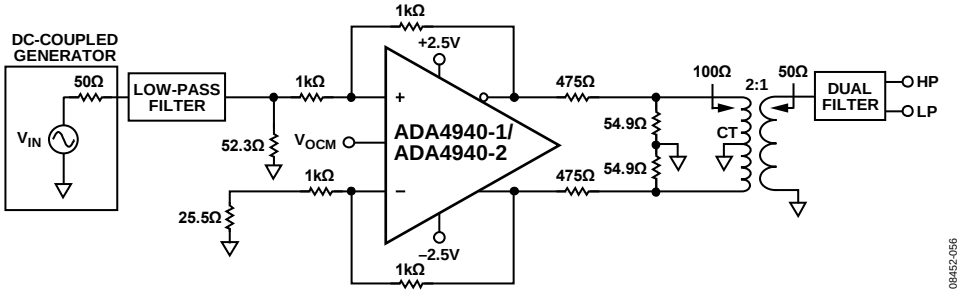


*Figure 52. Test Circuit for Distortion Measurements*

# TERMINOLOGY

## DEFINITION OF TERMS

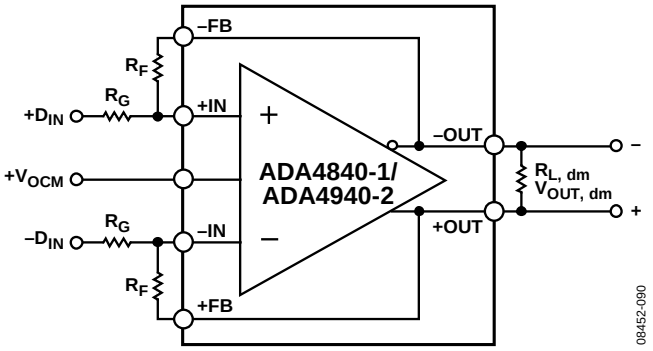


*Figure 53. Circuit Definitions*

### *Differential Voltage*

Differential voltage refers to the difference between two node voltages. For example, the differential output voltage (or equivalently, output differential mode voltage) is defined as

$$V_{OUT, dm} = (V_{+OUT} - V_{-OUT})$$

where $V_{+OUT}$ and $V_{-OUT}$ refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Similarly, the differential input voltage is defined as

$$V_{IN, dm} = (+D_{IN} - (-D_{IN}))$$

### *Common-Mode Voltage (CMV)*

CMV refers to the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT, cm} = (V_{+OUT} + V_{-OUT})/2$$

Similarly, the input common-mode voltage is defined as

$$V_{IN, cm} = (+D_{IN} + (-D_{IN}))/2$$

### *Common-Mode Offset Voltage*

The common-mode offset voltage is defined as the difference between the voltage applied to the $V_{OCM}$ terminal and the common mode of the output voltage.

$$V_{OS, cm} = V_{OUT, cm} - V_{OCM}$$

### *Differential $V_{OS}$, Differential CMRR, and $V_{OCM}$ CMRR*

The differential mode and common-mode voltages each have their own error sources. The differential offset ($V_{OS, dm}$) is the voltage error between the +IN and −IN terminals of the amplifier. Differential CMRR reflects the change of $V_{OS, dm}$ in response to changes to the common-mode voltage at the input terminals +$D_{IN}$ and −$D_{IN}$.

$$CMRR_{DIFF} = \frac{\Delta V_{OS, dm}}{\Delta V_{IN, cm}}$$

$V_{OCM}$ CMRR reflects the change of $V_{OS, dm}$ in response to changes to the common-mode voltage at the output terminals.

$$CMRR_{V_{OCM}} = \frac{\Delta V_{OS, dm}}{\Delta V_{OCM}}$$

### *Balance*

Balance is a measure of how well the differential signals are matched in amplitude; the differential signals are exactly 180° apart in phase. By this definition, the output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{V_{OUT, cm}}{V_{OUT, dm}} \right|$$

# THEORY OF OPERATION

The ADA4940-1/ADA4940-2 are high speed, low power differential amplifiers fabricated on Analog Devices advanced dielectrically isolated SiGe bipolar process. They provide two closely balanced differential outputs in response to either differential or single-ended input signals. An external feedback network that is similar to a voltage feedback operational amplifier sets the differential gain. The output common-mode voltage is independent of the input common-mode voltage and is set by an external voltage at the $V_{OCM}$ terminal. The PNP input stage allows input common-mode voltages between the negative supply and 1.2 V below the positive supply. A rail-to-rail output stage supplies a wide output voltage range.
The $\overline{\text{DISABLE}}$ pin can be used to reduce the supply current of the amplifier to 13.5 µA.

Figure 54 shows the ADA4940-1/ADA4940-2 architecture. The differential feedback loop consists of the differential transconductance $G_{DIFF}$ working through the $G_O$ output buffers and the $R_F/R_G$ feedback networks. The common-mode feedback loop is set up with a voltage divider across the two differential outputs to create an output voltage midpoint and a common-mode transconductance, $G_{CM}$.

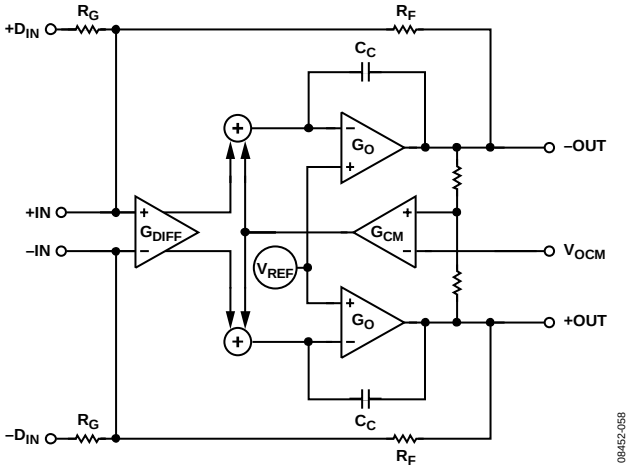


*Figure 54. ADA4940-1/ADA4940-2 Architectural Block*

The differential feedback loop forces the voltages at +IN and −IN to equal each other. This fact sets the following relationships:

$$\frac{+D_{IN}}{R_G} = -\frac{V_{-OUT}}{R_F}$$

$$\frac{-D_{IN}}{R_G} = -\frac{V_{+OUT}}{R_F}$$

Subtracting the previous equations gives the relationship that shows $R_F$ and $R_G$ setting the differential gain.

$$(V_{+OUT} - V_{-OUT}) = (+D_{IN} - (-D_{IN})) \times \frac{R_F}{R_G}$$

The common-mode feedback loop drives the output common-mode voltage that is sampled at the midpoint of the output voltage divider to equal the voltage at $V_{OCM}$. This results in the following relationships:

$$V_{+OUT} = V_{OCM} + \frac{V_{OUT,dm}}{2}$$

$$V_{-OUT} = V_{OCM} - \frac{V_{OUT,dm}}{2}$$

Note that the differential amplifier's summing junction input voltages, +IN and −IN, are set by both the output voltages and the input voltages.

$$V_{+IN} = +D_{IN}\left(\frac{R_F}{R_F + R_G}\right) + V_{-OUT}\left(\frac{R_G}{R_F + R_G}\right)$$

$$V_{-IN} = -D_{IN}\left(\frac{R_F}{R_F + R_G}\right) + V_{+OUT}\left(\frac{R_G}{R_F + R_G}\right)$$

# APPLICATIONS INFORMATION

## ANALYZING AN APPLICATION CIRCUIT

The ADA4940-1/ADA4940-2 use open-loop gain and negative feedback to force their differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN (see Figure 53). For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to $V_{OCM}$ can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

## SETTING THE CLOSED-LOOP GAIN

The differential mode gain of the circuit in Figure 53 can be determined by

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G}$$

This assumes that the input resistors ($R_G$) and feedback resistors ($R_F$) on each side are equal.

## ESTIMATING THE OUTPUT NOISE VOLTAGE

The differential output noise of the ADA4940-1/ADA4940-2 can be estimated using the noise model in Figure 55. The input-referred noise voltage density, $v_{nIN}$, is modeled as a differential input, and the noise currents, $i_{nIN-}$ and $i_{nIN+}$, appear between each input and ground. The noise currents are assumed to be equal and produce a voltage across the parallel combination of the gain and feedback resistances. $v_{nCM}$ is the noise voltage density at the $V_{OCM}$ pin. Each of the four resistors contributes $(4kTR_x)^{1/2}$. Table 13 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms. For more noise calculation information, go to the Analog Devices Differential Amplifier Calculator (DiffAmpCalc™), click **ADIDiffAmpCalculator.zip** and follow the on-screen prompts.

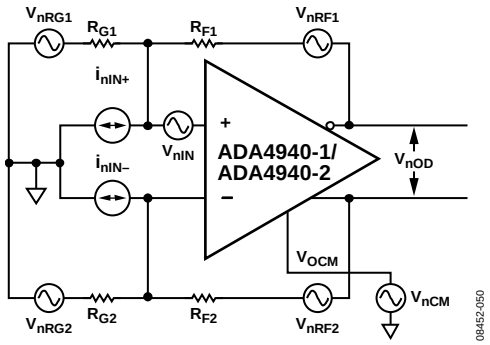


*Figure 55. ADA4940-1/ADA4940-2 Noise Model*

As with conventional op amp, the output noise voltage densities can be estimated by multiplying the input-referred terms at +IN and −IN by the appropriate output factor,

where:

$G_N = \frac{2}{(\beta_1 + \beta_2)}$ is the circuit noise gain.

$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$ and $\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$ are the feedback factors.

When $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, then $\beta 1 = \beta 2 = \beta$, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from $V_{OCM}$ goes to zero in this case. The total differential output noise density, $v_{nOD}$, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

**Table 13. Output Noise Voltage Density Calculations**

| Input Noise Contribution | Input Noise Term | Input Noise Voltage Density | Output Multiplication Factor | Output-Referred Noise Voltage Density Term |
|---|---|---|---|---|
| Differential Input | $v_{nIN}$ | $v_{nIN}$ | $G_N$ | $v_{nO1} = G_N (v_{nIN})$ |
| Inverting Input | $i_{nIN-}$ | $i_{nIN-} \times (R_{G2} \| \| R_{F2})$ | $G_N$ | $v_{nO2} = G_N [i_{nIN-} \times (R_{G2} \| \| R_{F2})]$ |
| Noninverting Input | $i_{nIN+}$ | $i_{nIN+} \times (R_{G1} \| \| R_{F1})$ | $G_N$ | $v_{nO3} = G_N [i_{nIN+} \times (R_{G1} \| \| R_{F1})]$ |
| $V_{OCM}$ Input | $v_{nCM}$ | $v_{nCM}$ | $G_N (\beta_1 - \beta_2)$ | $v_{nO4} = G_N (\beta_1 - \beta_2)(v_{nCM})$ |
| Gain Resistor $R_{G1}$ | $v_{nRG1}$ | $(4kTR_{G1})^{1/2}$ | $G_N (1 - \beta_2)$ | $v_{nO5} = G_N (1 - \beta_2)(4kTR_{G1})^{1/2}$ |
| Gain Resistor $R_{G2}$ | $v_{nRG2}$ | $(4kTR_{G2})^{1/2}$ | $G_N (1 - \beta_1)$ | $v_{nO6} = G_N (1 - \beta_1)(4kTR_{G2})^{1/2}$ |
| Feedback Resistor $R_{F1}$ | $v_{nRF1}$ | $(4kTR_{F1})^{1/2}$ | 1 | $v_{nO7} = (4kTR_{F1})^{1/2}$ |
| Feedback Resistor $R_{F2}$ | $v_{nRF2}$ | $(4kTR_{F2})^{1/2}$ | 1 | $v_{nO8} = (4kTR_{F2})^{1/2}$ |

Table 14 and Table 15 list several common gain settings, recommended resistor values, input impedances, and output noise density for both balanced and unbalanced input configurations.

**Table 14. Differential Ground-Referenced Input, DC-Coupled, $R_L$ = 1 kΩ (See Figure 56)**

| Nominal Gain (dB) | $R_F$ (Ω) | $R_G$ (Ω) | $R_{IN, dm}$ (Ω) | Differential Output Noise Density (nV/√Hz) | RTI (nV/√Hz) |
|---|---|---|---|---|---|
| 0 | 1000 | 1000 | 2000 | 11.3 | 11.3 |
| 6 | 1000 | 500 | 1000 | 15.4 | 7.7 |
| 10 | 1000 | 318 | 636 | 20.0 | 6.8 |
| 14 | 1000 | 196 | 392 | 27.7 | 5.5 |

**Table 15. Single-Ended Ground-Referenced Input, DC-Coupled, $R_S$ = 50 Ω, $R_L$ = 1 kΩ (See Figure 57)**

| Nominal Gain (dB) | $R_F$ (Ω) | $R_G$ (Ω) | $R_T$ (Ω) | $R_{IN, se}$ (Ω) | $R_{G1}$ (Ω)[1] | Differential Output Noise Density (nV/√Hz) | RTI (nV/√Hz) |
|---|---|---|---|---|---|---|---|
| 0 | 1000 | 1000 | 52.3 | 1333 | 1025 | 11.2 | 11.2 |
| 6 | 1000 | 500 | 53.6 | 750 | 526 | 15.0 | 7.5 |
| 10 | 1000 | 318 | 54.9 | 512 | 344 | 19.0 | 6.3 |
| 14 | 1000 | 196 | 59.0 | 337 | 223 | 25.3 | 5 |

[1] $R_{G1} = R_G + (R_S \| R_T)$

## IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

Even if the external feedback networks ($R_F/R_G$) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output, differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

As well as causing a noise contribution from $V_{OCM}$, ratio matching errors in the external resistors result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four resistor difference amplifier made from a conventional op amp.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential mode, output offset voltage. When G = 1, with a ground-referenced input signal and the output common-mode level set to 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst-case input CMRR of about 40 dB, a worst-case differential mode output offset of 25 mV due to the 2.5 V level-shift, and no significant degradation in output balance error.

## CALCULATING THE INPUT IMPEDANCE OF AN APPLICATION CIRCUIT

The effective input impedance of a circuit depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, as shown in Figure 56, the input impedance ($R_{IN, dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply $R_{IN, dm} = 2 \times R_G$.

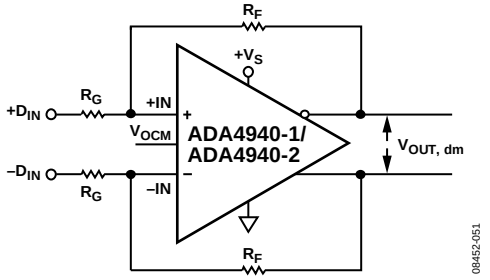


*Figure 56. ADA4940-1/ADA4940-2 Configured for Balanced (Differential) Inputs*

For an unbalanced, single-ended input signal (see Figure 57), the input impedance is

$$R_{IN, se} = \left( \frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

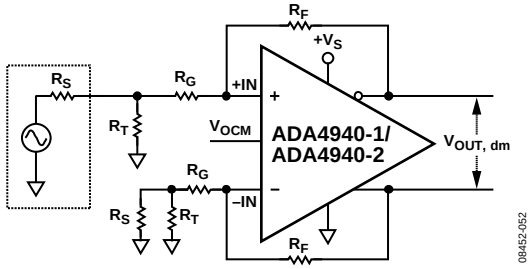


*Figure 57. ADA4940-1/ADA4940-2 Configured for Unbalanced (Single-Ended) Input*

The input impedance of the circuit is effectively higher than it is for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor, $R_G$. The common-mode voltage at the amplifier input terminals can be easily determined by noting that the voltage at the inverting input is equal to the noninverting output voltage divided by the voltage divider that is formed by $R_F$ and $R_G$ in the lower loop. This voltage is present at both input terminals due to negative voltage feedback and is in phase with the input signal, thus reducing the effective voltage across $R_G$ in the upper loop and partially bootstrapping $R_G$.

### *Terminating a Single-Ended Input*

This section describes how to properly terminate a single-ended input to the ADA4940-1/ADA4940-2 with a gain of 1, $R_F$ = 1 kΩ and $R_G$ = 1 kΩ. An example using an input source with a terminated output voltage of 1 V p-p and source resistance of 50 Ω illustrates the three steps that must be followed. Because the terminated output voltage of the source is 1 V p-p, the open-circuit output voltage of the source is 2 V p-p. The source shown in Figure 58 indicates this open-circuit voltage.

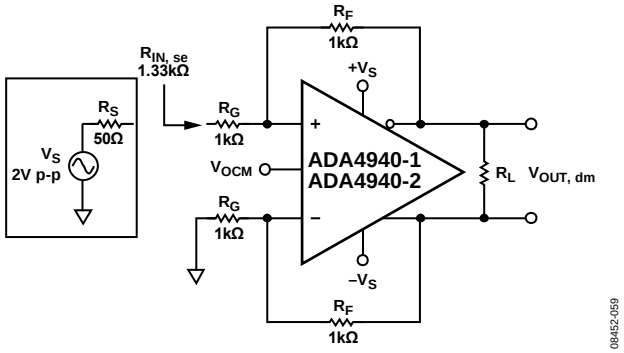


*Figure 58. Calculating Single-Ended Input Impedance, $R_{IN}$*

1. The input impedance is calculated by

$$R_{IN,\,se} = \left(\frac{R_G}{1-\dfrac{R_F}{2\times(R_G+R_F)}}\right) = \left(\frac{1000}{1-\dfrac{1000}{2\times(\ 1000\ +\ 1000)}}\right) = \ 1.33\ \text{k}\Omega$$

2. To match the 50 Ω source resistance, calculate the termination resistor, $R_T$, using $R_T||1.33\ \text{k}\Omega = 50\ \Omega$. The closest standard 1% value for $R_T$ is 52.3 Ω.

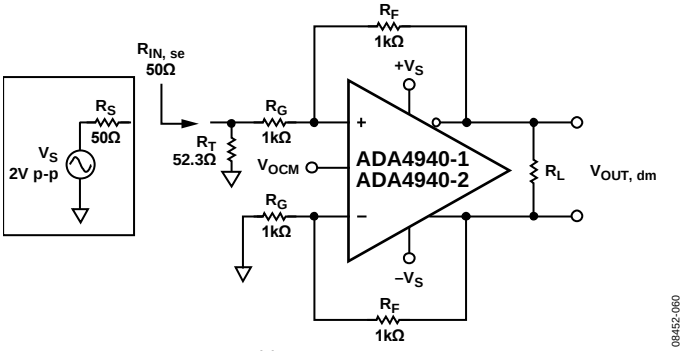


*Figure 59. Adding Termination Resistor $R_T$*

3. Figure 59 shows that the effective $R_G$ in the upper feedback loop is now greater than the $R_G$ in the lower loop due to the addition of the termination resistors. To compensate for the imbalance of the gain resistors, add a correction resistor ($R_{TS}$) in series with $R_G$ in the lower loop. $R_{TS}$ is the Thevenin equivalent of the source resistance, $R_S$, and the termination resistance, $R_T$, and is equal to $R_S||R_T$.


*Figure 60. Calculating the Thevenin Equivalent*

$R_{TS} = R_{TH} = R_S||R_T = 25.5\ \Omega$. Note that $V_{TH}$ is greater than 1 V p-p, which was obtained with $R_T$ = 50 Ω. The modified circuit with the Thevenin equivalent (closest 1% value used for $R_{TH}$) of the terminated source and $R_{TS}$ in the lower feedback loop is shown in Figure 61.

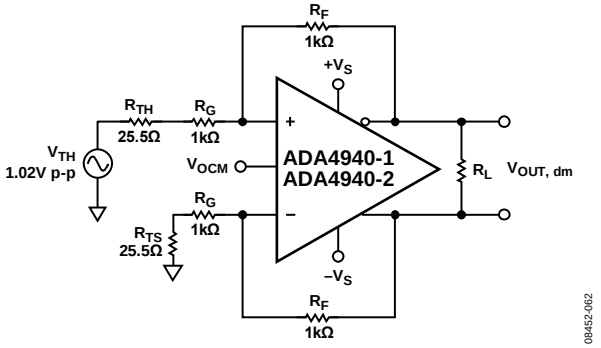


*Figure 61. Thevenin Equivalent and Matched Gain Resistors*

Figure 61 presents a tractable circuit with matched feedback loops that can be easily evaluated.

It is useful to point out two effects that occur with a terminated input. The first is that the value of $R_G$ is increased in both loops, lowering the overall closed-loop gain. The second is that $V_{TH}$ is a little larger than 1 V p-p, as it would be if $R_T$ = 50 Ω. These two effects have opposite impacts on the output voltage, and for large resistor values in the feedback loops (~1 kΩ), the effects essentially cancel each other out. For small $R_F$ and $R_G$, or high gains, however, the diminished closed-loop gain is not cancelled completely by the increased $V_{TH}$. This can be seen by evaluating Figure 61.

The desired differential output in this example is 1 V p-p because the terminated input signal was 1 V p-p and the closed-loop gain = 1. The actual differential output voltage, however, is equal to (1.02 V p-p)(1000/1025.5) = 0.996 V p-p. This is within the tolerance of the resistors, so no change to the feedback resistor, $R_F$, is required.

## INPUT COMMON-MODE VOLTAGE RANGE

The ADA4940-1/ADA4940-2 input common-mode range is shifted down by approximately 1 $V_{BE}$, in contrast to other ADC drivers with centered input ranges, such as the ADA4939-x. The downward-shifted input common-mode range is especially suited to dc-coupled, single-ended-to-differential, and single-supply applications.

For ±2.5 V or +5 V supply operation, the input common-mode range at the summing nodes of the amplifier is specified as −2.7 V to +1.3 V or −0.2 V to 3.8 V, and is specified as −0.2 V to +1.8 V with a +3 V supply.

## INPUT AND OUTPUT CAPACITIVE AC COUPLING

Although the ADA4940-1/ADA4940-2 is best suited to dc-coupled applications, it is nonetheless possible to use it in ac-coupled circuits. Input ac coupling capacitors can be inserted between the source and $R_G$. This ac coupling blocks the flow of the dc common-mode feedback current and causes the ADA4940-1/ADA4940-2 dc input common-mode voltage to equal the dc output common-mode voltage. These ac coupling capacitors must be placed in both loops to keep the feedback factors matched. Output ac coupling capacitors can be placed in series between each output and its respective load.

## SETTING THE OUTPUT COMMON-MODE VOLTAGE

The $V_{OCM}$ pin of the ADA4940-1/ADA4940-2 is internally biased at a voltage approximately equal to the midsupply point, $[(+V_S) + (-V_S)]/2$. Relying on this internal bias results in an output common-mode voltage that is within approximately 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (10 kΩ or greater resistors), be used. The output common-mode offset listed in the Specifications section assumes that the $V_{OCM}$ input is driven by a low impedance voltage source.

It is also possible to connect the $V_{OCM}$ input to a common-mode level (CML) output of an ADC. However, care must be taken to ensure that the output has sufficient drive capability. The input impedance of the $V_{OCM}$ pin is approximately 250 kΩ.

## $\overline{\text{DISABLE}}$ PIN

The ADA4940-1/ADA4940-2 feature a $\overline{\text{DISABLE}}$ pin that can be used to minimize the quiescent current consumed when the device is not being used. $\overline{\text{DISABLE}}$ is asserted by applying a low logic level to the $\overline{\text{DISABLE}}$ pin. The threshold between high and low logic levels is nominally 1.4 V above the negative supply rail. See Table 5 and Table 8 for the threshold limits.

The $\overline{\text{DISABLE}}$ pin features an internal pull-up network that enables the amplifier for normal operation. The ADA4940-1/ADA4940-2 $\overline{\text{DISABLE}}$ pin can be left floating (that is, no external connection is required) and does not require an external pull-up resistor to ensure normal on operation (see Figure 62). When the ADA4940-1/ADA4940-2 is disabled, the output is high impedance. Note that the outputs are tied to the inputs through the feedback resistors and to the source using the gain resistors. In addition, there are back-to-back diodes on the input pins that limit the differential voltage to 1.2 V.

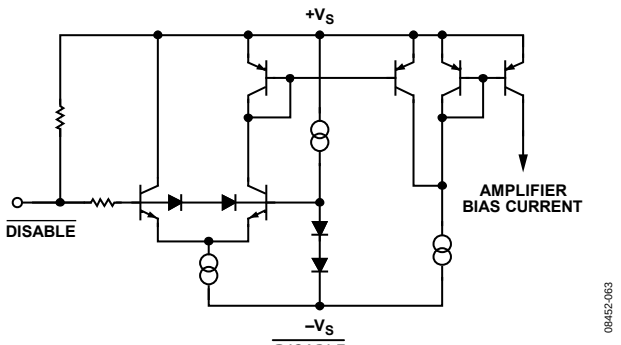


*Figure 62. $\overline{\text{DISABLE}}$ Pin Circuit*

## DRIVING A CAPACITIVE LOAD

A purely capacitive load reacts with the bond wire and pin inductance of the ADA4940-1/ADA4940-2, resulting in high frequency ringing in the transient response and loss of phase margin. One way to minimize this effect is to place a resistor in series with each output to buffer the load capacitance. The resistor and load capacitance form a first-order, low-pass filter; therefore, the resistor value should be as small as possible. In some cases, the ADCs require small series resistors to be added on their inputs.

Figure 63 illustrates the capacitive load vs. the series resistance required to maintain a minimum 45° of phase margin.

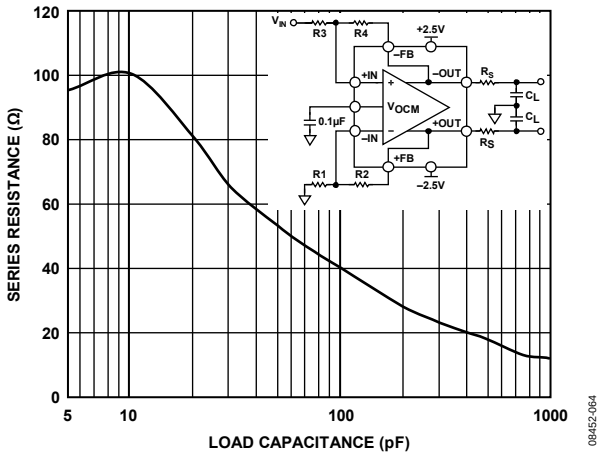


*Figure 63. Capacitive Load vs. Series Resistance*

## DRIVING A HIGH PRECISION ADC

The ADA4940-1/ADA4940-2 are ideally suited for broadband dc-coupled applications. The circuit in Figure 65 shows a front-end connection for an ADA4940-1 driving an AD7982, which is an 18-bit, 1 MSPS successive approximation, analog-to-digital converter (ADC) that operates from a single power supply, 3 V to 5 V. It contains a low power, high speed, 18-bit sampling ADC and a versatile serial interface port. The reference voltage, REF, is applied externally and can be set independent of the supply voltage. As shown in Figure 65, the ADA4940-1 is dc-coupled on the input and the output, which eliminates the need for a transformer to drive the ADC. The amplifier performs a single-ended-to-differential conversion if needed and level shifts the input signal to match the input common mode of the ADC. The ADA4940-1 is configured with a dual 7 V supply (+6 V and −1 V) and a gain that is set by the ratio of the feedback resistor to the gain resistor. In addition, the circuit can be used in a single-ended-input-to-differential output or differential-input-to-differential output configuration. If needed, a termination resistor in parallel with the source input can be used. Whether the input is a single-ended input or differential, the input impedance of the amplifier can be calculated as shown in the Terminating a Single-Ended Input section. If R1 = R2 = R3 = R4 = 1 kΩ, the single-ended input impedance is approximately 1.33 kΩ, which, in parallel with a 52.3 Ω termination resistor, provides a 50 Ω termination for the source. An additional 25.5 Ω (1025.5 Ω total) at the inverting input balances the parallel impedance of the 50 Ω source and the termination resistor driving the noninverting input. However, if a differential source input is used, the differential input impedance is 2 kΩ. In this case, two 52.3 Ω termination resistors are used to terminate the inputs.

In this example, the signal generator has a 10 V p-p symmetric, ground-referenced bipolar output. The $V_{OCM}$ input is bypassed for noise reduction and set externally with 1% resistors to 2.5 V to maximize the output dynamic range. With an output common-mode voltage of 2.5 V, each ADA4940-1 output swings between 0 V and 5 V, opposite in phase, providing a gain of 1 and a 10 V p-p differential signal to the ADC input. The differential RC section between the ADA4940-1 output and the ADC provides single-pole, low-pass filtering with a corner frequency of 1.79 MHz and extra buffering for the current spikes that are output from the ADC input when its sample-and-hold (SHA) capacitors are discharged.

The total system power in Figure 65 is under 35 mW. A large portion of that power is the current coming from supplies to the output, which is set at 2.5 V, going back to the input through the feedback and gain resistors. To reduce that power to 25 mW, increase the value of the feedback and gain resistor from 1 kΩ to 2 kΩ and set the value of the resistors R5 and R6 to 3 kΩ.

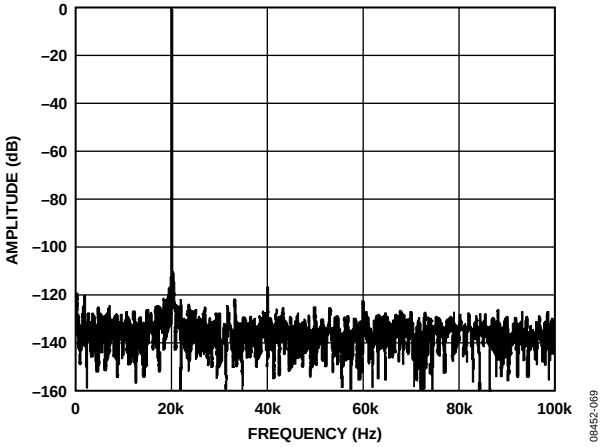


*Figure 64. Distortion Measurement of a 20 kHz Input Tone (CN-0237)*

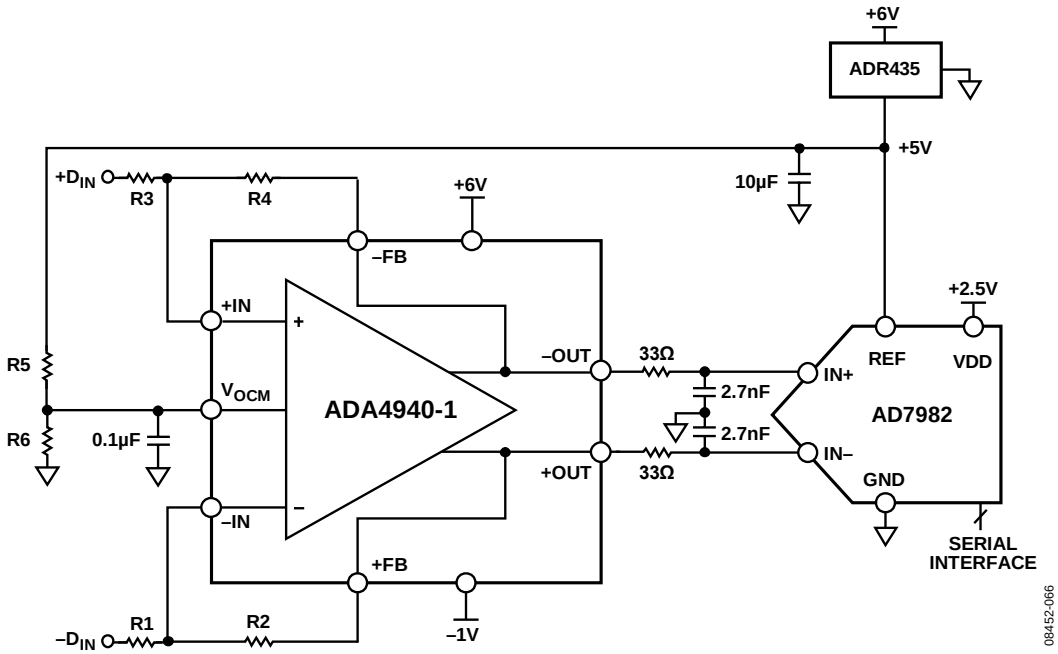


*Figure 65. ADA4940-1 Driving the AD7982 ADC*

# LAYOUT, GROUNDING, AND BYPASSING

As a high speed device, the ADA4940-1/ADA4940-2 are sensitive to the PCB environment in which they operate. Realizing their superior performance requires attention to the details of high speed PCB design.

## ADA4940-1 EXAMPLE

The first requirement is a solid ground plane that covers as much of the board area around the ADA4940-1 as possible. However, clear the area near the feedback resistors ($R_F$), gain resistors ($R_G$), and the input summing nodes (Pin 2 and Pin 3) of all ground and power planes (see Figure 66). Clearing the ground and power planes minimizes any stray capacitance at these nodes and prevents peaking of the response of the amplifier at high frequencies.

The thermal resistance, $\theta_{JA}$, is specified for the device, including the exposed pad, soldered to a high thermal conductivity 4-layer circuit board, as described in EIA/JESD 51-7.

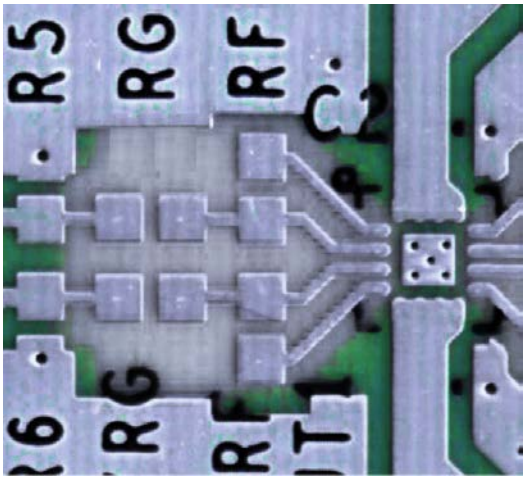


*Figure 66. Ground and Power Plane Voiding in Vicinity of $R_F$ and $R_G$*

Bypass the power supply pins as close to the device as possible and directly to a nearby ground plane. Use high frequency ceramic chip capacitors. Use two parallel bypass capacitors (1000 pF and 0.1 µF) for each supply. Place the 1000 pF capacitor closer to the device. Further away, provide low frequency bypassing using 10 µF tantalum capacitors from each supply to ground.

Ensure that signal routing is short and direct to avoid parasitic effects. Wherever complementary signals exist, provide a symmetrical layout to maximize balanced performance. When routing differential signals over a long distance, ensure that PCB traces are close together, and twist any differential wiring such that loop area is minimized. Doing this reduces radiated energy and makes the circuit less susceptible to interference.

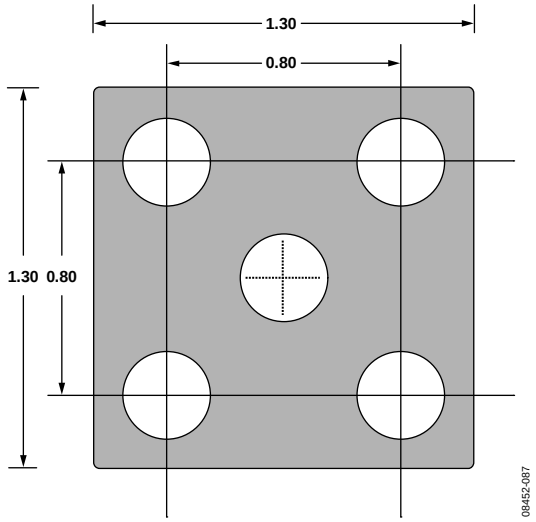


*Figure 67. Recommended PCB Thermal Attach Pad Dimensions (mm)*

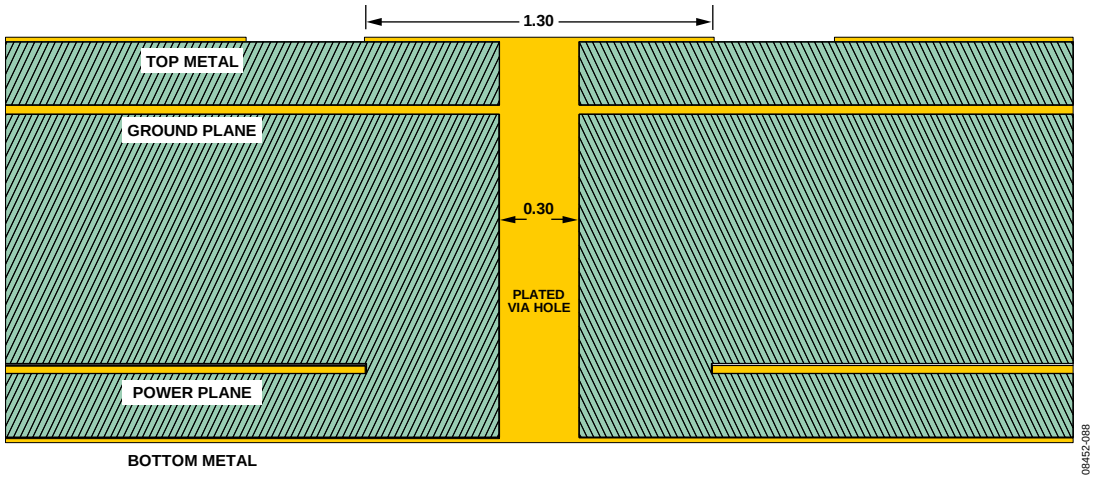


*Figure 68. Cross-Section of 4-Layer PCB Showing Thermal Via Connection to Buried Ground Plane (Dimensions in mm)*

# OUTLINE DIMENSIONS

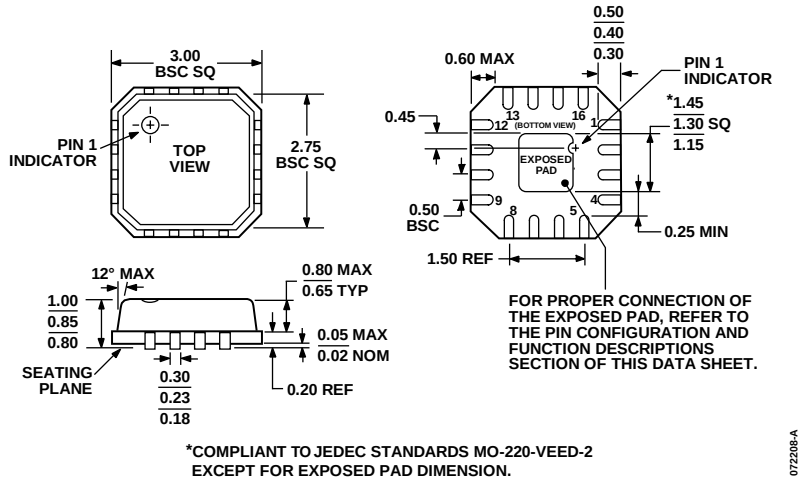


*Figure 69. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*3 mm × 3 mm Body, Very Thin Quad*
*(CP-16-2)*
*Dimensions shown in millimeters*

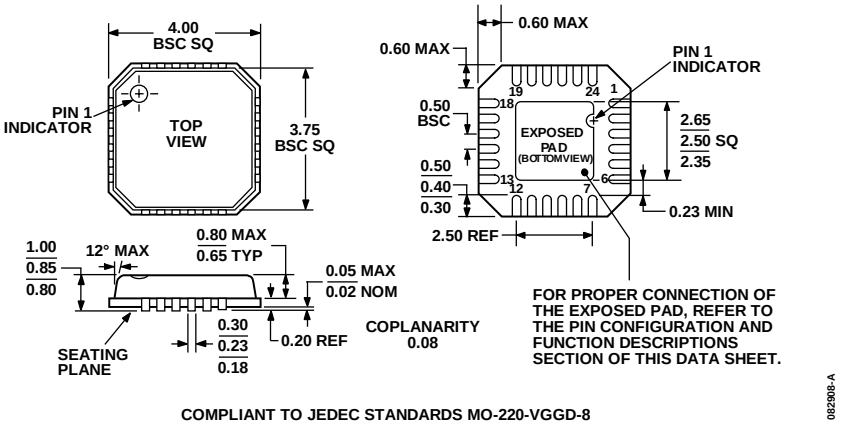


*Figure 70. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*4 mm × 4 mm Body, Very Thin Quad*
*(CP-24-3)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Ordering Quantity | Branding |
|---|---|---|---|---|---|
| ADA4940-1ACPZ-R2 | −40°C to +125°C | 16-Lead LFCSP_VQ | CP-16-2 | 250 | H29 |
| ADA4940-1ACPZ-RL | −40°C to +125°C | 16-Lead LFCSP_VQ | CP-16-2 | 5,000 | H29 |
| ADA4940-1ACPZ-R7 | −40°C to +125°C | 16-Lead LFCSP_VQ | CP-16-2 | 1,500 | H29 |
| ADA4940-1ACP-EBZ | | Evaluation Board | | | |
| ADA4940-2ACPZ-R2 | −40°C to +125°C | 24-Lead LFCSP_VQ | CP-24-3 | 250 | |
| ADA4940-2ACPZ-RL | −40°C to +125°C | 24-Lead LFCSP_VQ | CP-24-3 | 5,000 | |
| ADA4940-2ACPZ-R7 | −40°C to +125°C | 24-Lead LFCSP_VQ | CP-24-3 | 1,500 | |
| ADA4940-2ACP-EBZ | | Evaluation Board | | | |

[1] Z = RoHS Compliant Part.

## NOTES

## NOTES


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