Emulation and Trace Headers

Technical Reference Manual

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About This Manual

This technical reference describes how to incorporate Texas Instruments' next-generation emulation header on a board with a trace-enabled DSP.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.
- Measurements are in English standard units (inches, pounds, etc.).

Related Documentation

The following documents describe the TMS320C6000™ DSP platform and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

SPRA439 — *Emulation Fundamentals for TI's DSP Solutions.* This paper explains the fundamentals of how the emulation logic and emulation tools work together with the TI digital signal processors. By understanding the fundamentals of emulation, you will be able to accelerate the process of setting up and performing software debug, as well as aid in troubleshooting potential problems in the debugging setup. A detailed explanation of the setup of the emulator hardware systems for single and multi-processor applications, along with a discussion of how the system components interact during debug will be discussed in the sections to follow. Also included is a troubleshooting guide to assist in common setup problems.

SPRU641 — *TMS320C6000 DSP Designing for JTAG Emulation Reference Guide.* This document assists you in meeting the design requirements of the XDS510™ emulator with respect to JTAG designs and discusses the XDS510 cable. This cable supports both standard 3-volt and 5-volt target system power inputs.

SPRU589 — *XDS560 Emulator Reference Guide.* This technical reference describes the fundamentals of the XDS560™ PCI Emulator and Pod and how to interface it to a target system.

SPDU079 — *JTAG/MPSD Emulation Technical Reference.* A reference guide that provides detailed information to be used when designing for JTAG emulation.

SPRAAK6 — *Common Trace Transmission Problems and Solutions.* This document provides guidelines for identifying and solving common problems associated with the collecting of high speed data. On a trace-capable device, the trace interface is one of the highest performance interfaces. Although only used during design, development, and debug, the trace interface must be implemented correctly for full functionality and performance.

IEEE Std 1149.1-1990 — *IEEE Std 1149.1-1990 IEEE Standard Test Access Port and Boundary-Scan Architecture -Description.* Circuitry that may be built into an integrated circuit to assist in the test, maintenance, and support of assembled printed circuit boards is defined. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register, such that the component is able to respond to a minimum set of instructions designed to assist with testing of assembled printed circuit boards.

Emulation and Trace Headers

1 Introduction

This technical reference describes the requirements necessary to incorporate an emulation header on a board that includes devices that support trace export through the device's EMU pins to an emulator with trace capture support, such as the XDS560T. Texas Instruments device's support various combinations of DSP core trace and system trace. In all cases, the trace data rates require that the EMU pins be treated as high-speed clocks within your design. This specifically means that the EMU pins must be terminated properly and the correct header chosen for the number of EMU pins required. In the case of core trace or if core trace and system trace export are both supported, this requires utilizing a 60-pin header in place of the traditional TI 14-pin or TI 20-pin CTI emulation header. In the case where a device only supports export of system trace data, a TI 20-pin CTI header may be used.

Core trace typically provides at least processor PC trace, and depending on the silicon implementation may also provide processor data trace and event trace. System trace is a message-based technology that, in enabled silicon, can export application instrumentation and hardware generated messages from system-level monitors. Many devices support on-chip embedded trace buffers (ETBs) either exclusively or in combination with support for exporting trace data through the device's EMU pins. In cases where a device exclusively utilizes an ETB, a 60-pin header is not required to replace the traditional TI 14-pin or TI 20-pin CTI headers on the board, but keep in mind that ETBs only allow visibility to shallow snapshots of data (typically in the 4K to 32K range). To determine if your device supports exporting core or system trace through the EMU pins and/or supports one or multiple ETBs, see the device-specific data sheet. The advantage of exporting core and system trace data through the EMU pins to an emulator with trace capture support, such as the XDS560T, is that the capture depth is much greater (typically many Mbytes), providing a much larger region of visibility and enabling precise profiling and code coverage tooling.

If the device supports any type of core trace export that you want to capture using a TI trace-enabled emulator, then a 60-pin header in place of the traditional TI 14-pin or TI 20-pin CTI TI emulation headers is a requirement. If your device supports only export of system trace data, then you can choose the header that fits your needs.

Table 1. Emulation Header Use

Trace Type	Emulator Type	Native Emulator Header
DSP Core Trace	XDS560T	TI 60-Pin
System Trace	XDS560T	TI 60-Pin(1)
System Trace	XDS560 v2 System Trace	MIPI 60-Pin(1)

(1) Since system trace only utilizes 5 EMU pins, if your processor only supports system trace export through EMU0:4, then you may choose to use a TI-20 pin connector with an adapter.

Even though the 60-pin header supports all the features provided by the original TI 14-pin header, not all emulators, target cables, and target device combinations support all features. To confirm that the desired functionality is supported, see the documentation and device user guides for your specific emulator.

2 Adapters

Adapters allow the XDS560T and XDS560 v2 System Trace emulators to be used with standard TI 14-pin and TI 20-pin CTI target headers, or adaptors can be used to allow a standard XDS100, XDS510, or XDS560 emulator to be used with a target board that is implemented with a TI 60-pin or MIPI 60-pin header. The adapters, listed in Table 2, are available (or may be available in the future) from TI or its third parties.

Table 2. Adapters

For Emulator Type . . .	From Emulator	To Target	Notes
XDS560/XDS510/XDS100	TI 14-Pin	TI 60-Pin	
XDS560 Rev D	TI 20-Pin CTI	TI 60-Pin	
XDS560T	TI 60-Pin	TI 14-Pin	
XDS560T	TI 60-Pin	TI 20-Pin CTI	Check Availability
XDS560T	TI 60-Pin	MIPI 60-Pin	Check Availability
XDS560T	TI 60-Pin	TI 60-Pin	Pin Saver
XDS560 v2 System Trace	MIPI 60-Pin	TI 60-Pin	Check Availability
XDS560 v2 System Trace	MIPI 60-Pin	TI 20-Pin CTI	Check Availability

NOTE: Use of any adapter can have a negative impact on performance.

3 Fundamental Information

This technical reference offers guidance for creating new designs that take advantage of the extended emulation capabilities. This document is not intended to be the sole design guide.

In addition to this guide, good engineering practices for high-speed logic design and mechanical layout must be followed. Any deviation from such practices and design techniques will affect the end-product performance.

4 Alternate Target Impedance Configurations

Within specific end-use applications for TI's hardware emulation products, multiple printed circuit board (PCB) trace impedances may be required. The advanced emulation signals connecting to the emulation header require a 50-Ω trace impedance for optimal performance.

For additional information on DSP target applications that incorporate alternate interfaces including, but not limited to, PCI or external memory interfaces (EMIF), see Appendix A.

Table 3. Summary: Alternate Target Impedance Configurations

1	Target boards without special considerations must be designed for a 50-Ω character impedance.
2	All header EMU signals must be routed as if they are clock signal lines operating at 200 MHz. TI recommends designing JTAG signals for 100-MHz operation.

5 Header Information

Table 4, Table 5, and Table 6 summarize the header information. For specific pin assignments, see Section 8.

Table 4. Summary: TI 60-Pin Header Information

1	Connector Manufacturer is Samtec USA.
2	Connector Model Number is SOLC-115-02-S-Q-P.
3	Connector Specification Overview is located at URL http://www.samtec.com/technical_specifications/overview.aspx?series=SOLC.
4	Connector Drawing is located at URL http://www.samtec.com/ftppub/cpdf/SOLC-MKT.PDF
5	Connector Footprint Drawing is located at URL http://www.samtec.com/ftppub/cpdf/SOLC.PDF

Table 5. Summary: MIPI 60-Pin Header Information

1	Connector Manufacturer is Samtec USA.
2	Connector Model Number is QSH030.
3	Connector Specification Overview is located at URL http://www.samtec.com/technical_specifications/overview.aspx?series=QSH.

Table 5. Summary: MIPI 60-Pin Header Information (continued)

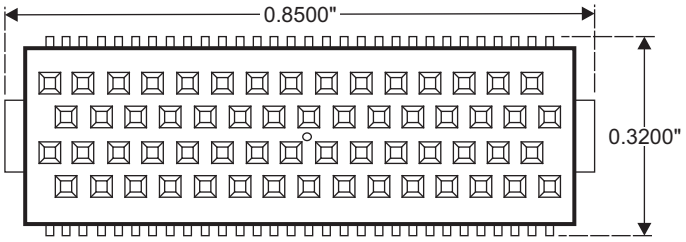
4	Connector Drawing is located at URL http://www.samtec.com/ftppub/cpdf/QSH-XXX-01-X-D-XXX-MKT.pdf.
5	Connector Footprint Drawing is located at URL http://www.samtec.com/ftppub/cpdf/QSH-XXX-01-X-D-XX-FOOTPRINT.pdf.

Table 6. Summary: TI 20-Pin CTI Header Information

1	Connector Manufacturer is Samtec USA.
2	Connector Model Number is FTR-110-51-S-D-06.
3	Connector Specification Overview is located at URL http://www.samtec.com/technical_specifications/overview.aspx?series=FTR.
4	Connector Drawing is located at URL http://www.samtec.com/ftppub/cpdf/FTR-MKT.PDF.
5	Connector Footprint Drawing is located at URL http://www.samtec.com/ftppub/cpdf/FTR-D.PDF.

6 Header Footprint Comparisons

Figure 1 through Figure 3 show TI target connector footprint drawings and Table 7 shows a comparison of the board space required for each connector type.



In this case, dimensions include space required for the target cable mating connector.

Figure 1. TI 60-Pin Emulation Header

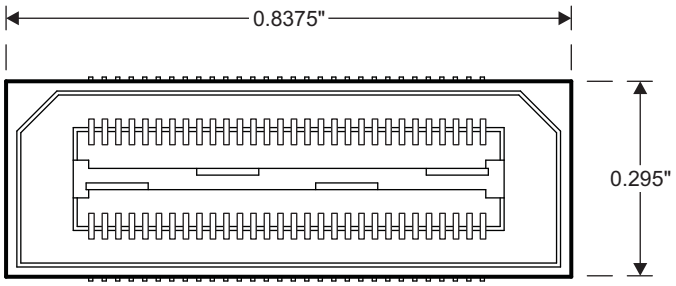


Figure 2. MIPI 60-Pin Header

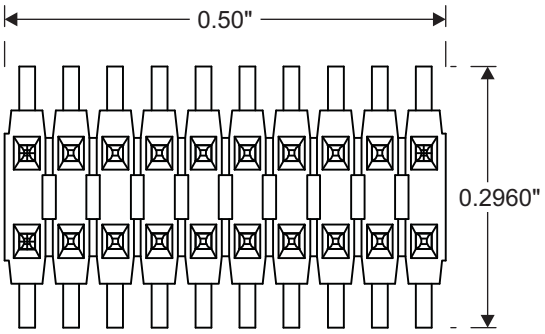


Figure 3. TI 20-Pin CTI Header

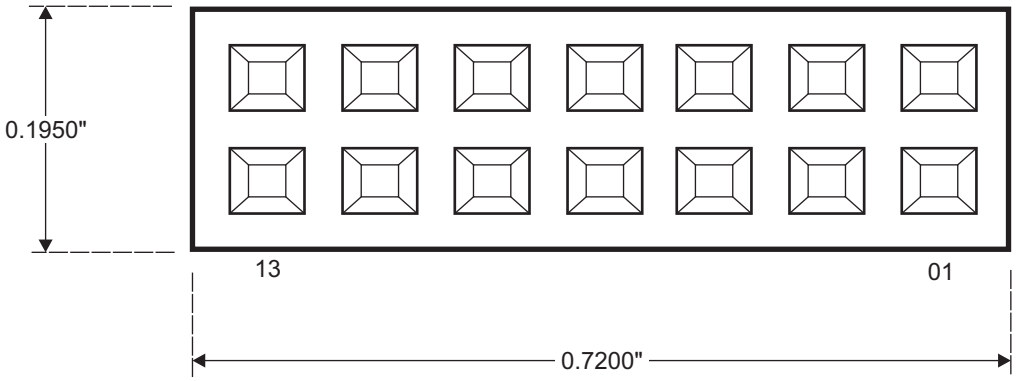


Figure 4. TI 14-Pin Traditional Through-Hole Emulation Interface

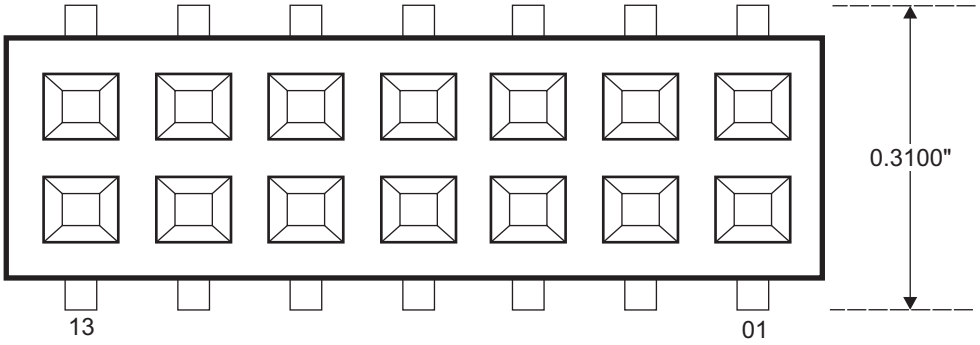


Figure 5. TI 14-Pin Traditional SMT Emulation Interface Header

Table 7. Summary: Header Footprint Comparisons

	Common Emulation Interfaces	Area (in square inches)	Notes
1	TI 60-pin	0.2720 in^2	Includes mounting pads
2	MIPI 60-pin	0.2471 in^2	Includes mounting pads
3	TI 20-pin CTI	0.148 in^2	Includes mounting pads
4	20-pin ARM™ ETM header	0.3451 in^2	Includes mounting pads
5	Original through-hole TI 14-pin connector form factor	0.2808 in^2	Includes both sides of PCB
6	Original TI 14-pin SMT connector form factor	0.2431 in^2	Includes mounting pads

7 Target Mating Caution

NOTE: All headers (emulator and target) should be examined for possible damage before being mated together. Damaged or bent pins may affect functionality and performance.

Never apply excessive force when mating connectors; if excessive force is required, the mating connector pairs are not aligned.

Table 8. Summary: Header Changes

1	Verify the target and emulator headers are intact and free of defects before mating.
2	Always use caution when mating connectors to ensure no damage occurs.
3	Verify connectors are parallel to one another before mating.

8 Header Pin Assignment

Table 9. TI 60-Pin Header Signal Naming Convention

Pin No.	Signal Name	Emulator Signal Direction	Notes
A1	GND[1]	-	Ground pin.
A2	GND	-	Ground pin.
A3	GND	-	Ground pin.
A4	GND	-	Ground pin.
A5	GND	-	Ground pin.
A6	GND	-	Ground pin.
A7	GND	-	Ground pin.
A8	TYPE0	Output	Type 0 is a No Connect.
A9	GND	-	Ground pin.
A10	GND	-	Ground pin.
A11	GND	-	Ground pin.
A12	GND	-	Ground pin.
A13	GND	-	Ground pin.
A14	GND	-	Ground pin.
A15	$\overline{\text{TGTRST}}$	Output	Even though the native TI 60-pin emulator (XDS560T) does not support the target reset function, other emulators, such as the XDS560 with the REV D cable do support this function. For compatibility, typically through the use of adapters, with emulators that support the target reset function it is recommended that on your target board this pin be pulled up with a 4.7-KΩ resistor.
B1	ID0	Input	Only header type 0000 is currently supported, where 0 is GND and 1 is a No Connect. All other combinations are reserved.
B2	TMS	Output	Connect to device pin of same name.
B3	EMU17[2]	Bidirectional	Connect to device pin of same name.
B4	TDI	Output	Connect to device pin of same name.
B5	EMU14[2]	Bidirectional	Connect to device pin of same name.
B6	EMU12[2]	Bidirectional	Connect to device pin of same name.
B7	TDO	Input	Connect to device pin of same name.
B8	TVD	Input	Chip I/O voltage current limited via 100-Ω resistor.
B9	EMU9[2]	Bidirectional	Connect to device pin of same name.
B10	EMU7[2]	Bidirectional	Connect to device pin of same name.
B11	EMU5[2]	Bidirectional	Connect to device pin of same name.
B12	TCK	Output	Connect to device pin of same name; may need to be buffered.
B13	EMU2[2]	Bidirectional	Connect to device pin of same name.
B14	EMU0[2]	Bidirectional	Connect to device pin of same name.
B15	ID1	Input	Only header type 0000 is currently supported, where 0 is GND and 1 is a No Connect. All other combinations are reserved.
C1	ID2	Input	Only header type 0000 is currently supported, where 0 is GND and 1 is a No Connect. All other combinations are reserved.
C2	EMU18[2]	Bidirectional	Connect to device pin of same name.
C3	$\overline{\text{TRST}}$	Output	Connect to device pin of same name.
C4	EMU16[2]	Bidirectional	Connect to device pin of same name.
C5	EMU15[2]	Bidirectional	Connect to device pin of same name.

(1) On some target applications, detection of the emulation pod is required. It is recommended that when this condition exists, pin A1 on the 60-pin header be used. Instead of grounding pin A1 on the target board, a pull-up resistor ≥ to 10K Ω should be connected to the pin. When the emulation pod header is connected, pin A1 will be grounded.

(2) The 60-pin header provides 19 EMU pins for advance emulation features. Not all devices support 19 EMU pins. Connect only the EMU pins present on the target DSP to the corresponding EMU pin on the header. Leave unused pins unconnected.

Table 9. TI 60-Pin Header Signal Naming Convention (continued)

Pin No.	Signal Name	Emulator Signal Direction	Notes
C6	EMU13[2]	Bidirectional	Connect to device pin of same name.
C7	EMU11[2]	Bidirectional	Connect to device pin of same name.
C8	TCKRTN	Input	Connect to either a loopback of the emulation header's TCK or a target device-supplied RTCK. If your target device has an RTCK signal, you must connect this signal to TCKRTN on the emulator header.[3]
C9	EMU10[2]	Bidirectional	Connect to device pin of same name.
C10	EMU8[2]	Bidirectional	Connect to device pin of same name.
C11	EMU6[2]	Bidirectional	Connect to device pin of same name.
C12	EMU4[2]	Bidirectional	Connect to device pin of same name.
C13	EMU3[2]	Bidirectional	Connect to device pin of same name.
C14	EMU1[2]	Bidirectional	Connect to device pin of same name.
C15	ID3	Input	Only header type 0000 is currently supported, where 0 is GND and 1 is a No Connect. All other combinations are reserved.
D1	NC	-	Not connected.
D2	GND	-	Ground pin.
D3	GND	-	Ground pin.
D4	GND	-	Ground pin.
D5	GND	-	Ground pin.
D6	GND	-	Ground pin.
D7	GND	-	Ground pin.
D8	TYPE1	Output	Type 1 must be connected to GND.
D9	GND	-	Ground pin.
D10	GND	-	Ground pin.
D11	GND	-	Ground pin.
D12	GND	-	Ground pin.
D13	GND	-	Ground pin.
D14	GND	-	Ground pin.
D15	GND	-	Ground pin.

[3] For additional notes, see Table 13.

Table 10. Summary: TI 60-Pin Header Pinout

1	Pin D1 should be left unconnected.
2	Pin A1, if required, enables or disables external multiplexers or buffers.
3	Only the appropriate trace pins should be connected.

The MIPI 60-pin header provides for up to four channels of independently clocked trace data, where the first channel of data can span up to 40 bits, the second channel can span up to 20 bits, and the third and forth channels can span up to 10 bits each. By overlaying the channel bit mapping, multiple configurations are provided such as four 10-bit ports, two 20-bit ports, or a 32-bit port and an 8-bit port. Since TI trace enabled emulators currently only support a single channel of data, the mapping to TI devices is currently for a single port. Future emulators may require a different mapping so always check the latest revision of this document before starting a new design using the MIPI 60-pin header.

The MIPI 60-pin connector also provides two level-dependent nTRST signals and trace and JTAG independent voltage references.

Note that not all TI devices use the EMU pin naming convention for designating trace pins. Devices that export only an ARM ETM trace port have a trace clock, trace control, and trace data pins. Typical pin designators are ETK_NAME and ETMNAME (where NAME is some variation of CLK, CNTL, and DATA). When connecting an ARM ETM port to the MIPI connector, trace clock is connected to TRC_CLK[0], trace control is connected to TRC_DATA[0][0], and trace data is connected to TRC_DATA[0][1] to TRC_DATA[0][n]. If your device has a *trace clock-in pin*, leave it disconnected or pull it up externally to increase noise immunity over the internal pull-up. Check with your emulator manufacturer on availability of ARM ETM trace support.

Table 11. MIPI 60-Pin Header Signal Naming Convention(1) (2)(3)

Pin No.	MIPI Name	Device Signal Name	Notes
1	VREF_DEBUG	JTAG IO V_{ref}	JTAG IO voltage reference current limited via 100-Ω resistor.
2	TMS/TMSC	TMS	
3	TCK	TCK	May need to be buffered.
4	TDO/EXTA	TDO	
5	TDI/EXTB	TDI	
6	nRESET	Connect to system reset	Open drain output from emulator; use 4.7-KΩ PU.(3)
7	RTCK/EXTC	RTCK	Connect to either a loopback of the emulation header's TCK or a target device-supplied RTCK. If your target device has an RTCK signal, you must connect this signal to RTCK on the emulator header.(3)
8	nTRST_PD	nTRST	It is expected that this pin be connected only to devices with internal PDs on their nTRST pins, or in cases where a PD is required externally on the device's nTRST pin (for PD information and requirements, see your device's data sheet).(4)
9	nTRST/EXTD	nTRST	nTRST is an open drain output. It is expected that this pin be connected only to devices with internal PUs on their nTRST pins, or in cases where a PU is required externally on the device's nTRST pin (for PU information and requirements, see your device's data sheet).(4)
10	EXTE/TRIGIN	NC	
11	EXTF/TRIGOUT	NC	

(1) The QSH-030 connector also has an additional 4 pins (61, 62, 63 and 64) used to connect the cable's ground shield to the target boards ground plane.
(2) Leave unused TRC_DATA and TRC_CLK pins unconnected.
(3) For additional notes, see Table 13.
(4) A device may be connected to either nTRST or nTRST_PD, not both at the same time.

Table 11. MIPI 60-Pin Header Signal Naming Convention[1] [2][3] (continued)

Pin No.	MIPI Name	Device Signal Name	Notes
12	VREF_TRACE	EMU IO Vref	EMU IO voltage reference current limited via 100-Ω resistor.
13	TRC_CLK[0]	EMU2	
14	TRC_CLK[1]	NC	
15	Target Presence Detect	Connected to GND thru 0 Ω	
16	GND	GND	
17	TRC_DATA[0][0]	EMU3	
18	TRC_DATA[1][0] or TRC_DATA[0][20]	NC	
19	TRC_DATA[0][1]	EMU0	
20	TRC_DATA[1][1] or TRC_DATA[0][21]	NC	
21	TRC_DATA[0][2]	EMU1	
22	TRC_DATA[1][2] or TRC_DATA[0][22]	NC	
23	TRC_DATA[0][3]	EMU4	
24	TRC_DATA[1][3] or TRC_DATA[0][23]	NC	
25	TRC_DATA[0][4]	EMU5	
26	TRC_DATA[1][4] or TRC_DATA[0][24]	NC	
27	TRC_DATA[0][5]	EMU6	
28	TRC_DATA[1][5] or TRC_DATA[0][25]	NC	
29	TRC_DATA[0][6]	EMU7	
30	TRC_DATA[1][6] or TRC_DATA[0][26]	NC	
31	TRC_DATA[0][7]	EMU8	
32	TRC_DATA[1][7] or TRC_DATA[0][27]	NC	
33	TRC_DATA[0][8]	EMU9	
34	TRC_DATA[1][8] or TRC_DATA[0][28]	NC	
35	TRC_DATA[0][9]	EMU10	
36	TRC_DATA[1][9] or TRC_DATA[0][29]	NC	
37	TRC_DATA[3][0] or TRC_DATA[0][10]	EMU11	
38	TRC_DATA[2][0] or TRC_DATA[1][10] or TRC_DATA[0][30]	NC	
39	TRC_DATA[3][1] or TRC_DATA[0][11]	EMU12	
40	TRC_DATA[2][1] or TRC_DATA[1][11] or TRC_DATA[0][31]	NC	
41	TRC_DATA[3][2] or TRC_DATA[0][12]	EMU13	
42	TRC_DATA[2][2] or TRC_DATA[1][12] or TRC_DATA[0][32]	NC	
43	TRC_DATA[3][3] or TRC_DATA[0][13]	EMU14	
44	TRC_DATA[2][3] or TRC_DATA[1][13] or TRC_DATA[0][33]	NC	
45	TRC_DATA[3][4] or TRC_DATA[0][14]	EMU15	
46	TRC_DATA[2][4] or TRC_DATA[1][14] or TRC_DATA[0][34]	NC	
47	TRC_DATA[3][5] or TRC_DATA[0][15]	EMU16	
48	TRC_DATA[2][5] or TRC_DATA[1][15] or TRC_DATA[0][35]	NC	
49	TRC_DATA[3][6] or TRC_DATA[0][16]	EMU17	
50	TRC_DATA[2][6] or TRC_DATA[1][16] or TRC_DATA[0][36]	NC	
51	TRC_DATA[3][7] or TRC_DATA[0][17]	EMU18	

Table 11. MIPI 60-Pin Header Signal Naming Convention[1] [2][3] (continued)

Pin No.	MIPI Name	Device Signal Name	Notes
52	TRC_DATA[2][7] or TRC_DATA[1][17] or TRC_DATA[0][37]	NC	
53	TRC_DATA[3][8] or TRC_DATA[0][18]	EMU19	
54	TRC_DATA[2][8] or TRC_DATA[1][18] or TRC_DATA[0][38]	NC	
55	TRC_DATA[3][9] or TRC_DATA[0][19]	NC	
56	TRC_DATA[2][9] or TRC_DATA[1][19] or TRC_DATA[0][39]	NC	
57	GND	GND	
58	GND	GND	
59	TRC_CLK[3]	NC	
60	TRC_CLK[2]	NC	

Table 12. TI 20-Pin CTI Header Signal Naming Convention

Pin No.	Signal Name	Notes
1	TMS	
2	$\overline{\text{TRST}}$	
3	TDI	
4	TDIS[1]	Connect to target GND.
5	VTRef	JTAG and EMU IO voltage reference current limited via 100-Ω resistor.
6	KEY	This pin may need to be cut to mate with the emulator's target cable.
7	TDO	
8	GND	
9	RTCK	Connect to either a loopback of the emulation header's TCK or a target device-supplied RTCK. If your target device has an RTCK signal, you must connect this signal to RTCK on the emulator header.[2]
10	GND	
11	TCK	May need to be buffered.
12	GND	
13	EMU0	
14	EMU1	
15	$\overline{\text{RESET}}$	Open drain output from emulator, use 4.7-KΩ PU.[2]
16	GND	
17	EMU2	
18	EMU3	
19	EMU4	
20	GND	

(1) A pulldown or current-limiting resistor on TDIS will not work with all XDS models. With TDIS connected directly to GND, some XDS models will sink a small amount of current (by design) through a pullup in the XDS. A pulldown or a current-limiting resistor connected to TDIS on the target may cause the XDS to not detect the target and result in a "far cable break" error.

(2) For additional notes, see Table 13.

Table 13. Summary: Header Pin Assignments

1	EMU0 and EMU1 should always be treated as bidirectional signals. For bidirectional debug port functions, check your device data sheet. Other EMU pins may also be bidirectional, but typically they are used for unidirectional core and system trace export.
2	If your target card contains multiple devices with RTCK pins see the *Adaptive Clock* article at http://tiexpressdsp.com/index.php/Adaptive_Clocking.

Table 13. Summary: Header Pin Assignments (continued)

3	The $\overline{\text{TGTRST}}$, nRESET, and $\overline{\text{RESET}}$ signals are open drain outputs that can be integrated into your card's POR circuit, in which case (if supported by the emulator), it may allow you to reset your entire board through the emulator. This feature is supported by the XDS560 with the rev. D cable and the XDS560 v2 System Trace emulator. The XDS560T does not support this feature.

Figure 6 is a top view of Texas Instruments' 60-pin emulation header, illustrating the orientation and pin location of the 60-pin emulation header. For specific pin assignments, see Table 9. Texas Instruments' emulation and debug pod incorporates a pin 1 (red dot) locator on the emulation and debug pod (Figure 7). Alignment with the pin 1 of the target board header is critical.

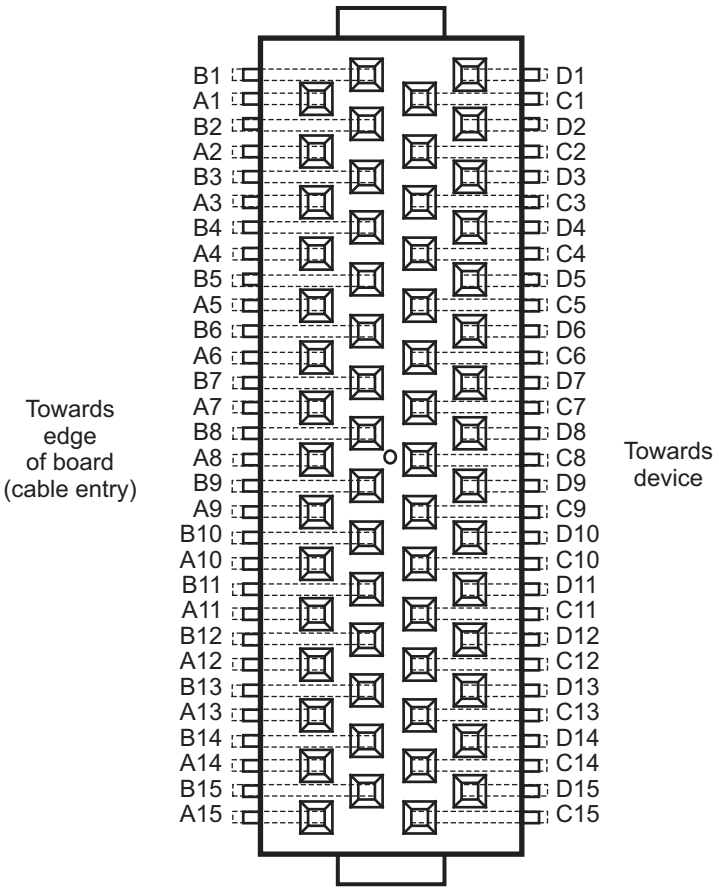


Figure 6. 60-Pin Header Orientation

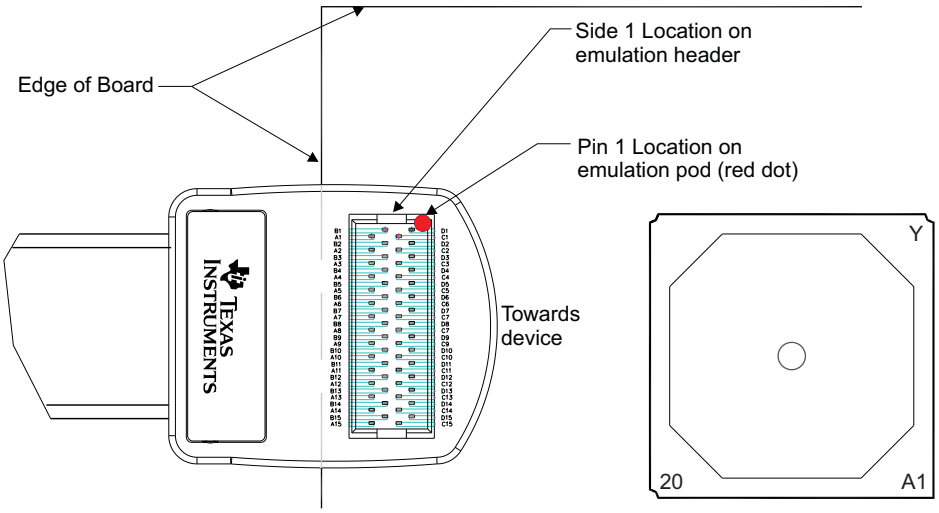
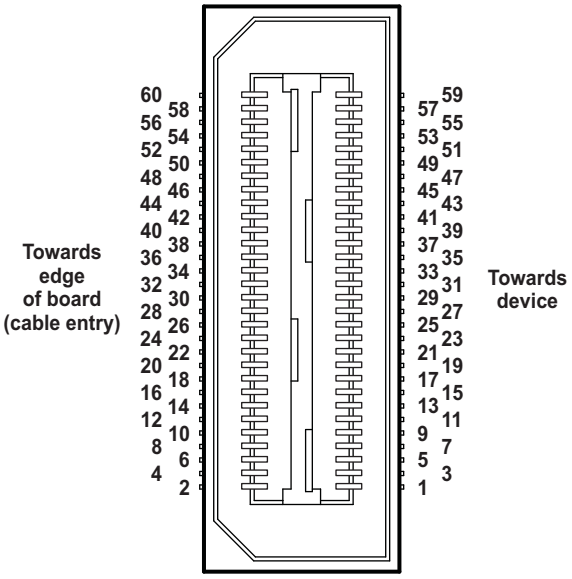


Figure 7. Emulator Cable Connector Superimposed Over 60-Pin Header

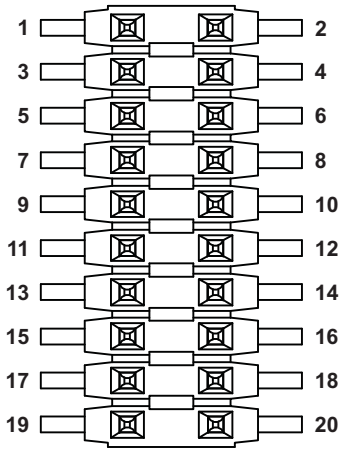
Figure 8 and Figure 9 are top views of the MIPI 60-pin and TI 20-pin CTI emulation headers, respectively. These illustrations show the orientation and pin location of the emulation headers.



Note:

- The QSH-030 connector also has an additional 4 pads; one of which, at a minimum, must be used to connect the cable's ground shield to the target boards ground plane.
- The QSH-030 connector is keyed so unlike the TI-60 connector there is no way to install it backwards.

Figure 8. MIPI 60-Pin Header Pin Location



Note: Pin 6 may need to be cut to mate with the emulator's target cable.

Figure 9. TI 20-Pin CTI Header Pin Location

9 Electrical Requirements

This section describes the basic electrical requirements. Deviation from these requirements may result in performance degradation.

Table 14 defines the chip pin input pull-up and pull-down characteristics.

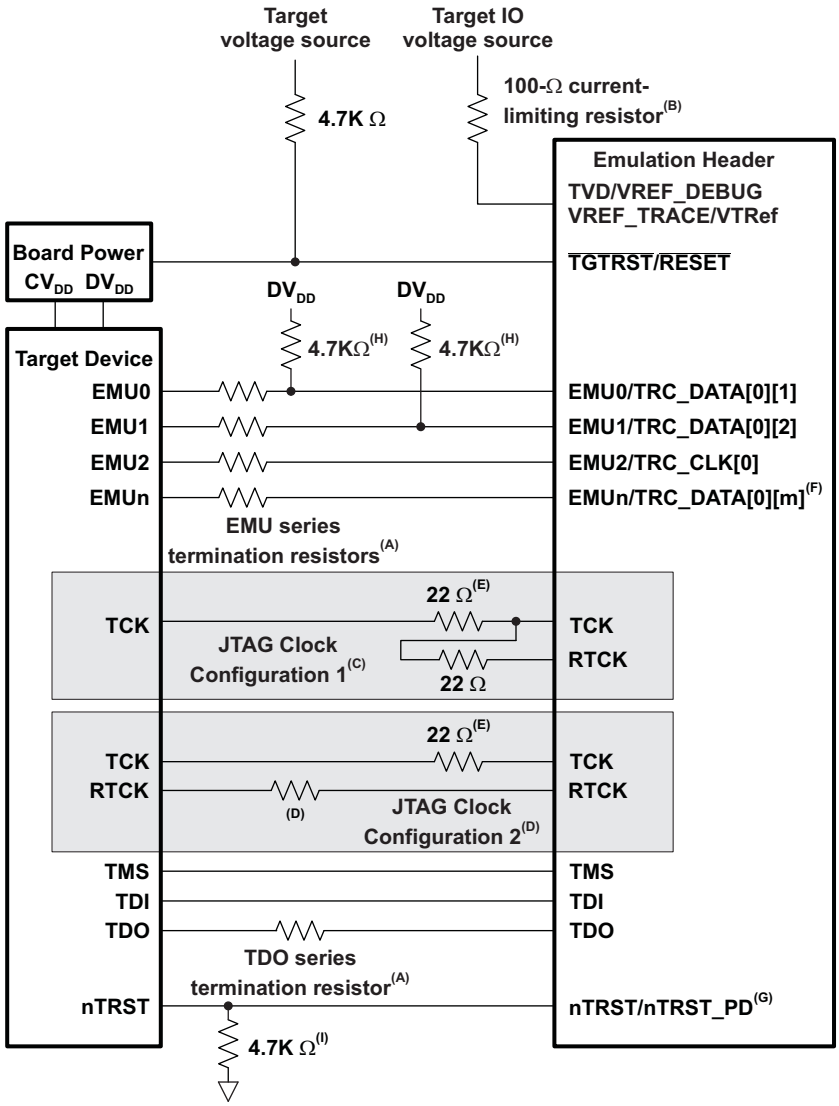
Table 14. JTAG Signal Directions

Signal Name	DSP Direction	Notes
EMU[N](1)	Bidirectional	Pull-up within device per device data sheet
TCK(2)	In	Pull-up within device per device data sheet
TDI(2)	In	Pull-up within device per device data sheet
TDO	Out	Pull-up within device per device data sheet
TMS(2)	In	Pull-up within device per device data sheet
$\overline{\text{TRST}}$ (2)	In	Pull-down within device per device data sheet

(1) Varies by device type, see the device data sheet for actual number of EMU pins.

(2) Internal device pull-ups and pull-downs are typically weak (~30K Ω). Your application may require stronger external pull-ups or pull-downs to improve noise margins on the JTAG input signals (TMS, TDI, TCK, $\overline{\text{TRST}}$) and EMU signals when an emulation cable is not connected.

In cases where your target board contains a single device that is connected to the emulation header and the emulation header is positioned within 3" of the target device, Figure 10 shows the basic connection for unbuffered signals.



Note: All routing distances from the device pins to the emulation header must be less than 3 inches.

A To select EMU and TDO series termination resistor values, see Section 10. The EMU and TDO series termination values should be placed within 0.5" of the device with total routing length not to exceed 3".

B If using a MIPI 60-pin connector, VREF_DEBUG and VREF_TRACE provide independent voltage sources for JTAG and EMU pins.

C If your target device does not have an RTCK pin, loopback TCK is supplied by the emulation header to RTCK per Configuration 1.

D If your device supports an RTCK pin, then connect the device's RTCK to the emulation header's RTCK per Configuration 2 and follow the instructions in Note A to size and place RTCK's series termination resistor.

E On JTAG signals that are inputs to the device, place 22-Ω series termination resistors in close proximity to the emulation header.

F For the MIPI 60-pin header the mapping between EMU and TRC_DATA signals is not one-to-one. For the correct EMU to MIPI 60-pin mapping, see Table 11.

G If using the MIPI 60-pin connector, see Table 11 for notes on nTRST and nTRST_PD use.

H Pull-ups on EMU0 and EMU1 may be optional. For cases where external pull-ups are required or should be considered, see the XDS Target Connection Guide. If you decide pull-ups are needed on EMU0 and EMU1 keep the length of the trace route from the EMU pin to the pull-up to a minimum.

I A pull-down on nTRST may be optional. For cases where an external pull-down is required or should be considered, see the XDS Target Connection Guide.

Figure 10. Target Connection for Unbuffered JTAG and EMU Signals

Table 15. Summary: Electrical Requirements

1	Always refer to the device data sheet for number and connectivity of EMU pins.
2	Leave unused EMU pins unconnected.

10 Single-Processor Termination

The information provided in this section applies to a single-processor system. For multi-processor configurations, see Section 18.

Current emulators operate the JTAG's clock in the 10-MHz to 50-MHz range, but future emulators will operate at higher clock rates. Thus, to provide some design margin for duty cycle distortion and compatibility with future emulators, TI recommends designing JTAG signals for 100-MHz operation.

Core trace currently operates with transfer rates as high 333 Mbits/sec, with 167-MHz DDR clocking and rise and fall times in the 250-1000 picoseconds range. System trace operates with transfer rates of 250 Mbits/s with 125-MHz DDR clocking. To provide some design margin for duty cycle distortion, TI recommends designing EMU signals for trace as 200-MHz clock signals.

The following termination information assumes that the impedance of the PCB traces from the DSP to the emulation header is controlled and is between 50 and 55 Ω. The ideal series termination resistor value for a single device connected to any EMU or JTAG output signal is determined by the following equation:

$Z_{Cable} - Z_{Device\_Output} = Z_{Termination\_Resistor}$

The impedance of the XDS560T and XDS560 V2 System Trace cables is 50 Ω.

Follow the guidelines in Table 16 to determine the placement and size of series termination resistors for the JTAG and EMU signals on your target board. For output pins you will need to know the impedance of the pin's buffer. To determine this, see Appendix G.

Table 16. Termination Values and Use Cases

Signal Name	Notes
TDO	Must be placed as close as possible to the pin on the device, not to exceed 1" trace length from the pin. Since TDO is a device output, use the equation $Z_{Cable} - Z_{Device\_Output} = Z_{Termination\_Resistor}$ to determine the proper termination resistor value.
TCKRTN/RTCK	If your device does not have an RTCK pin and the TCKRTN/RTCK signal is not buffered, this signal is routed from the emulation header's TCK with a 22-Ω series resistor using a routing length as short as possible. If your device has an RTCK pin and the TCKRTN/RTCK signal is not buffered, this signal is routed from the device's RTCK with a series termination resistor, sized using the equation $Z_{Cable} - Z_{Device\_Output} = Z_{Termination\_Resistor}$ and using a routing length as short as possible. If TCKRTN/RTCK is buffered, see Figure 26; if unbuffered, see Figure 27; and if there is a direct connection to the device's RTCK, see Figure 28.
TCK	100 Ω in series with 8.2-pF parallel termination to ground for buffered TCK configuration (Figure 26). Use a 22-Ω series termination (near header) for unbuffered configuration (Figure 27). Values should be modeled to ensure proper value.
EMU[N:2]	Must be placed as close as possible to the EMU pin on the device, placement should not exceed 1" trace length from the pin at the DSP (see Figure 29). To determine the proper termination resistor value, use the equation $Z_{Cable} - Z_{Device\_Output} = Z_{Termination\_Resistor}$.
EMU[1:0]	Must be placed as close as possible to the EMU pin on the device, placement should not exceed 1" (0.5" recommended) trace length from the pin of the DSP. If a TI 14-pin header is used in parallel, a separate series termination resistor must be used to route these signals to the TI 14-pin header, see Figure 31. To determine the proper termination resistor value, use the equation $Z_{Cable} - Z_{Device\_Output} = Z_{Termination\_Resistor}$.

For additional information on the trace lengths and impact of termination location, see Section 16 and Appendix B.

Table 17. Summary: Single-Processor Terminations

1	Use of termination resistors on JTAG device output signals and EMU pins used for core trace or system trace required.
2	Alternate termination values should be used if indicated by detailed modeling.
3	Model all critical nets to ensure termination values are correct.

Table 17. Summary: Single-Processor Terminations (continued)

4	Placement of indicated terminations is critical.

11 Buffering

If buffers are used, they should be selected based on the device source impedance and the potential load(s). In applications where multiple devices are used, selection of buffers and signals to be buffered are critical.

When buffering signals, it is imperative that timing, propagation delay, sink and source currents, and general buffer characteristics be considered.

See Appendix B for additional information on the buffering, location, and type of buffers to be used.

Table 18. Summary: Buffering

1	Buffer signals based on loading and signal integrity.
2	In most cases, a single target board is better than a target board with daughter cards consisting of multiple headers.
3	Timing is a critical consideration for all active signals.
4	Model all critical nets to ensure termination values are correct.

12 General Specifications

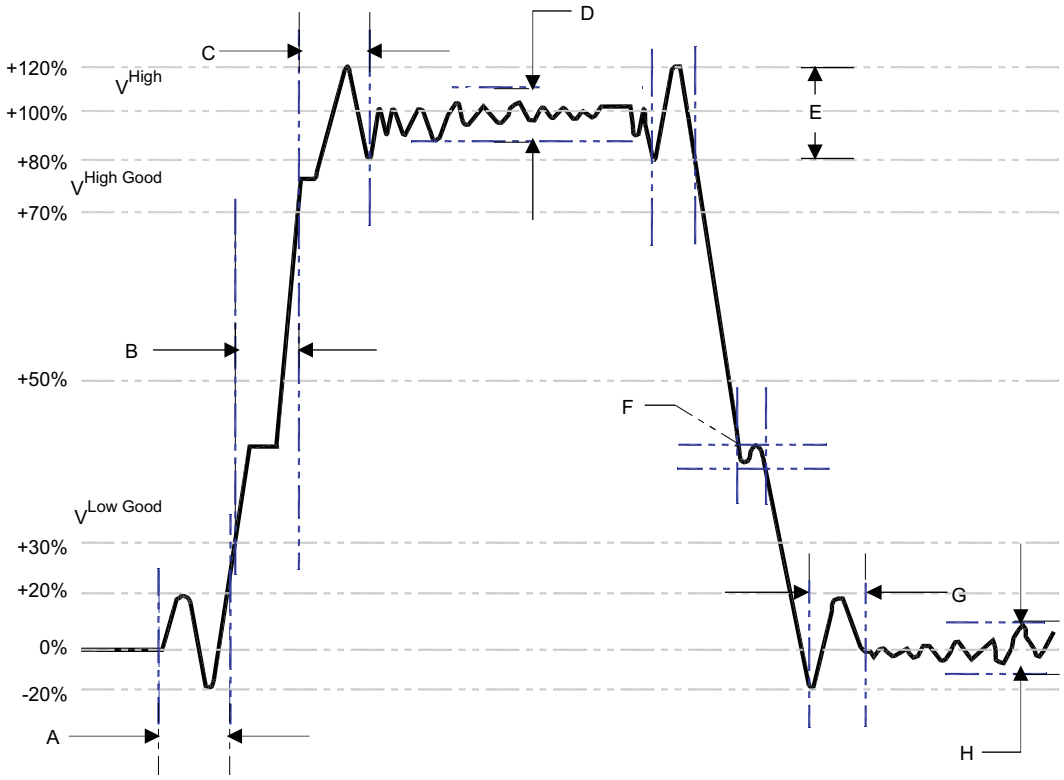
General specifications are shown in Table 19.

Table 19. General Specifications

Item	Description/Specification
Impedance	Target board impedance should be in the range of 50 Ω (±5Ω).
Connector Spacing	Maximum distance from header pin to respective emulation pin on DSP equals 3.0-inch trace length.
Signal Skew	For EMU signals, skew induced by the board should be 200 ps maximum between signals.
Capacitance	Maximum capacitance loading per pin (inclusive of all vias and components) equals 20 pF.
Signal Interconnect	Number of vias, not more than 2, and must be within the capacitive loading specified above.
Clock Source	The emulator must be provided a clock source through the header's TCKRTN or RTCK pin. For board requirement details, see Section 8 and Section 9.
Voltage Source	TVD (TI 60-pin header), VREF_DEBUG and VREF_TRACE (MIPI 60-pin header), and VTRef (TI 20-pin CTI header) require a current-limited customer-supplied voltage reference source.
Voltage Range	The XDS560T is designed to operate between 0.8 V to 5.0 V. The XDS560 v2 System Trace emulator is designed to operate in the 1.2-V to 3.3-V range.
Orientation Detect	The MIPI 60-pin header is self-aligning and cannot be installed backwards. The TI 20-pin CTI connector uses pin 6 as an orientation key that may need to be removed. On the TI 60-pin connector pin A8 is a NC; pin D8 must be connected to GND.
Vertical Connector Clearance	For TI 60-pin connector clearance, see Figure 16; for the MIPI 60-pin connector clearance, see Figure 17.
Horizontal Connector Clearance	Clearance surrounding the TI 60-pin emulator connector should be per Figure 18 and Figure 20. Clearance surrounding the MIPI 60-pin header should be per Figure 19 and Figure 21.
Signal Frequency	EMU signals should be designed to operate as 200-MHz clocks and JTAG signals should be designed to operate at 100 MHz.
Rise and Fall times	All rising and falling edges are assumed to be within 500-1500 picoseconds.

13 Acceptable Signal Qualifications

The criteria for determining an acceptable signal waveform during simulation at the emulator's input buffer or in actual application are illustrated in Figure 11. All percentages listed are with respect to the V^{High} reference levels (LVTTL 3.3 V).



A Details the maximum amount of reflection, or perturbations that may occur on the rising edge (pre-shoot). The magnitude of the reflections or perturbations should be less than 20% of V^{High}.

B Details the critical signal switching region. No inflections greater than 10% of the rise time or 5% greater than V^{High} are allowed. It is preferred that the signal be able to increase monotonically.

C Details the region of the rising edge above the critical signal switching area. Inflections and/or perturbations are allowed within this region as long as they do not exceed 20% of V^{High} or a duration less than the rise time of the pulse.

D Details the top of the pulse. The amplitude of all noise, crosstalk and other perturbations should be less than 10% of V^{High}. For a 3.3 V signal, the amplitude should not exceed 165 mV.

E Details the maximum amount of reflection, or perturbations that may occur on the falling edge. The magnitude of the reflections or perturbations should be less than 20% of V^{High}.

F Details the critical signal-switching region. No inflections greater than 10% of the fall time or 5% greater than V^{High} are allowed. It is preferred that the signal be able to decrease monotonically.

G Details the region of the falling edge below the critical signal switching area. Inflections and/or perturbations are allowed within this region as long as they do not exceed 20% of V^{High} or a duration less than the fall time of the pulse.

H Details the bottom of the pulse. The amplitude of all noise, crosstalk and other perturbations should be less than 10% of V^{High}.

- Duty cycle distortion should be less than 5%.
- All waveforms should be treated as dual edge clocks.
- Rise and fall times should be symmetrical.
- Switching thresholds are assumed to be 50% of V^{High}.

Figure 11. Acceptable Wave Form Criteria

Table 20. Summary: Acceptable Signals

1	Calculate reflections to verify they will not fall within the switching regions.
2	Perturbations should not exceed 20% of V^{High}.
3	Rise and fall times should be symmetrical.
4	The duration of overshoots should not exceed 20% of V^{High} or less than the rise time of the pulse.
5	Noise and crosstalk should not exceed 10% of V^{High} or 165 mV for a 3.3 V signal.
6	All wave forms should be treated as dual edge clocks.

Table 20. Summary: Acceptable Signals (continued)

7	Duty cycle distortion should be less than 5%.
8	Switching thresholds are assumed to be 50% of V^{High}.

14 Connecting Alternate Headers

Traditional target designs commonly incorporated multiple headers. However, with the advent of higher speed devices and faster off-chip emulation, it is strongly recommended that newer designs only use a single emulation header.

XDS100 and XDS510 class emulators typically operate at a maximum frequency of 10.368 MHz, where the XDS560, XDS560T, and the XDS560 v2 System Trace emulators can operate in the 35- to 50-MHz range. Future emulators will support JTAG clock rates in the 75- to 100-MHz range. More importantly, core trace can operate EMU pins at 333 Mbits/s (using 167-MHz dual-edge clocking) while system trace can operate EMU pins in the 167- to 250-Mbits/s (83- to 125-MHz dual-edge clocking) range.

For devices that support core trace or system trace, we do not recommend routing the EMU pins used for these functions to multiple headers.

If multiple headers are used for JTAG connections, consider how the alternate header's net lengths, timing, and the effect of stubs will impact performance and signal integrity.

Regardless of the number of alternate headers, only a single emulator may drive the JTAG pins of a device. Appendix C shows the recommended circuit for enforcing a single emulator connection.

14.1 TI 14-Pin and 60-Pin Headers in Parallel

If a board is designed with both (two and more) headers; for example a TI 14-pin and 60-pin header, the signals should be connected as shown in Figure 12. Each figure represents a split termination configuration. The traces should be kept as short as possible. The distance from the terminations and the pins on the DSP must not exceed a 0.5 inch trace length. EMU[0] and EMU[1] are terminated in the same manner as TDO (for recommended terminations, see Figure 12). The EMU[2]-EMU[n] terminations are not shown because they are not supported by the TI 14-pin header.

NOTE: For determining proper termination values, see Section 10.

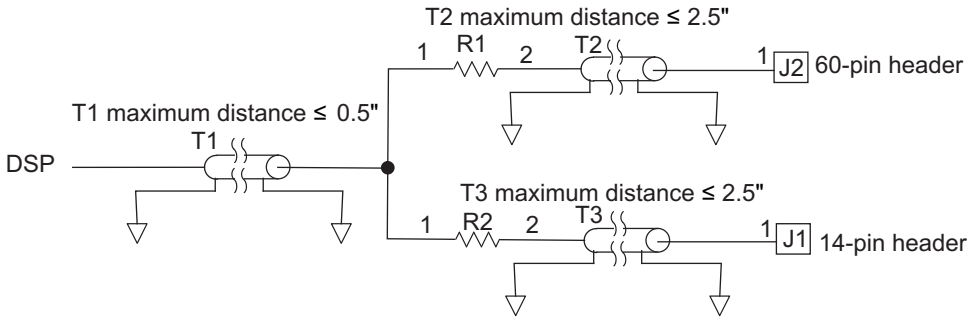


Figure 12. Multi-Header EMU0, EMU1, TDO Termination

Final termination values should be selected based on signal quality. Examine all signals against simulations and functional application. All nodes (see Figure 13) should have symmetrical lengths to the terminations to prevent reflections.

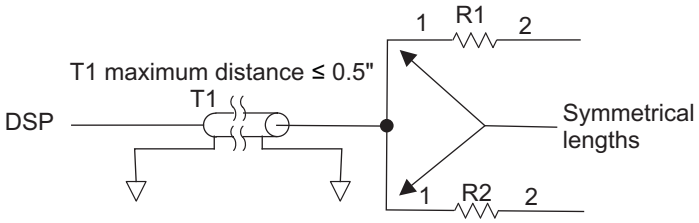


Figure 13. Symmetrical Nets

Table 21. Summary: TI 14-Pin and 60-Pin Headers in Parallel

1	The series termination closest to the DSP should be closer than 0.50".
2	Traces originating at nodes should have symmetrical lengths.
3	The maximum distance originating from the node to the respective header should not exceed 1.5" in length.
4	Final termination values must be based on simulation and functional testing.
5	All terminations and nets should be void of stubs.

15 Layout and Routing Requirements

15.1 Maximum Recommended Distances

The layout requires certain specifications. Figure 14 illustrates the maximum recommended routing distance between the header pin and respective DSP EMU (emulation trace) pin. All emulation signals should be treated as a separate net class and routed accordingly. Take special care to meet the skew specifications. Figure 14 shows a TI 60-pin connector orientation to a device such that the device's farthest EMU pin is no more than 3" from the corresponding header pin. Figure 15 shows a MIPI 60-pin connector orientation. In both figures the orientation provides for a left side cable entry.

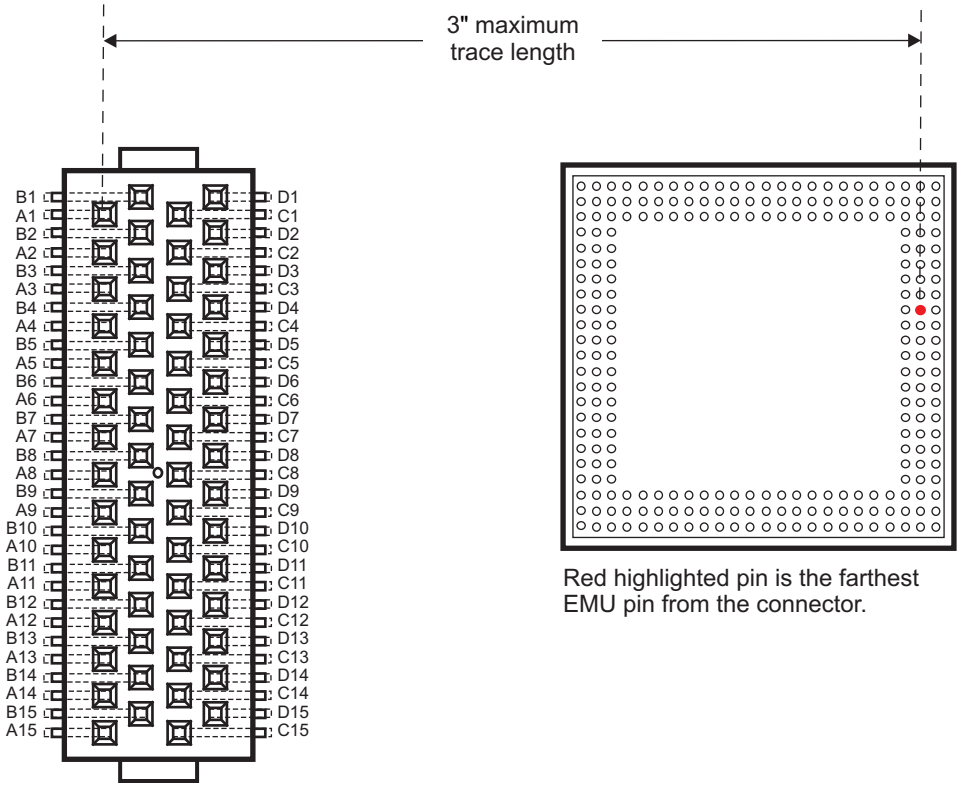
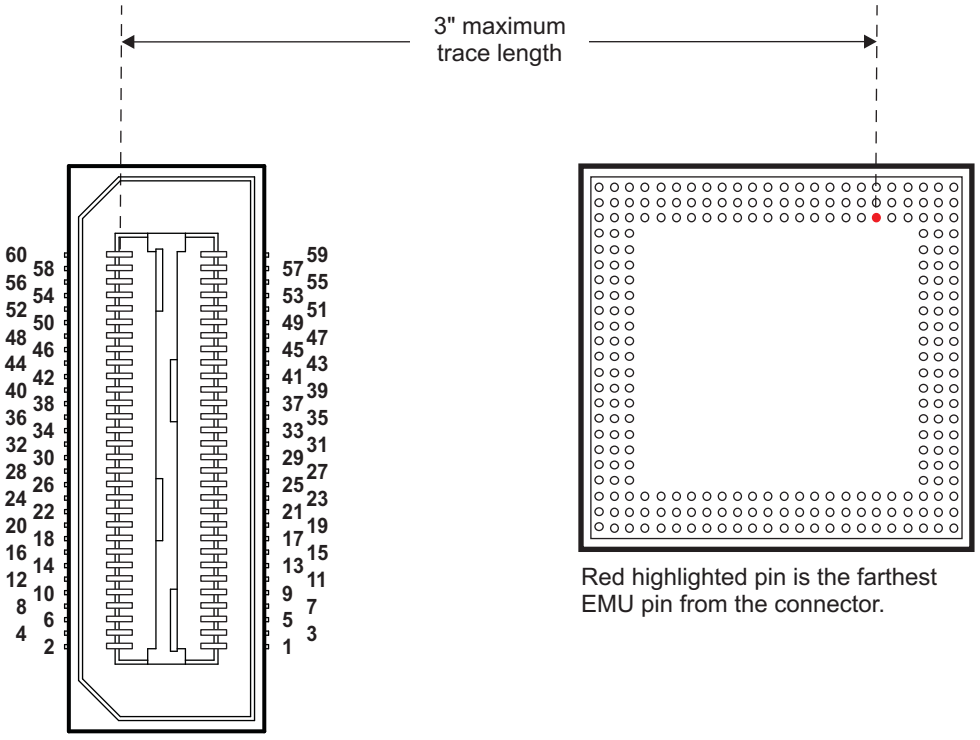


Figure 14. TI 60-Pin Connector Maximum Trace Length



Note: Orient the pin 1 side of the MIPI 60-pin connector to the target device or devices.

Figure 15. MIPI 60-Pin Connector Maximum Trace Length

16 Advanced Emulation - Layout and Route Distance Deviations

16.1 Signal-to-Signal Clearance

Consider routing key emulation or clock signals when laying out your target board with respect to the emulation header. The potential for signal noise, crosstalk, and coupling increases with the high frequency of TI's trace-enabled emulators. To minimize this variable, route all clock and emulation (EMU) signals with a minimum of a 5 mil (0.005") clearance, although 6 mil (0.006") is preferred.

16.2 PWB Routing Lengths

Regardless of the configuration (for configuration descriptions, see Section 18), the maximum recommended PWB routing length between a processor's EMU pin and the corresponding EMU pin on the target connector should be no more than 3". For multiple processor configurations, EMU0 and EMU1 may be used for global breakpoints and as cross triggers between devices that are in the JTAG scan chain but may or may not be connected for core or system trace. In this case, you may need to exceed the recommended maximum routing length when using an EMU pin for cross triggers or global breakpoints, possibly making these pins unusable for trace. In this case, core trace and system trace can typically be dedicated to EMU pins not used for global breakpoints or cross triggers by either shifting trace to the higher order EMU pins (if supported by your device) or by reducing the number of pins used for trace which, in turn, reduces the bandwidth available for trace. If your device supports more than 12 EMU pins, then shifting trace to higher-order bits may be an option, otherwise reducing the number of pins available for trace may be your only option.

PWB routing length considerations take on two key variables: propagation and skew.

Propagation involves the distance between the header and the respective pin on the DSP. Excessive PWB routing lengths present a problem, specifically with reflections. The key to minimizing the impact of reflections is to minimize PWB routing lengths. When possible, lay out critical signals such that they propagate between the insertion and terminating points in a period of time that does not result in the reflected energy occurring in the switching region or the additive effect of multiple reflections does not fall in the switching regions on either the rising or falling edge. All active PWB routing lengths (specifically for emulation, JTAG, and clock signals) should not exceed 3 inches in length. Lengths in excess of 3 inches increase the risk of reflections occurring in the critical regions of the signal waveform.

The remaining PWB routing length variable is signal skew. For the purposes of this document, signal skew is the difference between the minimum and maximum propagation delays (T_{pd}) for a net class (grouping of signals belonging together). In most high-speed applications, such as TI's trace supported emulators, skew is as important as propagation delays. TI's trace supported emulators accommodate a certain amount of skew; however, excessive skew greater than 200 ps (or 1.1" for FR4) introduced during layout and routing may reduce performance.

Excessive skew or propagation delays increase the risk in potential bit errors, loss of data or faulty operation. Figure 14 and Figure 15 illustrate the recommended header distance from the target processor.

While considering the routed length implications of propagation and skew, also consider the total circuit. Most traditional board designers are concerned with only the routes on their board. However, the target board is only one of three critical components of the typical emulation system. The interconnecting pod assembly and emulator are the other critical components. Consider all three components when designing a high-speed functional system.

The advanced emulation pins from the DSP to the header are grouped and routed as a net class to constrain the skew for all EMU[0] through EMU[n] signals. Emulation signals on the target board must be short because of the timing constraints. The distance for the EMU[n] net class of signals can also be interpreted as a maximum routed distance of 3 inches; this is inclusive of all supporting logic in each signal path on the target board.

Appendix E and Appendix F provide models representing the XDS560T and XDS560 v2 System Trace interconnect logic. Deviations from the recommended route distances, loading, or skew must be evaluated using the representative model to ensure optimum frequency operation and overall performance.

Table 22. Summary: Advanced Emulation Layout and Routing

1	All high speed emulation signals (CLKS and EMU) should be spaced a minimum of 5 mil from other signals.
2	PWB routing lengths for all clock and EMU signals should not exceed 3" maximum.
3	Skew between signals within a net class should not exceed 200 ps.
4	Layout and routing should also take into account the emulator and target.
5	PWB routing should have a character impedance of 50 Ω.

17 Traditional JTAG Emulation Layout and Route Distance Deviations

Layout and routing considerations include traditional JTAG signals, such as TDI, TDO, TMS, TCK, and TCKRTN/RTCK. The greater the distance (or skew) between the header and the target processor, the greater the potential for timing errors (set up and hold, etc.). Skewing routed signals such as TCK and TDI, or TDO and TCKRTN/RTCK, dramatically reduces the margin of setup timing to and from the target processor. Figure 14 and Figure 15 illustrate the recommended header distance from the target processor.

As with the advanced emulation features described above, the routed length is equally, if not more important. Traditional JTAG signals, especially in the interconnecting pod, may serve other purposes in future devices. The interconnecting pod assembly has a significant amount of support logic that contains a large portion of the allotted quota of the routed distance. That, coupled with the induced cable propagation delay, requires that the traditional JTAG emulation signals be short.

As stated previously, traditional board designers typically concern themselves with only the routes on the board they are designing. The basic emulation signals are critical, not because of their high speed, but because of their unique timing characteristics. As the TCK and TCKRTN/RTCK rates increase, the margin for setup and hold times decrease, so both must be considered when designing a high speed functional system.

The distance for the traditional JTAG emulation signals is inclusive of all supporting logic in each signal path on the target board. A model representing the pod interconnect logic is provided in Appendix E for the TI 60-pin cable and Appendix H for the MIPI 60-pin cable. Deviations from the recommended route distances, loading, or skew must be evaluated using this representative model to ensure optimum frequency operation and overall performance.

NOTE: Follow routing guideline for best operating frequency

Failure to follow the above routing guideline may result in a severely reduced operating frequency, resulting in lost bandwidth or the inability of the advanced features to function at full speed.

17.1 Layout and Routing - Mechanical Considerations

In addition to routing and layout considerations and electrical clearances, certain mechanical clearances must be observed and followed.

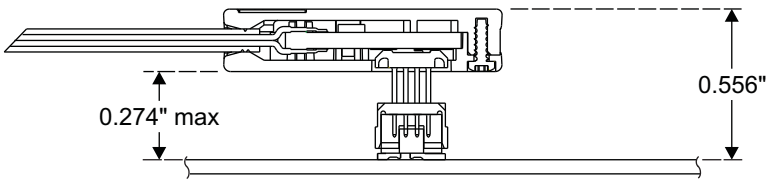


Figure 16. XDS560T TI 60-Pin Target Cable Connector Minimum Clearance - Height

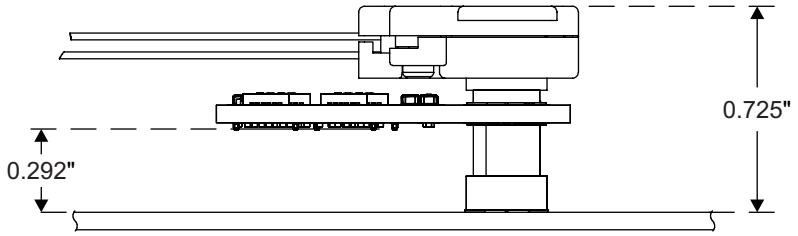


Figure 17. XDS560 v2 System Trace MIPI 60-Pin Target Cable Connector Minimum Clearance - Height

Figure 18 and Figure 19 illustrate the top view of the emulation and debug pod header enclosure; additional spacing is required for installing and removing the pod target connector and for clearance of the emulator cable assembly.

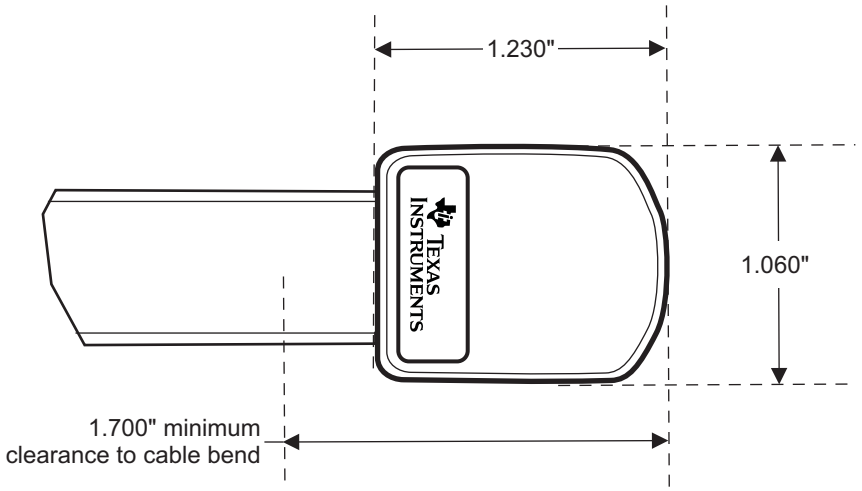


Figure 18. XDS560T TI 60-Pin Target Cable Header Dimensions

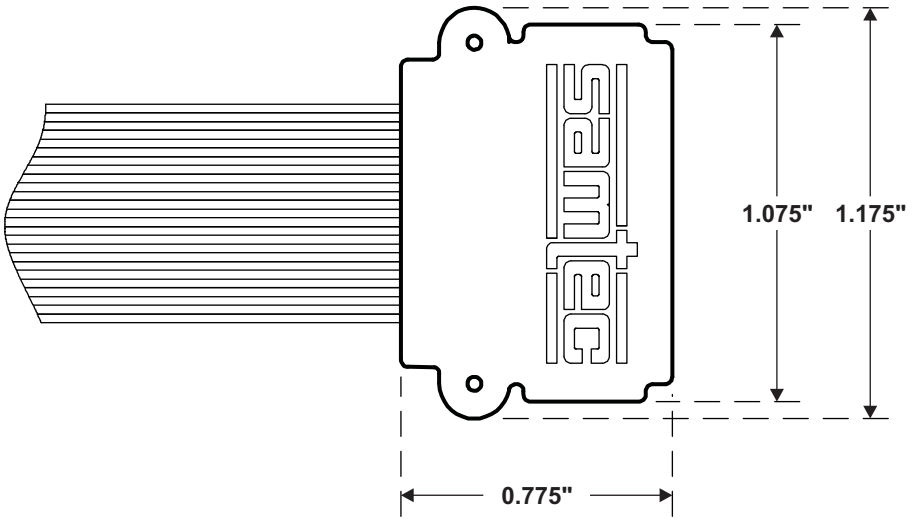


Figure 19. XDS560 v2 System Trace MIPI 60-Pin Target Cable Header Dimensions

The TI 60-pin target cable clearance area includes optional space on each side of the connector for griping the connector (see Figure 20). Given the connector housing is 0.274" off of the plane of the board, this space may be used by components that do not exceed the 0.274" height without impacting the ability to install or remove the connector.

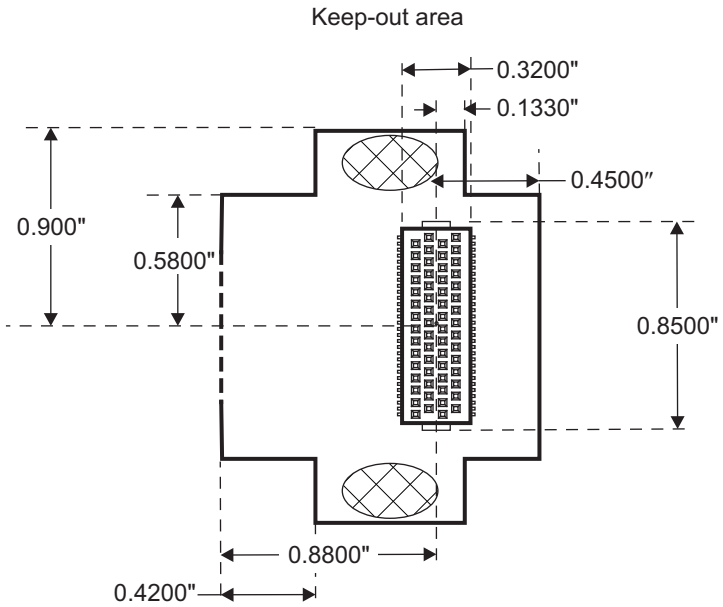


Figure 20. XDS560T TI 60-Pin Target Cable Board Keep-Out Area

Table 23. Summary: Layout and Routing - Mechanical Considerations (TI 60-Pin)

1	The maximum height of components in the keep-out area cannot exceed 0.274".
2	The basic area of concern beneath the pod header is 1.8" × 1.33".

The MIPI 60-pin target cable clearance area includes optional space on each side of the connector for griping the connector (see Figure 21). Given the cable's adapter board is 0.292" off of the plane of the board, this space may be used by components that do not exceed the 0.292" height without impacting the ability to install or remove the connector.

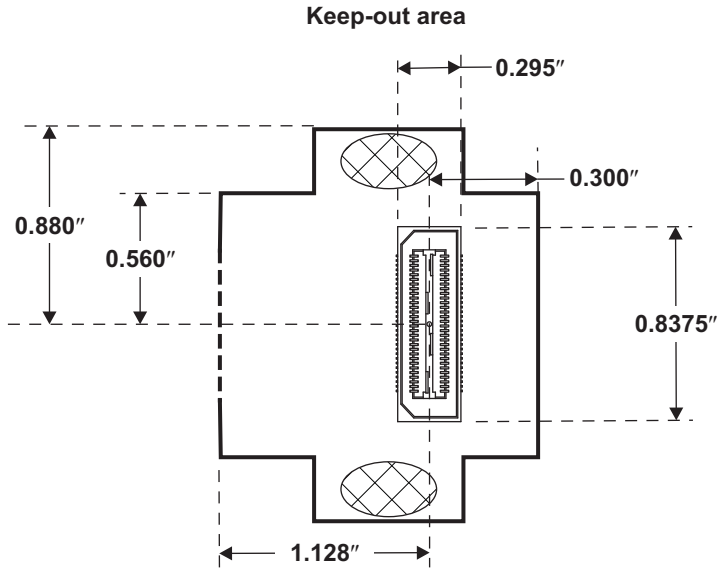


Figure 21. XDS560 v2 System Trace MIPI 60-Pin Target Cable Board Keep-Out Area

For mechanical specifications that may deviate from this guide, see your specific emulator manufacturer's documentation.

Table 24. Summary: Layout and Routing - Mechanical Considerations (MIPI 60-Pin)

1	The maximum height of components in the keep-out area cannot exceed 0.292".
2	The basic area of concern beneath the pod header is 1.76" × 1.428".

18 Multiple Device Considerations

There are three supported multiple device configurations: single trace, independent trace, and parallel trace. The single trace configuration allows for multiple devices to be connected to the JTAG serial scan chain, but only a single device connected to the emulation connector's EMU pins for trace support. Use this configuration if you are only interested in trace data from a single device or if the EMU signal routing to the other devices exceed the recommended lengths. Independent trace requires an emulation socket per device and should be utilized in cases where you need to observe trace from multiple sources simultaneously (using multiple emulators) or if the distance between processors and the emulation connector exceeds the recommended routing lengths. Parallel trace allows up to four devices to be connected to the emulation header's EMU pins for trace as long as the longest EMU signal route does not exceed the maximum recommended length while allowing additional devices to be connected to the serial scan chain. Any combination of these configurations may be deployed within a system as long as there is a single independent serial JTAG scan chain per emulation connector.

Figure 22 illustrates the basic single trace device interconnection method. This configuration supports global breakpoints and cross triggering using EMU0 and EMU1 routed in parallel between all processors. It also supports synchronous execution control by daisy-chaining the JTAG signals between processors, and advanced emulation capabilities with EMU[2:n] for a single processor. If the routing lengths for EMU0 and EMU1 exceed 3", they may not be usable for trace. For more details on EMU pin and trace options, see Section 16.2, *PWB Routing Lengths*. Given the source current capability of the individual devices, a maximum of 30 devices on the JTAG serial scan chain or for parallel routing of EMU0 and EMU1 should not be exceeded. Exceeding this number of devices may severely impact performance. When designing target systems with a large number of devices, always minimize the number of vias and trace lengths, and pay special attention to the lengths of individual trace stubs. For more information on sizing termination resistors, see Section 10.

Figure 22, Figure 23, and Figure 24 do not show RTCK. The header's RTCK signal must be connected on the target per the instructions in Section 8, *Header Pin Assignment*. For multiprocessor configurations that contain devices with RTCK, see Table 13 note 2.

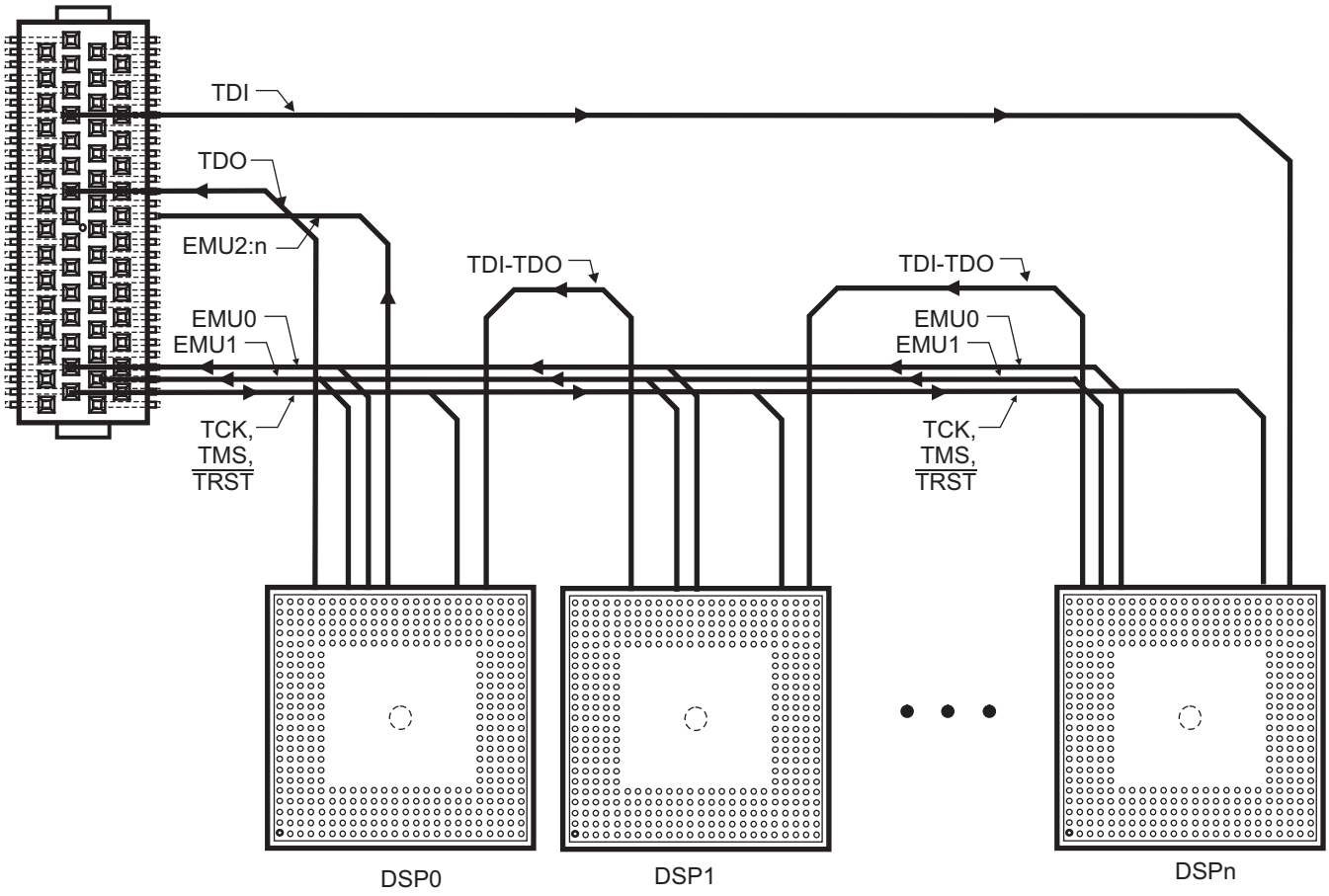


Figure 22. Multiple Device - Single Trace Configuration

Figure 23 illustrates the parallel trace configuration. You may connect up to four processors to the same emulation header pins in parallel, but the current TI trace products will force you to select a single device to capture trace data from. Also, keep in mind that if you want to use EMU0 and EMU1 for global breakpoints and cross triggers with more than four devices in the serial scan chain, these pins may not be usable for core or system trace pins. For more details on EMU pin and trace options, see Section 16.2, *PWB Routing Lengths*. For termination instructions for the parallel trace configuration, see Section 18.1.

As with the single trace configuration, the parallel trace configuration also supports synchronous execution and debug visibility to additional devices by daisy-chaining the JTAG signals between processors. The same 30-device restriction also applies to this configuration.

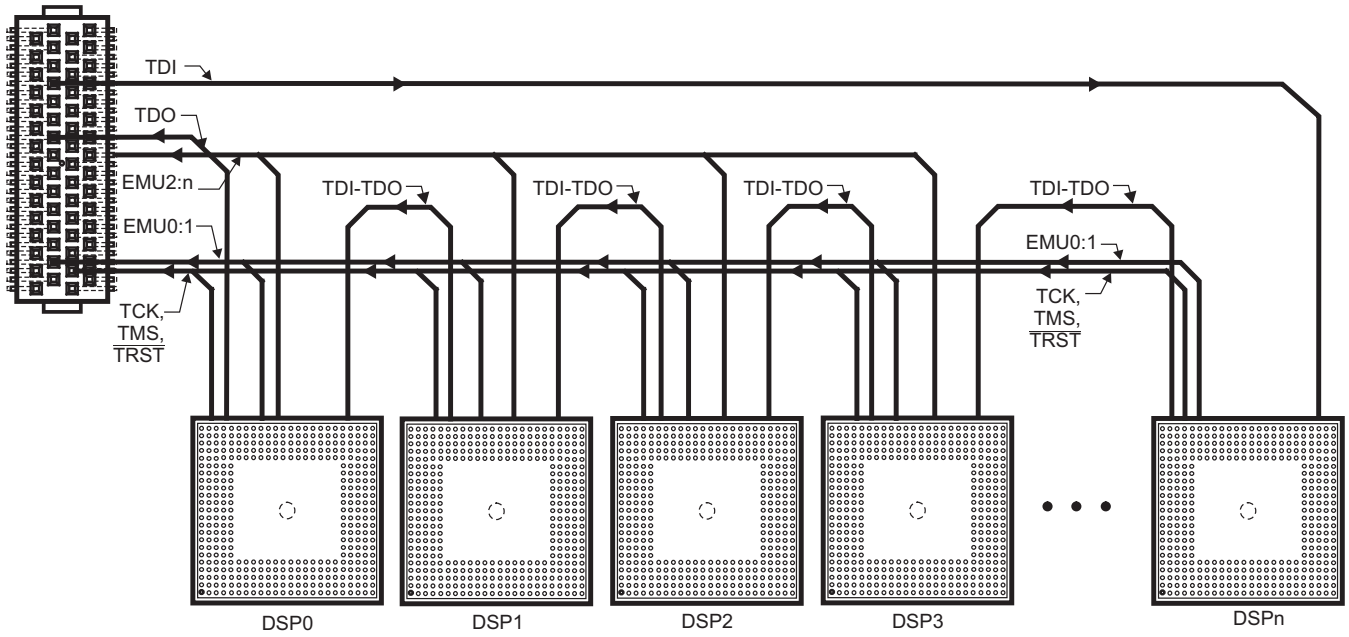


Figure 23. Multiple Device - Parallel Trace Configuration

Figure 24 illustrates the basic independent device interconnection method. Under the independent interconnection method, each device has its own independent emulation pins assigned per header. An independent configuration as indicated in Figure 24 minimizes the pin count efficiency but maximizes the performance. For more information on sizing termination resistors, see Section 10.

In the illustrated independent configuration (Figure 24), each device is in its own scan chain. Synchronous execution, cross triggers, and global breakpoints are not supported. Connecting EMU0 and EMU1 between devices in this configuration would allow cross triggers to operate, but if routes are long it could make the pins unusable for trace.

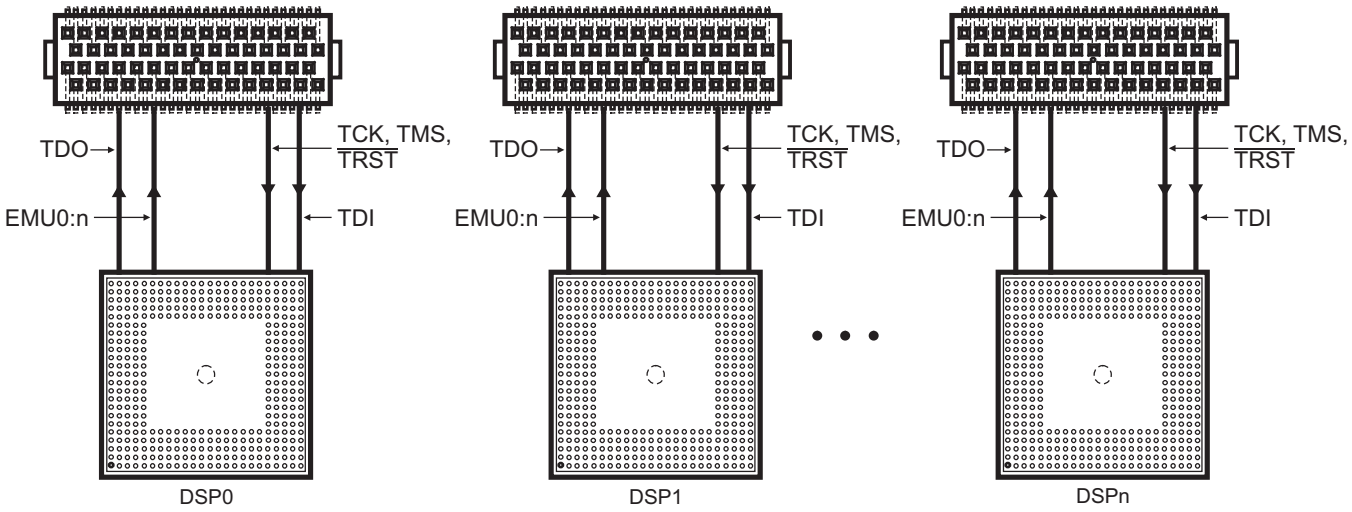


Figure 24. Device-Independent Trace Configuration

For all configurations, it is vital to both core and system trace that the routing length restrictions (Section 17.1) and termination requirements (Section 10 and Section 18.1) be followed.

18.1 Multiple-Processor Termination

If you are using the parallel trace configuration (see Figure 25), you may connect each EMU pin used for core trace or system trace from the emulation connector to no more than four processors. In this configuration, we recommend that each processor have an independent termination resistor whose routing distance from the processor to the termination resistor does not exceed 0.5", the stubs between termination resistors should be as short as possible, the distance between the termination resistors and the emulation connector do not exceed 2.25", and a total route length from the processor to the emulation connector of 3" or less. Other configurations may work, but you would need to model the configuration to validate.

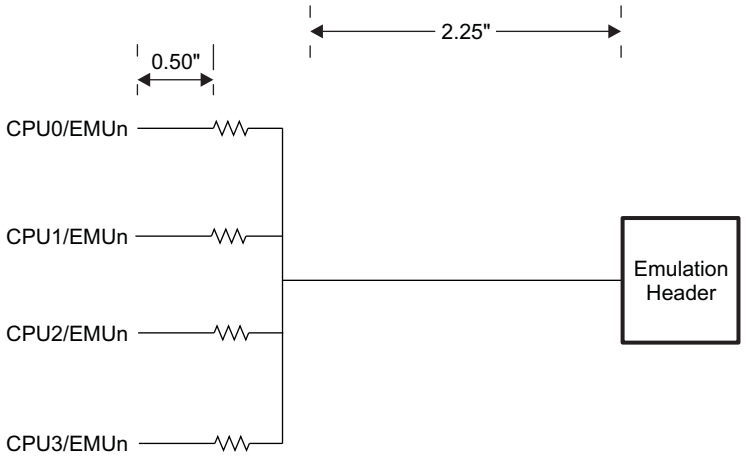


Figure 25. Parallel Termination

Special consideration must be given to sizing the termination resistors because of the additional parallel impedances contributed by the combination of the termination resistors and additional EMU pins. It is recommended you establish the termination value as if a single processor was being used (see Section 10) and then divide that value between the number of processors connected to the EMU pin of the emulator header. Table 25 should be used for sizing common termination resistor values.

Table 25. Sizing Common Termination Resistor Values

If Single Termination Value is:	2 Processors	3 Processors	4 Processors
42	20	10	10
33	16	10	10
24	12	10	10

It is not recommended to use termination resistor values lower than 10 Ω or not to use termination resistors if the value determined is smaller than 10. Use 10 Ω as a minimum.

Appendix A Alternate Target Impedance Configurations

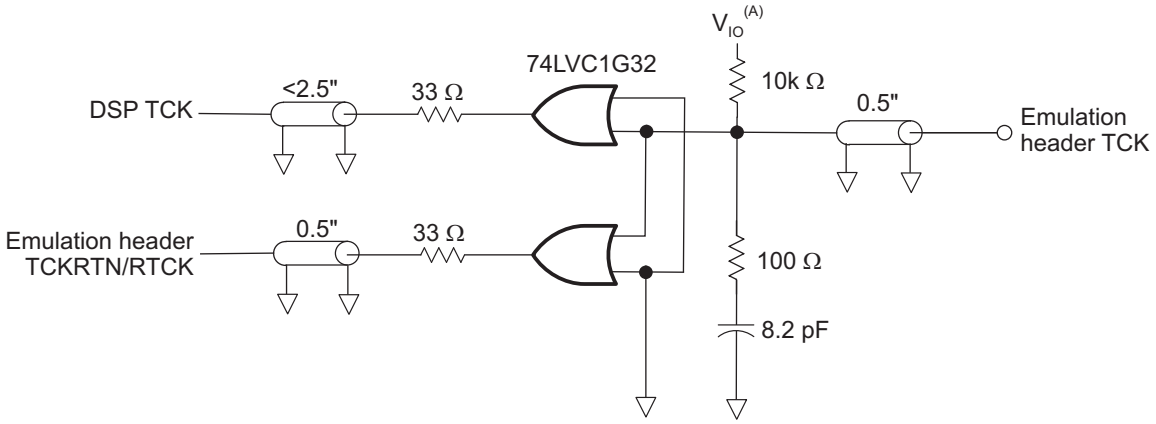
Most TI devices are designed to operate on a 50 Ω character impedance target board. For Texas Instruments' devices incorporating a built-in PCI, Ethernet, or memory interface, the trace impedance should also be 50 Ω. Other devices may require a different trace impedance in the range of 60 to 100 Ω.

Always see the device application reports or data sheets for detailed impedance requirements and confirm that the target board is designed accordingly.

Appendix H provides information to assist target board designers in obtaining the optimal interconnect impedance by varying widths of the appropriate traces. Various constraints are noted, such as the dielectric constant of the board material, the separation between layers, etc. This chart assumes an Er of 4.1, which is typical for FR-4 material. This appendix also shows how to design a multiple impedance printed circuit board.

Appendix B Buffering - Methods, Techniques and Terminations

Figure 26 represents the recommended buffering for TCK; alternate buffers may be used if appropriate. To confirm timing, drive, and voltage characteristics for your specific target, see the manufacturer's data sheets.



A JTAG IO voltage level.

Figure 26. Recommended TCK Buffered Configuration

Figure 27 represents the recommended termination for an unbuffered TCK line. Termination values should be placed in close proximity to the emulation header. This configuration should not be used if your device has an RTCK pin.

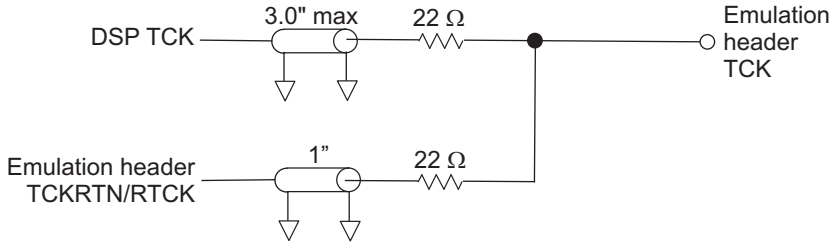
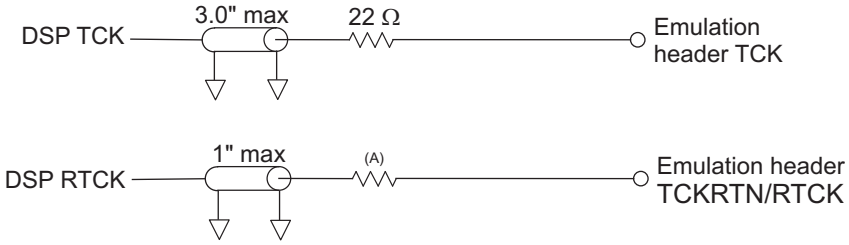


Figure 27. Recommended TCK Unbuffered Configuration

Figure 28 represents the recommended termination for a device that has an RTCK pin. Termination values should be placed in close proximity to the emulation header. The total routing distance for the TCK or RTCK signals between the device and the emulation header should not exceed 3".



A The RTCK series termination resistor is sized using the equation $Z_{Cable} - Z_{Device\_Output} = Z_{Termination\_Resistor}$. The series termination resistor should be placed as close to the device as possible with the total route not exceeding 3". For additional information on determining proper series termination values, see Section 10.

Figure 28. Recommended RTCK Configuration

Figure 29 illustrates the preferred placement for all emulation (EMU) terminations. Values and placements may vary depending on your device and trace lengths. Always model or simulate your design for optimal performance. For more information on sizing EMU termination resistors, see Section 10.

For additional recommendations, see your device data sheet.

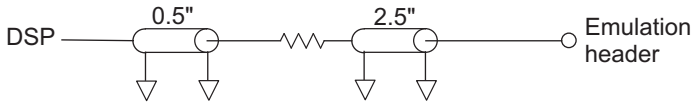


Figure 29. Recommended EMU Output Configuration

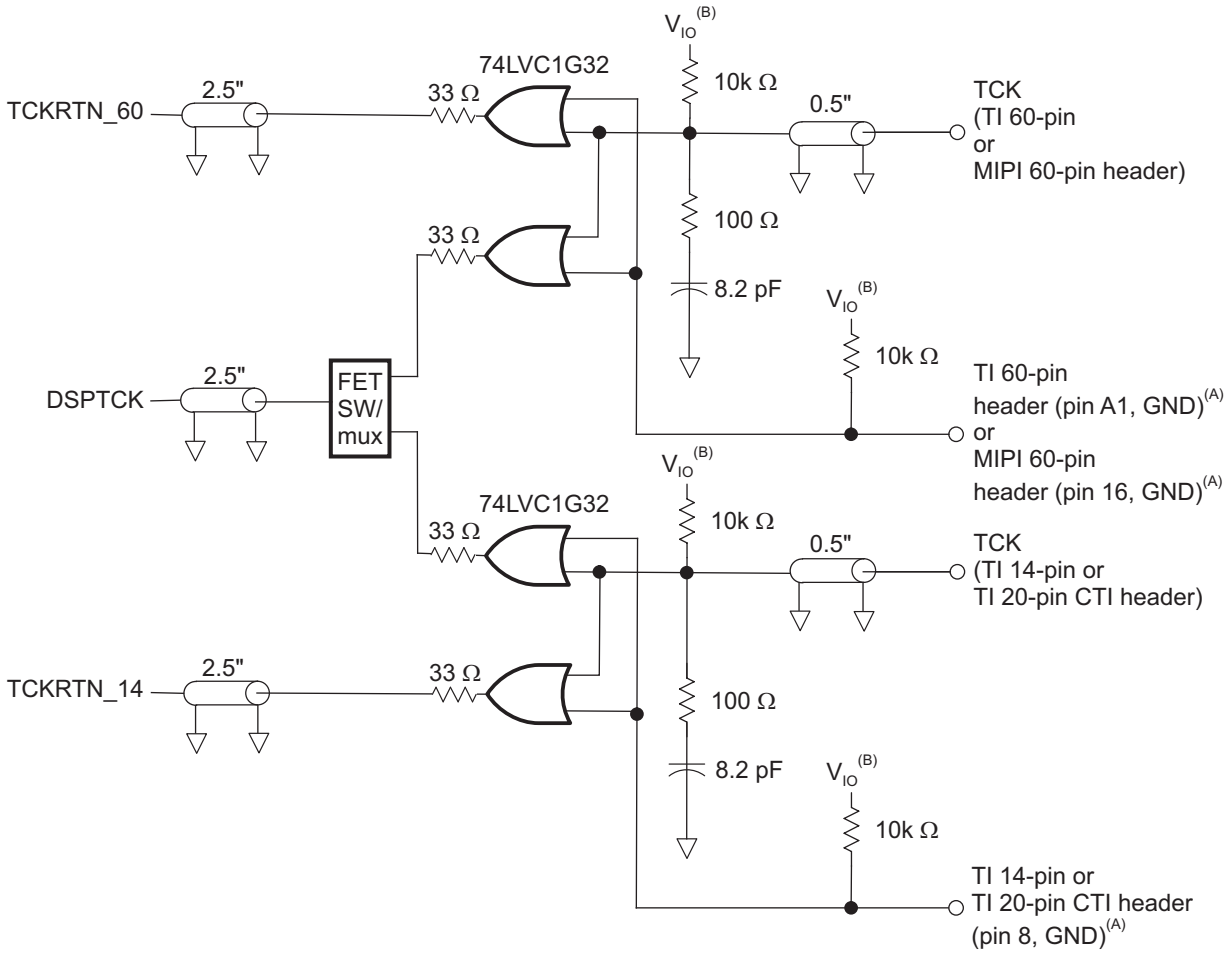
Figure 26 and Figure 29 recommend a maximum 0.5" trace distance between the device and the termination resistor. The distance for this node under all conditions cannot exceed 1.0".

Appendix C TI 14-Pin and 60-Pin Headers in Parallel

If a multi-header configuration is used, the TCK signal must be buffered. For recommended terminations, see Figure 30. The use of an FET style switch or multiplexer, such as a 74CBT3125 or 74CBT3257, is mandatory to minimize clock skew between TCKRTN and the TCK to the DSP.

The buffer, in this case a 74LVC1G32, is not mandatory, any suitable device can be used. The AC terminations and buffers must be located within 0.5-inch trace length of the header. The 33-Ω series termination should be located as close as possible to the buffer.

Designers should model their circuits including board impedance to determine the proper termination values.



A Active low cable-present signals are formed. The cable-present signal can also be used with the FET switch's OE pins.

B JTAG IO voltage level.

Figure 30. TCK, Multiple Header Configuration

Figure 31 illustrates the preferred placement for EMU0 and EMU1 terminations when multiple headers are used. Values and placements may vary depending on your device and trace lengths. The trace lengths listed are maximum values. Always model or simulate your design for optimal performance. For more information on sizing termination resistors, see Section 10 and Appendix G.

For additional recommendations, see your device data sheet.

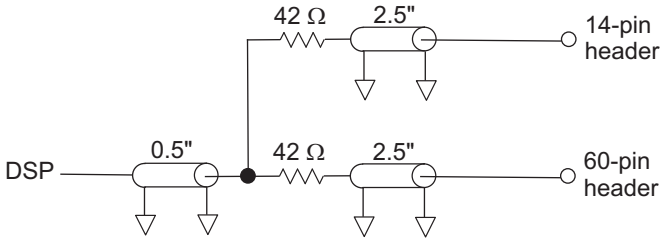


Figure 31. Preferred Configuration for EMU0 and EMU1 Terminations

Figure 31 recommends a maximum 0.5" trace distance between the device and the termination resistor. The distance for this node under all conditions cannot exceed 3".

Appendix D Layout and Routing Requirements

D.1 Layout and Route Deviations [Advanced Emulation]

To minimize routing deviations, provide a clean electrical environment for advance emulation capabilities. The greater the distance (or skew) between the header and the target processor, the greater the potential for timing errors. A small amount of skew is acceptable and can be accommodated. However, excessive propagation or skew, beyond an allotted amount, will produce bit errors, loss of data or faulty operation. The recommended header distance from the target processor is 3 inches maximum.

Models representing the target interconnect are provided in Appendix E and Appendix F for the XDS560T and XDS560 v2 System Trace emulators.

Appendix E XDS560T Spice Model

NOTE:

- The models provided are for spice simulation. TI recommends using tools that support simulating with IBIS models of the TI device and the LVDS buffer (SN65LVDS388A) rather than using the ideal voltage source shown in the following models.
- The models shown use Tran0 and Tran1 values that match the timing diagrams provided. When performing modeling of your system, you should replace these values with your actual values. TI does not recommend exceeding 3" between Tran0 and Tran1.

Figure 32 illustrates the EMU0 spice model for TI's XDS560T pod assembly and partial target board logic.

Example 1 is the spice net list for the spice model in Figure 32 . This illustration references a 50-Ω characteristic-impedance target PCB. Clock speeds are 200 MHz. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

Figure 33 illustrates an acceptable waveform for Figure 32 and Example 1 using TI's XDS560T and a 50-Ω character-impedance target board.

Example 2 illustrates the spice net list used to create the spice model for a 75-Ω target board impedance and TI's XDS560T pod.

Figure 34 illustrates the waveform for Figure 32 and Example 2 using TI's XDS560T and a 75-Ω character-impedance target board.

Figure 35 illustrates the EMU2 type signals (see Table 26) spice model for TI's XDS560T pod assembly and partial target board logic.

Example 3 is the spice net list for the spice model in Figure 35. This illustration references a 50-Ω character-impedance target PCB. Clock speeds are 200 MHz. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

Figure 36 illustrates an acceptable waveform for Figure 35 and Example 3 using TI's XDS560T and a 50-Ω character-impedance target board.

Figure 37 illustrates the EMU18 type signals (see Table 26) spice model for TI's XDS560T pod assembly and partial target board logic.

Example 4 is the spice net list for the spice model in Figure 37. This illustration references a 50-Ω character-impedance target PCB. Clock speeds are 200 MHz. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

Figure 38 illustrates an acceptable waveform for Figure 37 and Example 4 using TI's XDS560T and a 50-Ω character-impedance target board.

Figure 39 illustrates the dual header configuration EMU0 spice model for TI's XDS560T pod assembly and a partial target board logic. This model is provided to emphasize the advantages of using a single emulation header.

Example 5 is the spice net list for the spice model in Figure 39. This illustration references a 50-Ω character-impedance target PCB. Clock speeds are 200 MHz. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

Figure 40 illustrates the waveform for Figure 39 and Example 5 using TI's XDS560T and a 50-Ω character impedance target board in a two-header configuration.

Certain characteristics of the target board may change - the spice net list must be modified and rerun to determine the outcome.

Table 26. EMU Pins Modeled as EMU2 or EMU18

Model as EMU2	Model as EMU18
EMU2	EMU12
EMU3	EMU14
EMU4	EMU15
EMU5	EMU16
EMU6	EMU17
EMU7	EMU18
EMU8	
EMU9	
EMU10	
EMU11	
EMU13	

Figure 32 is a representative spice model for TI's XDS560T pod assembly. Clock speeds are 200 MHz. This illustration supports both a 75-Ω and 50-Ω character-impedance target PCB. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

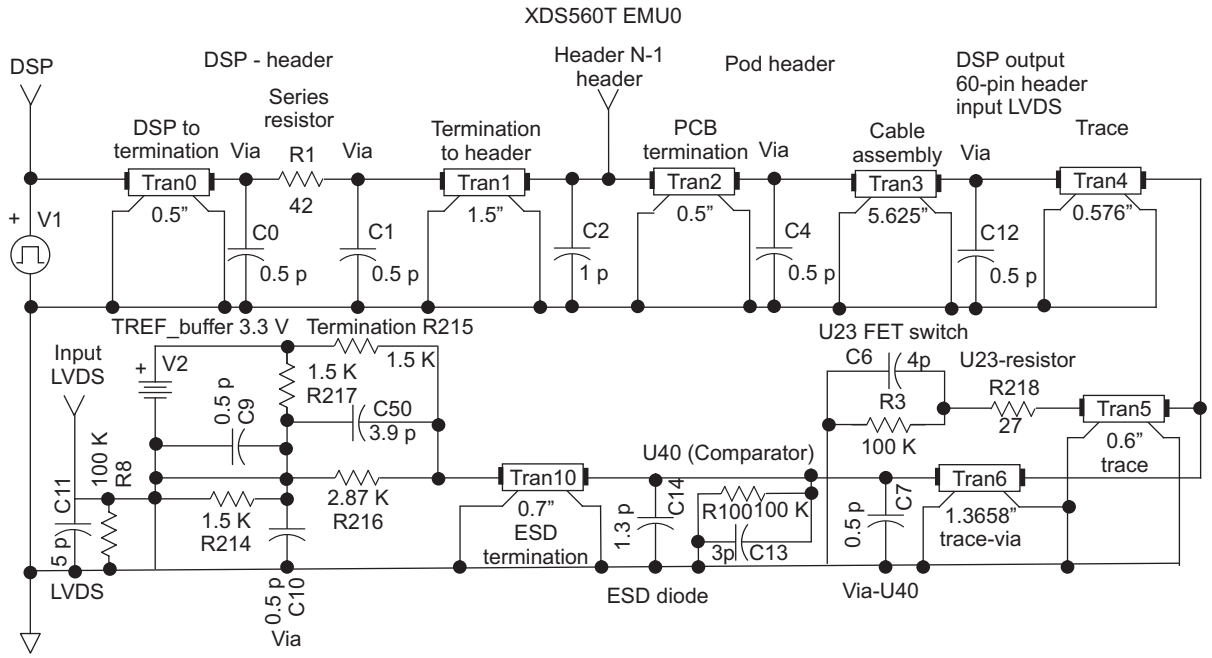


Figure 32. EMU0 Simulation Model (TI's XDS560T Pod Assembly - 50-Ω and 75-Ω Target and Pod Model)

Example 1 represents the spice net list used to create the spice model for a 50-Ω target board impedance and TI's XDS560T pod. Certain characteristics of the target board may change - the spice net list must be modified and re-run to determine the potential outcome.

Example 1. EMU0 Spice Net List (50-Ω Target and Pod Model)

```
*** Top Level Netlist ***
C4     0 10 0.5p
C50     6 InputLVDS 3.9p
V1     DSP 0    DC 3.3V AC 0 0 PULSE 0 3.3V 0 800.00p 800.00p 2.20n 4.40n
Tran0     1 0 DSP 0 ZO=50 TD=.088ns F=200Meg NL=0.5
Tran1     Header 0 9 0 ZO=50 TD=.264ns F=200Meg NL=1.5
Tran2     10 0 Header 0 ZO=50 TD=.176ns F=200Meg NL=0.5
Tran3     10 0 13 0 ZO=50 TD=0.990ns F=200Meg NL=5.625
Tran6     2 0 20 0 ZO=50 TD=0.2403808ns F=200Meg NL=1.3658
C2     0 Header 1p
C7     0 2 0.5p
C6     0 4 4p
V2     12 0    DC 3.30 AC 0 0
C9     0 InputLVDS 0.5p
C0     0 1 0.5p
C1     0 9 0.5p
C10     0 InputLVDS 0.5p
C11     0 InputLVDS 5p
C12     13 0 0.5p
Tran5     8 0 20 0 ZO=50 TD=.1056ns F=200Meg NL=0.6
Tran10     6 0 2 0 ZO=50 TD=0.1232ns F=200Meg NL=0.7
C13     0 2 3p
C14     0 2 1.3p
Tran4     13 0 20 0 ZO=50 TD=0.176ns F=200Meg NL=0.576
R1     1 9 42
R216     InputLVDS 6 2.87K
R217     12 InputLVDS 1.5K
R215     12 6 1.5K
R100     2 0 100K
R3     0 4 100K
R218     4 8 27
R214     InputLVDS 0 1.5K
R8     InputLVDS 0 100K

***** Spice models and macro models *****

***** End of spice models and macro models *****

.tran 1n 100n 0.0 1n
.save all
.end
```

The result of your 50-Ω target PCB simulation and modeling should be an acceptable waveform, similar to that illustrated in Figure 33.

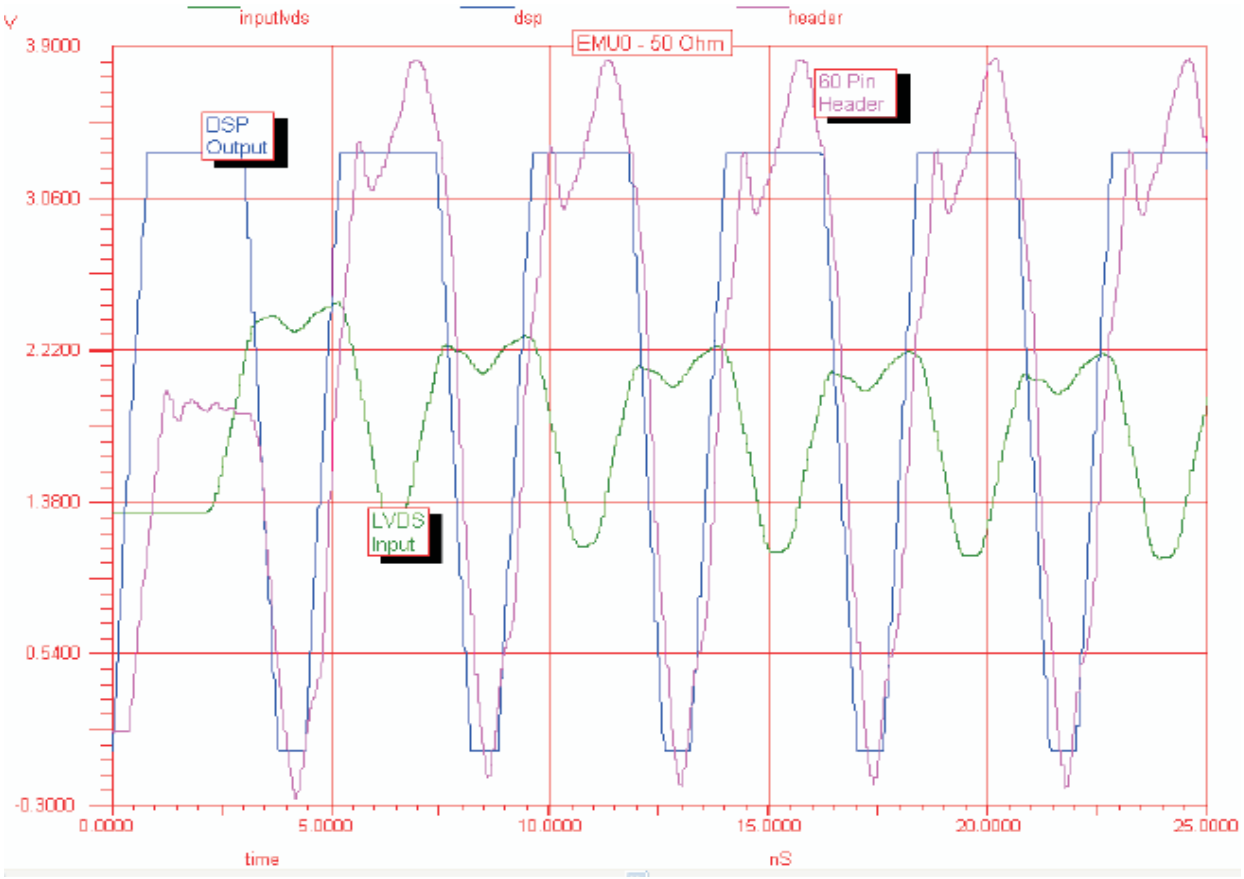


Figure 33. EMU0 Acceptable Wave Form (Host Side, TI's XDS560T Pod - 50 Ω)

Example 2 represents the spice net list used to create the spice model for a 75-Ω target board impedance and TI's XDS560T pod assembly.

Example 2. EMU0 Spice Net List (Host Side, TI's XDS560T Pod - 75 Ω)

```
*** Top Level Netlist ***
C4     0 10 0.5p
C50     6 InputLVDS 3.9p
V1     DSP 0    DC 3.3V AC 0 0 PULSE 0 3.3V 0 800.00p 800.00p 2.20n 4.40n
Tran0     1 0 DSP 0 ZO=75 TD=.088ns F=200Meg NL=0.5
Tran1     Header 0 9 0 ZO=75 TD=.264ns F=200Meg NL=1.5
Tran2     10 0 Header 0 ZO=75 TD=.176ns F=200Meg NL=0.5
Tran3     10 0 13 0 ZO=75 TD=0.990ns F=200Meg NL=5.625
Tran6     2 0 20 0 ZO=75 TD=0.2403808ns F=200Meg NL=1.3658
C2     0 Header 1p
C7     0 2 0.5p
C6     0 4 4p
V2     12 0    DC 3.30 AC 0 0
C9     0 InputLVDS 0.5p
C0     0 1 0.5p
C1     0 9 0.5p
C10     0 InputLVDS 0.5p
C11     0 InputLVDS 5p
C12     13 0 0.5p
Tran5     8 0 20 0 ZO=75 TD=.1056ns F=200Meg NL=0.6
Tran10     6 0 2 0 ZO=75 TD=0.1232ns F=200Meg NL=0.7
C13     0 2 3p
C14     0 2 1.3p
Tran4     13 0 20 0 ZO=75 TD=0.176ns F=200Meg NL=0.576
R1     1 9 42
R216     InputLVDS 6 2.87K
R217     12 InputLVDS 1.5K
R215     12 6 1.5K
R100     2 0 100K
R3     0 4 100K
R218     4 8 27
R214     InputLVDS 0 1.5K
R8     InputLVDS 0 100K

***** Spice models and macro models *****


***** End of spice models and macro models *****

.tran 1n 100n 0.0 1n
.save all
.end
```

The result of your 75-Ω target PCB simulation and modeling from Example 2 should be similar to the waveform illustrated in Figure 34.

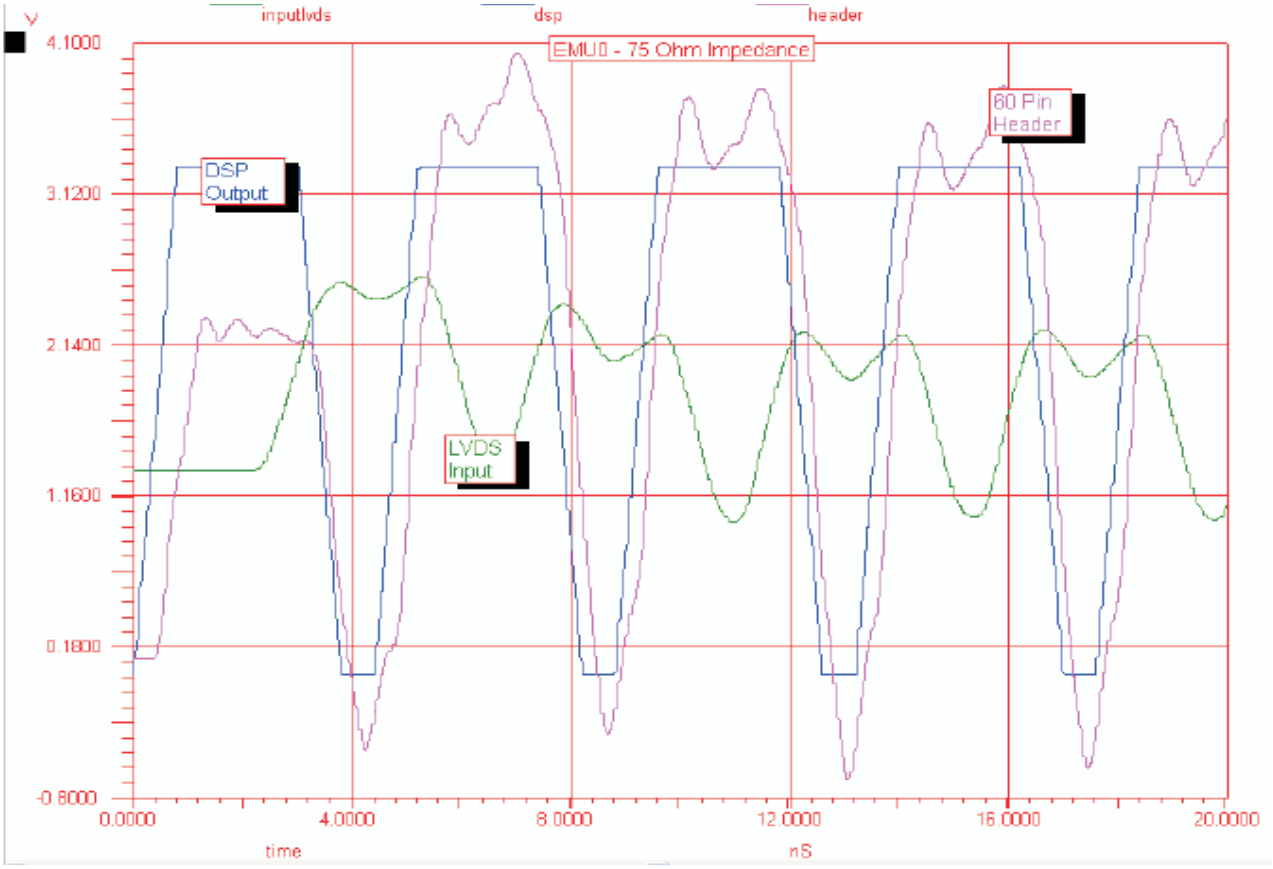


Figure 34. EMU0 Wave Form (Host Side, TI's XDS560T - 75 Ω)

Figure 35 is a representative spice model for TI's XDS560T pod assembly. Clock speeds are 200 MHz. This illustration supports a 50-Ω character-impedance target PCB. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

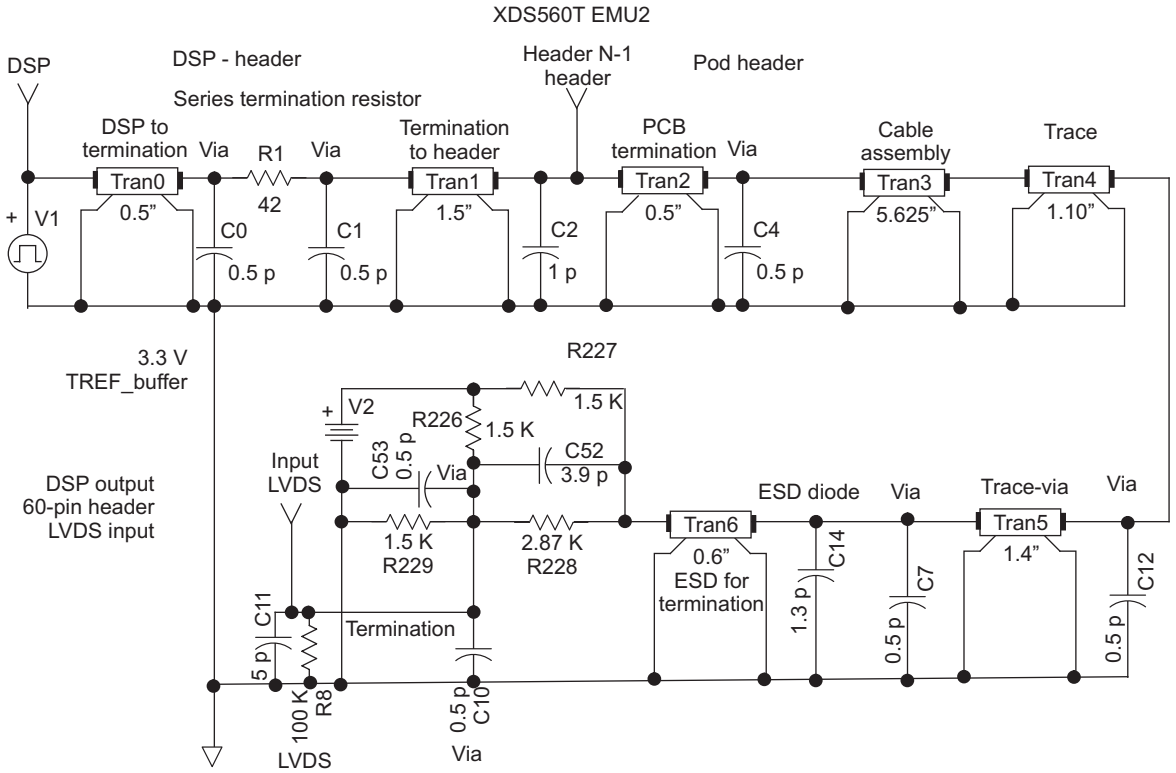


Figure 35. EMU2 Type Signals Simulation Model (TI's XDS560T Pod Assembly - 50-Ω Target and Pod Model)

Example 3 represents the spice net list used to create the spice model in Figure 35 for a 50-Ω target board impedance and TI's XDS560T pod.

Example 3. EMU2 Type Signals Spice Net List (Host Side, TI's XDS560T Pod - 50 Ω)

```
*** Top Level Netlist ***
C4     0 10 0.5p
C52     2 InputLVDS 3.9p
V1     DSP 0    DC 3.3V AC 0 0 PULSE 0 3.3V 0 1.00n 1.00n 1.50n 5.00n
Tran0     1 0 DSP 0 ZO=50 TD=.088ns F=200Meg NL=0.5
Tran1     Header 0 9 0 ZO=50 TD=.264ns F=200Meg NL=1.5
Tran2     10 0 Header 0 ZO=50 TD=.176ns F=200Meg NL=0.5
Tran3     10 0 13 0 ZO=50 TD=0.990ns F=200Meg NL=5.625
Tran5     17 0 3 0 ZO=50 TD=0.2464n F=200Meg NL=1.4
C2     0 Header 1p
C7     0 17 0.5p
V2     7 0    DC 3.30 AC 0 0
C0     0 1 0.5p
C1     0 9 0.5p
C10     0 InputLVDS 0.5p
C11     0 InputLVDS 5p
C12     0 3 0.5p
Tran6     2 0 17 0 ZO=50 TD=0.1056ns F=200Meg NL=0.6
C14     0 17 1.3p
Tran4     13 0 3 0 ZO=50 TD=0.0176ns F=200Meg NL=0.1
R1     1 9 42
R228     InputLVDS 2 2.87K
R226     7 InputLVDS 1.5K
R227     7 2 1.5K
R8     InputLVDS 0 100K
C53     0 InputLVDS 0.5p
R229     InputLVDS 0 1.5K

***** Spice models and macro models *****


***** End of spice models and macro models *****

.tran 10p 100n 0.0 5p
.save all
.end
```

The result of your 50-Ω target PCB simulation and modeling from Example 3 should be an acceptable waveform, similar to that illustrated in Figure 36.

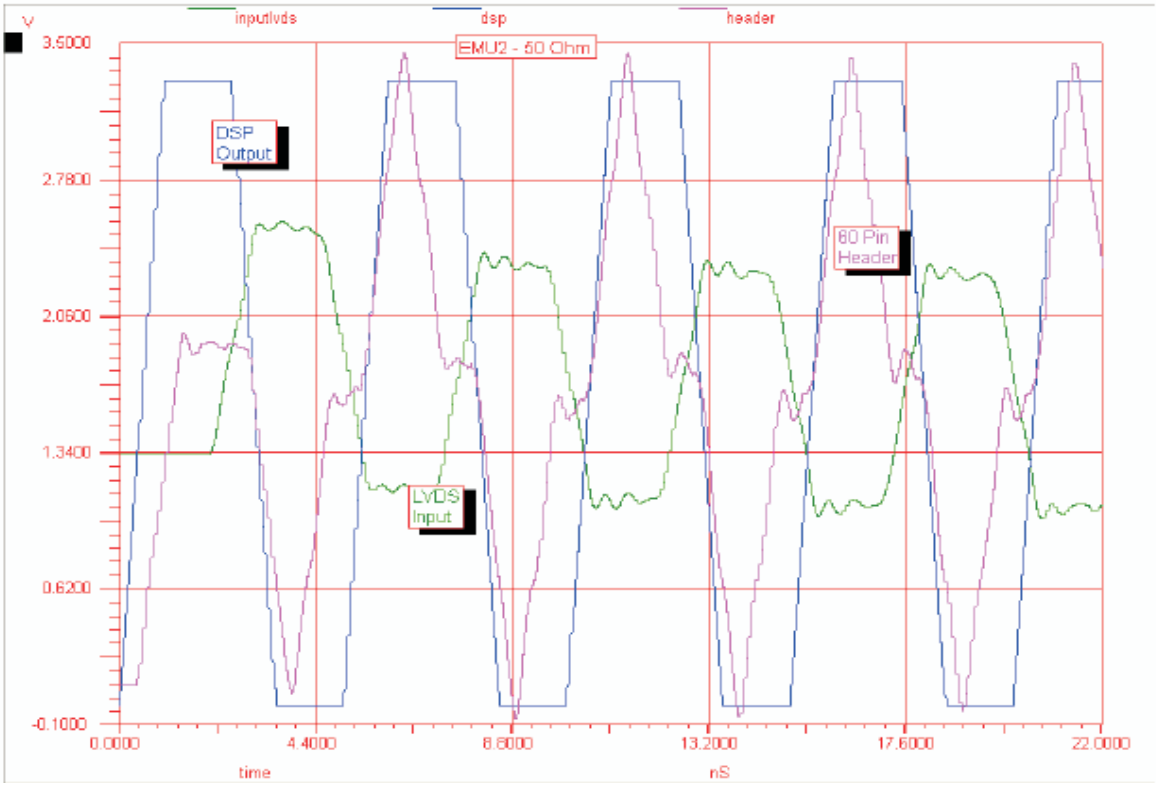


Figure 36. EMU2 Type Signals Acceptable Wave Form (Host Side, TI's XDS560T Pod - 50 Ω)

Figure 37 is a representative spice model for TI's XDS560T pod assembly. Clock speeds are 200 MHz. This illustration supports a 50-Ω character-impedance target PCB. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

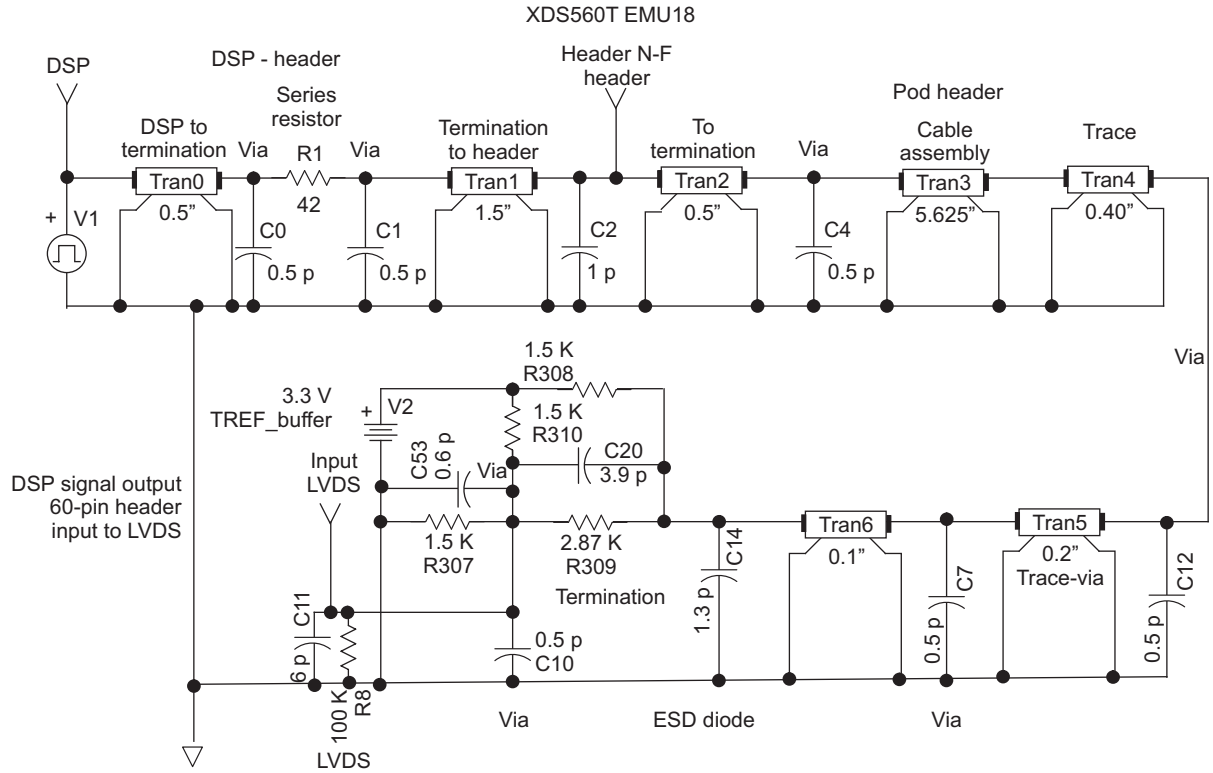


Figure 37. EMU18 Type Signals Simulation Model (TI's XDS560T Pod Assembly - 50-Ω Target and Pod Model)

Example 4 represents the spice net list used to create the spice model in Figure 37 for a 50-Ω target board impedance and TI's XDS560T pod.

Example 4. EMU18 Type Signals Spice Net List (Host Side, TI's XDS560T Pod - 50 Ω)

```
*** Top Level Netlist ***
C4     0 10 0.5p
C70     6 InputLVDS 3.9p
V1     DSP 0    DC 3.3V AC 0 0 PULSE 0 3.3V 0 1.00n 1.00n 1.50n 5.00n
Tran0     1 0 DSP 0 ZO=50 TD=.088ns F=200Meg NL=0.5
Tran1     Header 0 9 0 ZO=50 TD=.264ns F=200Meg NL=1.5
Tran2     10 0 Header 0 ZO=50 TD=.176ns F=200Meg NL=0.5
Tran3     10 0 13 0 ZO=50 TD=0.990ns F=200Meg NL=5.625
Tran5     18 0 8 0 ZO=50 TD=0.0528n F=200Meg NL=0.2"
C2     0 Header 1p
C7     0 18 0.5p
V2     7 0    DC 3.30 AC 0 0
C0     0 1 0.5p
C1     0 9 0.5p
C10     0 InputLVDS 0.5p
C11     0 InputLVDS 5p
C12     0 8 0.5p
Tran6     6 0 18 0 ZO=50 TD=0.0176ns F=200Meg NL=0.1
C14     0 6 1.3p
Tran4     13 0 8 0 ZO=50 TD=0.0704ns F=200Meg NL=0.4
R1     1 9 42
R309     InputLVDS 6 2.87K
R310     7 InputLVDS 1.5K
R308     7 6 1.5K
R8     InputLVDS 0 100K
C53     0 InputLVDS 0.5p
R307     InputLVDS 0 1.5K

***** Spice models and macro models *****


***** End of spice models and macro models *****

.tran 2n 100n 0.0 2n
.save all
.end
```

The result of your 50-Ω target PCB simulation and modeling from Figure 37 should be an acceptable waveform, similar to that illustrated in Figure 38.

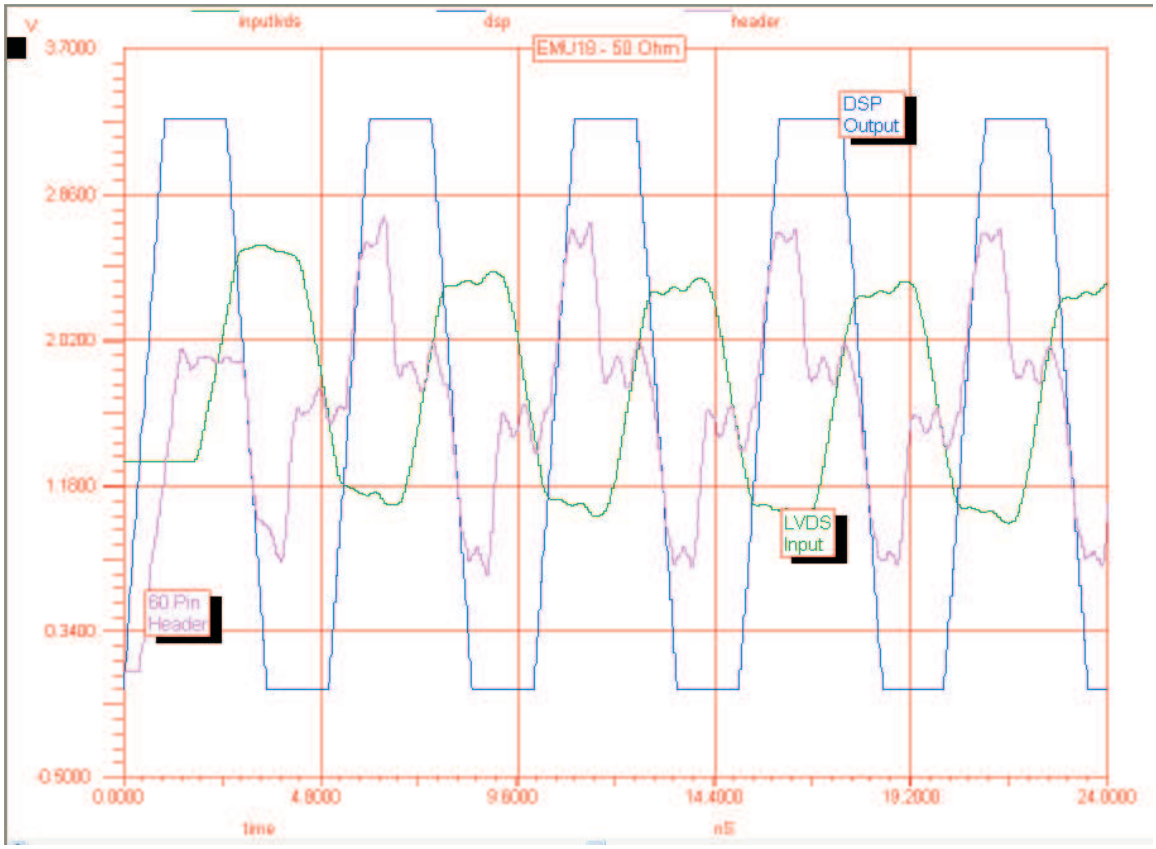


Figure 38. EMU18 Type Signals - Acceptable Wave Form (Host Side, TI's XDS560T Pod - 50 Ω)

Figure 39 is a spice model for a dual-header configuration using TI's XDS560T pod assembly. Clock speeds are 200 MHz. This illustration supports a 50-Ω character-impedance target PCB. Dual-header configurations are not recommended and require a variety of constraints to be modeled (trace length and supporting logic). Additional modeling should be done for signal cross talk.

It is strongly recommended that only TI's emulation header be used.

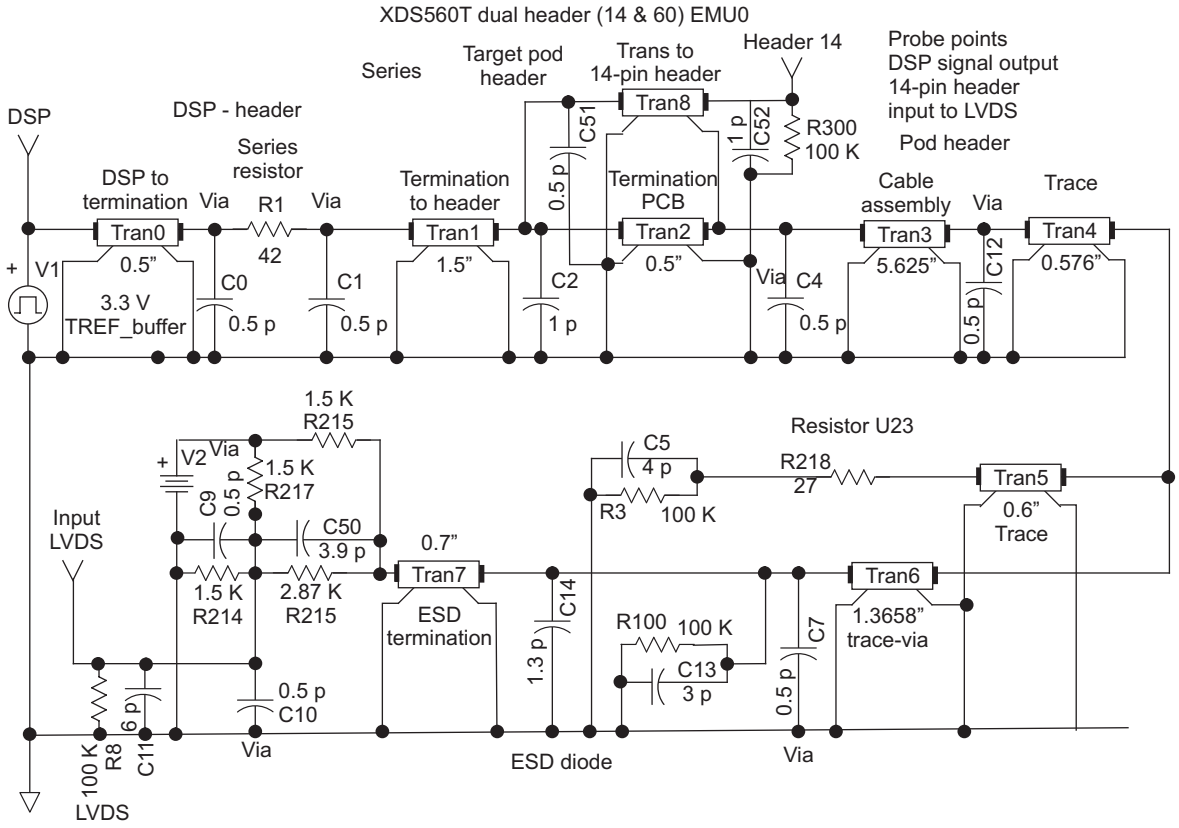


Figure 39. EMU0 Dual-Header Simulation Model (TI's XDS560T Pod Assembly - 50-Ω Target and Pod Model)

Example 5 represents the spice net list used to create the spice model in Figure 39 for a 50-Ω dual-header target board impedance and TI's XDS560T pod.

Example 5. EMU0 Dual-Header Spice Net List (Host Side, TI's XDS560T Pod - 50 Ω)

```
*** Top Level Netlist ***
C4     0 10 0.5p
C50     12 InputLVDS 3.9p
V1     DSP 0    DC 3.3V AC 0 0 PULSE 0 3.3V 0 800.00p 800.00p 2.20n 4.40n
Tran0     1 0 DSP 0 ZO=50 TD=.088ns F=200Meg NL=0.5
Tran1     5 0 9 0 ZO=50 TD=.264ns F=200Meg NL=1.5
Tran2     10 0 5 0 ZO=50 TD=.176ns F=200Meg NL=0.5
Tran3     10 0 13 0 ZO=50 TD=0.990ns F=200Meg NL=5.625
Tran6     2 0 18 0 ZO=50 TD=0.2403808ns F=200Meg NL=1.3658
C2     0 5 1p
C7     2 0 0.5p
C6     8 0 4p
V2     16 0    DC 3.30 AC 0 0
C9     0 InputLVDS 0.5p
C0     0 1 0.5p
C1     0 9 0.5p
C10     0 InputLVDS 0.5p
C11     0 InputLVDS 5p
C12     13 0 0.5p
Tran5     14 0 18 0 ZO=50 TD=.1056ns F=200Meg NL=0.6
Tran7     12 0 2 0 ZO=50 TD=0.1232ns F=200Meg NL=0.7
C13     0 2 3p
C14     0 2 1.3p
Tran4     13 0 18 0 ZO=50 TD=0.176ns F=200Meg NL=0.576
R1     1 9 42
R216     InputLVDS 12 2.87K
R217     16 InputLVDS 1.5K
R215     16 12 1.5K
R100     2 0 100K
R3     8 0 100K
R218     8 14 27
R214     InputLVDS 0 1.5K
R8     InputLVDS 0 100K
Tran8     5 0 Header14 0 ZO=50 TD=0.2816ns F=200Meg NL=1.6
C51     0 5 0.5p
C52     0 Header14 1p
R300     Header14 0 100K

***** Spice models and macro models *****


***** End of spice models and macro models *****

.tran 1n 100n 0.0 1n
.save all
.end
```

The result of your 50-Ω dual-header target PCB simulation and modeling from Figure 39 should be an acceptable waveform, similar to that illustrated in Figure 40.

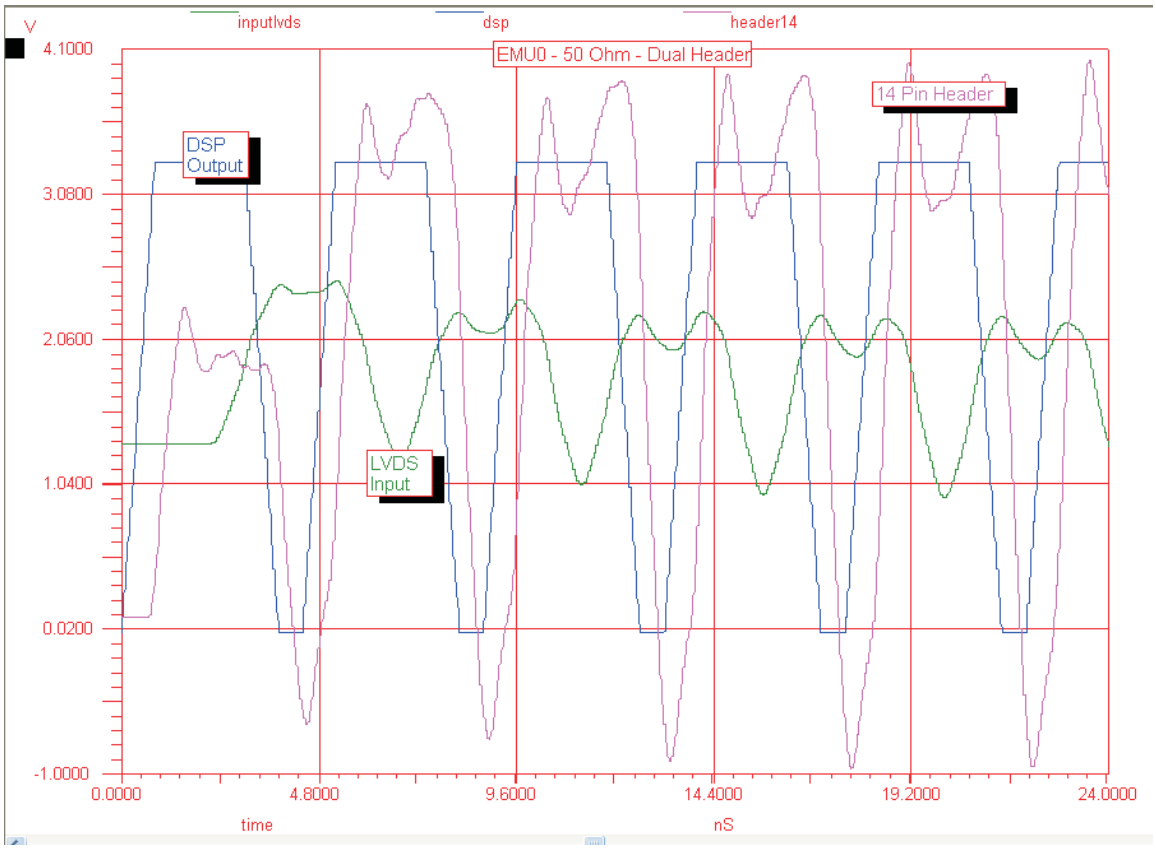


Figure 40. EMU0 Dual-Header - Wave Form (Host Side, TI's XDS560T Pod - 50 Ω)

Appendix F XDS560 v2 System Trace Modeling

Figure 41 shows the TRCLK[0] model schematic. SLM_qth01_qsh01 in the model represents the combination of the emulation header on the target card and the target cable connector. For the most accurate simulation, TI recommends using tools that support simulation with IBIS models of your target device (U11.1 in Figure 41) and the AVC4T245_RGY buffer.

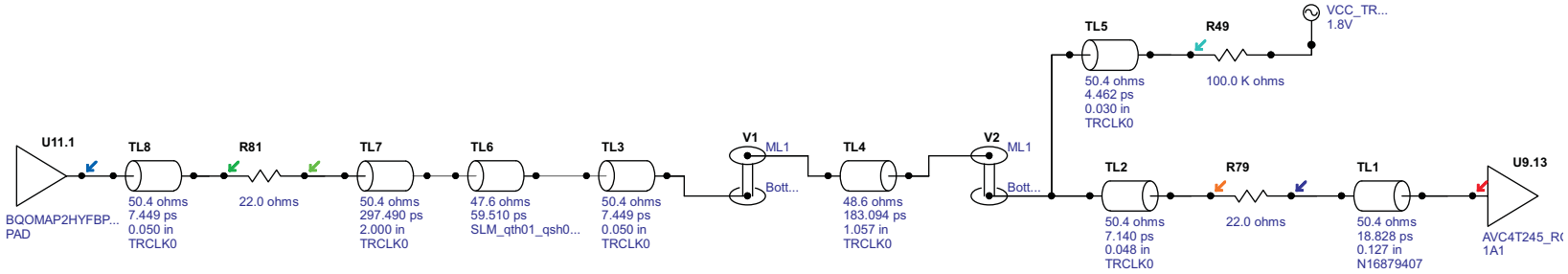


Figure 41. TRCLK[0] Model Schematic

Appendix G Finding a Buffer's Output Impedance

To determine the nominal impedance of a device's JTAG or EMU pin output buffer, reference the IBIS model for the device. Find the "model_name" of the pin's buffer using the name of the pin as defined in the device's data sheet (i.e., EMU0, TCK) and use the key from Table 27 to decode the name and determine the output impedance of the buffer. Table 28 provides a list of common buffers and the recommended series termination resistor value. In some cases, a shorthand version of the model_name is used. In this case, you must find the definition of the buffer in the IBIS file and look for the component comment (for an example, see Table 29).

Table 27. Buffer Name Decode and Output Impedance

Buffer Name: BT 3325 ET HYPU FZSC P18	
B	Driver/Receiver (O = Output).
T	TTL © = CMOS).
33	Supply voltage; i.e., 3.3 V.
25	Nominal impedance; i.e., 25 Ω.
E	Buffer's design frequency; i.e., 250 MHz.
	A = 50 MHz
	B = 100 MHz
	C = 150 MHz
	D = 200 MHz
	E = 250 MHz
	F = 300 MHz

Table 28. Recommended Series Termination Resistor Value

Buffer Types (1)	Output Impedance	Recommended Termination Resistor
BT3315DTHYPU	15	33
BT3325ETPU	25	24
BT3325ETHYPUFZSCP18	25	24
BC1825ETHYPUFZ	25	24
BC1825ESHYPUFZ	25	24
IDH04_UOT335_PS100	(2)	42

(1) Do not assume that all EMU and JTAG pins use the same buffers. Fore example, a TMS320C6457 uses a BC1825ETHYPUFZ for all the EMU pins, but the TDO pin uses a BC1840ETHYFZ. In this case, the EMU pins require 24-Ω series termination resistors, while TDO requires a much smaller, 10-Ω, termination resistor.

(2) In some early trace supported devices, the IBIS buffer naming convention was not used. If you find cases other than IDH04_UOT335_PS100, we recommend you contact your TI field service representative to get the buffer output impedance.

Table 29. Model_name Example

Pin	Signal_name	Model_name	R_pin	L_pin	C_pin
H23	TCK	KP18PUSR50	1.14E+00	2.78E-09	1.62E-12
J22	TDI	THYPUFZP18	1.10E+00	2.58E-09	1.66E-12
J23	TDO	EPUFZSCP18	1.16E+00	2.67E-09	1.47E-12
L22	TMS	THYPUFZP18	9.03E-01	2.34E-09	1.52E-12
L23	$\overline{\text{TRST}}$	THYPDFZP18	1.03E+00	2.62E-09	1.41E-12
K23	EMU0	EPUFZSCP18	1.08E+00	2.62E-09	1.49E-12
K22	EMU1	EPUFZSCP18	1.02E+00	2.47E-09	1.58E-12
K21	EMU2	EPUFZSCP18	7.51E-01	2.07E-09	1.39E-12
K20	EMU3	EPUFZSCP18	5.34E-01	1.66E-09	1.26E-12
L18	EMU4	EPUFZSCP18	2.72E-01	1.21E-09	1.07E-12
J21	EMU5	EPUFZSCP18	8.00E-01	2.22E-09	1.48E-12
K19	EMU6	EPUFZSCP18	4.11E-01	1.49E-09	1.19E-12
H21	EMU7	EPUFZSCP18	9.35E-01	2.47E-09	1.51E-12
J20	EMU8	EPUFZSCP18	6.07E-01	1.77E-09	1.33E-12
H20	EMU9	EPUFZSCP18	6.51E-01	1.98E-09	1.35E-12
J19	EMU10	EPUFZSCP18	4.39E-01	1.54E-09	1.18E-12
K18	EMU11	EPUFZSCP18	1.61E-01	1.32E-09	9.70E-13

In the case of TDO, you must search the IBIS model for the following comment:

```
|*****************************************************************************
||             Component BT3325ETHYPUFZSCP18 -May 28, 2007 Rev 1.1
|            Note: Shortened Model name is EPUFZSCP18
|*****************************************************************************
```

Appendix H Variable Board Impedance

Figure 42 illustrates the ability to alter individual printed circuit board impedances by varying the dielectric thickness and spacing for specific signal layers to reference planes.

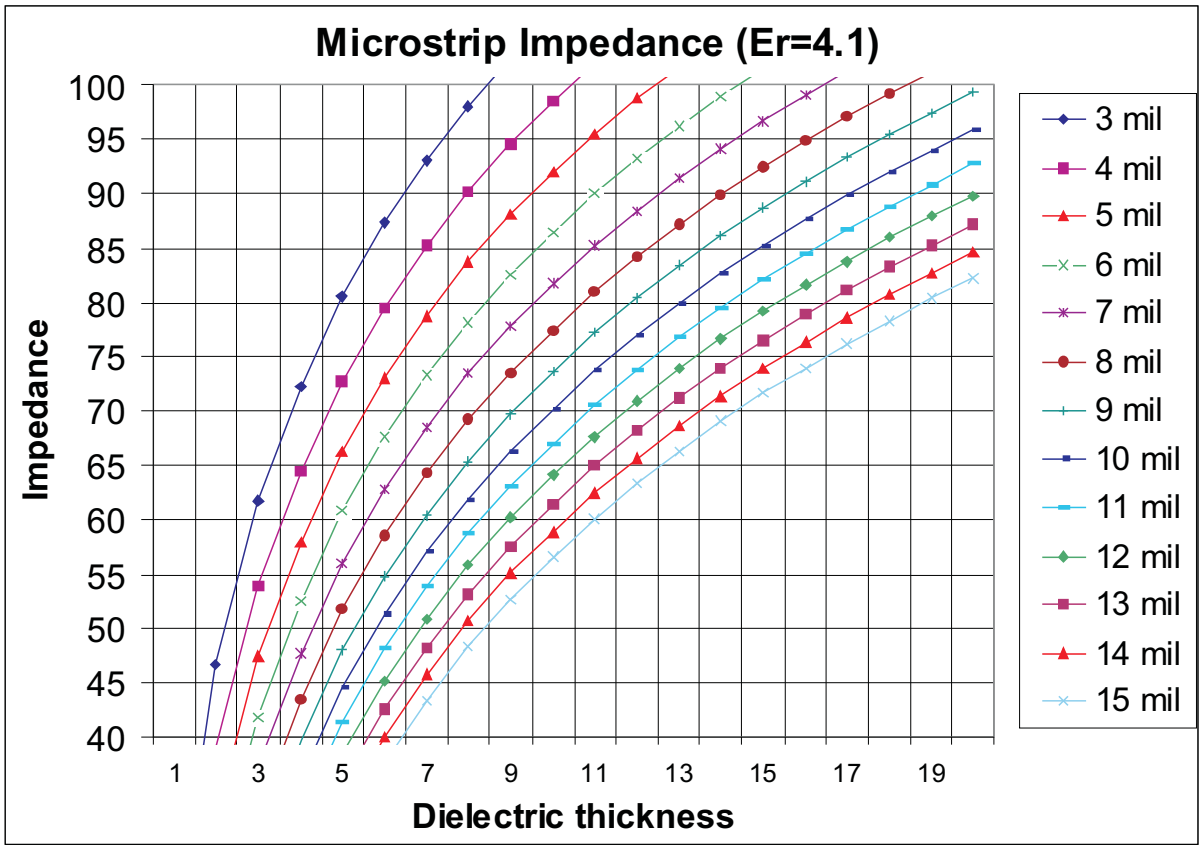
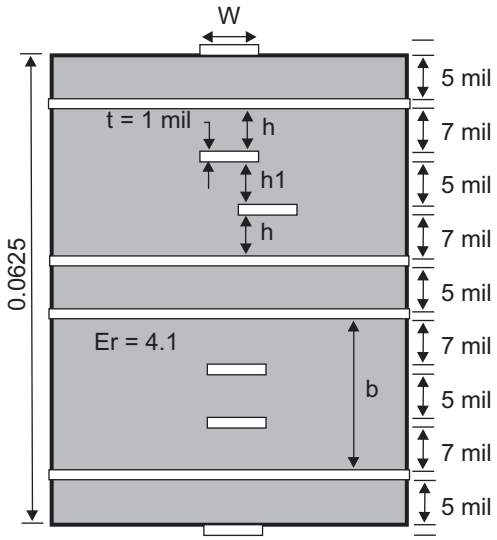


Figure 42. Various PCB Impedance Calculations



A typical layer stackup is shown to the left, all copper layers are assumed to be 1 mil thick. Total board thickness is 0.063.

If h=7 mils, and h1 = 5 mils, a 7.5-mil wide trace has a 50-Ω impedance and a 3.5-mil wide trace has a 71-Ω impedance.

Figure 43. Example of 10-Layer PCB Construction

Appendix I Revision History

This revision history highlights the technical changes made to the document in revision D.

Table 30. Emulation and Trace Headers Revision History

See	Additions/Modifications/Deletions
Table 12	Added Footnote (1) to TDIS signal

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