FAIRCHILD SEMICONDUCTOR®

November 2011

# FAN6756 — mWSaver™ PWM Controller

## Features

- Single-Ended Topologies, such as Flyback and Forward Converters
- mWSaver™ Technology
  - Achieves Low No-Load Power Consumption: Less than 30mW at $230V_{AC}$ (EMI Filter Loss Included)
  - Eliminates X Capacitor Discharge Resistor Loss with AX-CAP™ Technology
  - Linearly Decreases Switching Frequency to 23KHz
  - Burst Mode Operation at Light-Load Condition
  - Impedance Modulation in Standby Mode for "Deep" Burst Mode Operation
  - Low Operating Current (450μA) in Standby Mode
  - 500V High-Voltage JFET Startup Circuit to Eliminate Startup Resistor Loss
- Highly Integrated with Rich Features
  - Proprietary Asynchronous-Jitter to Reduce EMI
  - High-Voltage Sampling to Detect Input Voltage
  - Peak-Current-Mode Control with Slope Compensation
  - Cycle-by-Cycle Current Limiting with Line Compensation
  - Leading Edge Blanking (LEB)
  - Built-In 8ms Soft-Start
- Advanced Protections
  - Brown-In/Brownout Recovery
  - Internal Overload/Open-Loop Protection (OLP)
  - $V_{DD}$ Under-Voltage Lockout (UVLO)
  - $V_{DD}$ Over-Voltage Protection ($V_{DD}$ OVP)
  - Over-Temperature Protection (OTP)
  - Current-Sense Short-Circuit Protection (SSCP)

## Description

The FAN6756 is a next-generation Green Mode PWM controller with innovative mWSaver™ technology, which dramatically reduces standby and no-load power consumption, enabling conformance to worldwide Standby Mode efficiency guidelines.

An innovative AX-CAP™ method minimizes losses in the EMI filter stage by eliminating the X-cap discharge resistors while meeting IEC61010-1 safety requirements. Standby Mode clamps feedback voltage and modulates feedback impedance with a impedance modulator during Burst Mode operation, which forces the system to operate in a "deep" Burst Mode with minimum switching losses.

Protections ensure safe operation of power system in various abnormal conditions. Proprietary asynchronous jitter decreases EMI emission and built-in synchronized slope compensation allows more stable Peak-Current-Mode control over wide range of input voltage and load conditions. The proprietary internal line compensation ensures constant output power limit over entire universal line voltage range.

Requiring a minimum number of external components, FAN6756 provides a basic platform that is well suited for cost-effective flyback converter designs that require extremely low standby power consumption.

## Applications

Flyback power supplies that demand extremely low standby power consumption, such as:

- Adapters for Notebooks, Printers, Game Consoles, etc.
- Open-Frame SMPS for LCD TV, LCD Monitors, Printer Power, etc.

## Ordering Information

| Part Number | Protections[1] | | | | Operating Temperature Range | Package | Packing Method |
|---|---|---|---|---|---|---|---|
| | OLP | OVP | OTP | SSCP | | | |
| FAN6756MRMY | A/R | L | L | A/R | -40 to +105°C | 8-Pin, Small Outline Package (SOP) | Tape & Reel |
| FAN6756MLMY | L | L | L | A/R | | | |

**Note:**

1. A/R = Auto Recovery Mode protection, L = Latch Mode protection.

## Application Diagram

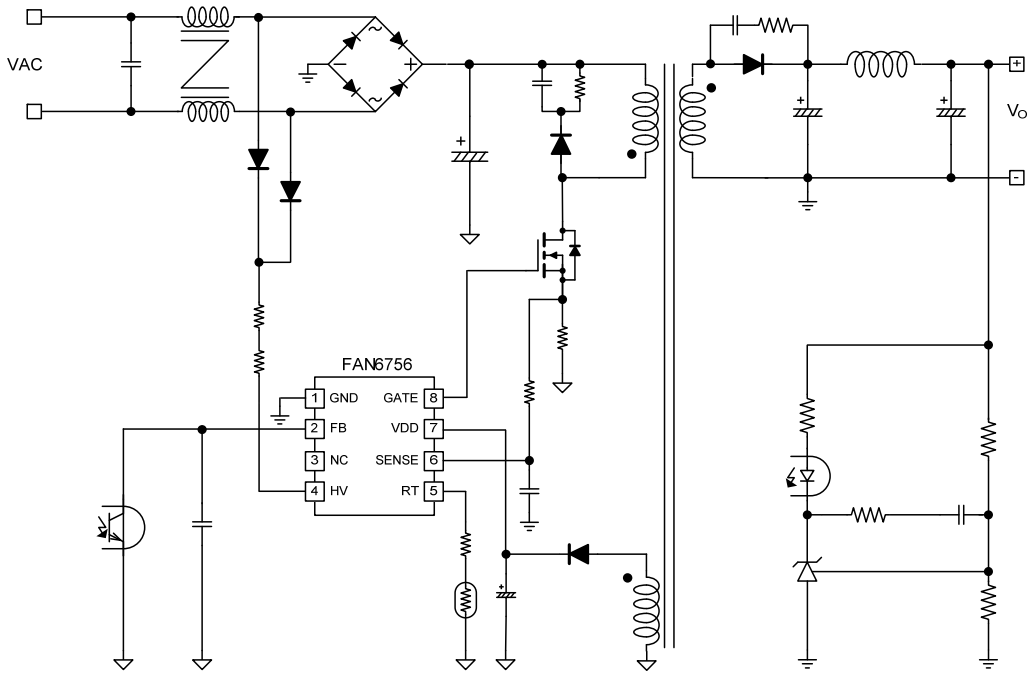



**Figure 1. Typical Application Diagram**

## Internal Block Diagram

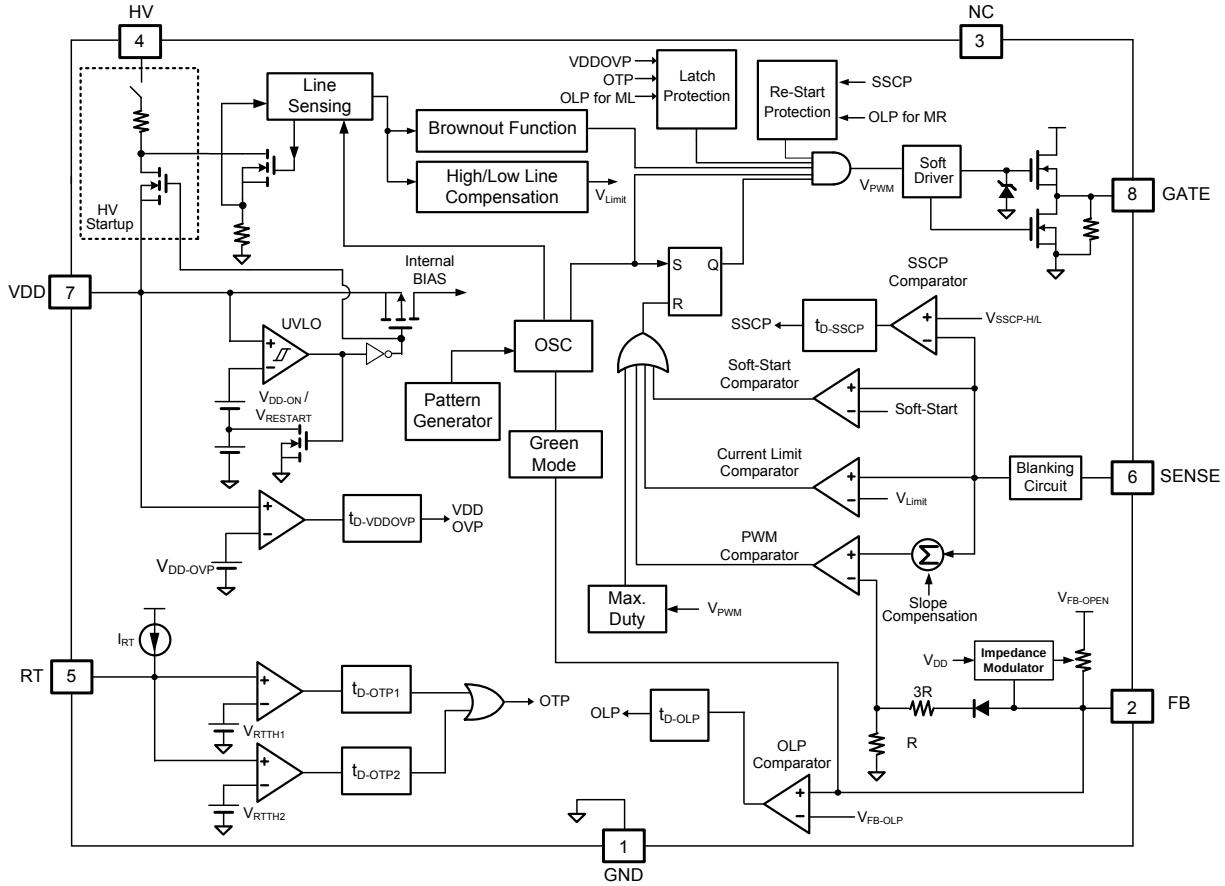
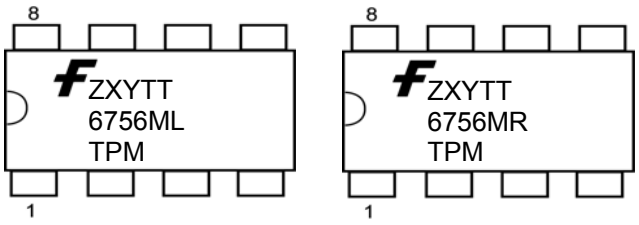



**Figure 2. Functional Block Diagram**

## Marking Information




*F* - Fairchild Logo
Z - Plant Code
X - 1-Digit Year Code
Y - 1-Digit Week Code
TT - 2-Digit Die Run Code
T - Package Type (M=SOP)
P - Y: Green Package
M - Manufacture Flow Code

**Figure 3. Top Mark**

## Pin Configuration

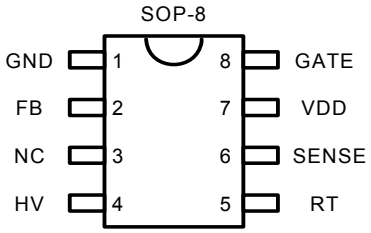



**Figure 4. Pin Configuration (Top View)**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1 | GND | Ground Pin. Placing a 0.1μF decoupling capacitor between VDD and GND is recommended. |
| 2 | FB | Feedback Pin. The output voltage feedback information from the external compensation circuit is fed into this pin. The PWM duty cycle is determined by comparing the FB signal with the current-sense signal from the SENSE pin. |
| 3 | NC | No Connection |
| 4 | HV | High-Voltage Startup. The HV pin is typically connected to the AC line input through two external diodes and one resistor ($R_{HV}$). This pin is used, not only to charge the $V_{DD}$ capacitor during startup, but also to sense the line voltage. The line voltage information is used for brownout protection and power limit line compensation. This pin also is used to intelligently discharge the EMI filter capacitor when the removal of the AC line voltage is detected. |
| 5 | RT | Over-Temperature Protection. An external NTC thermistor is connected from this pin to the GND pin. Once the voltage of the RT pin drops below the threshold voltage, the controller latches off the PWM. The RT pin also provides external latch protection. If the RT pin is not connected to the NTC resistor for over-temperature protection, it is recommended to place a 100kΩ resistor to ground to prevent noise interference. |
| 6 | SENSE | Current Sense. The sensed voltage is used for Peak-Current-Mode control, short-circuit protection, and cycle-by-cycle current limiting. |
| 7 | VDD | Power Supply of IC. Typically a hold-up capacitor connects from this pin to ground. A rectifier diode, in series with the transformer auxiliary winding, connects to this pin to supply bias during normal operation. |
| 8 | GATE | Gate Drive Output. The totem-pole output driver for the power MOSFET; internally limited to $V_{GATE-CLAMP}$. |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{VDD}$ | DC Supply Voltage[2,3] | | | 30 | V |
| $V_{FB}$ | FB Pin Input Voltage | | -0.3 | 7.0 | V |
| $V_{SENSE}$ | SENSE Pin Input Voltage | | -0.3 | 7.0 | V |
| $V_{RT}$ | RT Pin Input Voltage | | -0.3 | 7.0 | V |
| $V_{HV}$ | HV Pin Input Voltage | | | 500 | V |
| $P_D$ | Power Dissipation ($T_A$=50°C) | | | 400 | mW |
| $\Theta_{JA}$ | Thermal Resistance (Junction-to-Air) | | | 150 | °C/W |
| $T_J$ | Operating Junction Temperature | | -40 | +125 | °C |
| $T_{STG}$ | Storage Temperature Range | | -55 | +150 | °C |
| $T_L$ | Lead Temperature (Wave Soldering or IR, 10 Seconds) | | | +260 | °C |
| ESD | Human Body Model, JEDEC:JESD22-A114 | All Pins Except HV Pin[4] | | 6000 | V |
| | Charged Device Model, JEDEC:JESD22-C101 | All Pins Except HV Pin[4] | | 2000 | |

**Notes**:
2. All voltage values, except differential voltages, are given with respect to the network ground terminal.
3. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
4. ESD level with the HV pin is CDM=1250V and HBM=500V.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $R_{HV}$ | Resistance on HV Pin | 150 | 200 | 250 | kΩ |

## Electrical Characteristics

$V_{DD}$=15V and $T_A$=25°C unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **$V_{DD}$ Section** | | | | | | |
| $V_{OP}$ | Continuously Operating Voltage | Limited by $V_{DD}$ OVP | | | 22 | V |
| $V_{DD-ON}$ | Threshold Voltage to Startup | $V_{DD}$ Rising | 16 | 17 | 18 | V |
| $V_{DD-OFF}$ | Threshold Voltage to Stop Switching in Protection Mode | $V_{DD}$ Falling | 10 | 11 | 12 | V |
| $V_{DD-OLP}$ | Threshold Voltage to Turn-on HV Startup in Protection Mode | $V_{DD}$ Falling | 6 | 7 | 8 | V |
| $V_{UVLO}$ | Threshold Voltage to Stop Switching in Normal Mode | $V_{DD}$ Falling | 5.5 | 6.5 | 7.5 | V |
| $V_{RESTART}$ | Threshold Voltage to Enable HV Startup to charge $V_{DD}$ in Normal Mode | $V_{DD}$ Falling | | 5 | | V |
| $V_{DD-LH}$ | Threshold Voltage to Release Latch Mode | $V_{DD}$ Falling | 3.5 | 4.0 | 4.5 | V |
| $V_{DD-AC}$ | Threshold Voltage for Brown-in | | 9.0 | 9.5 | 10.0 | V |
| $I_{DD-ST}$ | Startup Current | $V_{DD-ON}$ – 0.16V | | | 30 | µA |
| $I_{DD-OP1}$ | Supply Current in PWM Operation | $V_{DD}$=15V, $V_{FB}$=3V, Gate Open | | | 1.8 | mA |
| $I_{LH}$ | Operating Current when $V_{DD}$<$V_{DD-OFF}$ in Protection Mode | $V_{DD}$=5V | | 70 | | µA |
| $I_{DD-OP2}$ | Supply Current when PWM Stops | $V_{DD}$=15V, $V_{FB}$ <1.4V, Gate Off | | 450 | | µA |
| $I_{DD-OLP}$ | Internal Sink Current from $V_{DD-OFF}$ to $V_{DD-OLP}$ in Protection Mode | $V_{DD-OLP}$+0.1V | 160 | 210 | 260 | µA |
| $V_{DD-OVP}$ | Threshold Voltage for $V_{DD}$ Over-Voltage Protection | | 23.5 | 24.5 | 25.5 | V |
| $t_{D-VDDOVP}$ | $V_{DD}$ Over-Voltage Protection Debounce Time | | 110 | 185 | 260 | µs |

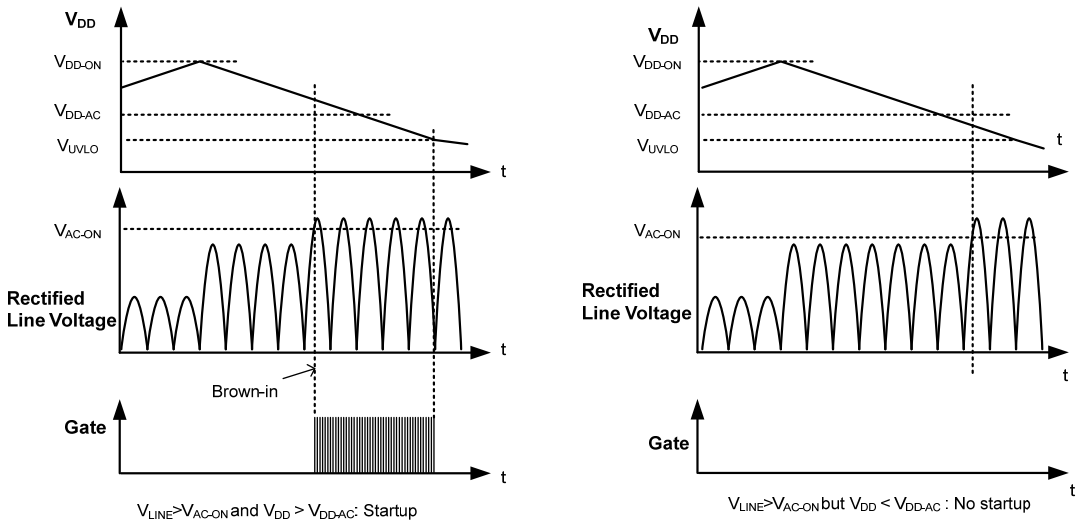



**Figure 5. Timing Diagram for Brown-in Function**

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## Electrical Characteristics (Continued)

$V_{DD}$=15V and $T_A$=25°C unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **HV Section** | | | | | | |
| $I_{HV}$ | Supply Current from HV Pin | $V_{AC}$=90V ($V_{DC}$=120V), $V_{DD}$=0V | 2.0 | 3.0 | 4.5 | mA |
| $V_{AC-OFF}$ | Threshold Voltage for Brownout | DC Source Series R=200kΩ to HV Pin | 90 | 100 | 110 | V |
| $V_{AC-ON}$ | Threshold Voltage for Brown-In | DC Source Series R=200kΩ to HV Pin | 100 | 110 | 120 | V |
| $\Delta V_{AC}$ | $V_{AC-ON}$ - $V_{AC-OFF}$ | DC Source Series R=200kΩ to HV Pin | 8 | 12 | 16 | V |
| $t_{D-AC-OFF}$ | Debounce Time for Brownout | | 40 | 65 | 90 | ms |
| $V_{HV-DIS}$ | X-Cap. Discharge Threshold | $V_{FB}$<$V_{FB-G}$ R=200kΩ to HV Pin | $V_{DC}$ ×0.45 | $V_{DC}$[5] ×0.51 | $V_{DC}$ ×0.56 | V |
| $t_{D-HV-DIS}$ | Debounce Time for Triggering X-Cap. Discharge | | 30 | 40 | 50 | ms |
| **Oscillator Section** | | | | | | |
| $f_{OSC}$ | Switching Frequency When $V_{FB}$>$V_{FB-N}$ | Center Frequency | 62 | 65 | 68 | kHz |
| | | Hopping Range ($V_{FB}$>$V_{FB-N}$) | ±3.7 | ±4.2 | ±4.7 | |
| $t_{HOP}$ | Hopping Period | $V_{FB}$>$V_{FB-N}$ | | 4.0 | 6.5 | ms |
| $f_{OSC-G}$ | Switching Frequency When $V_{FB}$<$V_{FB-G}$ | $V_{FB}$<$V_{FB-G}$ | 20 | 23 | 26 | kHz |
| $f_{DV}$ | Frequency Variation vs. $V_{DD}$ Deviation | $V_{DD}$=11V to 22V | | | 5 | % |
| $f_{DT}$ | Frequency Variation vs. Temperature Deviation | $T_A$=-40 to 105°C | | | 5 | % |
| **Feedback Input Section** | | | | | | |
| $A_V$ | Feedback Voltage to Current-Sense Attenuation | | 1/4.5 | 1/4.0 | 1/3.5 | V/V |
| $Z_{FB}$ | Regular FB Internal Pull-High Impedance | | | 8.5 | | kΩ |
| $V_{FB-OPEN}$ | FB internal Biased Voltage | FB Pin Open | 5.2 | 5.4 | 5.6 | V |
| $V_{FB-OLP}$ | Threshold Voltage for OLP | | 4.3 | 4.6 | 4.9 | V |
| $t_{D-OLP}$ | Debounce Time for OLP | | 45.0 | 57.5 | 70.0 | ms |
| $V_{FB-N}$ | Threshold Voltage for Maximum Switching Frequency | | 2.6 | 2.8 | 3.0 | V |
| $V_{FB-G}$ | Threshold Voltage for Minimum Switching Frequency | | 2.1 | 2.3 | 2.5 | V |
| $V_{FB-ZDC1}$ | Threshold Voltage for Zero-Duty Cycle | | 1.8 | 2.0 | 2.2 | V |
| $V_{FB-ZDCR1}$ | Threshold Voltage for Zero-Duty Cycle Recovery | | 1.9 | 2.1 | 2.3 | V |
| $V_{FB-ZDC2}$ | Threshold Voltage for Zero Duty Cycle in Standby Mode | | 2.35 | 2.55 | 2.75 | V |
| $V_{FB-ZDCR2}$ | Threshold Voltage for Zero-Duty Cycle Recovery in Standby Mode | | 2.4 | 2.6 | 2.8 | V |

*Continued on the following page…*

## Electrical Characteristics (Continued)

$V_{DD}$=15V and $T_A$=25°C unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Current-Sense Section** | | | | | | |
| $t_{LEB}$ | Leading-Edge Blanking | | 230 | 280 | 330 | ns |
| $V_{LIMIT-L}$ | Current Limit Level at Low Line ($V_{AC-RMS}$=86V) | $V_{DC}$=122V, Series R=200kΩ to HV | 0.43 | 0.46 | 0.49 | V |
| $V_{LIMIT-H}$ | Current Limit Level at High Line ($V_{AC-RMS}$=259V) | $V_{DC}$=366V, Series R=200kΩ to HV | 0.36 | 0.39 | 0.42 | V |
| $V_{SSCP-L}$ | The Lower Threshold Voltage for SSCP | $V_{DC}$=122V, Series R=200kΩ to HV | 30 | 50 | 70 | mV |
| $V_{SSCP-H}$ | The Upper Threshold Voltage for SSCP | $V_{DC}$=366V, Series R=200kΩ to HV | 80 | 100 | 120 | mV |
| $t_{ON-SSCP}$ | Minimum On Time of Gate to Trigger SSCP | $V_{SENSE}$<$V_{SSCP-L/H}$ | 4.00 | 4.55 | 5.10 | µs |
| $t_{D-SSCP}$ | Debounce Time for SSCP | $V_{SENSE}$<$V_{SSCP-L/H}$ | 110 | 170 | 230 | µs |
| $t_{SS}$ | Soft-Start Time | Startup | 6.50 | 7.75 | 9.00 | ms |
| **GATE Section** | | | | | | |
| $DCY_{MAX}$ | Maximum Duty Cycle | | 80 | 85 | 90 | % |
| $V_{GATE-L}$ | Gate Low Voltage | $V_{DD}$=15V, $I_O$=50mA | | | 1.5 | V |
| $V_{GATE-H}$ | Gate High Voltage | $V_{DD}$=12V, $I_O$=50mA | 8 | | | V |
| $t_r$ | Gate Rising Time | $V_{DD}$=15V, $C_L$=1nF | | 125 | | ns |
| $t_f$ | Gate Falling Time | $V_{DD}$=15V, $C_L$=1nF | | 50 | | ns |
| $t_{PD}$ | Propagation Delay to Output | | | 100 | 250 | ns |
| $V_{GATE-CLAMP}$ | Gate Output Clamping Voltage | $V_{DD}$=22V | 11.0 | 14.5 | 18.0 | V |
| **RT Section** | | | | | | |
| $I_{RT}$ | Output Current of RT Pin | | | 100 | | µA |
| $V_{RTTH1}$ | Threshold Voltage for Over-Temperature Protection | 0.7V < $V_{RT}$ < 1.035V, After 14.5ms Latch Off | 1.000 | 1.035 | 1.070 | V |
| $V_{RTTH2}$ | Threshold Voltage for Latch Triggering | $V_{RT}$ < 0.7V, After 185µs Latch Off | 0.65 | 0.70 | 0.75 | V |
| $R_{OTP}$ | Maximum External Resistance of RT Pin to Trigger Latch Protection | | 9.66 | 10.50 | 11.34 | kΩ |
| $t_{D-OTP1}$ | Debounce Time for Over-Temperature Protection Triggering | $V_{RTTH2}$ < $V_{RT}$ < $V_{RTTH1}$ | 11.0 | 14.5 | 18.0 | ms |
| $t_{D-OTP2}$ | Debounce Time for Latch Triggering | $V_{RT}$ < $V_{RTTH2}$ | 110 | 185 | 260 | µs |
| **Internal Over-Temperature Protection Section** | | | | | | |
| $T_{OTP}$ | Protection Junction Temperature[6] | | | +135 | | °C |
| $T_{Restart}$ | Restart Junction Temperature[7] | | | $T_{OTP}$-25 | | °C |

**Notes:**

5. $V_{DC}$ is $V_{AC}$ × √2.
6. When activated, the output is disabled and the controller is latched.
7. The threshold temperature to unlatch and restart output after OTP.

## Typical Performance Characteristics

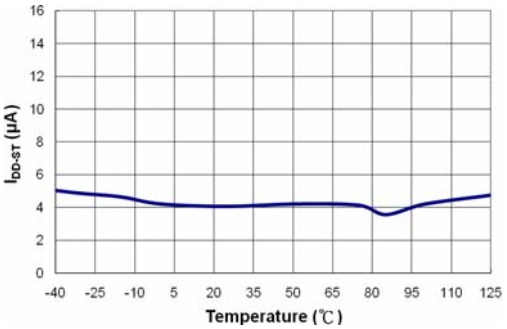


**Figure 6. Startup Current ($I_{DD-ST}$) vs. Temperature**

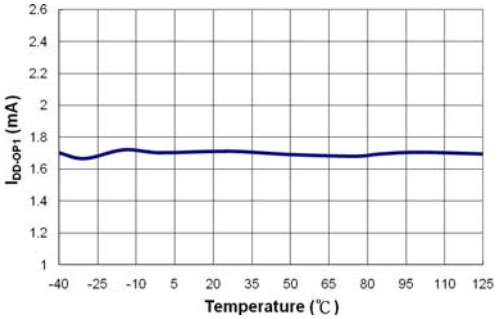


**Figure 7. Operation Supply Current ($I_{DD-OP1}$) vs. Temperature**

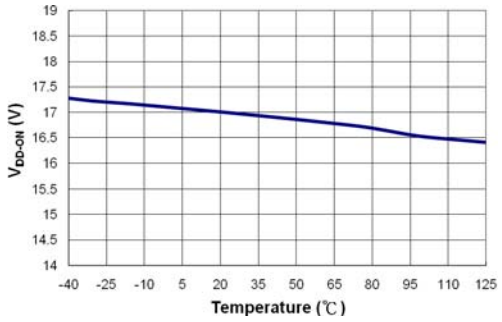


**Figure 8. Start Threshold Voltage ($V_{DD-ON}$) vs. Temperature**

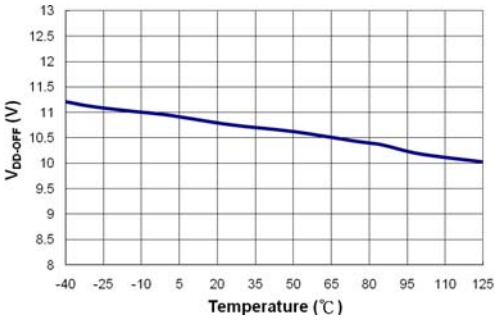


**Figure 9. Minimum Operating Voltage ($V_{DD-OFF}$) vs. Temperature**

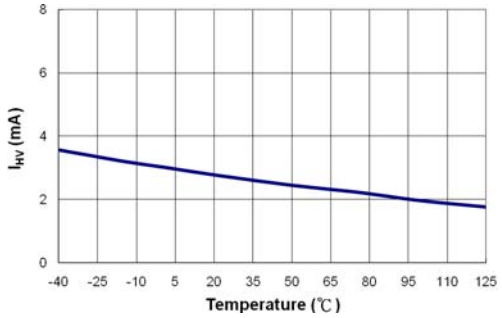


**Figure 10. Supply Current Drawn from HV Pin ($I_{HV}$) vs. Temperature**

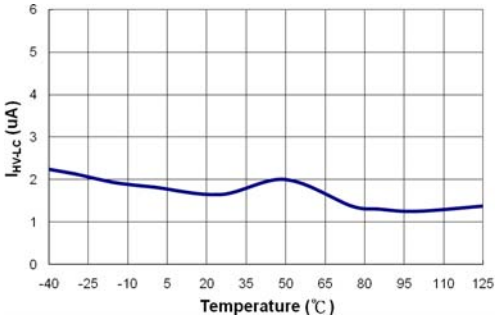


**Figure 11. HV Pin Leakage Current After Startup ($I_{HV-LC}$) vs. Temperature**

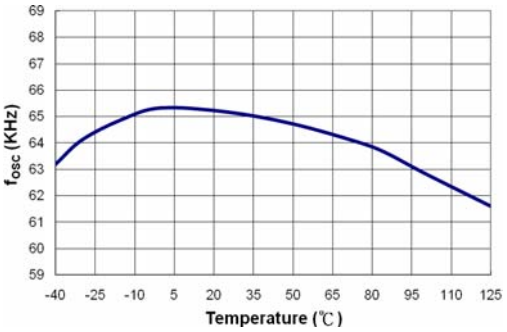


**Figure 12. Frequency in Normal Mode ($f_{OSC}$) vs. Temperature**

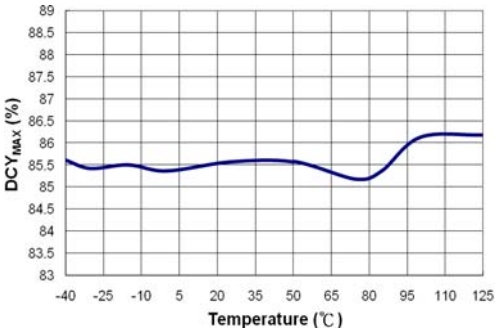


**Figure 13. Maximum Duty Cycle ($DCY_{MAX}$) vs. Temperature**

## Typical Performance Characteristics (Continued)

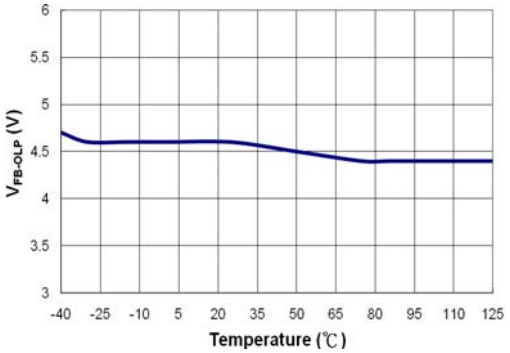


**Figure 14. FB Open-Loop Trigger Level ($V_{FB-OLP}$) vs. Temperature**

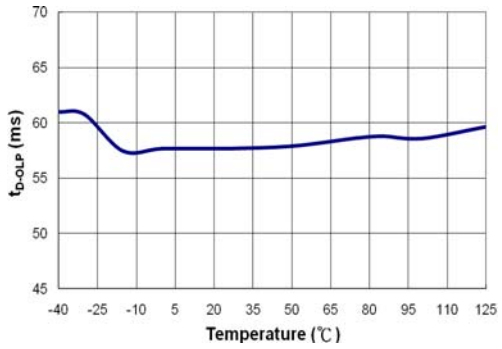


**Figure 15. Delay Time of FB Pin Open-Loop Protection ($t_{D-OLP}$) vs. Temperature**

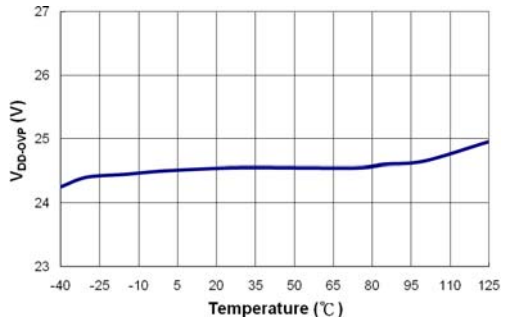


**Figure 16. $V_{DD}$ Over-Voltage Protection ($V_{DD-OVP}$) vs. Temperature**

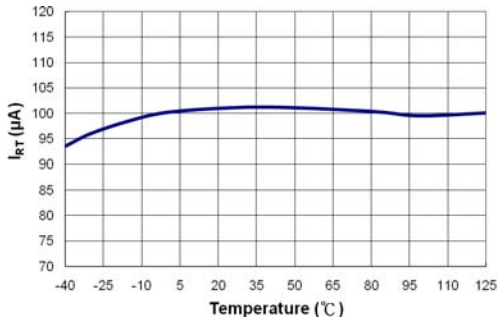


**Figure 17. Output Current from RT Pin ($I_{RT}$) vs. Temperature**

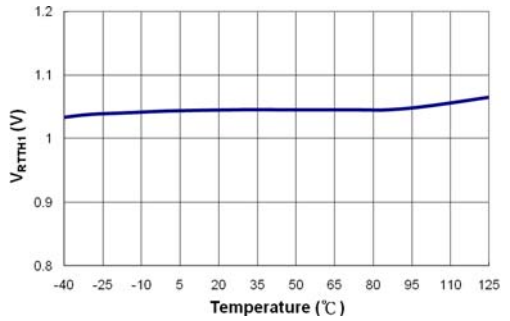


**Figure 18. Over-Temperature Protection Threshold Voltage ($V_{RTTH1}$) vs. Temperature**

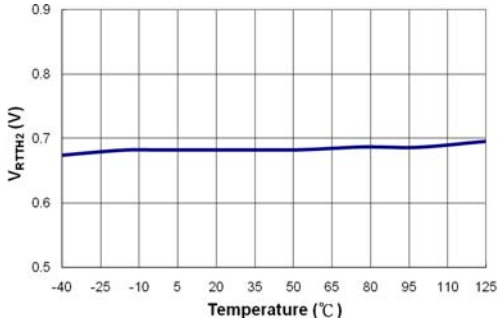


**Figure 19. Over-Temperature Protection Threshold Voltage ($V_{RTTH2}$) vs. Temperature**

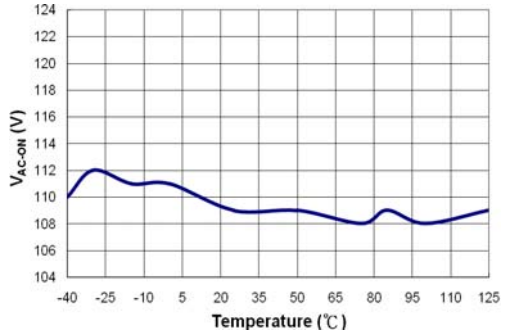


**Figure 20. Brown-In ($V_{AC-ON}$) vs. Temperature**

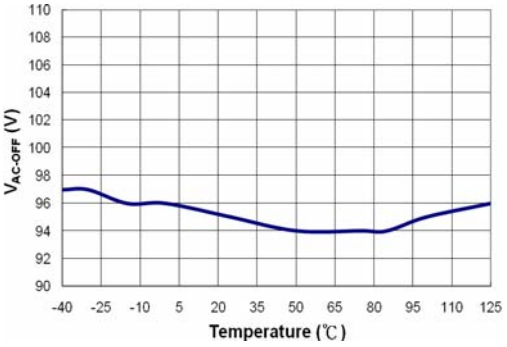


**Figure 21. Brownout ($V_{AC-OFF}$) vs. Temperature**

# Functional Description

## Current Mode Control

FAN6756 employs Peak-Current Mode control, as shown in Figure 22. An opto-coupler (such as the H11A817A) and a shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the $R_{sense}$ resistor makes it possible to control the switching duty cycle. A synchronized positive slope is added to the sensed current signal to guarantee stable Current-Mode control over a wide range of input voltages. The built-in slope compensation stabilizes the current loop and prevents sub-harmonic oscillation.

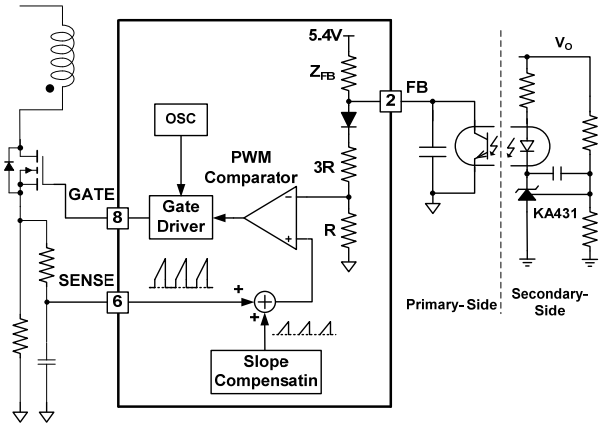


**Figure 22. Current Mode Control Circuit Diagram**

## Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time, $t_{LEB}$, is introduced. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

## mWSaver™ Technology

### Green-Mode

FAN6756 modulates the PWM frequency as a function of the FB voltage to improve the medium and light load efficiency, as shown in Figure 23. Since the output power is proportional to the FB voltage in Current-Mode control, the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is fixed at 65kHz. Once $V_{FB}$ decreases below $V_{FB-N}$ (2.8V), the PWM frequency starts linearly decreasing from 65kHz to 23kHz to reduce switching losses. As $V_{FB}$ drops to $V_{FB-G}$ (2.3V), where switching frequency is decreased to 23kHz, the switching frequency is fixed to avoid acoustic noise.

When $V_{FB}$ falls below $V_{FB-ZDC1}$ (2.0 V) as load decreases further, FAN6756 enters Burst Mode where PWM switching is disabled. Then the output voltage starts to drop, causing the feedback voltage to rise. Once $V_{FB}$ rises above $V_{FB-ZDCR1}$ (2.1V), switching resumes. Burst Mode alternately enables and disables switching, thereby reducing switching loss for lower power consumption, as shown in Figure 24.

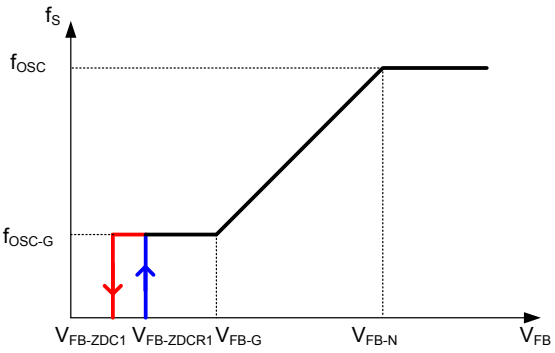


**Figure 23. $V_{FB}$ vs. PWM Frequency**

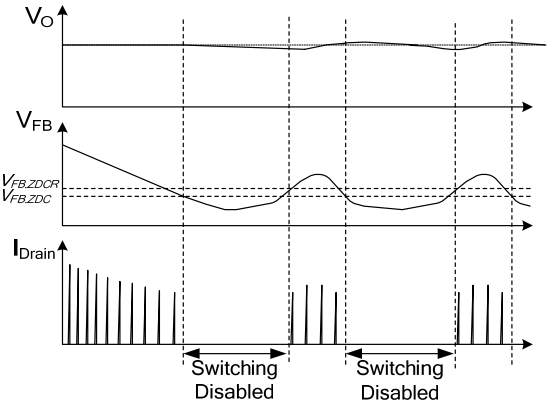


**Figure 24. Burst Switching in Green Mode**

### Standby Mode & Feedback Impedance Switching

Standby Mode is defined as a special operational mode to minimize power consumption at extremely light-load or no-load condition where, not only the switching loss, but also power consumption of FAN6756 itself, are reduced further than in Green Mode. Standby Mode is initiated when the non-switching state of burst switching in Green Mode persists longer than 10ms for three consecutive burst switchings (as shown in Figure 25). To prevent entering Standby Mode during dynamic load change, there is 900ms delay. If there are more than 104 consecutive switching pulses during the 900ms delay, FAN6756 does not go into Standby Mode.

Once FAN6756 enters Standby Mode, the feedback impedance, $Z_{FB}$, is modulated by the impedance modulator, as shown in Figure 26. When $V_{FB}$ is under a threshold level, the impedance modulator clamps $V_{FB}$ and disables switching. When $V_{DD}$ drops to 7V (0.5V higher than $V_{DD-OFF}$), the impedance modulator controls $Z_{FB}$, allowing $V_{FB}$ to rise and resume switching operation. As shown in Figure 27, by clamping $V_{FB}$ to disable switching, while modulating $Z_{FB}$ to enable switching, the system is forced into deep Burst Mode to reduce switching loss.

Deep Burst Mode maintains $V_{DD}$ as low as possible so power consumption can be minimized. When FAN6756 enters Standby Mode, several blocks are disabled and the operation current is reduced from 1.8mA ($I_{DD-OP1}$).

The feedback voltage thresholds where FAN6756 enters and exits Burst Mode change from $V_{FB-ZDC1}$

(2.0V) and $V_{FB-ZDCR1}$ (2.1V) to $V_{FB-ZDC2}$ (2.55V) and $V_{FB-ZDCR2}$ (2.6V) in deep Burst Mode. This reduces the switching loss more by increasing the energy delivered to the load per switching operation, which eventually reduces the total switching for a given load condition.

FAN6756 exits Standby Mode after more than 104 consecutive switching pulses in deep Burst Mode. Once FAN6756 exits Standby Mode, the feedback impedance is modulated to 8.5kΩ to keep original loop response. FAN6756 also exits Standby Mode when opto-coupler transistor current is virtually zero and $V_{FB}$ rises above 0.75V while switching is suspended in deep burst mode.

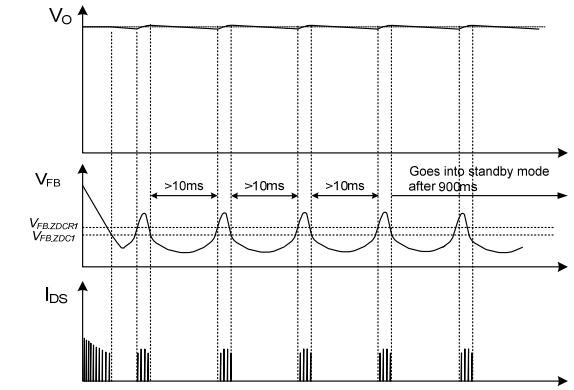


**Figure 25. Entering Standby Mode**

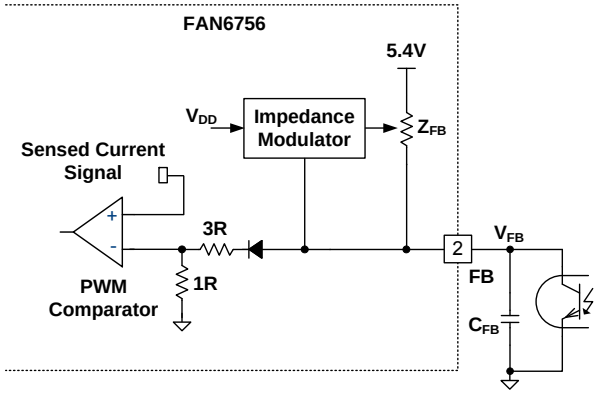


**Figure 26. Feedback Impedance Modulation**

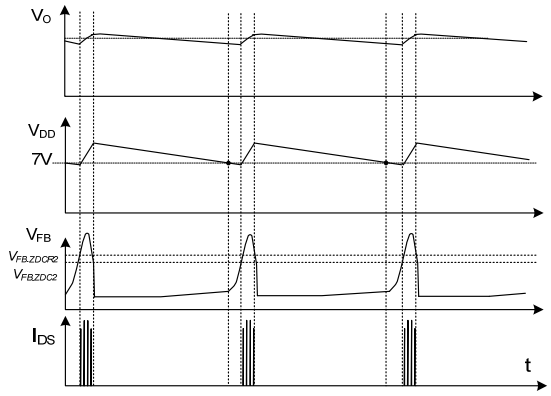


**Figure 27. Deep Burst Operation in Standby Mode**

### High-Voltage Startup and Line Sensing

The HV pin is typically connected to the AC line input through two external diodes and one resistor ($R_{HV}$), as shown in Figure 28. When the AC line voltage is applied, the $V_{DD}$ hold-up capacitor is charged by the line voltage through the diodes and resistor. After $V_{DD}$ voltage reaches the turn-on threshold voltage ($V_{DD-ON}$), the startup circuit charging $V_{DD}$ capacitor is switched off and $V_{DD}$ is supplied by the auxiliary winding of the transformer. Once FAN6756 starts, it continues operating until $V_{DD}$ drops below 6.5V ($V_{UVLO}$). IC startup time with a given AC line input voltage is given as:

$$t_{STARTUP} = R_{HV} \cdot C_{DD} \cdot \ln \frac{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi}}{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi} - V_{DD-ON}} \quad (1)$$

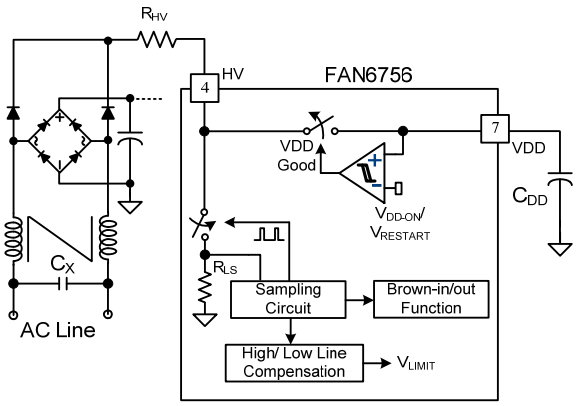


**Figure 28. Startup Circuit**

The HV pin detects the AC line voltage using a switched voltage divider that consists of external resistor ($R_{HV}$) and internal resistor ($R_{LS}$), as shown in Figure 28. The internal line-sensing circuit detects line voltage using a sampling circuit and peak-detection circuit. Since the voltage divider causes power consumption when it is switched on, the switching is driven by a signal with a very narrow pulse width to minimize power loss. The sampling frequency is adaptively changed according to the load condition to minimize power consumption in light-load condition.

Based on the detected line voltage, brown-in and brownout thresholds are determined as:

$$V_{BROWN-IN}\,(\text{RMS}) = \frac{R_{HV}}{200\text{k}} \cdot \frac{V_{AC-ON}}{\sqrt{2}} \quad (2)$$

$$V_{BROWNOUT}\,(\text{RMS}) = \frac{R_{HV}}{200\text{k}} \cdot \frac{V_{AC-OFF}}{\sqrt{2}} \quad (3)$$

Since the internal resistor ($R_{LS}$=1.6kΩ) of the voltage divider is much smaller than $R_{HV}$, the thresholds are simply given as s function of $R_{HV}$.

**Note:**

8. $V_{DD}$ must be larger than $V_{DD-AC}$ to start, even though the sensed line voltage satisfies Equation (2), as shown in Figure 5.

**AX-CAP™ Discharge**

The EMI filter in the front end of the switched-mode power supply (SMPS) typically includes capacitor across AC line connector. Most of the safety regulations, such as UL 1950 and IEC61010-1, require the capacitor be discharged to a safe level within a given time when the AC plug is abruptly removed from its receptacle. Typically, discharge resisters across the capacitor are used to make sure that capacitor is discharged naturally, which introduces power loss as long as it is connected to the receptacle.

The innovative AX-CAP™ technology intelligently discharges the filter capacitor only when the power supply is unplugged from the power outlet. Since the AX-CAP discharge circuit is disabled in normal operation, the power loss in the EMI filter can be virtually removed.

The discharge of the capacitor is achieved through the HV pin. Once AC outlet detaching is detected, the PWM gate remains off and $V_{DD}$ drops to $_{VDD-OFF}$. Then $V_{DD}$ is charged up, which discharges the filter capacitor.

## High/Low Line Compensation for Constant Power Limit

FAN6756 has pulse-by-pulse current limit as shown in Figure 29, which limits the maximum input power with a given input voltage. If the output consumes beyond this maximum power, the output voltage drops, triggering the overload protection.

As shown in Figure 29, based on the line voltage, $V_{LINE}^{PK}$; the high/low line compensation block adjusts the current limit level, $V_{LIMIT}$, defined as:

$$V_{LIMIT} = \frac{V_{LIMIT-H} - V_{LIMIT-L}}{2} \cdot \frac{R_{LS}}{R_{HV}} \cdot V_{LINE}^{PK} + \frac{3 \cdot V_{LMIT-L} - V_{LIMIT-H}}{2} \quad (4)$$

To maintain the constant output power limit regardless of line voltage, the cycle-by-cycle current limit level, $V_{LIMIT}$, decreases as line voltage increases. The current limit level is proportional to the $R_{HV}$ resistor value and power limit can be tuned using the $R_{HV}$ resistor. Figure 30 shows how the pulse-by-pulse current limit changes with the line voltage for different $R_{HV}$ resistors.

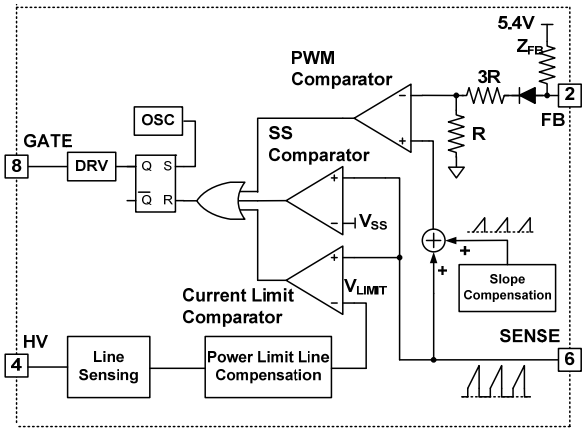


**Figure 29. Pulse-by-Pulse Current Limit Circuit**

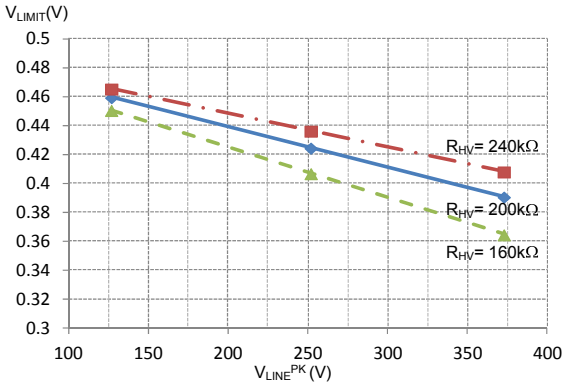


**Figure 30. Current Limit vs. Line voltage**

## Soft-Start

An internal soft-start circuit progressively increases the pulse-by-pulse current limit level of MOSFET for 8ms during startup to establish the correct working conditions for transformers and capacitors.

## Protections

FAN6756 provides full protection functions, including Overload / Open-Loop Protection (OLP), $V_{DD}$ Over-Voltage Protection (OVP), Over-Temperature Protection (OTP), and Current-Sense Short Circuit Protection (SSCP). SSCP is implemented as Auto-Restart Mode, while OVP and OTP are implemented as Latch Mode protections. OLP is Auto-Restart Mode for FAN6756MR and Latch Mode for FAN6756ML.

When an Auto-Restart Mode protection is triggered, switching is terminated and the MOSFET remains off, causing $V_{DD}$ to drop. When $V_{DD}$ drops to the $V_{DD-OFF}$ (11V), the protection is reset. When $V_{DD}$ drops further to $V_{DD-OLP}$ (7V), the internal startup circuit is enabled, and the supply current drawn from HV pin charges the hold-up capacitor. When $V_{DD}$ reaches the turn-on voltage of 17V, FAN6756 resumes normal operation. In this manner, the auto restart alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated.

When a Latch Mode protection is triggered, PWM switching is terminated and the MOSFET remains off, causing $V_{DD}$ to drop. When $V_{DD}$ drops to the $V_{DD-OLP}$ (7V), the internal startup circuit is enabled without resetting the protection and the supply current drawn from HV pin charges the hold-up capacitor. Since the protection is not reset, the IC does not resume PWM switching even when $V_{DD}$ reaches the turn-on voltage of 17V, disabling HV startup circuit. Then $V_{DD}$ drops again down to 7V. In this manner, the Latch Mode protection alternately charges and discharges $V_{DD}$ until there is no more energy in DC link capacitor. The protection is reset when $V_{DD}$ drops to 4V, which is allowed only after power supply is unplugged from the AC line.

**$V_{DD}$ Over-Voltage Protection (OVP)**

$V_{DD}$ over-voltage protection prevents IC damage from voltage exceeding the IC voltage rating. When the $V_{DD}$ voltage exceeds 24.5V, the protection is triggered. This protection is typically caused by an open circuit in the secondary-side feedback network.

**Over-Temperature Protection (OTP) and External Latch Triggering**

The RT pin provides adjustable Over-Temperature Protection (OTP) and external latch triggering function. For OTP, an NTC thermistor, $R_{NTC}$, usually in series with a resistor $R_A$, is connected between the RT pin and ground. The internal current source, $I_{RT}$ (100μA), introduces voltage on RT as:

$$V_{RT} = I_{RT} \cdot (R_{NTC} + R_A) \quad (5)$$

At high ambient temperature, $R_{NTC}$ decreases, reducing $V_{RT}$. When $V_{RT}$ is lower than $V_{RTTH1}$ (1.035V) for longer than $t_{D-OTP1}$ (14.5ms), the protection is triggered and FAN6756 enters Latch Mode protection.

The OTP can be trigged by pulling down the RT pin voltage using an opto-coupler or transistor. Once $V_{RT}$ is less than $V_{RTTH2}$ (0.7V) for longer than $t_{D-OTP2}$ (185μs), the protection is triggered and FAN6756 enters Latch Mode protection.

When OTP is not used, it is recommended to place a 100kΩ resistor between this pin and ground to prevent noise interference.

**Open-Loop/Overload Protection (OLP)**

Because of the pulse-by-pulse current limit capability, the maximum peak current is limited, and therefore the maximum input power is also limited. If the output consumes more than this limited maximum power, the output voltage ($V_O$) drops below the set voltage. Then, the currents through the opto-coupler and transistor become virtually zero and $V_{FB}$ is pulled HIGH. Once $V_{FB}$ is higher than $V_{FB-OLP}$ (4.6V) for longer than $t_{D-OLP}$ (57.5ms), OLP is triggered. OLP is also triggered when the feedback loop is open by soldering defect.

**Sense Short-Circuit Protection (SSCP)**

FAN6756 provides safety protection for Limited Power Source (LPS) test. When the current-sense resistor is short circuited by a soldering defect during production, the current sensing information is not properly obtained, resulting in unstable operation of power supply.

To protect the power supply against a short circuit across the current-sense resistor, FAN6756 shuts down when current sense voltage is very low; even with a relatively large duty cycle. As shown in Figure 31, the current-sense voltage is sampled $t_{ON-SSCP}$ (4.55μs) after the gate turn-on. If the sampled voltage ($V_{S-CS}$) is lower than $V_{SSCP}$ for 11 consecutive switching cycles (170μs), the FAN6756 shuts down immediately. $V_{SSCP}$ varies linearly with line voltage. At 122V DC input, it is typically 50mV ($V_{SSCP-L}$); at 366V DC, it is typically 100mV ($V_{SSCP-H}$).

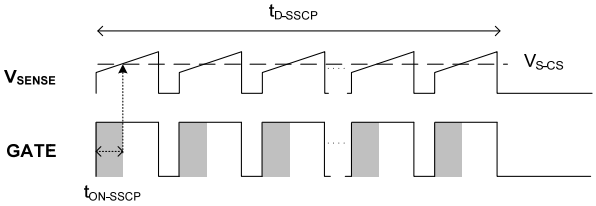


**Figure 31. Timing Diagram of SSCP**

**Two-Level Under-Voltage Lockout (UVLO)**

As shown in Figure 32, as long as protection is not triggered, the turn-off threshold of $V_{DD}$ is fixed internally at $V_{UVLO}$ (6.5V). When a protection is triggered, the $V_{DD}$ level to terminate PWM gate switching is changed to $V_{DD-OFF}$ (11V), as shown in Figure 33. When $V_{DD}$ drops below $V_{DD-OFF}$, the switching is terminated and the operating current from $V_{DD}$ is reduced to $I_{DD-OLP}$ to slow down the discharge of $V_{DD}$ until $V_{DD}$ reaches $V_{DD-OLP}$. This delays re-startup after shutdown by protection to minimize the input power and voltage/current stress of switching devices during a fault condition.

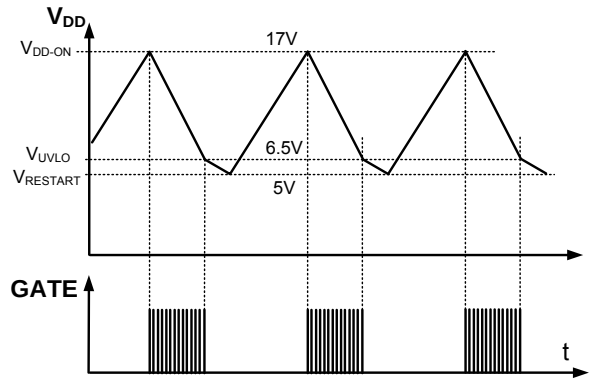


**Figure 32. $V_{DD}$ UVLO at Normal Mode**

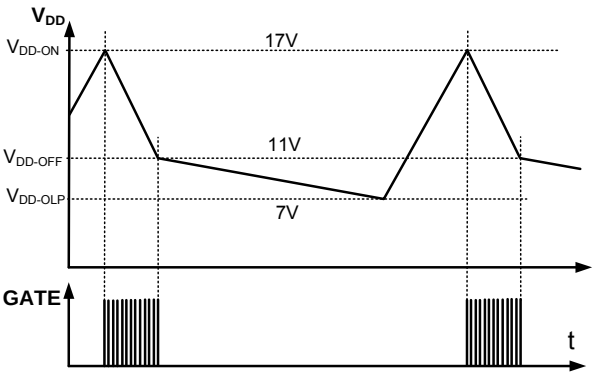


**Figure 33. $V_{DD}$ UVLO at Protection Mode**

## Gate Output / Soft Driving

The BiCMOS output stage has a fast totem-pole gate driver. The output driver is clamped by an internal 14.5V Zener diode to protect the power MOSFET gate from over voltage. A soft driving is implemented to minimize Electromagnetic Interference (EMI) by reducing the switching noise.

## Typical Application Circuit

| Application | PWM Controller | Input Voltage Range | Output |
|---|---|---|---|
| 65W Notebook Adapter | FAN6756 | $85V_{AC}$ ~ $265V_{AC}$ | 19V/3.42A |

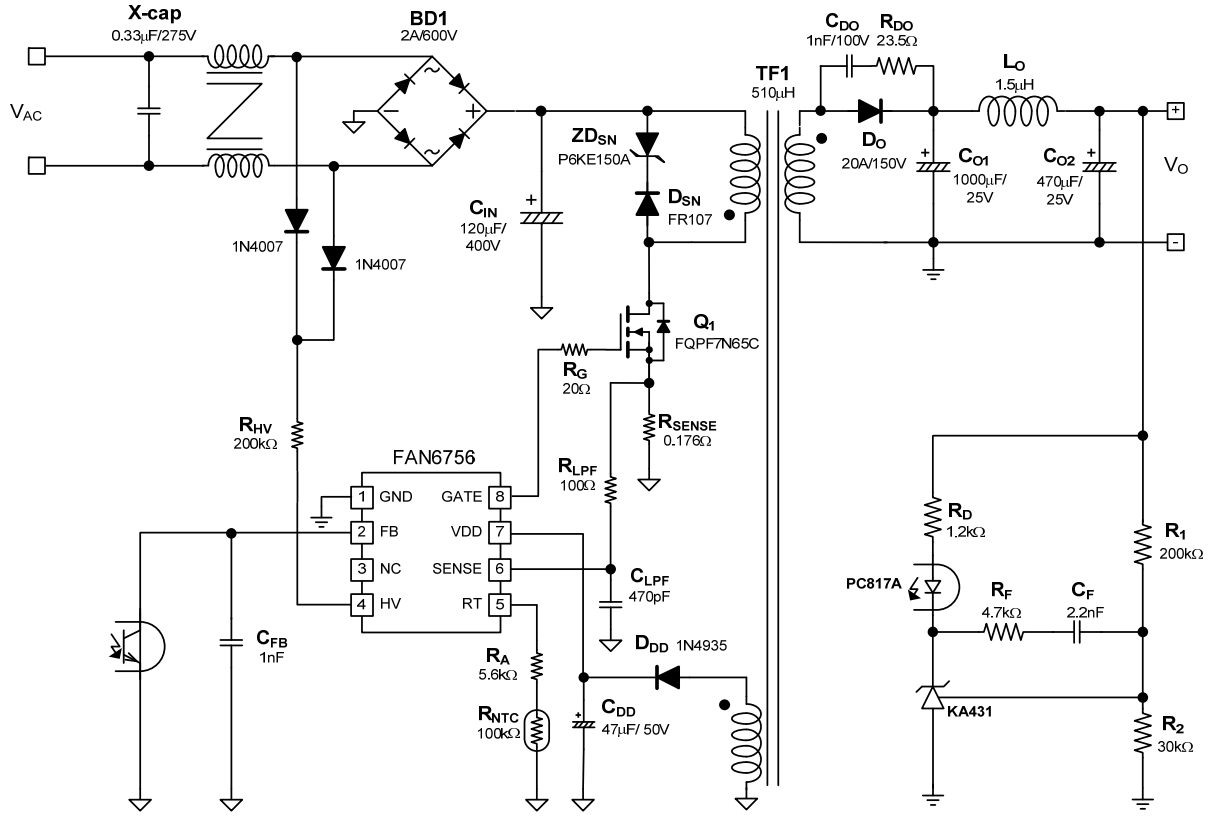


**Figure 34. Schematic of Typical Application Circuit**

## Transformer Schematic Diagram

- Core: Ferrite Core RM-10
- Bobbin: RM-10

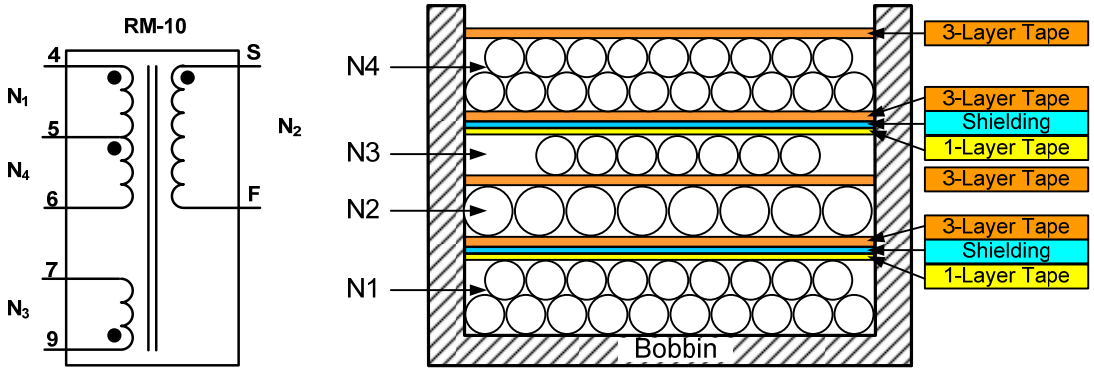


**Figure 35. Transformer Specification**

## Winding Specification

| | Pin (Start --> Finish) | Wire | Turns | Winding Method | Remark |
|---|---|---|---|---|---|
| N1 | 4 → 5 | 0.5φ×1 | 19 | Solenoid Winding | Enameled Copper Wire |
| Insulation: Polyester Tape, t = 0.025mm, 1-Layer | | | | | |
| Shielding: Adhesive Tape of Copper Foil, t = 0.025×7mm, 1.2 Layers Open Loop, Connected to Pin 4. | | | | | |
| Insulation: Polyester Tape t = 0.025mm, 3-Layer | | | | | |
| N2 | S → F | 0.9φ×1 | 8 | Solenoid Winding | Triple Insulated Wire |
| Insulation: Polyester Tape, t = 0.025mm, 3-Layer | | | | | |
| N3 | 9 → 7 | 0.4φ×1 | 7 | Solenoid Winding | Enameled Copper Wire |
| Insulation: Polyester Tape, t = 0.025mm, 1-Layer | | | | | |
| Shielding: Adhesive Tape of Copper Foil, t = 0.025×7mm, 1.2 Layers Open Loop, Connected to Pin 4. | | | | | |
| Insulation: Polyester Tape t = 0.025mm, 3-Layer | | | | | |
| N4 | 5 → 6 | 0.5φ×1 | 19 | Solenoid Winding | Enameled Copper Wire |
| Insulation: Polyester Tape t = 0.025mm, 3-Layer | | | | | |

## Electrical Characteristics

| | Pin | Specification | Remark |
|---|---|---|---|
| Primary-Side Inductance | 4 – 6 | 510μH ±5% | 1kHz, 1V |
| Primary-Side Effective Leakage Inductance | 4 – 6 | 20μH Maximum | Short All Other Pins |

## Typical Performance

### Power Consumption

| Input Voltage | Output Power | Actual Output Power | Input Power | Specification |
|---|---|---|---|---|
| $230V_{AC}$ | No Load | 0W | 0.024W | Input Power < 0.03W |
| | 0.25W | 0.232W | 0.339W | Input Power < 0.5W |
| | 0.5W | 0.495W | 0.643W | Input Power < 1W |

### Efficiency

| Output Power | 16.25W | 32.5W | 48.75W | 65W | Average |
|---|---|---|---|---|---|
| 115V/ 60Hz | 88.48% | 88.58% | 87.45% | 86.22% | 87.68% |
| 230V/ 60Hz | 88.00% | 87.89% | 87.92% | 87.47% | 87.82% |

## Physical Dimensions

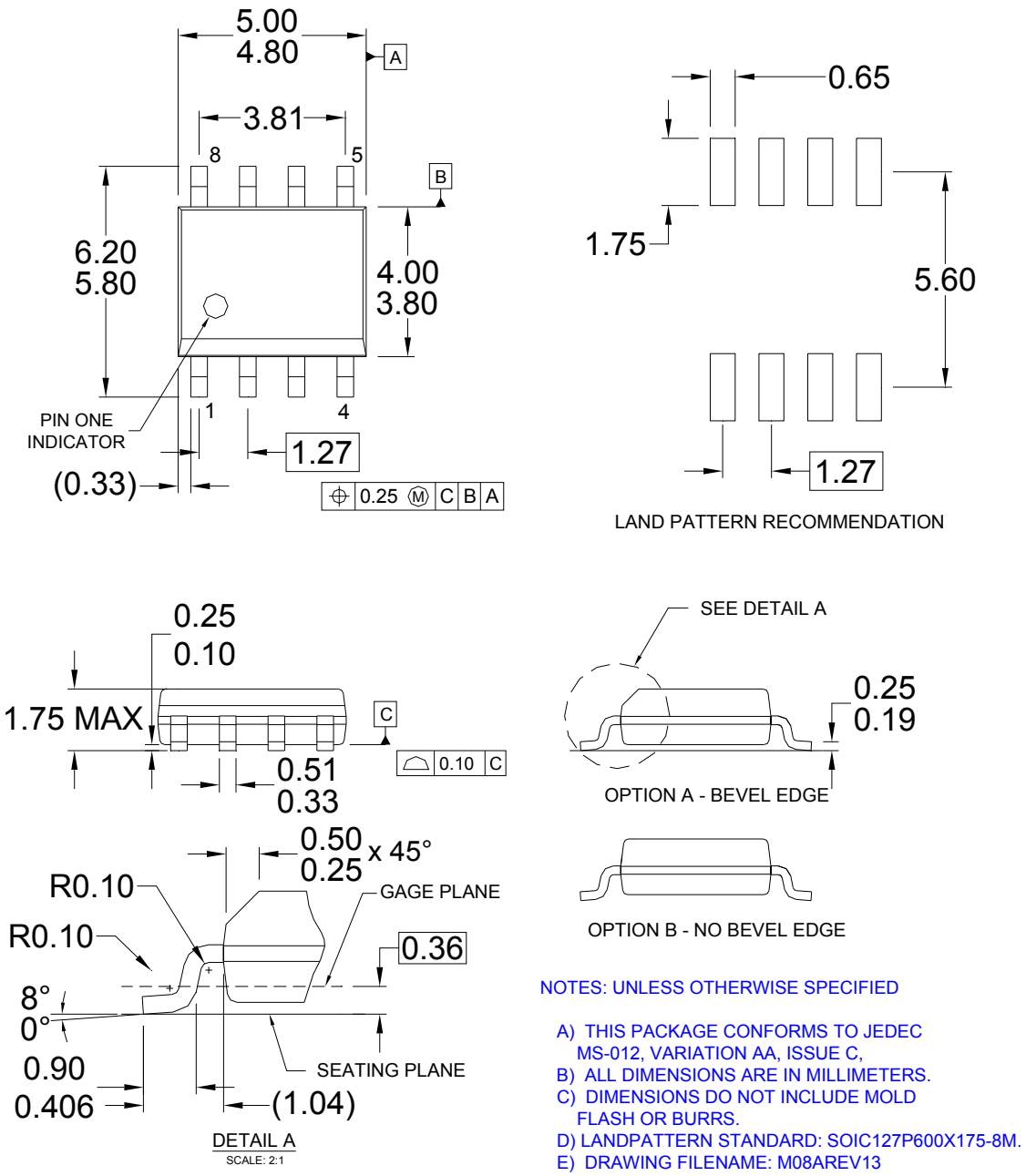


**Figure 36. 8-Pin, Small Outline Package (SOP-8)**

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DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
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Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
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MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
Motion-SPM™
mWSaver™
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OPTOPLANAR®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
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μSerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

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