

Specification for BTHQ 21603V-STF-LV-LED Y.G. with connector

Version June 2003

Supplied by:

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**Specification
of
LCD Module Type
Item No.: BTHQ 21603VSS-06**

1. General Description

- ⌘ 16 characters (5x8 dots) x 2 lines STN Positive Yellow Transflective Dot Matrix LCD module.
- ⌘ Viewing Angle: 6 O'clock direction.
- ⌘ Driving scheme: 1/16 Duty, 1/5 bias.
- ⌘ 'NOVATEK' NT3881DH-01/AI (Die form) LCD Controller and Driver or equivalent.
- ⌘ 'SAMSUNG' KS0065B-PCC (Die form) 40-Channel Segment/Common Driver for Dot Matrix LCD or equivalent.
- ⌘ Connector: 16 pins SMD "FULLCONN" connector (CON-16X1-35).
- ⌘ Yellow - Green LED01 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	53.0(W) x 20.0(H) x 8.0 MAX.(D) (Excluded connector)	mm
Effective viewing area	36.0(W) x 10.0(H)	mm
Active area	34.10(W) x 7.40(H)	mm
Display format	16 characters x 2 lines	-
Character size	1.85(W) x 3.15(H) (5 x 8 dots)	mm
Character spacing	0.30(W) x 1.10(H)	mm
Character pitch	2.15(W) x 4.25(H)	mm
Dot size	0.358(W) x 0.381(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.373(W) x 0.396(H)	mm
Weight:	Approx. 11.0	grams

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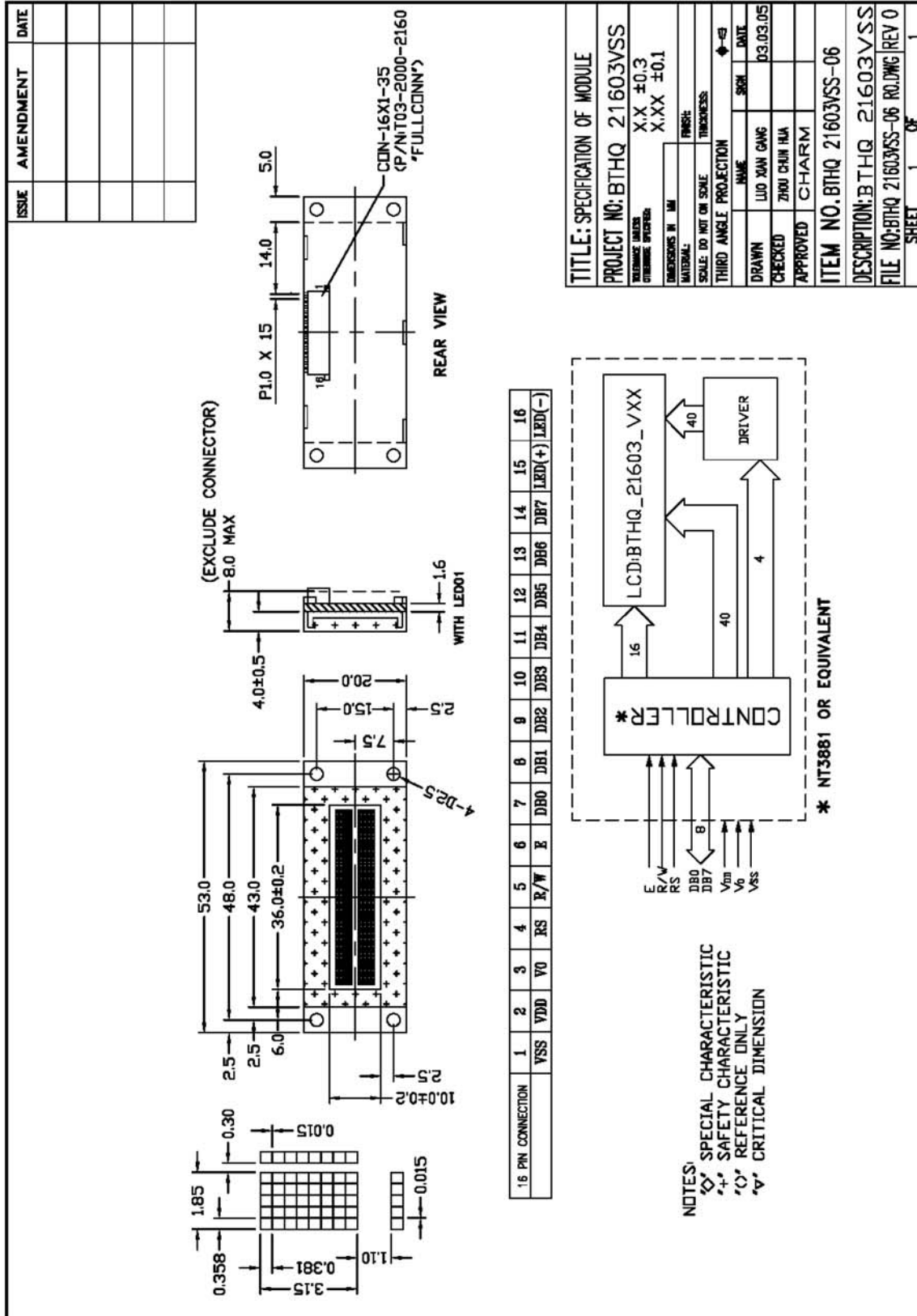


Figure 1: Outline Drawing

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3. Interface signals

Table 2

Pin No.	Symbol	Description
1	VSS	Ground (0V).
2	VDD	Power supply for logic (+5V)
3	V0	Power supply for LCD driver
4	RS	Register Select Input: “High” for Data register (for read and write) “Low” for Instruction register (for write), Busy flag, address counter (for read)
5	R/W	Read/Write signal: “High” for Read mode. “Low” for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Data input/output (LSB)
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output (MSB)
15	LED(+)	Anode of LED backlight
16	LED(-)	Cathode of LED backlight

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4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings (Ta = 25 °C)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD=VDD – V0	-0.3	+13.5	V
Input voltage	Vin	-0.3	VDD +0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s ² = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

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5. Electrical Specifications

5.1 Typical Electrical Characteristics

At $T_a = 25\text{ }^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VDD-V0	VDD=5.0V, $T_a=0\text{ }^\circ\text{C}$, Note1.	-	4.7	-	V
		VDD=5.0V, $T_a=25\text{ }^\circ\text{C}$, Note1.	4.0	4.5	5.0	V
		VDD=5.0V, $T_a=50\text{ }^\circ\text{C}$, Note1.	-	4.2	-	V
Input signal voltage 1 for E,DB0-DB7,R/W,RS.	V_{IH1}	“H” level	2.2	-	VDD	V
	V_{IL1}	“L” level	-0.3	-	0.8	V
Input signal voltage 2 for OSC1.	V_{IH2}	“H” level	VDD -1.0	-	VDD	V
	V_{IL2}	“L” level	VSS	-	1.0	V
Supply Current (Logic & LCD)	IDD	Character mode, Note 1	-	1.3	2.0	mA
		Checker board mode, Note 1	-	1.5	2.2	mA
Supply Current (LCD)	I0	Character mode, Note 1	-	0.2	0.3	mA
		Checker board mode, Note 1	-	0.2	0.3	mA
Supply voltage of yellow green LED01 backlight	VLED	Forward current =20mA Number of LED dies =2x2=4	3.9	4.0	4.1	V

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

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5.2 Timing Specifications

At $T_a = 0\text{ }^{\circ}\text{C}$ To $+50\text{ }^{\circ}\text{C}$, $V_{DD} = +5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Refer to Fig. 2, the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit	Remarks
Enable cycle time	t_{CYCE}	500	-	ns	
Enable "High" level pulse width	t_{WHE}	300	-	ns	
Enable rise time	t_{RE}	-	25	ns	
Enable fall time	t_{FE}	-	25	ns	
RS, R/W set-up time	t_{AS}	60	-	ns	8-bit operation mode
		100			4-bit operation mode
RS, R/W address hold time	t_{AH}	10	-	ns	
Data output delay	t_{DS}	100	-	ns	
Data hold time	t_{DHR}	10	-	ns	

Refer to Fig. 3, the bus timing diagram for read mode .

Table 7

Parameter	Symbol	Min.	Max.	Unit	Remarks
Enable cycle time	t_{CYCE}	500	-	ns	
Enable "High" level pulse width	t_{WHE}	300	-	ns	
Enable rise time	t_{RE}	-	25	ns	
Enable fall time	t_{FE}	-	25	ns	
RS, R/W set-up time	t_{AS}	60	-	ns	8-bit operation mode
		100			4-bit operation mode
RS, R/W address hold time	t_{AH}	10	-	ns	
Read data output delay	t_{RD}	-	190	ns	
Read data hold time	t_{DHR}	20	-	ns	

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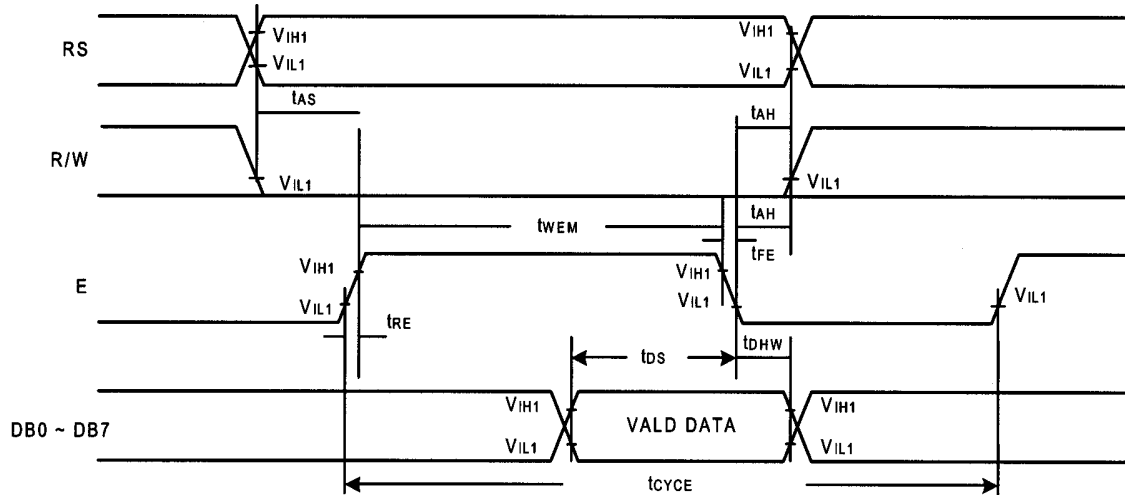


Figure 2: Bus write operation sequence (Writing data from MPU to NT3881D).

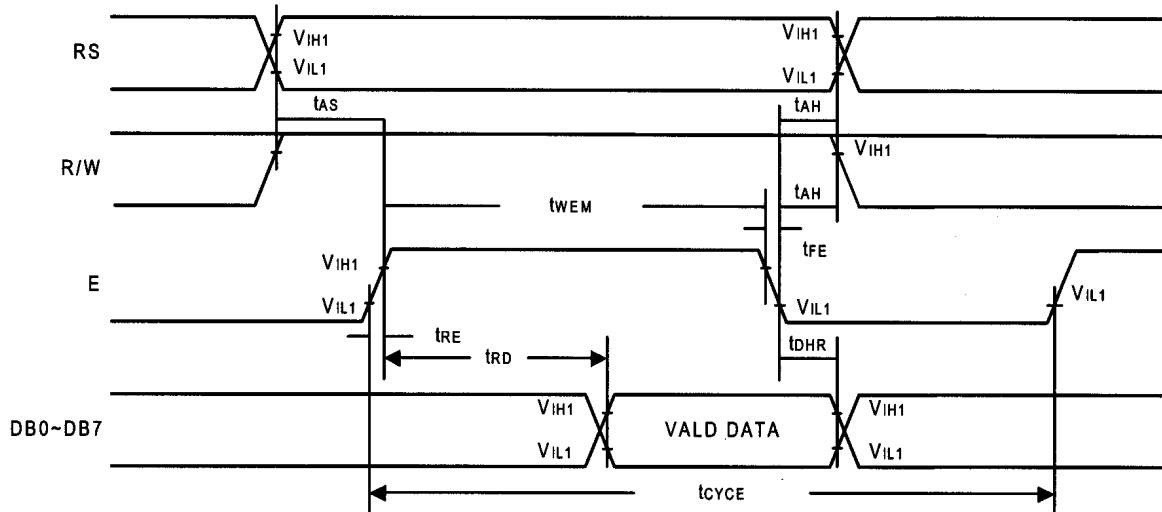


Figure 3: Bus read operation sequence (Reading out data from NT3881D to MPU).

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5.3 Timing Diagram of VDD against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

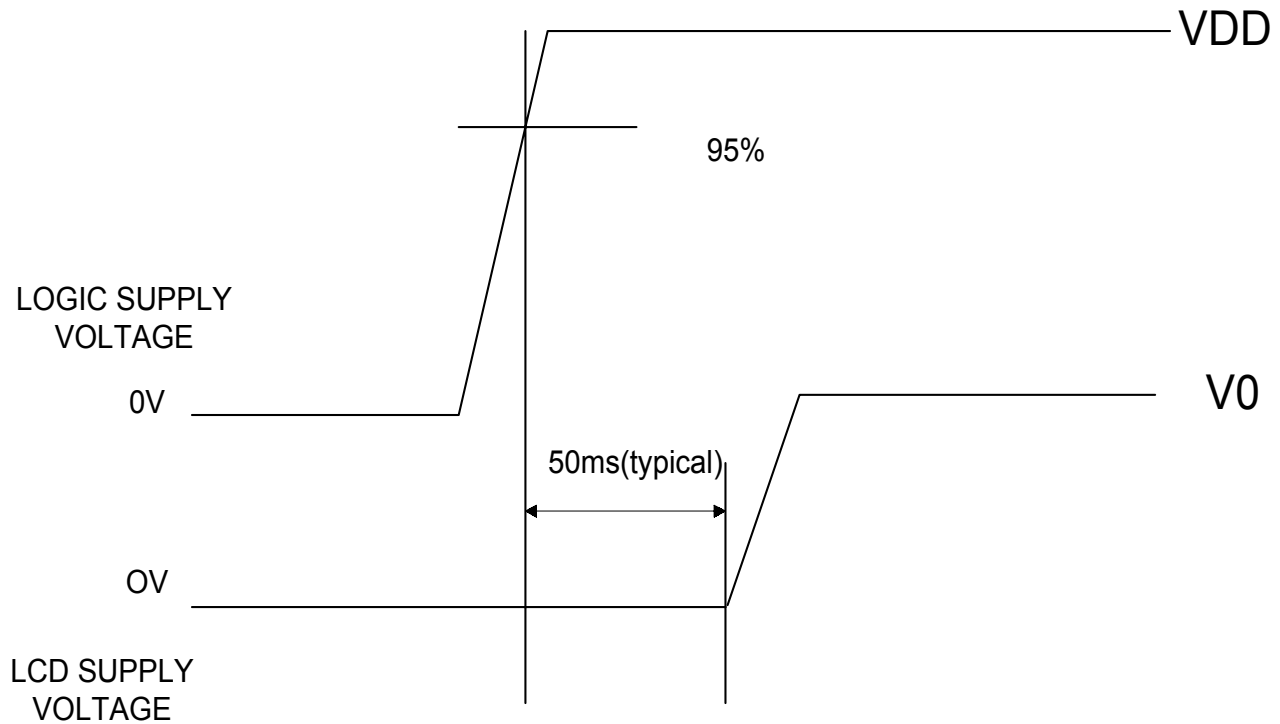


Figure 4: Timing diagram of VDD against V0.

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5.4 Correspondence between Character Codes and Character Patterns (NOVATEK Standard NT3881D-01)

		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F		
Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	0	CG RAM (1)			0	a	P	`	P					一	夕	三	α	P	
	1	CG RAM (2)		!	1	A	Q	a	9					。	ア	チ	△	ä	9
	2	CG RAM (3)		"	2	B	R	b	r					「	イ	ウ	×	β	θ
	3	CG RAM (4)		#	3	C	S	c	s					」	ウ	テ	モ	ε	ω
	4	CG RAM (5)		\$	4	D	T	d	t					、	エ	ト	ト	μ	Ω
	5	CG RAM (6)		%	5	E	U	e	u					。	オ	オ	1	ε	ü
	6	CG RAM (7)		&	6	F	V	f	v					ヲ	カ	ニ	ヨ	ρ	Σ
	7	CG RAM (8)		'	7	G	W	g	w					ア	キ	ヌ	ラ	9	π
	8	CG RAM (1)		(8	H	X	h	x					イ	ク	ネ	リ	μ	×
	9	CG RAM (2))	9	I	Y	i	y					ウ	ケ	ル	ル	´	γ
	A	CG RAM (3)		*	:	J	Z	j	z					エ	コ	ン	レ	j	〒
	B	CG RAM (4)		+	;	K	[k	[オ	サ	ヒ	ロ	*	π
	C	CG RAM (5)		,	<	L	¥	l	l					カ	シ	フ	フ	φ	π
	D	CG RAM (6)		-	=	M]	m]					ユ	ヌ	ン	ン	ト	÷
	E	CG RAM (7)		.	>	N	^	n	→					ヨ	セ	ホ	´	ñ	
	F	CG RAM (8)		/	?	O	_	o	+					ウ	リ	マ	°	ö	

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