

Specification

BTHQ12864AVE-STF-06-LED02YG-COG

Version May 2005

Supplied by:

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DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2005.05.05	<p>First Release. Based on a.) Test Specification: VL-TS-COG-BTHQ12864-05 Rev. A, 2005.05.05. b.) VL-QUA-012A REV. R, 2004.03.20.</p> <p>According to VL-QUA-012A, LCD size is small because Unit Per Laminate=14 which is more than 6pcs/Laminate.</p>	CHEN HUI JUAN	VIVIAN LUO

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**Specification
of
LCD Module Type
Model No.: COG-BTHQ12864-05**

1. General Description

- 128 x 64 dots STN Positive Yellow Transflective Dot Matrix LCD Module.
- Viewing Angle: 6 o'clock direction.
- Driving scheme: 1/65 duty, 1/7 bias.
- 'Epson' SED1565D0B (COG) Dot Matrix LCD Driver.
- 8080 Series MPU interface (default).
- 6800 Series MPU interface (Optional).
- FPC connection.
- Yellow green LED02 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	89.7(W) x 49.8(H) x 6.0(D)(Exclude FPC & gate) 89.7(W) x 149.8(H) x 6.0(D)(Include FPC. Exclude gate) 89.7(W) x 150.0(H) x 6.0(D)(Include FPC and gate)	mm
View area	66.8 MIN.(W) x 35.5 MIN. (H)	mm
Active area	63.985(W) x 31.985(H)	mm
Display format	128 (W) x 64(H)	dots
Dot size	0.485(W) x 0.485(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.500(W) x 0.500(H)	mm
Weight	56	gram

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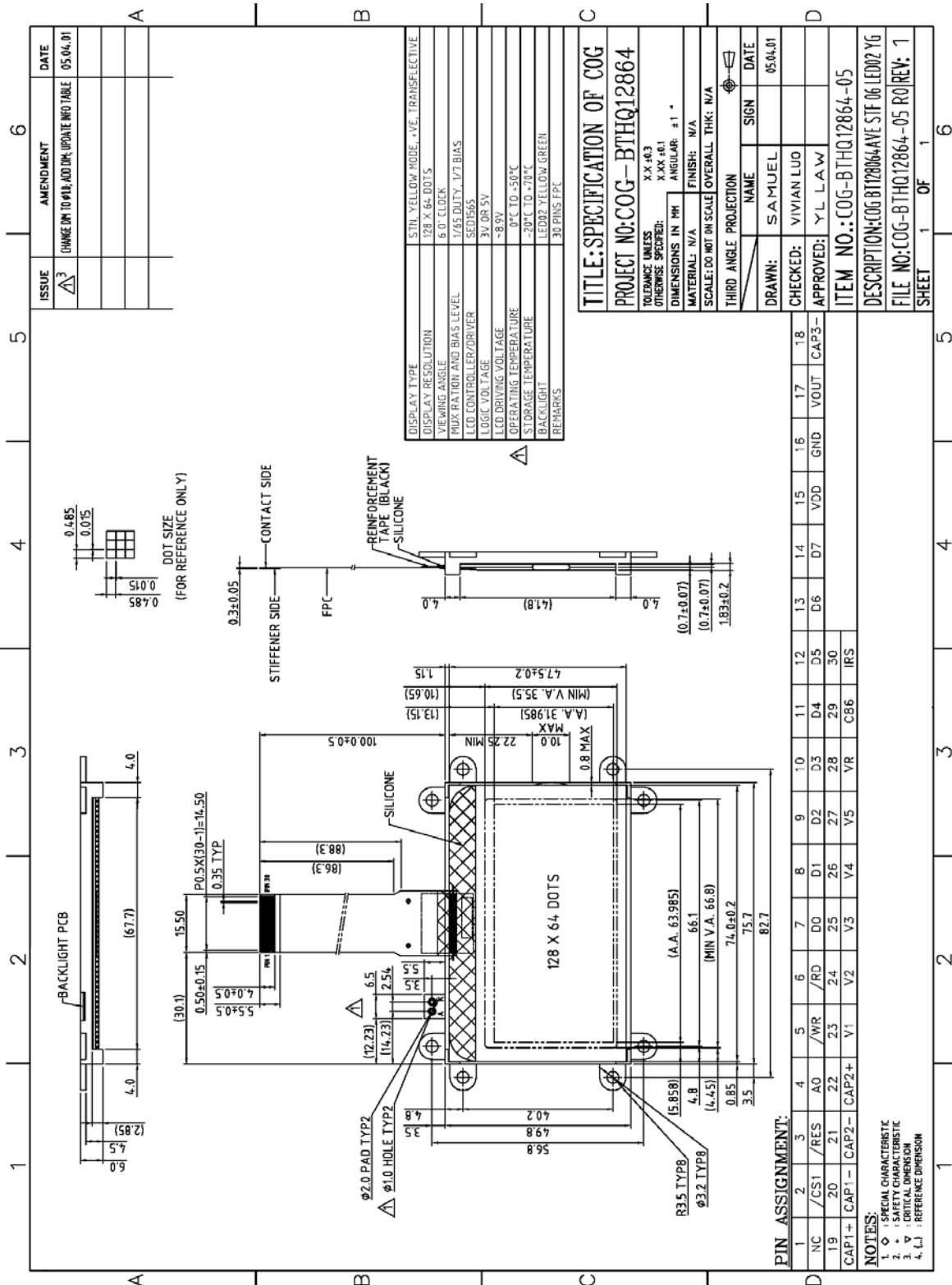


Figure 1: Module Specification

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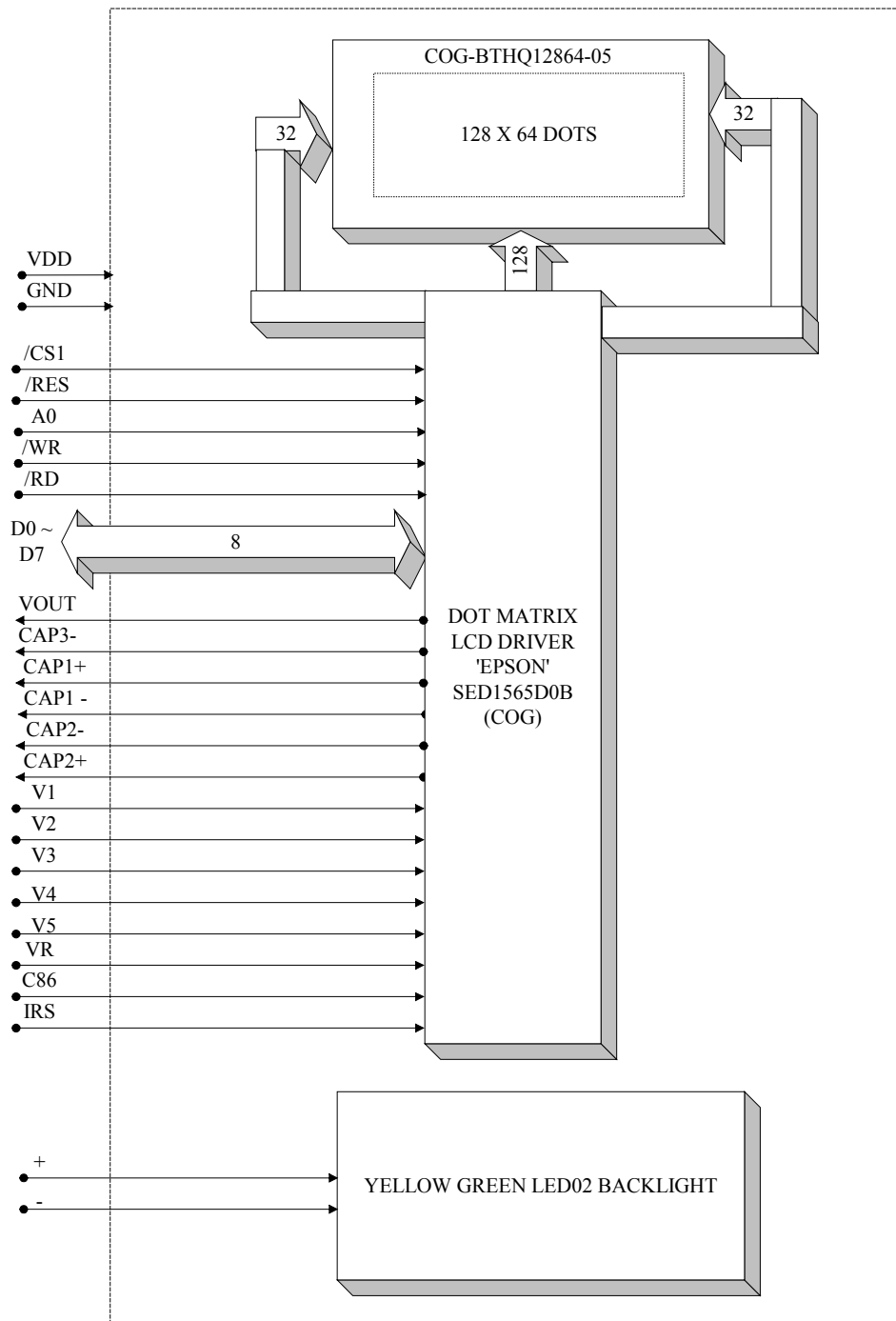


Figure 2: Block Diagram

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3. Interface signalsTable 2 (a)

Pin No.	Symbol	Description
1	NC	No connection.
2	/CS1	This is the chip select signal. When /CS1 = "L", then the chip select become active, and data/command I/O is enabled.
3	/RES	When /RES is set to "L," the settings are initialized. The reset operation is performed by the /RES signal level.
4	A0	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
5	/WR	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal.
6	/RD	When connected to an 8080 MPU, this is active LOW. This pin is connected to the /RD signal of the 8080 MPU, and the SED1565 series data bus is in an output status when this signal is "L".
7	D0	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit 8 standard MPU data bus.
8	D1	
9	D2	
10	D3	
11	D4	
12	D5	
13	D6	
14	D7	
15	VDD	Power supply. Shared with the MPU power supply terminal VCC.
16	GND	Connection with ground.
17	VOUT	DC/DC voltage converter. Connect a capacitor between this terminal and GND.
18	CAP3-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
19	CAP1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
20	CAP1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
21	CAP2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.
22	CAP2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.

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Table 2 (b)

Pin No.	Symbol	Description
23~27	V1,V2, V3,V4, V5	<p>This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divider or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below.</p> $VDD (= V0) \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ <p>Master operation: When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.</p> <p>For 1/7 bias: $V1=(1/7) \times V5$, $V2=(2/7) \times V5$, $V3=(5/7) \times V5$, $V4=(6/7) \times V5$.</p>
28	VR	<p>Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divider.</p> <p>These are only enabled when the V5 voltage regulator internal resistors are not used (IRS = "L").</p> <p>These cannot be used when the V5 voltage regulator internal resistors are used (IRS = "H").</p>
29	C86	<p>This is the MPU interface switch terminal.</p> <p>C86 = "H": 6800 Series MPU interface.</p> <p>C86 = "L": 8080 MPU interface.</p>
30	IRS	<p>This terminal selects the resistors for the V5 voltage level adjustment.</p> <p>IRS = "H": Use the internal resistors</p> <p>IRS = "L": Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.</p> <p>This pin is enabled only when the master operation mode is selected.</p> <p>It is fixed to either "H" or "L" when the slave operation mode is selected.</p>
	+	Anode of backlight.
	-	Cathode of backlight.

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4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – for IC Only

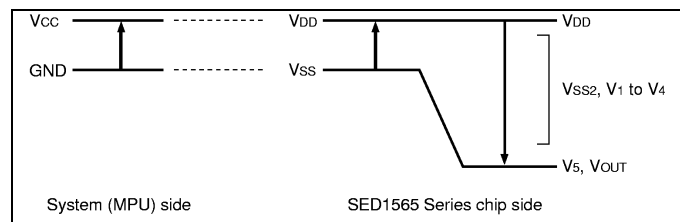
Table 3

Parameter	Symbol	Min.	Max.	Unit	
Power Supply voltage (Logic)	VDD-GND =VDD-VSS	-0.3	+7.0	V	
Power supply voltage (VDD standard)	GND(=VSS2)	-7.0	+0.3	V	
		With Triple set-up	-6.0	+0.3	V
		With Quad step-up	-4.5	+0.3	V
Power Supply voltage(V5,VOUT) (VDD standard)	V5,VOUT	-18.0	+0.3	V	
Power Supply voltage(V1~V4) (VDD standard)	V1,V2,V3,V4	V5	+0.3	V	
Input voltage	Vin	-0.3	VDD+0.3	V	

Note: 1.) The module may be destroyed if they are used beyond the absolute maximum ratings.

2.) Insure that the voltage levels of V1, V2, V3, and V4 are always such that
 $VDD \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$.

3.) The VSS2, V1 to V5 and VOUT are relative to VDD=0V reference.



4.2 Environmental Conditions

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-20°C	+70°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s ² = 100 g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

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5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, GND =0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-GND		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VDD-V5	VDD=5.0V, Ta=0°C Note (1)	8.65	8.87	9.1	V
		VDD=5.0V, Ta=25°C Note (1)	8.5	8.75	9.0	V
		VDD=5.0V, Ta=50°C Note (1)	8.43	8.65	8.87	V
Low-level input signal voltage	V _{ILC}		GND	-	0.2xVDD	V
High-level input signal voltage	V _{IHC}		0.8xVDD	-	VDD	V
Supply Current (Logic & LCD)	IDD	VDD = 5V, Character mode	-	0.5	0.75	mA
		VDD = 5V, Checker board mode	-	1.0	1.5	mA
Supply voltage of yellow-green LED02 backlight	VLED	Forward current =60mA Number of LED dies =2x6=12	4.5	4.75	4.85	V
Wavelength of Yellow-Green LED02 backlight	λ		570	572	576	nm

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

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5.2 Timing Specifications

Reset Timing

At $T_a = 0\text{ }^\circ\text{C}$ to $+50\text{ }^\circ\text{C}$, $V_{DD} = +5.0\text{V} \pm 5\%$, $GND = 0\text{V}$.

Table 6

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
Reset time		t_R		—	—	0.5	μs
Reset "L" pulse width	RES	t_{RW}		0.5	—	—	μs

Note: All timing is specified with 20% and 80% of VDD as the standard.

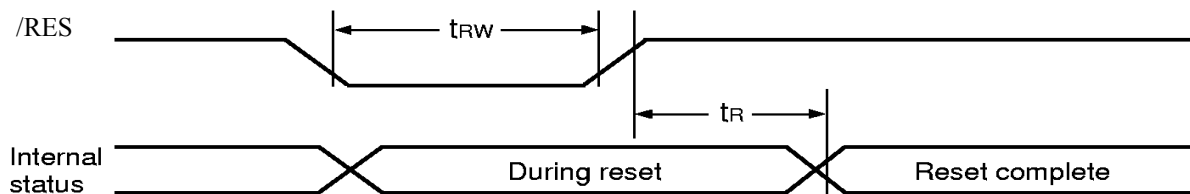


Figure 3:Reset Timing

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System Bus Read/Write Characteristics (8080 Series MPU)

At $T_a = 0\text{ }^\circ\text{C}$ to $+50\text{ }^\circ\text{C}$, $V_{DD} = +5.0\text{V} \pm 5\%$, $GND = 0\text{V}$.

Table 7

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t _{AH8}		0	—	ns
Address setup time	A0	t _{AW8}		0	—	ns
System cycle time	A0	t _{CYC8}		166	—	ns
Control L pulse width (\overline{WR})	\overline{WR}	t _{CCLW}		30	—	ns
Control L pulse width (\overline{RD})	\overline{RD}	t _{CCLR}		70	—	ns
Control H pulse width (\overline{WR})	\overline{WR}	t _{CCHW}		30	—	ns
Control H pulse width (\overline{RD})	\overline{RD}	t _{CCHR}		30	—	ns
Data setup time	D0 to D7	t _{DS8}		30	—	ns
Address hold time		t _{DH8}		10	—	ns
\overline{RD} access time		t _{ACC8}	CL = 100 pF	—	70	ns
Output disable time		t _{OH8}		5	50	ns

- *1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ for $(t_r + t_f) \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$ are specified.
- *2 All timing is specified using 20% and 80% of V_{DD} as the reference.
- *3 t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being "L" ($CS2 = "H"$) and \overline{WR} and \overline{RD} being at the "L" level.

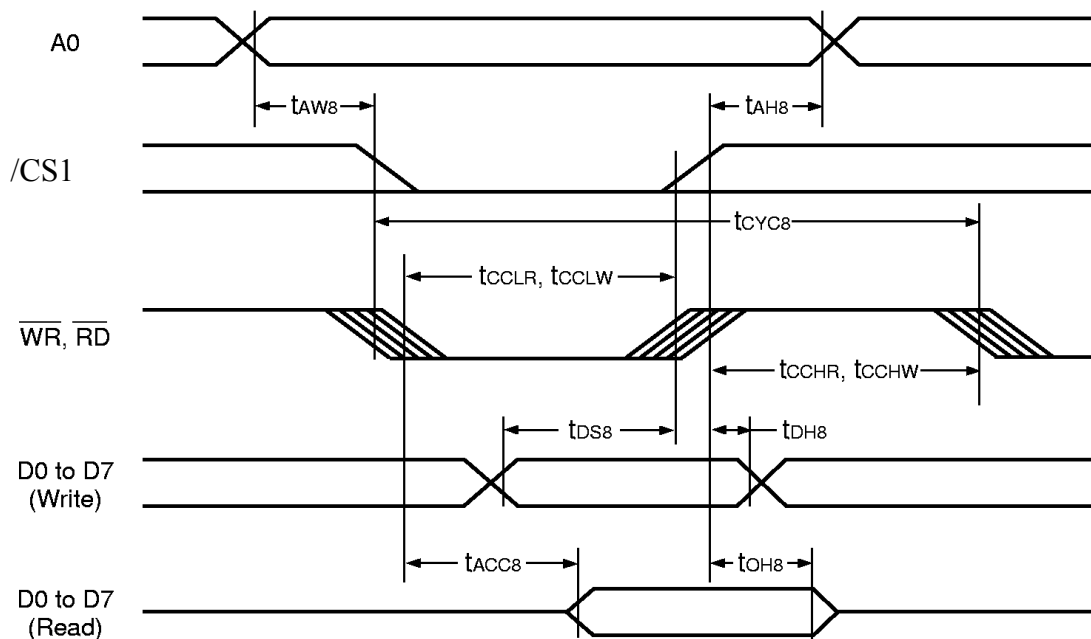


Figure 4: MPU bus read / write timing diagram (80 family MPU)

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System Bus Read/Write Characteristics (6800 Series MPU)

At $T_a = 0\text{ }^\circ\text{C}$ to $+50\text{ }^\circ\text{C}$, $V_{DD} = +5.0\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Table 8

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time	A0	t_{AW6}		0	—	ns
System cycle time	A0	t_{CYC6}		166	—	ns
Data setup time	D0 to D7	t_{DS6}		30	—	ns
Data hold time		t_{DH6}		10	—	ns
Access time		t_{ACC6}	CL = 100 pF	—	70	ns
Output disable time		t_{OH6}		10	50	ns
Enable H pulse time	Read	E	t_{EWHR}	70	—	ns
	Write		t_{EWHW}	30	—	ns
Enable L pulse time	Read	E	t_{EWLR}	30	—	ns
	Write		t_{EWLW}	30	—	ns

- *1 The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ for $(t_r + t_f) \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$ are specified.
- *2 All timing is specified using 20% and 80% of V_{DD} as the reference.
- *3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being "L" ($CS2 = "H"$) and E.

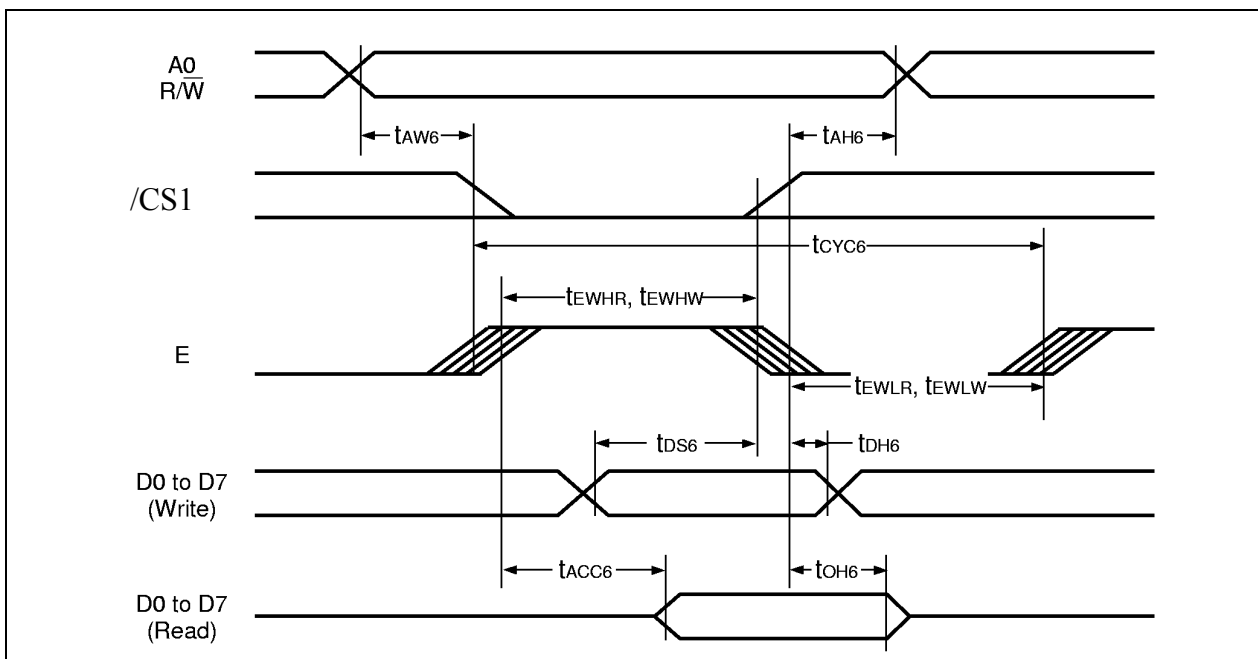


Figure 5: MPU bus read / write timing diagram (68 family MPU)

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5.3 Instruction Set

Table 9

Command	Command Code											Function	
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0		
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address	
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address	
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.	
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.	
(5) Status read	0	0	1	Status				0	0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM	
(7) Display data read	1	0	1	Read data								Reads from the display RAM	
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0	1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0	1	Sets the LCD display normal/reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0	1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0	1	Sets the LCD drive voltage bias ratio SED1565*** 0: 1/9, 1: 1/7 SED1566*** /SED1568*** /SED1569*** 0: 1/8, 1: 1/6 SED1567** 0: 1/6, 1: 1/5
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0	*	*	*	*	Select COM output scan direction 0: normal direction, 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode	
(17) V5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode	
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	0	1	Set the V5 output voltage electronic volume register
Electronic volume register set	0	1	0	*	*	Electronic volume value							
(19) Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0	1	0: OFF, 1: ON
Static indicator register set	0	1	0	*	*	*	*	*	*	Mode			Set the flashing mode
(20) Power saver													Display OFF and display all points ON compound command
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	1	Command for non-operation
(22) Test	0	1	0	1	1	1	1	*	*	*	*	*	Command for IC test. Do not use this command

(Note) *: disabled data

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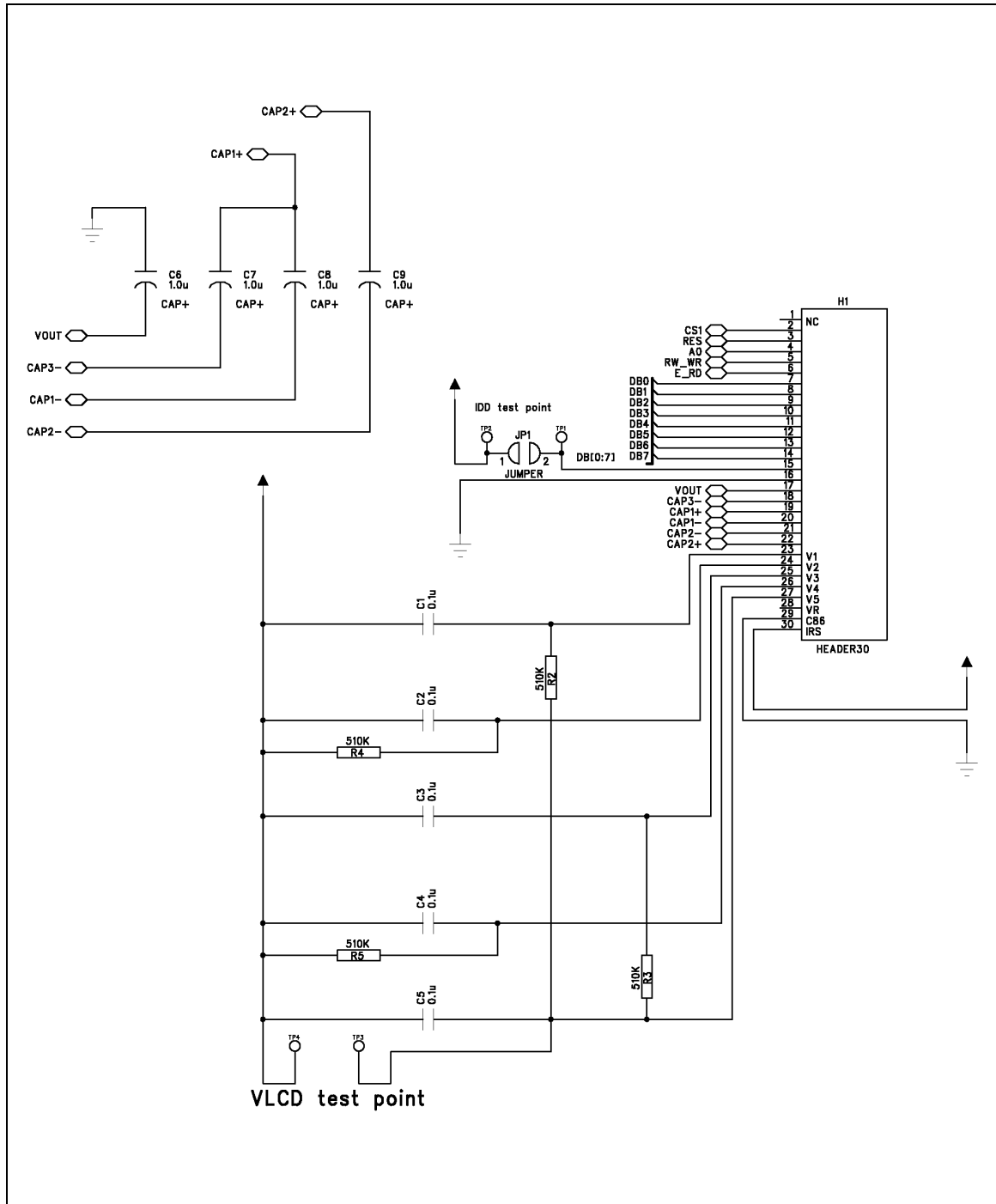
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6. Reference Application Circuit (8080) Example

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