

Specification

BTHQ 128064AVO-FETF-06-LEDWHITE02-COG (NT7538)

Version June 2008

Supplied by: Midas Components Limited, Electra House, 32 Southtown Road, Great Yarmouth, Norfolk, NR31 0DU



RECORDS OF REVISION

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1. SPECIFICATIONS

1.1 Features

Item	Standard Value
Display Type	128 * 64 Dots
LCD Type	FSTN, Positive, Transflective type
Driver Condition	LCD Module : 1/65 Duty , 1/9 Bias
Viewing Direction	6 O'clock
Backlight	White LED B/L
Weight	32g
Interface	8- bit parallel data input / Serial data input
Other(controller / driver IC)	NOVATEK NT7538
ROHS	THIS PRODUCT CONFORMS THE ROHS OF PTC

1.2 Mechanical Specifications

Item	Standard Value			
Outline Dimension	89.7 (L) * 49.8 (w) * 6.3 (H)(Max)	mm		
Viewing Area	69.0 (L) *36.5 (w)	mm		
Active Area	63.857 (L) * 31.921 (w)	mm		
Dot Size	0.484(L) * 0.484 (w)	mm		
Dot Pitch	0.499 (L) * 0.499 (w)	mm		

Note: For detailed information please refer to LCM drawing

1.3 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit				
Power Supply Voltage	V_{dd}	_	-0.3	4.0	V				
LCD Driver Supply Voltage	V _{LCD}	—	0.3	15.0	V				
Input Voltage	V _{IN}	—	-0.3	VDD+0.3	V				
Operating Temperature	T _{OP}	_	-20	70	°C				
Storage Temperature	T _{ST}	—	-30	80	°C				
Storage Humidity	H _D	Ta<60 °C	-	90	%RH				

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1.4 DC Electrical Characteristics

					Ta = 2	25℃
Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Logic Supply Voltage	V_{dd}	-	2.7	3.0	3.3	V
"H" Input Voltage	\mathbf{V}_{IH}	-	0.8VDD	-	VDD	V
"L" Input Voltage	V_{IL}	-	VSS	-	0.2VDD	V
"H" Output Voltage	V _{OH}	IOH=-0.5 mA	0.8VDD	-	VDD	V
"L" Output Voltage	V _{OL}	IOL=0.5 mA	VSS	-	0.2VDD	V
Summ by Common t	T	VDD= 3.0V;VOP=9.0V; Pattern= Full display	-	0.6	-	
Supply Current	I _{dd}	V _{DD} = 3.0V;V _{OP} =9.0V; Pattern= Horizontal line*1	-	2.0	3.0	mA
	V _{OP}	-20°C				
LCM Driver Voltage		25°C	13.0	13.2	13.4	V
	*2	70°C				

NOTE: *1 The Maximum current display

*2 The VOP test point is V1-VSS.



1.5 Optical Characteristics

			LC	CD Panel:1	/65Duty,1/9	Bias,V _{LCD}	=13.2V,	Ta =25°C
Item		Symbol	Conditions	Min.	Тур.	Max.	Unit	Reference
Response Time	Rise	tr		-	70	105	ma	Note2
Response Time	Fall	tf		-	210	315	ms	Note2
	Тор	ΘY^+	C <u>></u> 2.0,	-	-	40		
Viewing angle	Bottom	ΘY-	$\varnothing = 270^{\circ}$	-	-	40	Deg.	Notes 1
range	Left	ΘΧ-		-	-	45		
	Right	ΘX+		-	-	45		
Contrast Rat	io	С	$\theta = 0^{\circ},$ $\emptyset = 270^{\circ}$	11	-	-		Note 3
Average Bright (with LCD)		IV	IF=60mA	80	100	-	cd/m ²	
CIE Color Coor	CIE Color Coordinate		VF=3.5V	0.27	0.30	0.33		Note 4
(With LCD)	*1	Y		0.29	0.32	0.35		Note 4
Uniformity '	*2	∆B		70	-	-	%	

Note 4 :

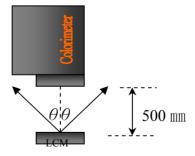
1 : △B=B(min) / B(max) * 100%

2 : Measurement Condition for Optical Characteristics:

a : Environment: $25^{\circ}C \pm 5^{\circ}C / 60\pm 20\%$ R.H , no wind , dark room below 10 Lux at typical lamp current and typical operating frequency.

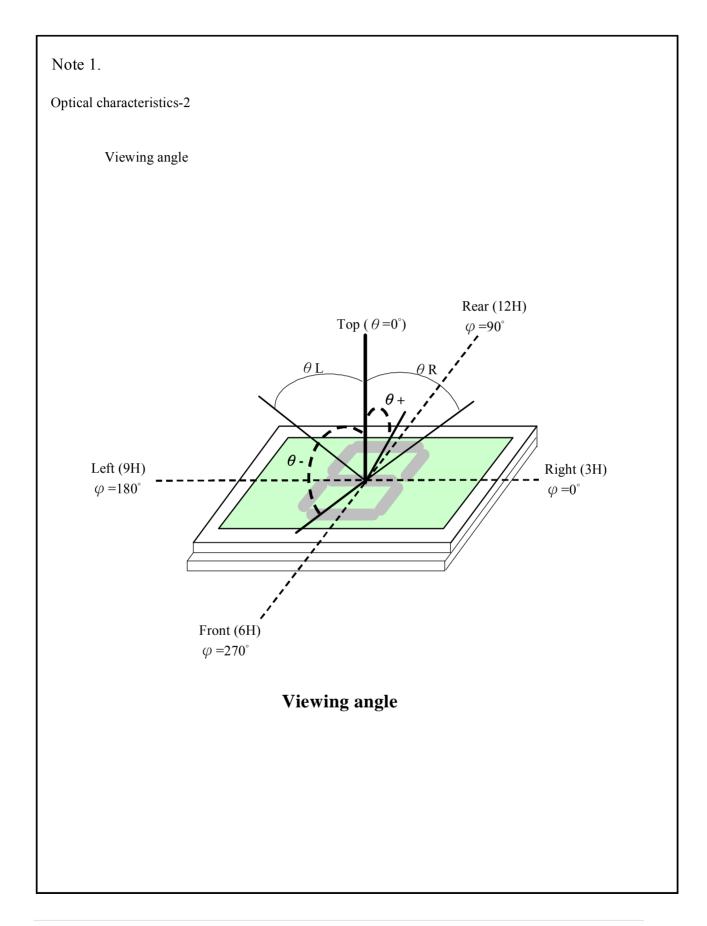
- b : Measurement Distance: $500 \pm 50 \text{ mm}$, ($\theta = 0^{\circ}$)
- c: Equipment: TOPCON BM-7 fast, (field 1°), after 10 minutes operation.
- d : The uncertainty of the C.I.E coordinate measurement ± 0.01 , Average Brightness $\pm 4\%$



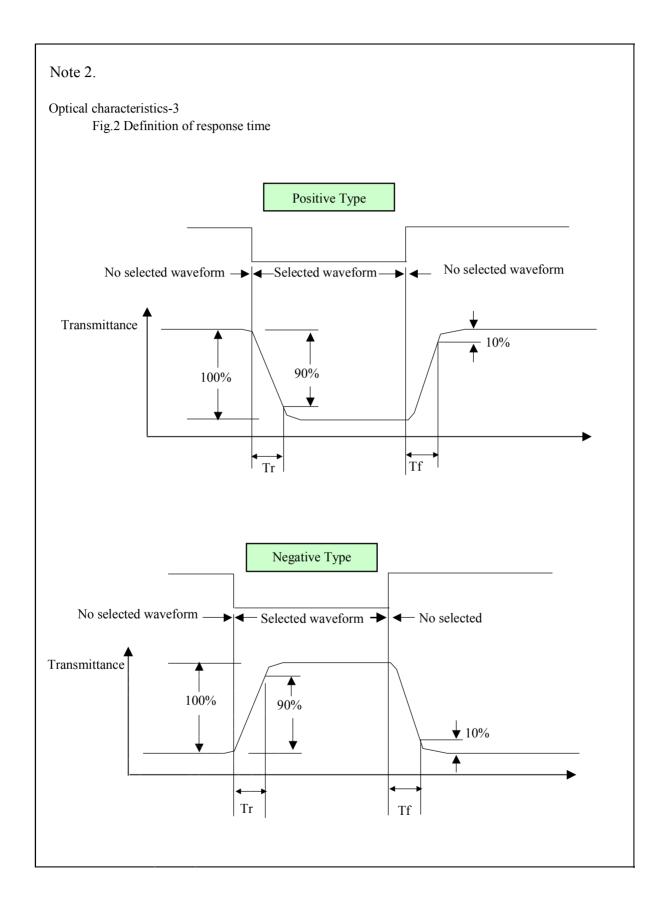


Colorimeter=BM-7 fast

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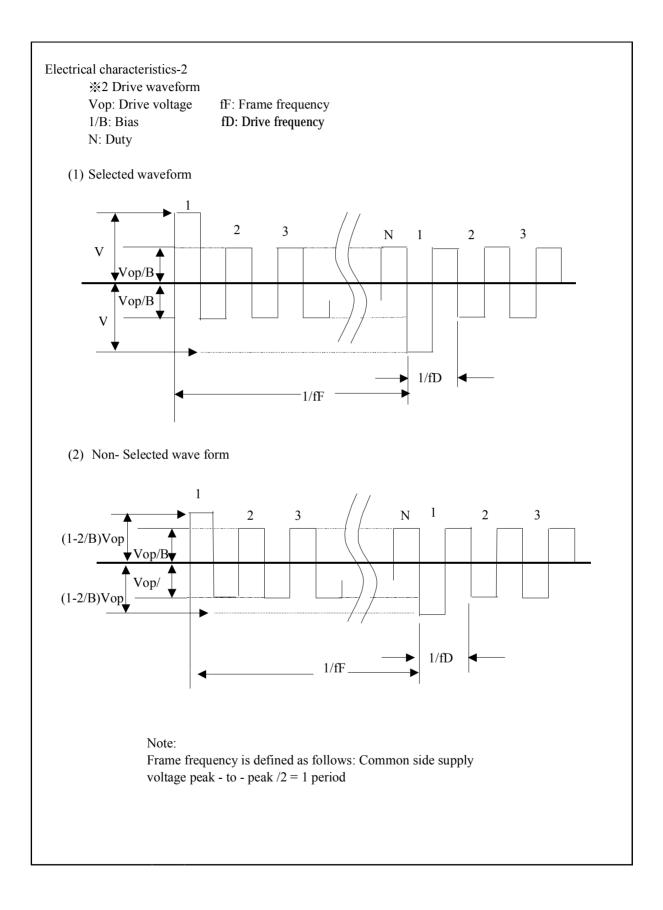


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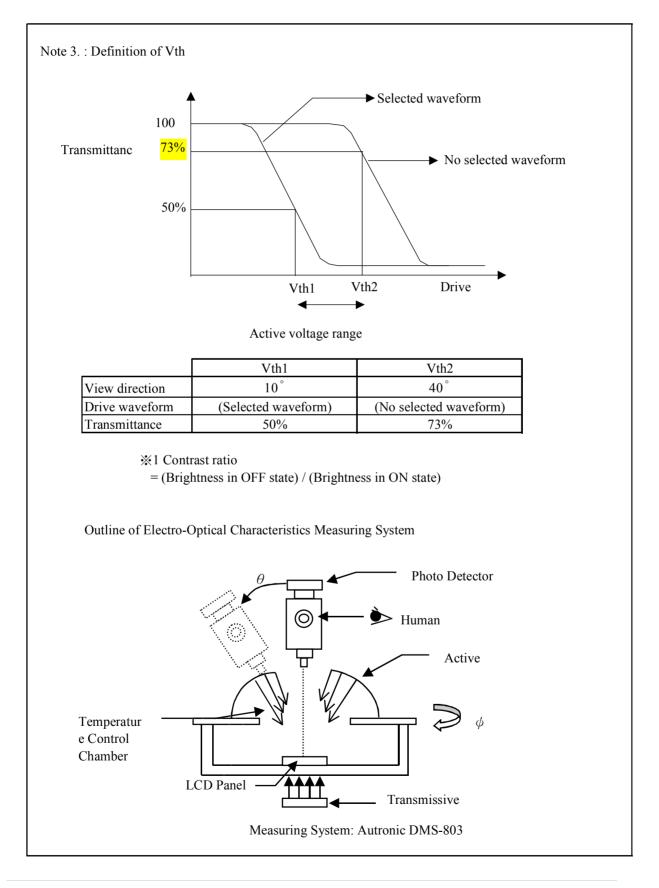
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1.6 Backlight Characteristics

LCD Module with LED Backlight

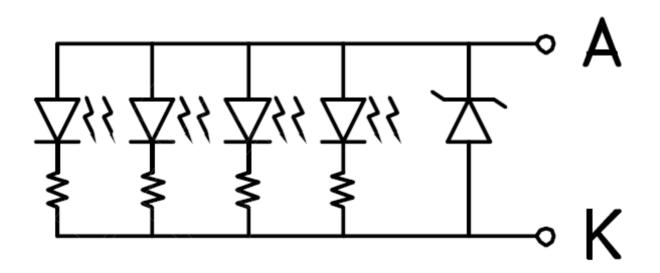
Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward Current	IF	Ta =25℃	-	100	mA
Reverse Voltage	VR	Ta =25℃	-	1.0	V
Power Dissipation	PD	Ta =25℃	-	300	W

Electrical / Optical Characteristics

Item	Symbol	Conditions	Min.	Тур.	Max.	Unit
Forward Voltage	VF		-	3.5	3.8	V
Average Brightness (without LCD)	IV	IV IF=60mA		250	-	cd/m ²
CIE Color Coordinate	Х		0.25	0.28	0.31	
(Without LCD)	Y		0.25	0.28	0.31	-
Color		·	White			

Internal Circuit Diagram:





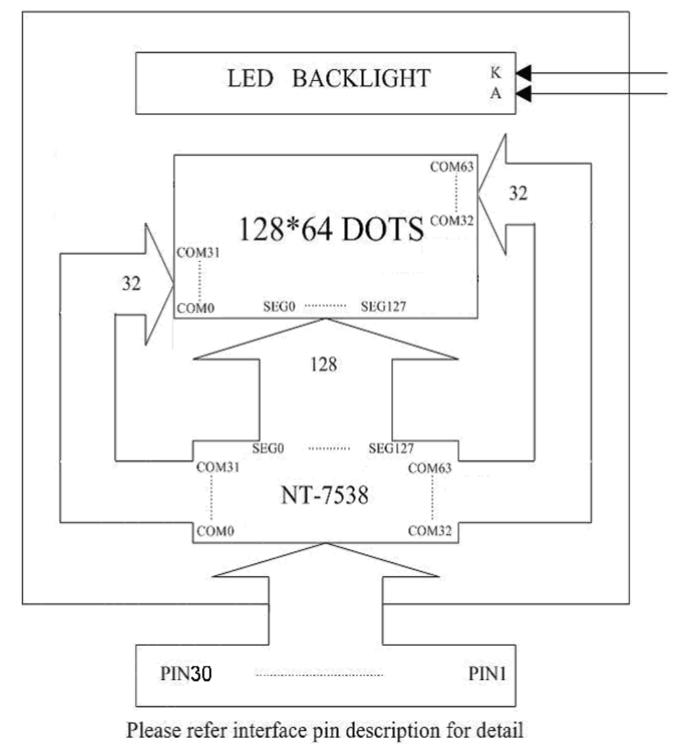
2. MODULE STRUCTURE

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram

* See Appendix

2.1.2 Block Diagram



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2.2 Interface Pin Description

1	CS1	This is the chip select signal. When /CS1="L" and CS2="H",
	_	then the chip select becomes active, and data/command I/O is enabled.
2	RES	When /RES is set to "L", the settings are initialized. The reset
		operation is performed by the /RES signal level
		This is connected to the least significant bit of the normal MPU
3	A0	address bus, and it determines whether the data bits are data or a command.
		A0 = "H": Indicate that D0 to D7 are display data
		A0 = "L": Indicates that D0 to D7 are control data
		When connected to an 8080 MPU, this is active LOW. This
		terminal connects to the 8080 MPU /WR signal. The signals
		on the data bus are latched at the rising edge of the /WR signal.
4	WR	When connected to a 6800 Series MPU, this is the read/write
		control signal input terminal.
		When R/W = "H": Read
		When R/W = "L": Write
	RD	When connected to an 8080 MPU, it is active LOW. This pad
		is connected to the /RD signal of the 8080MPU, and the
5		NT7538 data bus is in an output status when this signal is "L".
		When connected to a 6800 Series MPU, this is active HIGH.
		This is used as an enable clock input of the 6800 series MPU
6	D0	
7	D1	This is an 8-bit bi-directional data bus that connects to an 8-bit
8	D2	or 16-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then D7
9	D3	serves as the serial data input terminal (SI) and D6 serves as
10	D4	the serial clock input terminal (SCL). When the serial interface
11	D5	is selected, fix D0~D5 pads to VDD or VSS level.
12	D6	When the chip select is inactive, D0 to D7 are set to high
13	D7	impedance.
14	VDD	Power Supply (VDD=3.3)
15	VSS	Power Supply (VSS=0)
16	VOUT	DC/DC voltage converter output
17	C3+	Capacitor 3+ pad for internal DC/DC voltage converter.
18	C1+	Capacitor 1+ pad for internal DC/DC voltage converter.
19	C1-	Capacitor 1- pad for internal DC/DC voltage converter.
L	1	Supplied by: 13

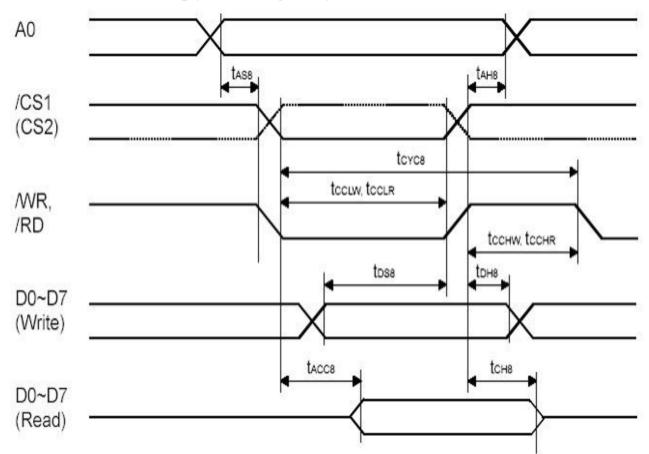


20	C2-	Capacitor 2- pad for internal DC/DC voltage converter.							
21	C2+	Capacitor 2+ pad for internal DC/DC voltage converter.							
22	V1	LCD driver supplies voltages. The voltage determined by the							
23	V2	LCD cell is impedance-converted by a resistive driver or an							
24	V3	operation amplifier for application. Voltages should be according to the following relationship:							
25	V4	$V1 \ge V2 \ge V3 \ge V4 \ge V5 \ge VSS2$							
26	V5	When the on-chip operating power circuit is on, the following voltages are supplied to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the LCD Bias Set command.							
27	VR	Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.							
28	C86	This is the MPU interface switch terminal C86 = "H": 6800 Series MPU interface C86 = "L": 8080 Series MPU interface							
29	P/S	C86 = "L": 8080 Series MPU interface This is the parallel data input/serial data input switch terminal P/S = "H": Parallel data input P/S = "L": Serial data input The following applies depending on the P/S status: P/S Data/Command Data Read/Write Serial Clock "H" A0 D0 to D7 /RD, /WR "L" A0							
30	C4+	Capacitor 4+ pad for internal DC/DC voltage converter.							



2.3 Timing Characteristics

System Bus Read/Write Timing (8080 Family MPU)

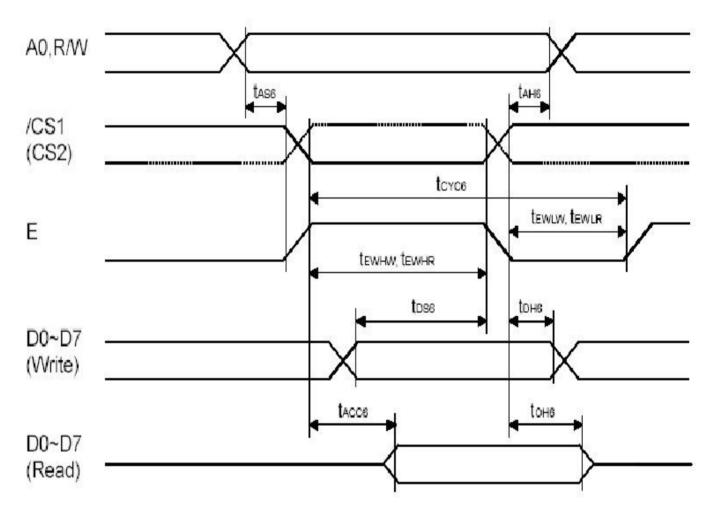


		(VDD = 3.0 ~ 3.6V, Ta = -20 ~					
Item	Signal	Symbol	Condition	Rating		Units	
				Min.	Max.		
Address hold time	A0	t _{AH8}		0	-		
Address setup time		t _{AS8}		0	-		
System cycle time		t _{CYC8}		240	-		
Enable L pulse width (WRITE)	WR	t _{CCLW}		90	-		
Enable H pulse width (WRITE)		t _{CCHW}		100	-		
Enable L pulse width (READ)	RD	t _{CCLR}		120	-	ns	
Enable H pulse width (READ)		t _{CCHR}		60			
Data setup time	D0	t _{DS8}		40	-		
Data hold time	to	t _{DH8}		0	-		
/RD access time	D7	t _{ACC8}	C _L =100pF	-	140		
Output disable time		t _{OH8}	C _L =100pF	5	50		

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System Bus Read/Write Timing (6800 Family MPU)



(VDD = 3.0 ~ 3.6V, Ta = -20 ~ 70° C)

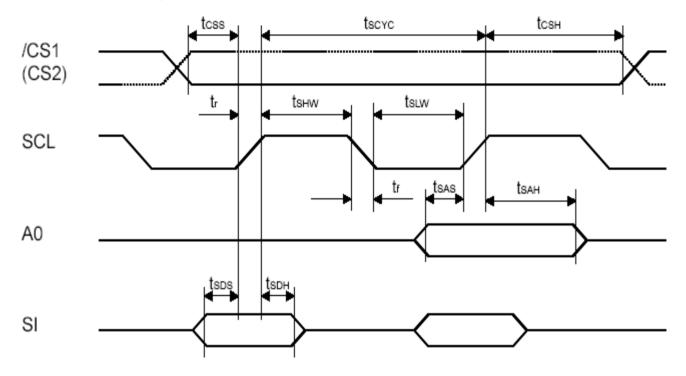
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0,RW	t _{AH6}		0	-	
Address setup time		t _{AS6}		0	-	
System cycle time		t _{CYC6}		240	-	
Enable L pulse width (WRITE)	E	T _{EWHW}		90	-	
Enable H pulse width (WRITE)		T _{EWHW}		100	-	
Enable L pulse width (READ)	Е	T _{EWHR}		120	-	ns
Enable H pulse width (READ)		T _{EWHR}		60		
Data setup time	D0	t _{DS6}		40	-	
Data hold time	to	t _{DH6}		0	-	
/RD access time	D7	t _{ACC6}	C _L =100pF	-	140	
Output disable time		t _{OH6}	C _L =100pF	5	50	

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Serial Interface Timing



 $(VDD = 3.0 \sim 3.6V, Ta = -20 \sim 70^{\circ} C)$

Symbol	Parameter	Min	Тур	Max	Unit	Condition
tscyc	Serial clock cycle	120	-	-	ns	SCL
tshw	Serial clock H pulse width	60	-	-	ns	SCL
tslw	Serial clock L pulse width	60	-	-	ns	SCL
tsas	Address setup time	30	-	-	ns	A0
tsaf	Address hold time	20	-	-	ns	A0
tsds	Data setup time	30	-	-	ns	SI
t sdh	Data hold time	20	-	-	ns	SI
tcss	Chip Serial setup time	20	-	-	ns	/CS1,CS2
tсsн	Chip Serial hold time	40	-	-	ns	/CS1,CS2

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2.4 Display command

Command	A0	/RD	/WR	Code			Function												
Command	AU	/RD	WWR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function						
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1		Turn on LCD panel when high, and turn off when low						
(2) Display Start Line Set	0	1	0	0	1		Disp	lay Sta	art Ad	dress		40h to 7Fh	Specifies RAM display line for COM0						
(3) Page Address Set	0	1	0	1	0	1	1	F	Page A	\ddres	s	B0h to B8h	Set the display data RAM page in Page Address register						
(4) Column Address Set	0	1	0	0	0	0	1		Add	Colum ress		00h to	Set 4 higher bits and 4 lower bits of column address of display data						
	0	1	0	0	0	0	0	L		Colum ress	n	18h	RAM in register						
(5) Read Status	0	0	1		Sta	itus		0	0	0	0	XX	Reads the status information						
(6) Write Display Data	1	1	0				Write	Data	-	_	-	XX	Write data in display data RAM						
(7) Read Display Data	1	0	1				Read	Data				XX	Read data from display data RAM						
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1		Set the display data RAM address SEG output correspondence						
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1		Normal indication when low, but full indication when high						
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Select normal display (0) or entire display on						
(11)LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio						
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write						
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write						
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions						
(15)Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Select COM output scan direction *: invalid data						
(16)Power Control Set	0	1	0	0	0	1	0	1	Oper	ation \$	Status	28h to 2Fh	Select the power circuit operation mode						
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Res	istor F	Ratio		Select internal resistor ratio Rb/Ra mode						
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h							
Electronic Volume Register Set	0	1	0	*	*		Electr	onic C	Control Value		xx	Sets the V0 output voltage electronic volume register							
(19)Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1		Sets static indicator ON/OFF 0: OFF, 1: ON						
Set Static Indicator Register	0	1	0	*	*	*	*	*	*			* Mode		Mode		Mode		XX	Sets the flash mode
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON						
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation						

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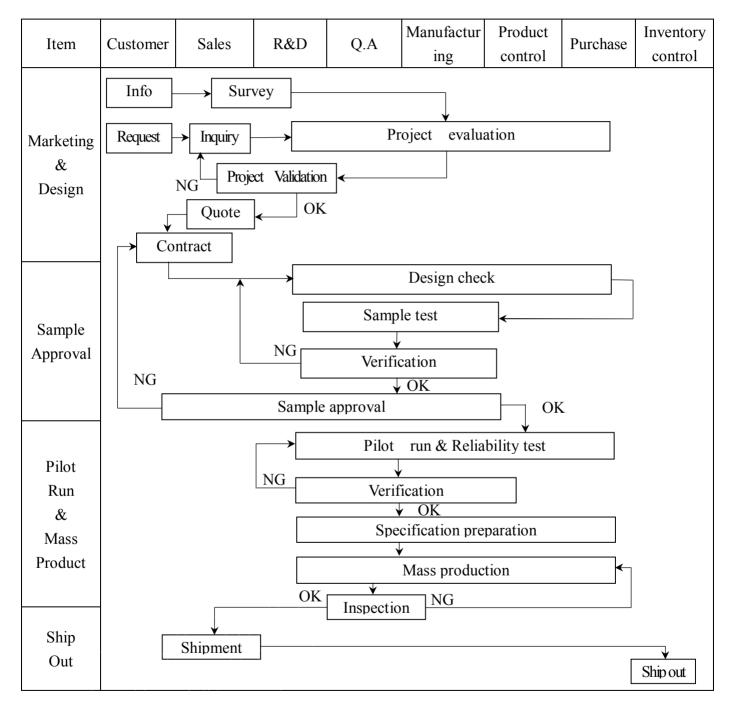
Comment	A0 /RD		A.0 /D.0		(00	/WR					Code					Function
Command	A0	/RD	/wĸ	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function			
(22)Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Select the oscillation frequency			
(23)Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0 1		Enter/Release the partial display mode			
(24)Partial Display Duty Set	0	1	0	0	0	1	1	0	Du	.ty Ra	tio		Sets the LCD duty ratio for partial display mode			
(25)Partial Display Bias Set	0	1	0	0	0	1	1	1	Bi	Bias Ratio			Sets the LCD bias ratio for partial display mode			
(26)Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set			
Partial Start Line Set	0	1	0	1	1		Partial Start Line		ΧХ	Sets the LCD Number of partial display start line						
(27)N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion			
Number of Line Set	0	1	0	*	*	*		Num	ber of	Line		ΧХ	Sets the number of line used for N-Line inversion			
(28)N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion			
(29)DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency			
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division		Clock Division		xx	Set the Division of DC/DC Clock Frequency			
(30)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!			
(31)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset			

Note: Do not use any other command, or system malfunction may result.



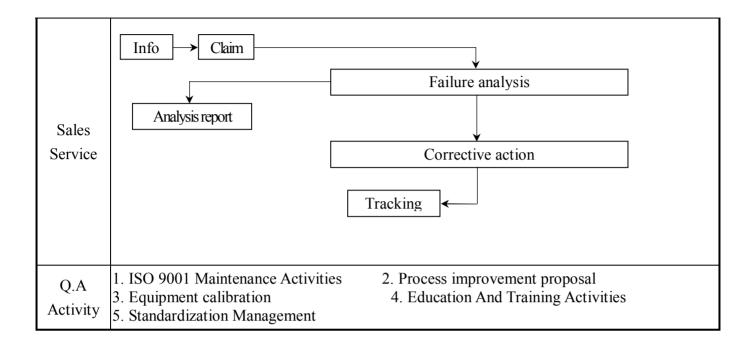
3. QUALITY ASSURANCE SYSTEM

3.1 Quality Assurance Flow Chart



Item	Customer	Sales	R&D	Q.A	Manufactu ring	Product control	Purchase	Inventory control
		Supplied by: Midas Components	U	20				
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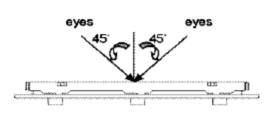


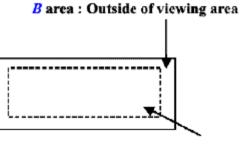


3.2 Inspection Specification

◆Inspection Standard : MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ.

- ◆Equipment : Gauge、MIL-STD、Powertip Tester、Sample
- ◆Defect Level : Major Defect AQL 0.4; Minor Defect AQL 1.5 .
- ♦ OUT Going Defect Level : Sampling .
- ◆Manner of appearance test :
 - (1). The test be under 40W×2 fluorescent light ' and distance of view must be at 30 cm.
 - (2). The test direction is base on about around 45° of vertical line. (Fig. 1)
 - (3). Definition of area . (Fig. 2)





A area : viewing area

Specification:

NO	Item	Criterion	level
01	Product condition	 1.1 The part number is inconsistent with work order of Production. 1.2 Mixed production types. 1.3 Assembled in inverse direction. 	Major Major Major
02	Quantity	2.1 The quantity is inconsistent with work order of production.	Major
03	Outline dimension	3.1 Product dimension and structure must conform to Structure diagram.	Major
		4.1 Missing line character	Major Major
04	Electrical Testing	4.2 No function of no display. 4.3 Output data is error.	Major
		4.4 LCD viewing angle defect.	Major
		4.5 Current consumption exceeds product specifications.	Major
05	Black or white dot < scratch < contamination Round type	 5.1 Round type: 5.1.1 display only : White and black spots on display ≤ 0.30mm, no more than Four white or black spots present. Densely spaced : NO more than two spots or lines within 3mm 	Minor

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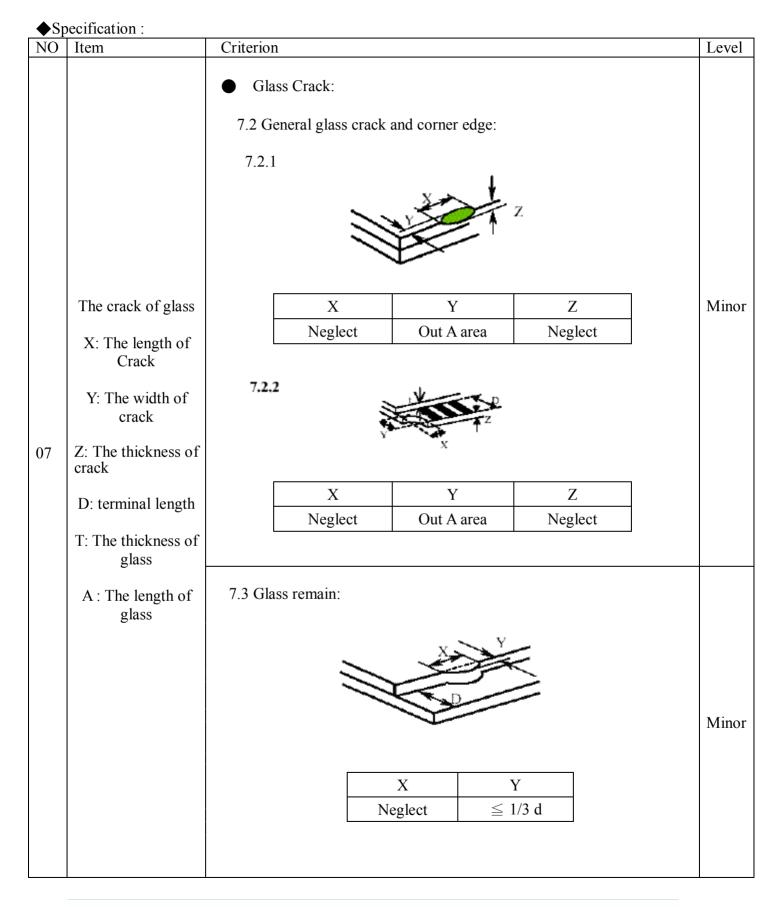
NO	Item	Criterion					level			
05	Black or white dot γ scratch γ		5.1.2 Nom-display :							
	contamination	Dir	Dimension (diameter : Φ) Acceptance(Q'ty)							
	Round type		$\Phi \leq 0.10 \text{mm} \qquad \text{Accept no dense}$							
	→ _x ←		$10 \text{mm} < \Phi \leq 0.20$		3					
	Y	0.	$20 \mathrm{mm} < \Phi \leq 0.30$	mm	2					
	-		Total		4					
	$\Phi = (x+y)/2$	5.1.3 Line t	ype:				Minor			
	· (A ·)) =	Dimens	ion (diameter : Φ)	Acceptan	ce (Q'ty)				
		Length	width		A area	B area				
	т		$w \leq 0.03mm$		Accept no dense	Don't count				
		L≦ 3.0mm				Don't count				
		L≦ 2.5mm	0.05 mm $< \Phi \leq 0$		4	Don't count				
			w>0.075m	m	As round	d type				
				1						
				•	Acceptance(Q'1	-				
		Dimension	(diameter : Φ)	A	area	B area				
		Φ≦	≦0.20mm	Acc	ept no dense	Don't count				
00	Polarizer	0.20mm	$<\Phi \leq$ 0.50mm		3	Don't count	Minor			
06	Bubble	0.50mm	$<$ $\Phi \leq$ 1.00mm		2	Don't count				
		Φ.2	>1.00mm		0	Don't count				
		Tota	ll quantity		4	Don't count				
07	The crack of glass	-	Crack: ck on the circuit o	f electrod	le terminal :	Z	Minor			
		Fro		a .		$\frac{Z}{Z \leq t}$				
		Ba		a						
		Ba	UK I		Neglect					

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◆Specification :

NO	Item	Criterion			Level		
07	The crack of glass X: The length of Crack Y: The width of crack Z: The thickness of crack D: terminal length T: The thickness of	7.4 Corner cr	ack and medial crack: $ \begin{array}{c} z \\ \hline z \\ \hline \hline$	SP 3]	Minor		
	glass	X	Y	Z			
	A : The length of glass	$ \leq 1/5a $ $ \leq 1/5a $	Crack can't enter viewing area Crack can't exceed the half of width of SP width of SP	$\leq 1/2t$ $1/2t < Z \leq 2t$			
		8.1 Backlight	can't work normally.		Major		
08	Backlight elements	8.2 Backlight of	doesn't light or color is wrong.		Major		
		8.3 Illumination source flickers when lit.					
		9.1 pin type m	ust match type in specification she	et	Major		
		9.2 No short circuits in components on PCB or FPC					
09	General appearance	9.3Product packaging must the same as specified on packaging specification sheet.					
		9.4 The folding and peeled off in polarizer are not acceptable					
	9.5 The PCB or FPC between B/L assembled distance (PCB or FPC) is ≤ 1.5 mm						



4. RELIABILITY TEST

4.1	Reliability	Test	Condition
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NO.	TEST ITEM	TEST CONDITION							
1	High Temperature Storage Test	-	Keep in 80 $\pm 2^{\circ}$ C 96 hrs Surrounding temperature, then storage at normal condition 4hrs						
2	Low Temperature Storage Test	-	Keep in $-30 \pm 2^{\circ}$ C 96 hrs Surrounding temperature, then storage at normal condition 4hrs						
3	High Humidity Storage	Surrounding	Keep in $+60^{\circ}$ C/90%RH duration for 96 hrs surrounding temperature, then storage at normal condition 4hrs Excluding the polarizer)						
		Discharge fo	ge: ' with 5 times or each polarity +/- ature Ambient: 15° C ~ 35	Contact Discharge: Apply 250V with 5 discharge for each p					
4	ESD Test	 Prempetature remotent 15 € - 55 € Humidity relative:30%~60% Energy Storage Capacitance(Cs+Cd):150pF±10% Discharge Resistance(Rd):330 Ω±10% Discharge, mode of operation: Single Discharge (time between successive discharges at least 1 s) (Tolerance If the output voltage indication: ±5%) 							
5	Temperature Cycling Test	Surrounding	$-20^{\circ}C \rightarrow 25^{\circ}C \rightarrow 70^{\circ}$ $(30 \text{ mins}) (5 \text{ mins}) (6 \text{ mins}) (7 \text{ mins}$	(30mins) (5mins) cle	4hrs				
6	Vibration Test (Packaged)	2. The amp	ve $10 \sim 55$ HZ frequency plitude of vibration :1.5 rection (XYZ) duration :	mm					
			Packing Weight (Kg)	Drop Height (cm)					
			$0 \sim 45.4$	122					
7	Drop Test (Packaged)		$45.4 \sim 90.8$	76					
			$90.8 \sim 454$	61					
			Over 454	46					
		D	rop direction : 3 come	/1 edges /6 sides etch	1 times				



5. PRECAUTION RELATING PRODUCT HANDLING 5.1 SAFETY

- 5.1.1 If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
- 5.1.2 If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

5.2 HANDLING

- 5.2.1 Avoid any strong mechanical shock which can break the glass.
- 5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module , be sure to ground your body and any electrical equipment you may be using.
- 5.2.3 Do not remove the panel or frame from the module.
- 5.2.4 The polarizing plate of the display is very fragile. So, please handle it very carefully ,do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)
- 5.2.5 Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
- 5.2.6 Do not touch the display area with bare hands, this will stain the display area.
- 5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.
- 5.2.8 To control temperature and time of soldering is $320\pm10^{\circ}$ C and 3-5 sec.
- 5.2.9 To avoid liquid (include organic solvent) stained on LCM .

5.3 STORAGE

- 5.3.1 Store the panel or module in a dark place where the temperature is $25^{\circ}C \pm 5^{\circ}C$ and the humidity is below 65% RH.
- 5.3.2 Do not place the module near organics solvents or corrosive gases.
- 5.3.3 Do not crush , shake , or jolt the module.

5.4 TERMS OF WARRANTY

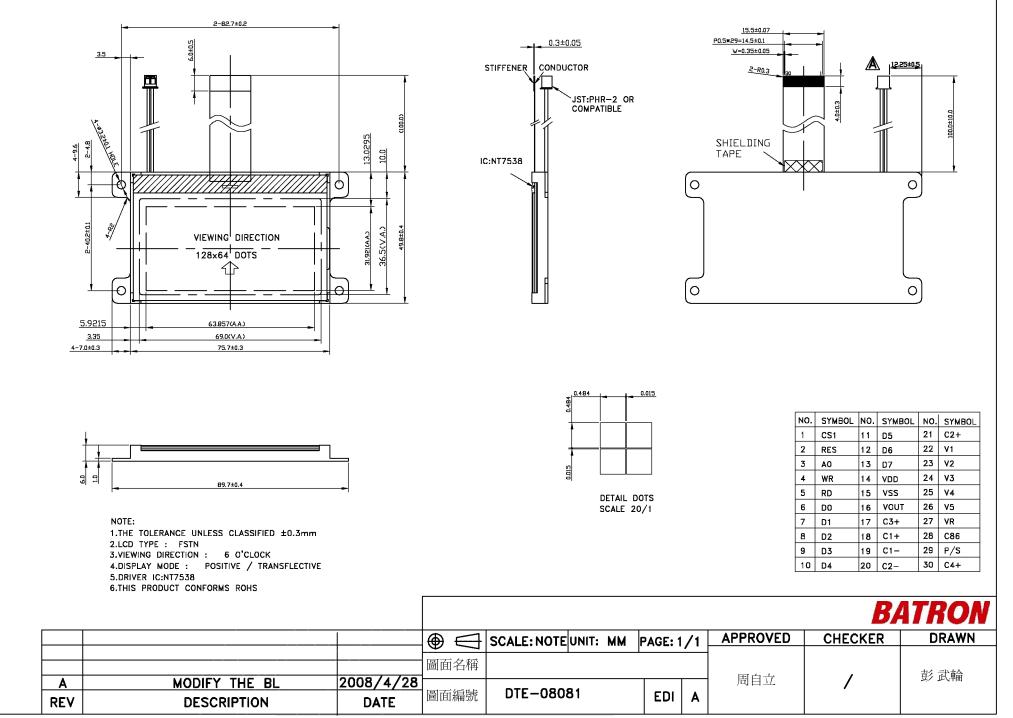
5.4.1 Applicable warrant period

The period is within thirteen months since the date of shipping out under normal using and storage conditions.

5.4.2 Unaccepted responsibility

This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in nuclear power control equipment, aerospace equipment, fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.

Supplied by:



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