ADSP-BF527 EZ-KIT Lite®
Evaluation System Manual

Revision 1.4, August 2009

Part Number
82-000208-01

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ANALOG DEVICES

Copyright Information

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Regulatory Compliance

The ADSP-BF527 EZ-KIT Lite is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-BF527 EZ-KIT Lite has been certified to comply with the essential requirements of the European EMC directive 2004/108/EC and therefore carries the "**CE**" mark.

The ADSP-BF527 EZ-KIT Lite has been appended to Analog Devices, Inc. EMC Technical File (EMC TF) referenced **DSPTOOLS1**, issue 2 dated June 4, 2008 and was declared CE compliant by an appointed Notified Body (No.0673) as listed below.

Notified Body Statement of Compliance: Z600ANA2.031 dated November 7, 2008.

Issued by: Technology International (Europe) Limited
60 Shrivenham Hundred Business Park
Shrivenham, Swindon, SN6 8TY, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

CONTENTS

ADSP-BF527 EZ-KIT LITE HARDWARE REFERENCE

PREFACE

Thank you for purchasing the ADSP-BF527 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for the ADSP-BF523, ADSP-BF525, and ADSP-BF527 Blackfin® processors.

Blackfin processors embody a new type of embedded processor designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. They deliver breakthrough signal-processing performance and power efficiency within a reduced instruction set computing (RISC) programming model.

Blackfin processors support a media instruction set computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics. Blackfin processors deliver signal-processing performance in a microprocessor-like environment.

Based on the Micro Signal Architecture (MSA), Blackfin processors combine a 32-bit RISC instruction set, dual 16-bit multiply accumulate (MAC) DSP functionality, and eight-bit video processing performance that had previously been the exclusive domain of very-long instruction word (VLIW) media processors.

The evaluation board is designed to be used in conjunction with the VisualDSP++® development environment to test capabilities of the ADSP-BF523/BF525/BF527 Blackfin processors. The VisualDSP++ development environment aids advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-BF527 assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the processor from a personal computer (PC) is achieved through a USB port or an external JTAG emulator. The USB interface provides unrestricted access to the ADSP-BF527 processor and evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to http://www.analog.com/dsp/tools/.

The ADSP-BF527 EZ-KIT Lite provides example programs to demonstrate the evaluation board capabilities.

The ADSP-BF527 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. For details about evaluation license restrictions after the 90 days, refer to "Evaluation License Restrictions" on page 1-7 and the *VisualDSP++ Installation Quick Reference Card*.

Product Overview

The board features:

- Analog Devices ADSP-BF527 Blackfin processor
  - Core performance up to 600 MHz
  - External bus performance up to 133 MHz
  - 289-pin mini-BGA package
  - 25 MHz crystal
- Synchronous dynamic random access memory (SDRAM)
  - Micron MT48LC32M16A2TG – 64 MB (8M x 16-bits x 4 banks)
- Parallel flash memory
  - ST Micro M29W320EB – 32 Mb (2M x 16-bits)
- NAND flash memory
  - ST Micro NAND04 – 4 Gb
- SPI flash memory
  - ST Micro M25P16 – 16 Mb
- Analog audio interface
  - Low-power audio codec
  - 1 stereo `LINE OUT` jack
  - 1 input `MIC` jack
  - 1 input stereo `LINE IN` jack

- TFT LCD display with touchscreen
  - Varitronix VLGT-6272-01 – 320 x 240, 3.5” touchscreen LCD
  - Maxim MAX1233 – touchscreen and keypad controller
- Ethernet interface
  - SMSC LAN8700 PHY device
  - 10-BaseT and 100-BaseTX Ethernet controller
  - Auto-MDIX
- Keypad
  - ACT components– 4 x 4 keypad assembly
- Thumbwheel
  - CTS Corp rotary encoder
- Universal asynchronous receiver/transmitter (UART)
  - ADM3202 RS-232 line driver/receiver
  - DB9 female connector
- LEDs
  - Eight LEDs: one power (green), one board reset (red), three general-purpose (amber), and one USB monitor (amber), PHY link (amber), PHY activity (green).
- Push buttons
  - Three push buttons: one reset, two programmable flags with debounce logic

- Expansion interface
  - Provides access to all ADSP-BF527 processor signals
- Other features
  - JTAG ICE 14-pin header
  - USB OTG connector
  - `HOST` interface connector
  - Power measurement jumpers
  - `PPI` IDC connector
  - `SPORT0` and `SPORT1` IDC connectors
  - TWI, SPI, timers, and `UART0` IDC connectors

For information about the hardware components of the EZ-KIT Lite, refer to "ADSP-BF527 EZ-KIT Lite Hardware Reference" on page 2-1.

Purpose of This Manual

The *ADSP-BF527 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF527 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference guide for future designs.

The product software installation is detailed in the *VisualDSP++ Installation Quick Reference Card*.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set. Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts (such as the *ADSP-BF52x Blackfin Processor Hardware Reference* and *Blackfin Processor Instruction Set Reference*) that describe your target architecture.

Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and user's or getting started guides. For the locations of these documents, see "Related Documents".

Manual Contents

The manual consists of:

- Chapter 1, "Using ADSP-BF527 EZ-KIT Lite" on page 1-1
  Describes EZ-KIT Lite operation from a programmer's perspective and provides an easy-to-access memory map.
- Chapter 2, "ADSP-BF527 EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the EZ-KIT Lite hardware components.
- Appendix A, "ADSP-BF527 EZ-KIT Lite Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1
  Provides the resources to allow board-level debugging or to use as a reference guide. Appendix B is part of the online Help.

What's New in This Manual

The *ADSP-BF527 EZ-KIT Lite Evaluation System Manual* has been updated to reflect the latest board revision. In addition, modifications and corrections based on errata reports against the previous manual revision have been made.

Technical or Customer Support

You can reach Analog Devices, Inc. Customer Support in the following ways:

- Visit the Embedded Processing and DSP products Web site at
  `http://www.analog.com/processors/technicalSupport`
- E-mail tools questions to
  `processor.tools.support@analog.com`
- E-mail processor questions to
  `processor.support@analog.com (World wide support)`
  `processor.europe@analog.com (Europe support)`
  `processor.china@analog.com (China support)`
- Phone questions to **1-800-ANALOGD**
- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:
  `Analog Devices, Inc.`
  `One Technology Way`
  `P.O. Box 9106`
  `Norwood, MA 02062-9106`
  `USA`

Supported Processors

This evaluation system supports Analog Devices ADSP-BF523, ADSP-BF525, and ADSP-BF527 Blackfin embedded processors.

Product Information

Product information can be obtained from the Analog Devices Web site, VisualDSP++ online Help system, and a technical library CD.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

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VisualDSP++ Online Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, Dinkum Abridged C++ library, and FLEXnet License Tools software documentation. You can search easily across the entire VisualDSP++ documentation set for any topic of interest.

For easy printing, supplementary Portable Documentation Format (`.pdf`) files for all manuals are provided on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

File	Description
`.chm`	Help system files and manuals in Microsoft help format
`.htm` or `.html`	Dinkum Abridged C++ library and FLEXnet License Tools software documentation. Viewing and printing the `.html` files requires a browser, such as Internet Explorer 6.0 (or higher).
`.pdf`	VisualDSP++ and processor manuals in PDF format. Viewing and printing the `.pdf` files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).

Technical Library CD

The technical library CD contains seminar materials, product highlights, a selection guide, and documentation files of processor manuals, VisualDSP++ software manuals, and hardware tools manuals for the following processor families: Blackfin, SHARC, TigerSHARC, ADSP-218x, and ADSP-219x.

To order the technical library CD, go to `http://www.analog.com/processors/technical_library`, navigate to the manuals page for your processor, click the request CD check mark, and fill out the order form.

Data sheets, which can be downloaded from the Analog Devices Web site, change rapidly, and therefore are not included on the technical library CD. Technical manuals change periodically. Check the Web site for the latest manual revisions and associated documentation errata.

Related Documents

For information on product related development software, see the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-BF522/ADSP-BF525/ADSP-BF527 Blackfin Embedded Processor Data Sheet	General functional description, pinout, and timing.
ADSP-BF2x Blackfin Processor Hardware Reference	Description of the internal processor architecture and all register functions.
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions

Table 2. Related VisualDSP++ Publications

Title	Description
ADSP-BF527 EZ-KIT Lite Evaluation System Manual	Description of the hardware capabilities of the evaluation system; description of how to access these capabilities in the VisualDSP++ environment.
VisualDSP++ User's Guide	Description of the VisualDSP++ features and usage.
VisualDSP++ Assembler and Preprocessor Manuals	Description of the assembler function and commands.
VisualDSP++ C/C++ Complier and Library Manual for Blackfin Processors	Description of the complier function and commands for Blackfin processors.
VisualDSP++ Linker and Utilities Manual	Description of the linker function and commands.

Table 2. Related VisualDSP++ Publications (Cont'd)

Title	Description
VisualDSP++ Loader and Utilities Manual	Description of the loader/splitter function and commands.
VisualDSP++ Device Drivers and System Services Manual for Blackfin Processors	Description of the device drivers' and system services' functions and commands.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.

Example	Description
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

1 USING ADSP-BF527 EZ-KIT LITE

This chapter provides information to assist you with development of programs for the ADSP-BF527 EZ-KIT Lite evaluation system.

The following topics are covered.

For information about VisualDSP++, including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online Help.

For more detailed information about the ADSP-BF527 Blackfin processor, see documents referred to as "Related Documents".

Package Contents

Your ADSP-BF527 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF527 EZ-KIT Lite board
- *VisualDSP++ Installation Quick Reference Card*
- CD containing:
  - VisualDSP++ software
  - ADSP-BF527 EZ-KIT Lite debug software
  - USB driver files
  - Example programs
  - *ADSP-BF527 EZ-KIT Lite Evaluation System Manual*
- Universal 7.0V DC power supply
- 7-foot Ethernet patch cable
- Three 6-foot 3.5 mm male-to-male audio cables
- 3.5 mm headphones
- 10-foot USB A-B male cable for USB debug agent
- 5-in-1cable and connectors for USB on-the-go (OTG) applications
- Ethernet loopback connector

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The ADSP-BF527 EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components. Figure 1-1 shows the default jumper settings, switches, connector locations, and LEDs used in installation. Confirm that your board is in the default configuration before using the board.

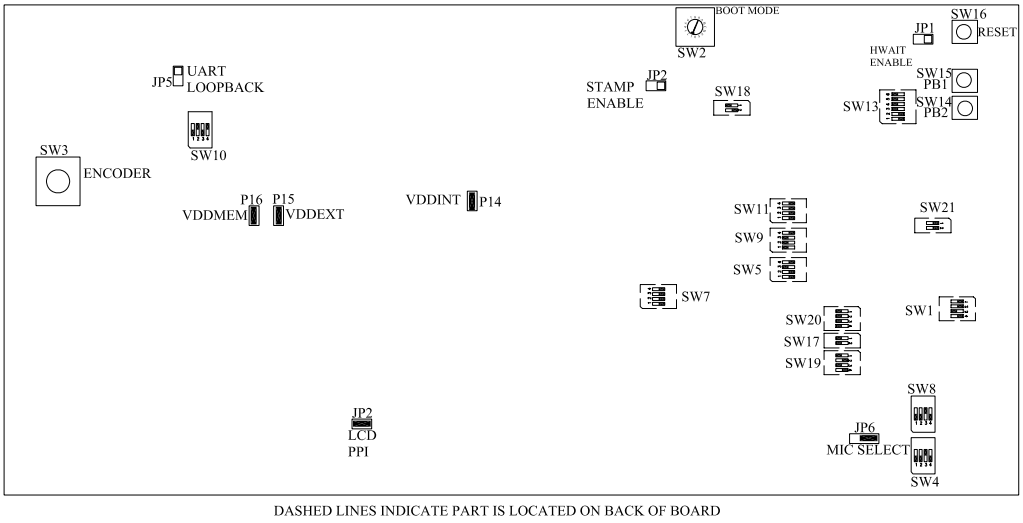


Figure 1-1. EZ-KIT Lite Hardware Setup

Installation and Session Startup

For correct operation, install the software and hardware in the order presented in the *VisualDSP++ Installation Quick Reference Card*.

There are two USB interfaces on the ADSP-BF527 EZ-KIT Lite. Be sure to use the debugger's interface (ZJ1) when connecting your computer to the board with provided USB cable. The other USB interface (labelled USB-OTG, P1) is for applications use.

1. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start–>Programs** menu. The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 3.

   If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 4.
3. To connect to a new EZ-KIT Lite session, start **Session Wizard** by selecting one of the following.
   - From the **Session** menu, **New Session**.
   - From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
   - From the **Session** menu, **Connect to Target**.

4. The **Select Processor** page of the wizard appears on the screen. Ensure **Blackfin** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-BF527**. Click **Next**.

5. The **Select Connection Type** page of the wizard appears on the screen. Select **EZ-KIT Lite** and click **Next**.

6. The **Select Platform** page of the wizard appears on the screen. Ensure that the selected platform is **ADSP-BF527 EZ-KIT Lite via Debug Agent**. Specify your own **Session name** for the session or accept the default name.

   The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and open a new session.

   Click **Next**.

7. The **Finish** page of the wizard appears on the screen. The page displays your selections. Check the selections. If you are not satisfied, click **Back** to make changes; otherwise, click **Finish**. VisualDSP++ creates the new session and connects to the EZ-KIT Lite. Once connected, the main window's title is changed to include the session name set in step 6.

To disconnect from a session, click the disconnect button  or select **Session–>Disconnect from Target**.

To delete a session, select **Session –> Session List**. Select the session name from the list and click **Delete**. Click **OK**.

Evaluation License Restrictions

The ADSP-BF527 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ restricts a connection to the ADSP-BF527 EZ-KIT Lite via the USB debug agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a user program to 20 KB of memory for code space with no restrictions for data space.
- The EZ-KIT Lite hardware must be connected and powered up to use VisualDSP++ with a valid evaluation or permanent license.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

Lockbox Key

The ADSP-BF527 Blackfin processors feature Lockbox™ secure technology: hardware-enabled code security and content protection for one-time programmable (OTP) memory. Customers purchasing the ADSP-BF527 processors can program their own customer public key in OTP memory.

The ADSP-BF527 EZ-KIT Lites are special cases—evaluation boards with the Lockbox keys pre-programmed and publicly documented—the burden of key generation and OTP programming is removed from the customer. For EZ-KIT Lites, Analog Devices publicly document the public and private key pair for customer evaluation and support of the Lockbox feature, all while avoiding any keys information exchange. As a result, there is no confidentiality associated with the Lockbox key on EZ-KIT Lites.

To demonstrate Lockbox features using an EZ-KIT Lite, you must use the keys that are provided pre-programmed on your EZ-KIT Lite.

Use the EZ-KIT Lite key pair to generate a demo and then provide the keys to the demo users. Note that the EZ-KIT Lite cannot be used to secure any confidential information. If you wish to create a demo with confidential keys, you must build your own Blackfin board and personalize it with your own keys.

Memory Map

The ADSP-BF527 processor has internal static random access memory (SRAM) used for instructions or data storage. See Table 1-1. The internal memory details can be found in the *ADSP-BF2x Blackfin Processor Hardware Reference.*

The ADSP-BF527 EZ-KIT Lite board includes four types of external memory: synchronous dynamic random access memory (SDRAM), serial peripheral interconnect (SPI), parallel flash, and NAND flash. See Table 1-2. For more information about a specific memory type, go the respective section in this chapter.

Table 1-1. EZ-KIT Lite Internal Memory Map

Start Address	Content
0xEF00 0000	BOOT ROM (32K BYTE)
0xEF00 8000 0xFEB0 0000 0xFEB2 0000 0xFF40 0000 0xFF40 4000 0xFF40 8000 0xFF50 0000 0xFF50 4000 0xFF50 8000 0xFF60 0000 0xFF60 4000 0xFF60 8000 0xFF60 C000 0xFF61 0000 0xFF61 4000 0xFF70 0000 0xFF70 1000	Reserved
0xFF80 0000	L1 DATA BANKA SRAM (16K BYTE)
0xFF80 4000	L1 DATA BANKA SRAM/CACHE (16K BYTE)
0xFF80 8000	Reserved
0xFF90 0000	L1 DATA BANKB SRAM (16K BYTE)
0xFF90 4000	L1 DATA BANKB SRAM/CACHE (16K BYTE)
0xFF90 8000	Reserved
0xFFA0 0000	L1 INSTRUCTION BANKA LOWER SRAM (16K BYTE)
0xFFA0 4000	L1 INSTRUCTION BANKA UPPER SRAM (16K BYTE)

Table 1-1. EZ-KIT Lite Internal Memory Map (Cont'd)

Start Address	Content
0xFFA0 8000	L1 INSTRUCTION BANKB LOWER SRAM (16 BYTE)
0xFFA0 C000	Reserved
0xFFA1 0000	L1 INSTRUCTION SRAM/CACHE (16K BYTE)
0xFFA1 4000 0xFFA1 8000 0xFFA1 C000 0xFFA2 0000 0xFFA2 4000	Reserved
0xFFB0 0000	L1 SCRATCHPAD SRAM (4K BYTE)
0xFFB0 1000	Reserved
0xFFC0 0000	SYSTEM MMR REGISTERS
0xFFE0 0000	CORE MMR REGISTERS

Table 1-2. EZ-KIT Lite External Memory Map

Start Address	End Address	Content
0x0000 0000	0x03FF FFFF	SDRAM bank 0 (SDRAM)
0x2000 0000	0x200F FFFF	ASYNC memory bank 0 (flash)
0x2010 0000	0x201F FFFF	ASYNC memory bank 1 (flash)
0x2020 0000	0x202F FFFF	ASYNC memory bank 2 (flash)
0x2030 0000	0x203F FFFF	ASYNC memory bank 3 (flash)
0x2040 0000	0xEEFF FFFF	Reserved

SDRAM Interface

The ADSP-BF527 processor connects to a 64 MB Micron MT48LC32M16A2TG-75 chip through the external bus interface unit (EBIU). The SDRAM chip can operate at a maximum clock frequency of 133 MHz.

With a VisualDSP++ session running and connected to the EZ-KIT Lite board via the USB debug agent, the SDRAM registers are configured automatically with values listed in Table 1-3 each time the processor is reset. The values are used whenever SDRAM is accessed through the debugger (for example, when viewing memory windows or loading a program).

To disable the automatic setting of the SDRAM registers, select **Target Options** from the **Settings** menu in VisualDSP++ and uncheck **Use XML reset values**. For more information on changing the reset values, refer to the online Help.

Table 1-3. SDRAM Default Settings with a 133 MHz SCLK

Register	Value	Function
pEBIU_SDRRC	0x0407	Calculated with SCLK = 133 MHz fSCLK = 133 MHz tREF = 64 ms NRA = 8192 row addresses tRAS = 6 clock cycles tRP = 2 clock cycles RDIV = 0x407
pEBIU_SDBCTL	0x0025	EBCAW = 10 bits EBSZ = 64M byte EBE = enabled

Table 1-3. SDRAM Default Settings with a 133 MHz SCLK (Cont'd)

Register	Value	Function
pEBIU_SDGCTL	0x0091998d	TSCSR = 45 degrees C EMREN = disabled FBBRW = disabled PSSE = enables SDRAM powerup sequence on next SDRAM access PSM = precharge, 8 BCBR refresh cycles, mode register set PUPSD = no extra delay added before first precharge command TWR = 2 cycles TRCD = 3 cycles TRP = 3 cycles TRAS = 6 cycles PASR = all 4 banks refreshed CL = CAS latency 3 cycles SCTLE = CLOUT disabled

Table 1-4 shows configuration of the PLL registers using a 400 MHz CCLK and 133 MHz SCLK. The PLL_CTL and PLL_DIV registers are initialized in the user code to achieve maximum performance.

Table 1-4. PLL Register Settings

Register	SCLK = 133 MHz CCLK = 400 MHz
PLL_CTL	16
PLL_DIV	3

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the SDRAM interface. For more information on how to initialize the registers after a reset, search the VisualDSP++ online Help for "reset values".

Parallel Flash Memory Interface

The parallel flash memory interface of the ADSP-BF527 EZ-KIT Lite contains a 4 MB (2M x 16 bits) ST Micro M29W320EB chip. Flash memory connects to the 16-bit data bus and address lines 1 through 19. Chip enable is decoded by using AMS0-3 select lines through NAND and AND gates. The address range for flash memory is 0x2000 0000 to 0x203F FFFF.

Flash memory is pre-loaded with boot code for the blink, LCD images, and power-on-self test (POST) programs. For more information, refer to "Power-On-Self Test" on page 1-27.

By default, the EZ-KIT Lite boots from the 16-bit parallel flash memory. The processor boots from flash memory if the boot mode select switch (SW2) is set to a position of 1 (see "Boot Mode Select Switch (SW2)" on page 2-11).

Flash memory code can be modified. For instructions, refer to the online Help and example program included in the EZ-KIT Lite installation directory.

NAND Flash Interface

The ADSP-BF527 processor is equipped with an internal NAND flash controller, which allows the 4 Gbit ST Micro's NAND04 device to be attached gluelessly to the processor. NAND flash is attached via the processor's specific NAND flash control and data lines. NAND flash shares pins with the Ethernet PHY, host connector, and expansion interface.

The NAND chip enable signal (NDCE#_HOSTD10) can be disconnected from NAND flash by turning OFF SW11.4 (switch 11 position 4). This ensures that the NAND will not be driving data when HOSTD10 changes state. See "Rotary NAND Enable Switch (SW11)" on page 2-16 for more information.

The Ethernet PHY (U14) must be disabled in order for NAND flash to function properly. This is accomplished by setting SW1 to OFF, OFF, ON, OFF.

For more information about the NAND04 device, refer to the ST Microelectronics Web site at: http://www.st.com/stonline/products/families/memories/memory/index.htm.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the NAND flash interface.

SPI Interface

The ADSP-BF527 processor has one serial peripheral interface (SPI) port with multiple chip select lines. The SPI port connects directly to serial flash memory, MAX1233 touchscreen and keypad controller, audio codec, and expansion interface.

Serial flash memory is a 16 Mb ST Micro M25P16 device, which is selected using the SPISEL1 line of the processor. SPI flash memory is pre-loaded with boot code for the blink and POST programs. For more information, refer to "Power-On-Self Test" on page 1-27. By default, the EZ-KIT Lite boots from the 16-bit flash parallel memory. SPI flash can be selected as the boot source by setting the boot mode select switch (SW2) to position 3 (see "Boot Mode Select Switch (SW2)" on page 2-11).

SPI flash code can be modified. For instructions, refer to the VisualDSP++ online Help and example program included in the EZ-KIT Lite installation directory.

By default, the EZ-KIT Lite is set to use the SPISEL2 pin as the chip select for the MAX1233 touchscreen and keypad controller (see "KEY/PEN CS Switch (SW18)" on page 2-19). SPISEL2 is shared with the CDG signal, which is connected to the rotary encoder. It is important not to use the

rotary encoder while trying to access the MAX1233 controller. Shutting OFF SW11.2 disables the rotary encoder. See "Rotary Encoder Interface" on page 1-19 for more information. There are also provisions to use the SPISEL4 signal as the MAX1233 chip select by setting SW18 to OFF, ON. SPISEL4 signal is shared with the ERXD1_HOSTD8 signal. Using signal SPISEL4 will interfere with the ability to use Ethernet, but will allow the use of rotary, keypad, and touchscreen, all at the same time. The appropriate port function needs to be set up to use programmable flag (PF) PH8 of the processor as SPISEL4 (refer to the hardware reference manual for details). For more information, refer to "Touchscreen and Keypad Interface" on page 1-18.

By default, the audio codec is setup to use the SPISEL5 signal as the SPI chip select when configuring the codec. The chip select is shared with the HOSTD9 signal. For more information, refer to see "Audio Interface" on page 1-21.

PPI Interface

The ADSP-BF527 processor provides a parallel peripheral interface (PPI), supporting data widths up to 16 bits. The PPI interface provides three multiplexed frame syncs, a dedicated clock input, and 16 data lines. The EZ-KIT Lite uses an eight-bit data connection to the TFT LCD module. The full PPI port is accessible on the PPI connector P8 and expansion interface.

The PPI interface can be disconnected from the LCD module by removing jumper on JP2. The JP2 jumper enables the U31 and U32 buffer ICs. For more information on the LCD module, refer to "LCD Module Interface" on page 1-17. For information on how to enable the PPI connection to the LCD module, see "LCD PPI Jumper (JP2)" on page 2-21.

The PPI signals connect to multi-function pins; the upper eight data bit signals are configured for the rotary, SPI, UART1, and LED0 interfaces. See "Touchscreen and Keypad Interface" on page 1-18 for more information.

The PPI interface has a dedicated clock, generated from an on-board oscillator (default) or the expansion interface. The source of the PPI clock can be configured by software via the PPI_SEL signal. The signal connects to the processor's flag pin PG12 by setting SW13 position 4 ON. Flag pin PG12 is shared with the HOSTACK_LED2 signal. When the clock select line is used, HOSTACK and LED2 are not available. The PPISEL signal does not need to be driven if the default on-board oscillator is used; PPISEL is driven when the expansion interface is used as the clocking source. Refer to "GPIO Enable Switch (SW13)" on page 2-16 for more information.

LCD Module Interface

The EZ-KIT Lite features a Varitronix VL_PS_COG_T350MCQB TFT LCD module with touchscreen overlay. This is a 3.5" landscape display with a resolution of 320 x 240 and a color depth of 24 bits. The interface is an RGB-888 serial parallel interface, eight bits of red, followed by eight bits of green, and then eight bits of blue.

To configure the PPI interface, refer to the LCD software example located in the…\Blackfin\Examples\ADSP-BF527 EZ-KIT Lite\POST subdirectory of the VisualDSP++ installation directory. The values are obtained from the timing characteristics section of the VL_PS_COG_T350MCQB datasheet.

The interface is set to control frame sync 1 and 2 (PPIFS1, PPIFS2) natively from the ADSP-BF527 processor. The LCD data enable (DEN) is controlled by a Xilinx CPLD XC9536XL. You do not need to change CPLD code, which should work for the VL_PS_COG_T350MCQB display. The verilog source code for the CPLD can be found in the reference resource zip file in the <*install_path*>\Blackfin\Examples\ADSP-BF527 EZ-KIT Lite\XC9536XL_ConfigFiles directory of VisualDSP++.

The LCD module can be disconnected from PPI by removing the jumper on JP2. Refer to "LCD PPI Jumper (JP2)" on page 2-21 for more information.

Touchscreen and Keypad Interface

The MAX1233 touchscreen and keypad controller connects to the SPI interface of the ADSP-BF527 processor and uses the SPISEL2 signal. The controller provides the X and Y positions, as well as a measurement for the pressure applied to the touchscreen. The touchscreen can be used with either a stylus or a finger.

Two interrupt signals connect to the device:

- The key interrupt (KEYIRQ#) signal is mapped to PF9 and used to notify the processor that a key on the keypad has been pressed.
- The pen interrupt (PENIRQ#) signal is mapped to PF10 and used to notify the processor that the screen has been touched. The PENIRQ# signal is shared with UART1RTS.

SW5 positions 1 and 2 are ON by default and allow the MAX1233 controller to be disconnected from PF pins PF9 and PF10 of the processor. SW5 positions 3 and 4 are (OFF, ON) by default and select the board reset as the reset input to the LCD module. The GPIO function of PF PG11 also can be used to control the LCD reset (SW5 positions 3 and 4 ON and OFF); however, PG11 is used to control LED1 by default.

The EZ-KIT Lite features a 4 x 4 keypad assembly connected to the MAX1233 touchscreen controller (U16). The keypad interface connects to the EZ-KIT Lite via a nine-pin connector (P2). The ADSP-BF527 processor receives input from the keypad through the SPI interface after a KEYIRQ# interrupt. The row/column pull-ups and pull-downs are handled internally by the MAX1233 controller.

For more options on the MAX1233 controller, refer to "Keypad LCD Enable Switch (SW5)" on page 2-13.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the touchscreen and keypad interface.

Rotary Encoder Interface

The ADSP-BF527 processor has a built-in, up-down counter with support for a rotary encoder. The three-wire rotary encoder interface connects to the rotary switch (SW3) and expansion interface connector. The rotary encoder can be turned clockwise for the up function, counter clockwise for the down function, or can be used as a push button for clearing the counter.

The rotary switch is a two-bit quadrature (Gray code) counter with detent, meaning that both the down signal (CDG) and up signal (CUD) will toggle when the count register increases on a rotation to the right. Upon rotating to the left, both CDG and CUD will toggle, and the over all count decreases.

If the processor pins are needed for the expansion interface, disconnect the rotary encoder switch via the four-position rotary NAND enable switch (SW11). For more information, see "Rotary NAND Enable Switch (SW11)" on page 2-16.

The CDG signal is shared with the SPISEL2 signal; care must be taken not to rotate the switch while issuing SPI commands to the keypad and touch-screen controller. To ensure that there is no interference from the rotary encoder on SPISEL2, turn SW1 position 2 OFF. Shutting off connection to CDG causes the rotary switch not to operate correctly. Both CDG and CUD are necessary for the switch to output accurate counts.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the rotary encoder interface.

Ethernet Interface

The ADSP-BF527 processor has an integrated Ethernet MAC with media independent interface (MII) and reduced media independent interface (RMII), which connects to an external PHY. The EZ-KIT Lite provides a SMSC LAN8700 RMII Ethernet PHY with Auto-MDIX, fully compliant with IEEE 802.2/802.2u standards. The SMSC LAN8700 chip supports 10BASE-T and 100BASE-TX operations. The part is attached gluelessly to the processor.

The Ethernet signals are shared with NAND flash, and the Ethernet is by default turned off (SW1 OFF, OFF, ON, OFF). See "ETH Enable Switch (SW1)" on page 2-10 for more information. It is important not to run code that accesses the NAND while using the Ethernet interface.

The Ethernet mode is set by the SW9 switch and defaults to all capable, auto negotiation with settings OFF, OFF, OFF, ON. See "ETH Mode Flash CS Switch (SW9)" on page 2-15 for more information.

The Ethernet chip is pre-loaded with a MAC address for the EZ-KIT Lite. The MAC address is stored in the public one-time programmable (OTP) memory of the processor and can be found on a sticker on the bottom side of the EZ-KIT Lite.

The PHY portion of the Ethernet chip connects to a Pulse HX1188 (U26) magnetics, then to a standard RJ-45 Ethernet connector (J9). For more information, see "Ethernet Connector (J9)" on page 2-28.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate how to use the Ethernet interface.

Audio Interface

The audio interface of the EZ-KIT Lite consists of a low-power stereo codec with integrated headphone driver and its associated passive components. There are two inputs, stereo line in, and mono microphone as well as two outputs, headphone, and stereo line out. The codec has integrated stereo analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) and requires minimal external circuitry.

The codec connects to the ADSP-BF527 processor via the processor's serial port 0A (alternate). The SPORT0A port is disconnected from the codec by turning SW17 and SW20. This allows SPORT0A to be used on the expansion interface.

The TFS0A signal is shared with the Ethernet and host connectors, as well as the RMIIMDINT# and HOSTCE# signals. SW21 allows this signal to be disconnected from the host connector by setting position 1 OFF, and STAMP connectors position 2 OFF. To connect signal TFS0A_RMIIMDINT#_HOSTCE# to either interface, turn the corresponding switch position ON. Refer to "TFS0A/HOSTCE Enable Switch (SW21)" on page 2-19 for more information.

The control interface for the codec is selectable by the SW8 and SW19 switches between the two-wire interface (TWI) and SPI. The board default is SPI mode, set by the SW19 switch (ON, OFF, ON, OFF) and by the SW8 switch positions 3 ON and 4 OFF. To select TWI mode, turn SW8 positions 3 OFF and 4 ON, as well as SW19 (OFF, ON, OFF, ON). Refer to "Mic/HP LPBK Audio Mode Switch (SW8)" on page 2-14 and "SPI/TWI Switch (SW19)" on page 2-19 for more information.

Mic gain is selectable through the SW4 switch, with values of 14 dB, 0 dB, or –6 dB, by turning ON position 1, 2, or 3 respectively. All other positions must be OFF to achieve the desired gain. Refer to "MIC Gain Switch (SW4)" on page 2-12 for more information.

Microphone bias is provided through a low-noise reference voltage. A jumper on position 2 and 3 of JP6 connects the MICBIAS to the audio jack. Placing the jumper on positions 1 and 2 of JP6 connects the bias directly to the mic signal. Refer to "MIC Select Jumper (JP6)" on page 2-22 for more information.

J7 and J8 are 3.5 mm connectors for the audio portion of the board. J7 connects the mic on the top portion and line-in on the bottom. J8 connects the headphone on the top portion and line-out on the bottom. If there is no 3.5 mm cable plugged into the bottom of J7 or J8, the signals are looped back inside the connector.

For testing purposes, SW8 positions 1 and 2 allow the MICIN signal to be connected to either the left or right headphone. Do not connect both left and right to the MICIN signal at the same time—only position 1 or 2 of SW8 should be ON at the same time. Refer to "Mic/HP LPBK Audio Mode Switch (SW8)" on page 2-14 for more information.

For more information, see "Dual Audio Connectors (J7–8)" on page 2-28.

The EZ-KIT Lite is shipped with a headphone and multiple 3.5 mm cables, which allow you to run the example programs provided in the EZ-KIT Lite installation directory and learn about the audio interface.

USB OTG Interface

The ADSP-BF527 processor has a built-in, high-speed USB on-the-go (OTG) interface and integrated PHY. The interface connects to a 24 MHz clock (U12), has surge protection, and can be configured as a host or device. When in device mode, the USB 5V regulator (VR3) and FET switch (U28) are turned OFF. When in host mode, the USB 5V regulator and FET are turned ON and can supply 5V at 500 mA.

The control mechanism to turn the two devices on and off are via the PG13 flag pin of the processor and must be connected on the board to signal USB_VRSEL through switch SW13. By default, USB_VRSEL is held low or a logic 0 via a pull-down resistor, and both devices are turned off. To use host mode and provide 5V to a device, SW13 position 2 needs to be turned OFF and position 6 ON. This disables push button 2. Note that signal USB_VRSEL is shared with HOSTADDR. The default for positions 2 and 6 of SW13 are ON and OFF, which shuts off the VR3 regulator and U28 FET. For more information, see "GPIO Enable Switch (SW13)" on page 2-16.

The USB OTG interface has a mini-AB connector (P1); cables that plug into P1 are shipped with the EZ-KIT Lite.

Use the example programs in the EZ-KIT Lite installation directory to learn about the ADSP-BF527 processor's device and host modes. For more information about the USB interface, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.

UART Interface

The ADSP-BF527 processor has two built-in universal asynchronous receiver transmitters (UARTs). UART1–0 share the processor pins with other peripherals on the EZ-KIT Lite.

UART1 has full RS-232 functionality via the Analog Devices 3.3V ADM3202 (U25) line driver and receiver. The UART can be disconnected from the ADM3202 by turning OFF all positions of SW10. See "UART Enable Switch (SW10)" on page 2-15. When using UART1, jumpers JP5 should not be installed. JP5 is a UART loopback jumper and should be installed only when running the POST program. If signals RTS and CTS are needed for flow control, the UART1RTS_PENIRQ# port pin PF10 can be configured as a GPIO for RTS. The HWAIT port pin PG0 can be used for CTS by setting up the pin accordingly. See "UART1 Loopback Jumper (JP5)" on page 2-22 and "UART Enable Switch (SW10)" on page 2-15 for more information.

UART0 and UART1 are connected to the expansion interface. UART0 of the processor also is available via a STAMP connector (P5). See "UART0 Connector (P5)" on page 2-29.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate UART and RS-232 operations.

For more information on the UART interface, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.

RTC Interface

The ADSP-BF527 processor has a real-time clock (RTC) and a watchlog timer. Typically the RTC interface is used to implement a real-time watchlog or life counter of the time elapsed since the last system reset. The EZ-KIT Lite is equipped with a Sanyo (CR2430) lithium coin 3V battery supplying 280 mAh. The 3V battery and the 3.3V supply of the board connect to the RTC power pin of the processor. When the EZ-KIT Lite is powered, the RTC circuit uses the board power to supply voltage to the RTC pin. When the EZ-KIT Lite is not powered, the RTC circuit uses the lithium battery to maintain the power to the RTC pin. After removing the mylar, the battery will last for about 1 year with the EZ-KIT Lite unpowered.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate the RTC features.

The EZ-KIT Lite is shipped with a protective Mylar sheet placed between the coin battery and the positive pin of the battery holder. Please remember to remove the Mylar sheet before trying to use RTC functionality of the processor.

For more information on the RTC and watchdog timer, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.

LEDs and Push Buttons

The EZ-KIT Lite provides two push buttons and three LEDs for general-purpose I/O.

The three LEDs, labeled LED1 through LED3, are accessed via the PF8, PG11, and PG12 pins of the processor respectively. For information on how to program the pins, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.

LED1 is shared with signal HOSTWR#, while LED2 is shared with signal HOSTACK. The LED1 signal can be used for the LCD reset by turning SW5 positions 3 ON and 4 OFF. LED2 is shared with PPI_SEL; turn SW13 position 4 OFF to use the LED.

The two general-purpose push buttons are labeled PB1 and PB2. The status of each individual button can be read through programmable flag inputs, PG0 and PG13. The flag reads 1 when a corresponding switch is being pressed. When the switch is released, the flag reads 0. A connection between the push button and processor input is established through the SW13 DIP switch. Push button 1 is shared with HWAIT and alternatively can be connected to signal keypad_busy by setting SW13 position 1 OFF and position 5 ON. Push button 2 is shared with HOSTADDR and also can be connected to USB_VRSEL by setting SW13 position 2 OFF and position 6 ON. USB_VRSEL allows the USB OTG to power an external USB device with 5V. See "USB OTG Interface" on page 1-22 and "GPIO Enable Switch (SW13)" on page 2-16 for more information.

An example program is included in the EZ-KIT Lite installation directory to demonstrate functionality of the LEDs and push buttons.

JTAG Interface

The JTAG emulation port allows an emulator to access the processor's internal and external memory through a six-pin interface. The JTAG emulator port of the processor can be accessed via the on-board USB debug agent or with an external emulator via the JTAG connector (ZP4). When an external emulator connects to the board, the on-board USB debug agent is disabled. See "JTAG Connector (ZP4)" on page 2-33 for more information.

For more information about emulators, contact Analog Devices or go to: http://www.analog.com/processors/blackfin/evaluationDevelopment/crosscore/.

Expansion Interface

The expansion interface consists of three 90-pin connectors (J1–3). These connectors contain a majority of the ADSP-BF527 processor's signals. For the pinout of the connectors, go to "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1. The expansion interface allows an EZ-Extender or a custom-design daughter board to be tested across various hardware platforms. The mechanical dimensions of the expansion connectors can be obtained by contacting Technical or Customer Support.

Analog Devices offers many EZ-Extender products. For more information about EZ-Extenders, visit the Analog Devices Web site at: http://www.analog.com/processors/blackfin/evaluationDevelopment/crosscore/.

Limits to current and interface speed must be taken into consideration when using the expansion interface. Current for the expansion interface is sourced from the EZ-KIT Lite; therefore, the current should be limited to 1A for both the 5V and 3.3V planes. If more current is required, then a

separate power connector and a regulator must be designed on a daughter card. Additional circuitry can add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

Power Measurements

Several locations are provided for measuring the current draw from various power planes. Precision 0.05 ohm shunt resistors are available on the VDDINT, VDDEXT, and VDDMEM pins. For current draw measuments, the associated jumper (P14, P15, or P16) should be removed. Once the jumper is removed, voltage across the resistor can be measured using an oscilloscope. Once voltage is measured, current can be calculated by dividing the voltage by 0.05. For the highest accuracy, a differential probe should be used for measuring the voltage across the resistor.

For more information, see "VDDINT Power Jumper (P14)", "VDDEXT Power Jumper (P15)", and "VDDMEM Power Jumper (P16)" on page 2-23.

Power-On-Self Test

The power-on-self program (POST) tests all EZ-KIT Lite peripherals, validates functionality, as well as connectivity to the processor. Once assembled, each EZ-KIT Lite is fully tested for an extended period of time with a POST. All boards are shipped with the POST pre-loaded into parallel flash (U5) and SPI flash (U8) memories. The POST is executed by resetting the board and pressing the proper push button(s). The POST also can be used for reference in a custom software design or hardware troubleshooting.

When running the POST, you may need to place switches and jumpers in specific test modes. In some instances, such as Ethernet, you may need to plug in an Ethernet loopback connector (provided with the EZ-KIT Lite) to run the POST. The user LEDs (LED1–3) will convey whether the specific tests have passed or failed.

The source code for the POST program is included in the EZ-KIT Lite installation directory of VisualDSP++ along with the readme file, which describes how the board is configured to run a POST.

Example Programs

Example programs are provided with the ADSP-BF527 EZ-KIT Lite to demonstrate various capabilities of the product. The programs are installed with the VisualDSP++ software and can be found in the *<install_path>*\Blackfin\Examples\ADSP-BF527 EZ-KIT Lite directory. Refer to a readme file provided with each example for more information.

Background Telemetry Channel

The USB debug agent supports the background telemetry channel (BTC), which facilitates data exchange between VisualDSP++ and the processor without interrupting processor execution.

The BTC allows you to read and write data in real time while the processor continues to execute. For increased performance of the BTC, including faster reading and writing, please check our latest line of processor emulators at: http://www.analog.com/processors/blackfin/evaluationDevelopment/crosscore/. For more information about BTC, see the online Help.

Reference Design Information

A reference design info package is available for download on the Analog Devices Web site. The package provides information on the design, layout, fabrication, and assembly of the EZ-KIT Lite and EZ-Board products.

The information can be found at:
http://www.analog.com/en/embedded-processing-dsp/content/reference_designs/fca.html.

2 ADSP-BF527 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF527 EZ-KIT Lite board.

The following topics are covered.

- "System Architecture" on page 2-2
  Describes the ADSP-BF527 EZ-KIT Lite board configuration and explains how the board components interface with the processor.
- "Programmable Flags" on page 2-3
  Shows the locations and describes the programming flags (PFs).
- "Push Buttons and Switches" on page 2-10
  Shows the locations and describes the on-board push buttons and switches.
- "Jumpers" on page 2-20
  Shows the locations and describes the on-board configuration jumpers.
- "LEDs" on page 2-23
  Shows the locations and describes the on-board LEDs.
- "Connectors" on page 2-25
  Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board (Figure 2-1).

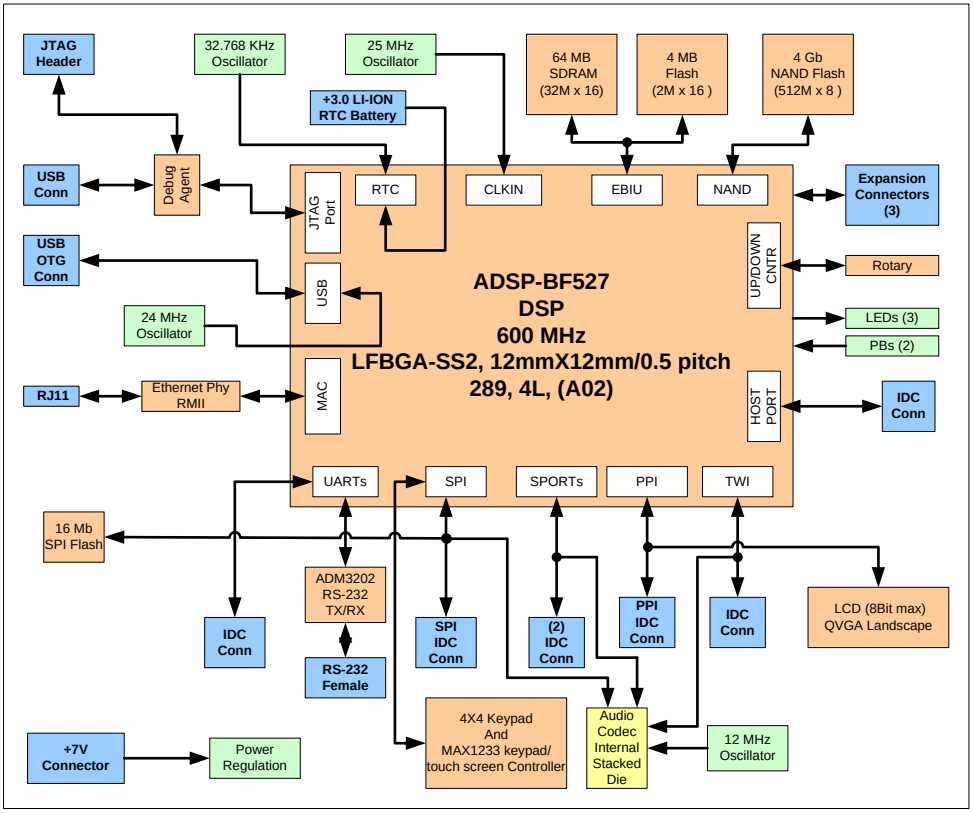


Figure 2-1. System Architecture

The EZ-KIT Lite is designed to demonstrate the capabilities of the ADSP-BF527 processors. The processor has an I/O voltage of 3.3V. The core voltage of the processor is controlled by the internal voltage regulator.

The core voltage and clock rate can be set on the fly by the processor. The input clock is 25 MHz. A 32.768 kHz crystal supplies the real-time clock (RTC) inputs of the processor. The default boot mode for the processor is external parallel flash boot. See "Boot Mode Select Switch (SW2)" on page 2-11 for information on how to change the default boot mode.

Programmable Flags

The processor has 50 general-purpose input/output (GPIO) signals spread across four ports (PF, PG, PH, and PJ). The pins are multi-functional and depend on the ADSP-BF527 processor setup. The following tables show how the programmable flag pins are used on the EZ-KIT Lite.

- PF programmable flag pins – Table 2-1
- PG programmable flag pins – Table 2-2
- PH programmable flag pins – Table 2-3
- PJ programmable flag pins – Table 2-4

Table 2-1. PF Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PF0	PPID0/DR0PRI/ND_D0A	Default: LCD via U31 buffer. Expansion interface J1.72, PPI connector P8.8.
PF1	PPID1/RFS0/ND_D1A	Default: LCD via U31 buffer. Expansion interface J1.73, PPI connector P8.9.
PF2	PPID2/RSCLK0/ND_D2	Default: LCD via U31 buffer. Expansion interface J1.74, PPI connector P8.10.
PF3	PPID3/DT0PRI/ND_D3A	Default: LCD via U31 buffer. Expansion interface J1.75, PPI connector P8.11.
PF4	PPID4/TFS0/ND_D4A/TACLK0	Default: LCD via U31 buffer. Expansion interface J2.43, PPI connector P8.12.

Table 2-1. PF Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PF5	PPID5/TSCLK0/ND_D5A/TACLK1	Default: LCD via U31 buffer. Expansion interface J2.44, PPI connector P8.13.
PF6	PPID6/DT0SEC/ND_D6A/TACI0	Default: LCD via U31 buffer. Expansion interface J2.45, PPI connector P8.14.
PF7	PPID7/DR0SEC/ND_D7A/TACI1	Default: LCD via U31 buffer. Expansion interface J2.46, PPI connector P8.15.
PF8	PPID8/DR1PRI	Default: LED0. Expansion interface J1.79, J2.29, J2.47, via quick switch U34 to the following connectors: VPP board P4.2, SPORT0 P6.25, SPORT1 P7.8, SPI P9.14, TWI P10.10, and PPI P8.24.
PF9	PPID9/RSCLK1/SPISEL6#	Default: KEYIRQ (U16) via SW5.2. Expansion interface J2.48, J2.33, SPORT1 connector P7.16, and PPI connector P8.17.
PF10	PPID10/PRFS1/SPISEL7#	Default: PENIRQ (U16) via SW5.1. RTS UART1 U25 via SW10.3, expansion interface J2.31, J2.49, SPORT1 connector P7.7, and PPI connector P8.18.
PF11	PPID11/TFS1/CZM	Default: CZM rotary (SW3) via SW11.3. Expansion interface J2.32, J2.50, via quick switch U34 to the following connectors: PPI P8.19, SPORT1 P7.11.
PF12	PPID12/DT1PRI/SPISEL2#/CDG	Default: CDG rotary (SW3) via SW11.2. SPISEL2# keypad/touchscreen controller via SW18.1, expansion interface J2.30, J2.51, via quick switch U30 to the following connectors: SPI P9.9, SPORT1 P7.14 and P7.19, PPI P8.20 and P8.26, SPORT0 P6.19.
PF13	PPID13/TSCLK1/SPISEL3#/CUD	Default: CUD rotary (SW3) via SW11.1. Expansion interface J2.34, J2.52, via quick switch U34 to the following connectors: SPORT1 P7.6 and P7.21, SPORT0 P6.21, PPI P8.21 and P8.25, SPI P9.12.

Table 2-1. PF Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PF14	PPID14/DT1SEC/UART1TX	Default: UART1 (U25) TX. Expansion interface J2.28, J2.53, J2.55, J3.8, SPORT1 connector P7.12, and PPI connector P8.22.
PF15	PPID15/DR1SEC/UART1RX /TACI3	Default: UART1 (U25) RX via SW10.2. Expansion interface J2.27, J2.54, J2.56, J3.7, SPORT1 connector P7.10, and PPI connector P8.23

Table 2-2. PG Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PG0	HWAIT	Default: PB1 via SW13.1. UART1 CTS (HWAIT) via JP1 and SW10.1, KEYPAD_BUSY via SW13.1 OFF and SW13.5 ON. Host connector P13.12, and expansion interface J1.84.
PG1	SPISS#/SPISEL1#	Default: SPI flash (U8) CS via SW9.4. Expansion interface J2.11, via quick switch U30 to the following connectors: SPI P9.10, PPI P8.27, SPORT0 P6.17, and SPORT1 P7.17.
PG2	SPISCK	Default: SPI flash (U8), codec (U2) via SW19.3, keypad/touch-screen controller (U16). Expansion interface J2.9, via quick switch U30 to the following connectors: SPI P9.8, SPORT0 P6.22, SPORT1 P7.22, and PPI P8.34.
PG3	SPIMISO/DR0SECA	Default: SPI flash (U8), keypad/touchscreen controller (U16). Via quick switch (U30) to the following connectors: SPI P9.6, SPORT0 P6.10 and P6.20, SPORT1 P7.20, and PPI P8.32, and expansion interface J2.12, J2.35.
PG4	SPIMOSI/DT0SECA	Default: SPI flash (U8), codec (U2) via SW19.1, keypad/touchscreen controller (U16). Via quick switch (U30) to the following connectors: SPORT0 P6.12 and P6.18, SPORT1 P7.18, SPI P9.5, PPI P8.30, and expansion interface J2.10, J2.36.

Table 2-2. PG Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PG5	TMR1/PPIFS2/TFS0A	Default: LCD via buffer (U32). PPI connector P8.33, expansion interface J2.24.
PG6	DT0PRIA/TMR2/PPIFS3	Default: SPORT0 audio codec (U2) via SW20.2. PPI connector P8.29, SPORT0 connector P6.14, Expansion interface J2.38, J2.23.
PG7	TMR3/DR0PRIA/UART0TX	Default: SPORT0 audio codec (U2) via SW20.3. Via quick switch (U34) to the following connectors: UART0 P5.6, SPORT0 P6.8 and P6.28, SPORT1 P7.28, Timers P11.6, and expansion interface J2.37, J3.6.
PG8	TMR4/RFS0A/UART0RX/TACI4	Default: SPORT0 audio codec (U2) via SW20.4. Via quick switch (U34) to the following connectors: SPORT0 P6.7 and P6.30, SPORT1 P7.30, Timers P11.8, UART0 P5.10, and expansion interface J2.39, J3.5.
PG9	TMR5/RSCLK0A/TACI5	Default: SPORT0 audio codec (U2) via SW17.2. Via quick switch (U34) to the following connectors: SPORT0 P6.32 and P6.16, SPORT1 P7.32, Timers P11.10, and expansion interface J2.41.
PG10	TMR6/TSCLK0A/TACI6	Default: SPORT0 audio codec (U2) via SW17.1. SPORT0 connector P6.6, expansion interface J2.42.
PG11	TMR7/HOST_WR#	Default: LED1. LCD GPIO reset via SW5.3, host connector P13.4, via quick switch to the following connectors: SPORT0 P6.27, UART0 P5.3, SPORT1 P7.29, TWI P10.9, Timers P11.3, SPI P9.15, and expansion interface J1.80.
PG12	DMAR1/UART1TXA/HOST_ACK	Default: LED2. PPI_SEL via SW13.4, host connector P13.10, via quick switch (U34) to the following connectors: UART0 P5.5, Timers P11.5, TWI P10.12, SPORT0 P6.29, SPORT1 P7.31, SPI P9.16, and expansion interface J1.81.

Table 2-2. PG Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PG13	DMAR0/UART1RXA/HOST_ADDR/TACI2	Default: PB2 via SW13.2. OTG USB_VRSEL via SW13.6 ON and SW13.2 OFF, host connector P13.8, and expansion interface J1.85.
PG14	TSCLK0A/MDC/HOST_RD#	Default: host connector P13.2.13.6 MDIO PHY (U14) via SW1.2, expansion interface J3.41
PG15	TFS0A/MIIPHY-INT#/RMIIM-DINT#/HOST_CE#	Default: SPORT0 audio codec (U2) via SW20.1 RMIIMDINT# PHY (U14), host connector P13.6, SPORT0 connector P6.11, and expansion interface J2.40, J3.31.

Table 2-3. PH Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PH0	ND_D0/MIICRS/RMII-CRSDV/HOST_D0	Default: NAND Data 0 (U4). RMII carrier sense/receive data valid (U14.36), host connector data 0 (P13.31), and expansion interface (J3.40).
PH1	ND_D1/ERXER/HOST_D1	Default: NAND Data 1 (U4). PHY receive error (U14.21), host connector data 1 (P13.29), expansion interface (J3.39).
PH2	ND_D2/MDIO/HOST_D2	Default: NAND Data 2 (U4). PHY management bus MDIO via SW1.1, host connector data 2 (P13.27), and expansion interface (J3.42).
PH3	ND_D3/ETXEN/HOST_D3	Default: NAND Data 3 (U4). PHY transmit enable (U14.6), host connector data 3 (P13.25), and expansion interface (J3.15).
PH4	ND_D4/MIITX-CLK/RMIIREF_CLK/HOST_D4	Default: NAND Data 4 (U4). PHY RMII ref clock (U14.14) via SW1.3 OFF, oscillator output U24, host connector data 4 (P13.23), and expansion interface (J3.16).
PH5	ND_D5/ETXD0/HOST_D5	Default: NAND Data 5 (U4). PHY RMII transmit data 0 (U14.23), host connector data 5 (P13.21), and expansion interface (J3.11).

Table 2-3. PH Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PH6	ND_D6/ERXD0/HOST_D6	Default: NAND Data 6 (U4). PHY RMII receive data 0 (U14.18), PHY mode via SW9.3, host connector data 6 (P13.19), and expansion interface (J3.33).
PH7	ND_D7/ETXD1/HOST_D7	Default: NAND Data 7 (U4). PHY RMII transmit data 1 (U14.24), host connector data 7 (P13.17), and expansion interface (J3.12).
PH8	SPISEL4#/ERXD1/HOST_D8/TACLK2	Default: NAND Data 7 (U4). PHY RMII transmit data 1 (U14.24), keypad/touch-screen chip select via SW18.2, host connector data 8 (P13.17), and expansion interface (J3.12).
PH9	SPISEL5#/ETXD2/HOST_D9/TACLK3	Default: SPI SEL5 audio codec U2. Chip select keypad/touchscreen controller via resistors (U16), host connector data 9 (P13.13), and expansion interface (J3.13).
PH10	ND_CE#_ERXD2/HOST_D10	Default: NAND chip enable via SW11.4 ON. Host connector data 10 (P13.17) and expansion interface (J3.35).
PH11	ND_WE/ETXD3/HOST_D11	Default: NAND write enable (U4). Host connector data 11 (P13.9) and expansion interface (J3.14).
PH12	ND_RE/ERXD3/HOST_D12	Default: NAND output enable (U4). Host connector data 12 (P13.7), expansion interface (J3.36).
PH13	ND_BUSY/ERXCLK/HOST_D13	Default: NAND busy (U4). Host connector data 13 (P13.5), expansion interface (J3.38).
PH14	ND_CLE/ERXDV/HOST_D14	Default: NAND command latch enable (U4). Host connector data 14 (P13.3), expansion interface (J3.37).
PH15	ND_ALE/COL/HOST_D15	Default: NAND address latch enable (U4). Host connector data 15 (P13.1), expansion interface (J3.32).

Table 2-4. PJ Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-KIT Lite Function
PJ0	PPIFS1/TMR0	Default: PPI frame sync 1 via buffer U32 to LCD conn (P12) and CPLD U33. PPI connector (P8.31) and expansion interface (J2.25).
PJ1	PPICLK/TMRCLK	Default: PPI clock via buffer U32 to LCD conn (P12) and CPLD U33. Output of switch (U20), PPI connector (P8.6), and expansion interface (J1.71).
PJ2	SCL	Default: not used. Codec via SW19.4, expansion interface (J2.57), the following connectors via quick switch (U30): TWI (P10.5), PPI (P8.38), SPORT0 (P6.26), and SPORT1 (P7.26).
PJ3	SDA	Default: not used. Codec via SW19.4, expansion interface (J2.58), the following connectors via quick switch (U30): TWI (P10.6), PPI (P8.36), SPORT0 (P6.24), and SPORT1 (P7.24).

Push Buttons and Switches

This section describes operation of the push buttons and switches. The push button and switch locations are shown in Figure 2-2.

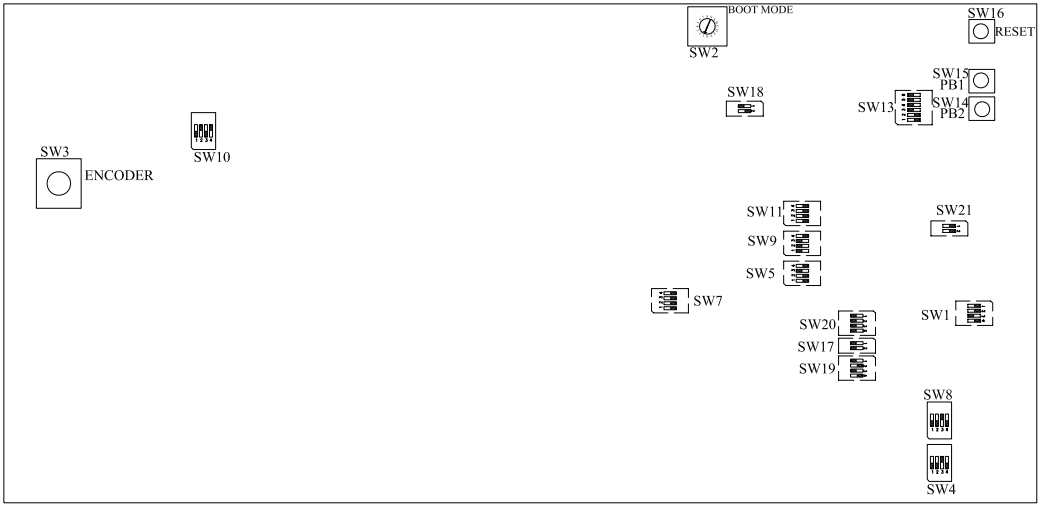


Figure 2-2. Push Button and Switch Locations

ETH Enable Switch (SW1)

The Ethernet enable switch (SW1) allows the Ethernet to operate. Ethernet and NAND flash share the same lines and cannot operate at the same time. The SW1 default settings are OFF, OFF, ON, OFF (see Table 2-5). Ethernet is enabled by setting the switch to ON, ON, OFF, ON. SW1 positions 1 and 2 connect the management bus (MDIO and MDC); SW1 position 3 enables the 50 MHz RMII clock; and SW1 position 4 holds the PHY in reset (set to OFF) or connects the PHY reset to the EZ-KIT Lite reset (set to ON).

Table 2-5. ETH Enable Switch (SW1)

SW1 Switch Setting	Ethernet Mode
OFF, OFF, ON, OFF	**OFF (default)**
ON, ON, OFF, ON	ON

Boot Mode Select Switch (SW2)

The rotary switch (SW2) determines the boot mode of the processor. Table 2-6 shows the available boot mode settings. By default, the ADSP-BF527 processor boots from the on-board parallel flash memory.

The selected position of SW2 is marked by the notch down the entire rotating portion of the switch, not the small arrow.

Table 2-6. Boot Mode Select Switch (SW2)

SW2 Position	Processor Boot Mode
0	Reserved
1	**Boot from 8-bit external flash memory (default)**
2	Boot from 16-bit asynchronous FIFO
3	Boot from serial SPI memory
4	Boot from SPI host device
5	Boot from serial TWI memory
6	Boot from TWI host
7	Boot from UART0 host
8	Boot from UART1 host
9	Reserved
A	Boot from SDRAM
B, C, D	Reserved

Table 2-6. Boot Mode Select Switch (SW2) (Cont'd)

SW2 Position	Processor Boot Mode
E	Boot from 16-bit host DMA
F	Boot from 8-bit host DMA

Rotary Encoder with Momentary Switch (SW3)

The rotary encoder (SW3) can be turned clockwise for an up count or counter-clockwise for a down count. The encoder also features a momentary switch, activated by pushing down the switch and setting the counter to zero. The rotary encoder is a two-bit quadrature (Gray code) encoder. Refer to the "Rotary Counter" section of the *ADSP-BF52x Hardware Reference Manual* for additional information about interfacing with this style rotary encoder.

The rotary encoder can be disconnected from the processor by setting the rotary enable switch SW11 positions 1, 2 and 3 to OFF. See "Rotary NAND Enable Switch (SW11)" on page 2-16 for more information.

MIC Gain Switch (SW4)

The microphone gain switch (SW4) sets the gain of the MIC signal, which is connected to the top 3.5 mm jack (J7). The gain can be set to 14 dB, 0 dB, or –6 dB by turning ON position 1, 2 or 3 of the switch (see Table 2-7). When the corresponding position for the desired gain is ON, the remaining positions should be OFF. Refer to "Audio Interface" on page 1-21 for more information on the audio codec.

Table 2-7. MIC Gain Switch (SW4)

Gain	SW4 Switch Settings
5 (14 dB)	ON, OFF, OFF, OFF
1 (0 dB)	OFF, ON, OFF, OFF

Table 2-7. MIC Gain Switch (SW4) (Cont'd)

Gain	SW4 Switch Settings
0.5 (–6 dB)	**OFF, OFF, ON, OFF (default)**
Unused	OFF, OFF, OFF, OFF

Keypad LCD Enable Switch (SW5)

The keypad LCD enable switch (SW5) connects the interrupt request signals PENIRQ and KEYIRQ to the MAX1233 keypad and touchscreen controller (U16) on positions 1 and 2 (see Table 2-8). Positions 3 and 4 of SW5 control the LCD reset line connection, selecting between GPIO (SW5 position 3 ON, position 4 OFF) or the board reset (SW5 position 3 OFF, position 4 ON). Note that the GPIO reset line shares the pin with the HOSTWR# and LED1 signals. The default setting is ON, ON, OFF, ON.

Table 2-8. Keypad LCD Enable Switch (SW5)

SW5 Position (Default)	From	To	Function
1 (ON)	DSP (U2, PF10)	Keypad IC (U16)	OFF (SW10.3 used as GPIO RTS of UART1, expansion interface J2.31, J2.49, SPORT1 conn P7.7, PPI conn P8.18)
2 (ON)	DSP (U2, PF9)	Keypad IC (U16)	OFF (expansion interface pins: J2.33 J2.48, SPORT1 conn P7.16, PPI conn P8.17)
3 (OFF)	DSP (U2, PG11)	LCD conn (P12)	ON (GPIO control of LCD_RESET), OFF (host conn P13.4, LED1, expansion interface J1.80, STAMP buffer U34.15)
4 (ON)	RESET IC (U27)	LCD conn (P12)	OFF (LCD not connected to board reset)

Flash Enable Switch (SW7)

The flash enable switch (SW7) disconnects ~AMS signals from flash memory, allowing other devices to utilize the signals via the expansion interface. For each switch listed in Table 2-9 that is turned OFF, the size of available flash memory is reduced by 1 MB.

Table 2-9. Flash Enable Switch (SW7)

SW7 Switch Position (Default)	Processor Signal
1 (ON)	~AMS0
2 (ON)	~AMS1
3 (ON)	~AMS2
4 (ON)	~AMS3

Mic/HP LPBK Audio Mode Switch (SW8)

The SW8 switch allows the EZ-KIT Lite to be placed in loopback mode to test for signal/circuit continuity and functionality (see "Power-On-Self Test" on page 1-27). SW8 positions 1 and 2 connect the MICIN signal to the headphone left and right outputs for audio loopback. Do not turn SW8 positions 1 and 2 ON at the same time.

SW8 positions 3 and 4 select the control interface for the audio codec. SW8 position 3 ON and 4 OFF select SPI interface, while position 3 OFF and position 4 ON select TWI mode. The SW8 default settings are OFF, OFF, ON, OFF. See "SPI/TWI Switch (SW19)" on page 2-19 for more information.

ETH Mode Flash CS Switch (SW9)

The Ethernet mode flash CS switch (SW9) sets the bootstrapping options for the LAN8700 RMII PHY chip (U14). Table 2-10 shows the SW9 default as well as the alternate switch settings.

SW9 position 4 disconnects SPISEL1 from the SPI flash chip (U8). Setting SW9 position 4 OFF is useful when using SPISEL1 on the expansion interface at connector J2 pin 11. SW9 position 4 is ON by default.

Table 2-10. ETH Mode Flash CS Switch (SW9)

SW9 Switch Setting	MODE[2:0] Setting	Mode Definitions
ON, ON, ON	**111**	**All capable, auto negotiation (default)**
ON, ON, OFF	110	Power down mode
ON, OFF, ON	101	Repeater mode, auto negotiation
ON, OFF, OFF	100	100Base-TX half duplex advertised, auto negotiation
OFF, ON, ON	011	100Base-TX full duplex
OFF, ON, OFF	010	100Base-TX half duplex
OFF, OFF, ON	001	10Base-T full duplex
OFF, OFF, OFF	000	10Base-T half duplex

UART Enable Switch (SW10)

The UART enable switch (SW10) disconnects the UART1 signals from the GPIO pins of the processor. When SW10 is OFF, its associated GPIO signals can be used for other functions on the board. SW10 default is OFF, ON, OFF, ON. Flow control is not implemented in POST, so SW10 positions 1 and 3 are OFF. Refer to the ADM3202 datasheet for more information about the UART interface.

Rotary NAND Enable Switch (SW11)

The rotary NAND enable switch (SW11) disconnects the rotary encoder signals from the GPIO pins of the processor. When SW11 is OFF, its associated GPIO signals can be used on the host interface (see Table 2-11). Position 4 of SW11 disconnects the chip enable for NAND flash memory (U4).

Table 2-11. Rotary NAND Enable Switch (SW11)

SW11 Position (Default)	From	To	Alternate Function/OFF Mode
1 (ON)	Encoder (SW3)	DSP (U2, PF13)	Expansion interface (J2.34, J2.52) STAMP buffer (U34)
2 (ON)	Encoder (SW3)	DSP (U2, PF12)	CS audio codec (U2), CS keypad/touch controller (U16), expansion interface (J2.30, J2.51), STAMP buffer (U30)
3 (ON)	Encoder (SW3)	DSP (U2, PF11)	Expansion interface (J2.32, J2.50), STAMP buffer (U34)
4 (ON)	DSP (U2, PH10)	NAND (U4)	Host connector (P13.11), expansion interface (J3.35)

GPIO Enable Switch (SW13)

The general-purpose input/output (GPIO) switch (SW13) disconnects the associated push buttons and LED circuits from the GPIO pins of the processor and allows the signals to be used for other functions. Depending on the switch configuration, the signals can be used as PPI clock select, keypad_busy, or OTG host mode 5V select (see Table 2-12).

To select an on-board or external PPI clock through software, set SW13 position 4 ON. Drive the PG12 programmable flag to low (0) to connect an external expansion interface clock. Drive PG12 high to select the on-board PPI oscillator. By default, SW13 position 4 is OFF and the PPI clock source is on-board.

Table 2-12. GPIO Enable Switch (SW13)

SW13 Position (Default)	From	To	Function
1 (ON)	Push button 1	DSP (U2, PG0)	ON (PB1), OFF (UART1 CTS U25, host connector P13.12, keypad busy SW13.8, expansion interface J1.84)
2 (ON)	Push button 2	DSP (U2, PG13)	ON (PB2), OFF (host connector P13.8, OTG voltage select SW13.7, expansion interface J1.85)
3 (OFF)			NC
4 (OFF)	DSP (U2, PG12)	PPI CLK (U20)	OFF (LED2, host connector P13.10, expansion interface J1.81, STAMP buffer U34), ON (PPI CLK U20)
5 (OFF)	Keypad BUSY (U16)	DSP (U2, PG0)	OFF (PB1, UART1 CTS U25, host conn P13.12, expansion interface J1.84), ON (GPIO keypad busy U16, SW13.1)
6 (OFF)	OTG PWR (VR3, U28)	DSP (U2, PG13)	OFF (host connector P13.8, expansion interface J1.85), ON (PB2 SW13.11, OTG power VR3, U28)

The USB_VRSEL signal is used to provide 5V to a device connected over the USB OTG interface when running in host mode. Signal USB_VRSEL is connected by setting SW13 position 2 OFF and position 6 ON. Then the PG13 programmable flag pin of the processor can be used to control the 5V regulator (VR3). Refer to "USB OTG Interface" on page 1-22 for more information.

The PG0 PF pin of the processor can be used as GPIO or other functions if SW13 position 1 is turned OFF. Turning SW13 position 1 OFF and position 5 ON allows the keypad_busy signal to connect to the processor from the keypad and touchscreen controller (U16). SW13 default settings are ON, ON, OFF, OFF, OFF, OFF.

Programmable Flag Push Buttons (SW14–15)

Two momentary push buttons (SW14-15) are provided for general-purpose user input. The buttons connect to the PG0 and PG13 GPIO pins of the processor. The push buttons are active high and, when pressed, send a high (1) to the processor. The GPIO enable switch (SW13) disconnects the push buttons from the corresponding PB signal. Refer to "GPIO Enable Switch (SW13)" on page 2-16 for more information.

Reset Push Button (SW16)

The reset push button (SW16) resets the following ICs.

- processor (U2), parallel flash (U5), PHY (U14) if SW1 position 4 is ON
- LCD (P12) if SW5 position 3 is OFF and 4 is ON
- CPLD (U33)

The reset push button does not reset the following ICs.

- SDRAM (U7), NAND flash (U4), SPI flash (U8)
- audio codec (U2), keypad/touchscreen controller (U16)
- UART1 (U25)

The reset push button does not reset the debug agent once it has been connected to a PC. The USB chip is not reset when the push button is pressed after the USB cable has been plugged in and communication with the PC has been initialized correctly. After USB communication has been initialized, the only way to reset the USB chip is by powering down the board.

SPORT0A ENBL Switches (SW17 and SW20)

The SPORT0A enable switches (SW17 and SW20) connect the SPORT0A interface of the processor to the audio codec. When the SPORT0A interface is needed at the expansion interface, turn SW17 and SW20 all OFF. The SW17 or SW20 switches are all ON by default.

KEY/PEN CS Switch (SW18)

The KEY/PEN CS switch (SW18) enables the chip select for the MAX1233 touchscreen controller to be connected to either signal: SPISEL2 (ON, OFF) or SPISEL4 (OFF, ON). SPISEL4 is one function on a multiplexed pin of PF PH8. When using the PH8 programmable flag pin as SPISEL4, signals ERXD1 and HOSTD8 do not operate as Ethernet and host data pins.

SPI/TWI Switch (SW19)

The SPI/TWI switch (SW19) selects the control interface for the audio codec. SW19 default is ON, OFF, ON, OFF, which selects SPI interface. TWI is selected by setting the SW19 switch to OFF, ON, OFF, ON. See "Mic/HP LPBK Audio Mode Switch (SW8)" on page 2-14 for more information on how to setup the audio mode.

TFS0A/HOSTCE Enable Switch (SW21)

The TFS0A/HOSTCE enable switch (SW21) disconnects the PG15 programmable flag signal TFS0A_RMIIMDINT#_HOSTCE# from the SPORT0 (position 1) connector P6 pin 11 and the host connector (position 2) P13 pin 6. SW21 is OFF, OFF by default.

Jumpers

This section describes functionality of the configuration jumpers. Figure 2-3 shows the jumper locations.

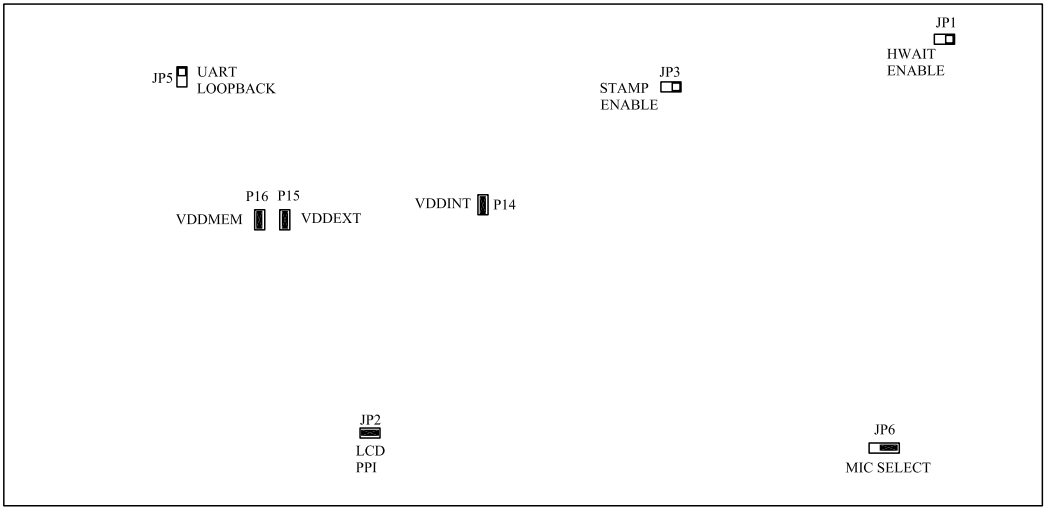


Figure 2-3. Configuration Jumper Locations

HWAIT Enable Jumper (JP1)

The HWAIT enable jumper (JP1) connects processor signal HWAIT_PUSHBUTTON1, PF PG0, to SW10 position 1. SW10 position 1 then connects to the transmit 2 input of the UART1 IC (U25). This allows the implementation of flow control functionality CTS through the HWAIT signal of the processor. Install JP1 if implementing flow control. JP1 is uninstalled by default.

LCD PPI Jumper (JP2)

The PPI port connects to the LCD through two buffers (U31-32). JP2 enables both buffers when installed and drives PPI signals to LCD connector (P12). Removing JP2 is useful when using the PPI at the PPI connector (P8) or expansion interface. JP2 is installed by default.

STAMP Enable Jumper (JP3)

The STAMP connectors have a number of nets connected by enabling quick switches at locations U30 and U34. When installed, the STAMP enable jumper (JP3) enables the quick switches. Table 2-13 lists the signals that are connected when JP3 is installed. JP3 is uninstalled by default.

Table 2-13. STAMP Enable Jumper (JP3)

STAMP Signals Connected through Quick Switches U30 and U34	
SCL	DROPRIA
SDA	RFSOA
SPISCK	CZM
SPISEL1	CUD
SPISEL2#_CDG	LEDO
SPIMISO	HOSTWR#_LED1
SPIMOSI	HOSTACK_LED2
RSCLKOA	

UART1 Loopback Jumper (JP5)

The UART1 loopback jumper (JP5) is used to place the UART1 port of the processor in a loopback condition. The jumper connects the UART1_TX line of the processor to the UART1_RX signal of the processor. The jumper is required when the power-on-self-test (POST) is run to test the serial port interface. The default setting is uninstalled.

MIC Select Jumper (JP6)

The MIC select jumper (JP6) connects the MICBIAS signal to the MICIN (JP6 on 1 and 2) or connects MICBIAS to the 3.5 mm connector J7 (JP6 on 2 and 3). The default setting is JP6 installed on 2 and 3.

VDDINT Power Jumper (P14)

The VDDINT power jumper (P14) is used to measure the core voltage and current supplied to the processor core. P14 is ON by default, and the power flows through the two-pin IDC header. To measure power, remove the jumper and measure the voltage across the 0.05 ohm resistor. Once the voltage is measured, the power can be calculated. For more information, refer to "Power Measurements" on page 1-27.

VDDEXT Power Jumper (P15)

The VDDEXT power jumper (P15) is used to measure the processor's I/O voltage and current. JP15 is ON by default, and the power flows through the two-pin IDC header. To measure power, remove the jumper and measure the voltage across the 0.05 ohm resistor. Once the voltage is measured, the power can be calculated.

VDDMEM Power Jumper (P16)

The VDDMEM power jumper (P16) is used to measure the voltage and current supplied to the memory interface of the processor. P16 is ON by default, and the power flows through the two-pin IDC header. To measure power, remove the jumper and measure the voltage across the 0.05 ohm resistor. Once the voltage is measured, the power can be calculated.

LEDs

This section describes the on-board LEDs. Figure 2-3 shows the LED locations.

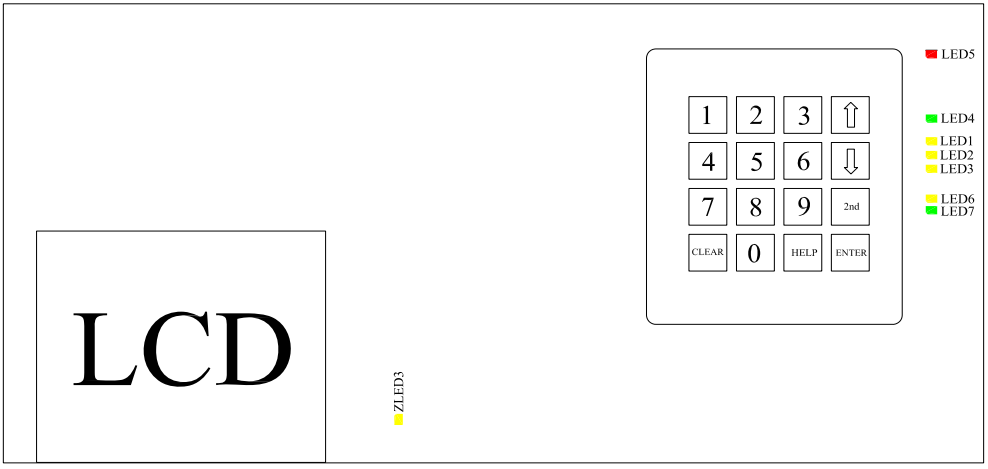


Figure 2-4. LED Locations

User LEDs (LED1–3)

Three LEDs connect to three general-purpose I/O pins of the processor (see Table 2-14). The LEDs are active high and are lit by writing a 1 to the correct PF signal.

Table 2-14. User LEDs

LED Reference Designator	Processor Programmable Flag Pin
LED1	PF8
LED2	PG11
LED3	PG12

Power LED (LED4)

When LED4 is lit (green), it indicates that power is being properly supplied to the board.

Reset LED (LED5)

When LED5 is lit, it indicates that the master reset of all major ICs is active. The reset LED is controlled by the Analog Devices ADM708 supervisory reset circuit. You can assert the reset push button (SW16) to assert a master reset and to activate LED5. For more information, see “Reset Push Button (SW16)” on page 2-18.

Ethernet LEDs (LED6–7)

When LED6 is lit solid, it indicates that the SMSC LAN8700 chip (U14) detects a valid link. When transmit or receive activity is sensed, LED7 flashes as an activity indicator. For more information on the LEDs, refer to the LAN8700 chip datasheet provided by the product manufacturer.

Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in Figure 2-5.

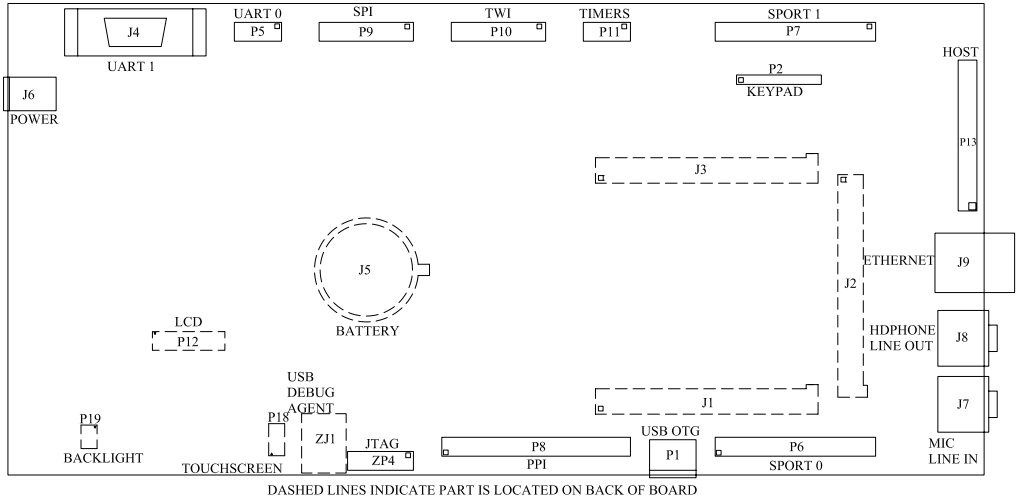


Figure 2-5. Connector Locations

Expansion Interface Connectors (J1–3)

Three board-to-board connector footprints provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information, see "Expansion Interface" on page 1-26. For availability and pricing of the `J1-3` connectors, contact Samtec.

Part Description	Manufacturer	Part Number
90-position 0.05" spacing, SMT	SAMTEC	SFC-145-T2-F-D-A
Mating Connector		
90-position 0.05" spacing (through hole)	SAMTEC	TFM-145-x1 series
90-position 0.05" spacing (surface mount)	SAMTEC	TFM-145-x2 series
90-position 0.05" spacing (low cost)	SAMTEC	TFC-145 series

RS-232 Connector (J4)

Part Description	Manufacturer	Part Number
DB9, female, vertical mount	NORCOMP	191-009-213-L-571
Mating Cable		
2m female-to-female cable	DIGI-KEY	AE1020-ND

Battery Holder (J5)

Part Description	Manufacturer	Part Number
24 mm battery holder	KEYSTONE	105
Mating Battery (shipped with EZ-KIT Lite)		
3V 280MAH 24 mm LI-COIN	SANYO	CR2430

Power Connector (J6)

The power connector (J6) provides all of the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm power jack	SWITCHCRAFT	RAPC712X
Mating Power Supply (shipped with EZ-KIT Lite)		
7.0VDC@2.14A power supply	CUI INC	DMS070214-P6P-SZ

Dual Audio Connectors (J7–8)

Part Description	Manufacturer	Part Number
3.5 mm dual stereo jack	SWITCHCRAFT	35RAPC7JS
Mating Cable (shipped with EZ-KIT Lite)		
3.5 mm male/male 6' cable	RANDOM	10A3-01106
Mating Headphone (shipped with EZ-KIT Lite)		
3.5 mm stereo headphones	KOSS	151225 UR5

Ethernet Connector (J9)

Part Description	Manufacturer	Part Number
RJ-45 Ethernet jack	STEWART	SS-6488-NF
Mating Cable (shipped with EZ-KIT Lite)		
Cat 5E patch cable	RANDOM	PC10/100T-007

USB OTG Connector (P1)

The pinout of the `P1` connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
USB 5-pin mini AB	MOLEX	56579-0576
Mating Cables (shipped with EZ-KIT Lite)		
5-in-1 USB 2.0 cable	JO-DAN INTERNAT	GXQU-06

Keypad Connector (P2)

Part Description	Manufacturer	Part Number
IDC header female	SAMTEC	SSW-109-01-TM-S
Mating Keypad (shipped with EZ-KIT Lite)		
4 x 4 keypad	ACT COMPONENTS	ACT-07-30008-000-R

VPP Board Connector (P4)

The VPP board connector (P4) is not populated and is for testing purposes only, not intended for use.

UART0 Connector (P5)

The pinout of the P5 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-410HLF
Mating Connector		
IDC socket	DIGI-KEY	S4205-ND

SPORT0 Connector (P6)

The pinout of the P6 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-434HLF
Mating Connector		
IDC socket	DIGI-KEY	S4217-ND

SPORT1 Connector (P7)

The pinout of the P7 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-434HLF
Mating Connector		
IDC socket	DIGI-KEY	S4217-ND

PPI Connector (P8)

The pinout of the P8 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-440HLF
Mating Connector		
IDC socket	DIGI-KEY	S4220-ND

SPI Connector (P9)

The pinout of the P9 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-420HLF
Mating Connector		
IDC socket	DIGI-KEY	S4210-ND

Two-Wire Interface Connector (P10)

The pinout of the P10 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-420HLF
Mating Connector		
IDC socket	DIGI-KEY	S4210-ND

TIMERS Connector (P11)

The pinout of the P11 connector can be found in "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-410HLF
Mating Connector		
IDC socket	DIGI-KEY	S4205-ND

LCD Data Connector (P12)

Part Description	Manufacturer	Part Number
FPC 16-pin 1 mm	HIROSE	FH12-16S-1SH(55)
Mating LCD Display Module (shipped with EZ-KIT Lite)		
3.5” TFT LCD with touchscreen	Varitronix	COG-T350MCQB-01

Host Interface Connector (P13)

The pinout of the P13 connector can be found in “ADSP-BF527 EZ-KIT Lite Schematic” on page B-1.

Part Description	Manufacturer	Part Number
IDC header	SAMTEC	TSW-116-26-T-D
Mating Connector		
IDC socket	SAMTEC	TSW-116-01-T-D

CPLD JTAG Connector (P17)

The CPLD JTAG connector (P17) is not populated; the CPLD code should not be altered for LCD operations.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-410HLF
Mating Connector		
IDC socket	DIGI-KEY	S4205-ND

LCD Touchscreen Connector (P18)

There is no connector for the touchscreen; the flex cable is soldered directly to the board.

LCD Backlight Connector (P19)

There is no connector for the backlight; the flex cable is soldered directly to the board.

USB Debug Agent Connector (ZJ1)

The USB debug agent connector is the connecting point for the JTAG USB debug agent interface. The JTAG header (ZP4) should not be used whenever ZJ1 and its mating cable are used to communicate to the processor via VisualDSP++.

JTAG Connector (ZP4)

The JTAG header is the connecting point for a JTAG in-circuit emulator pod. When an emulator connects to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

A ADSP-BF527 EZ-KIT LITE BILL OF MATERIALS

The bill of materials corresponds to "ADSP-BF527 EZ-KIT Lite Schematic" on page B-1.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	1	74LVC14A SOIC14	U17	TI	74LVC14AD
2	3	IDT74FCT3244 APY SSOP20	U22,U31-32	IDT	IDT74FCT3244APYG
3	1	SN74AHC1G00 SOT23-5	U6	TI	SN74AHC1G00DBVR
4	1	32.768KHZ OSC008	U1	EPSON	MC-156-32.7680KA-A0: ROHS
5	1	25MHZ OSC003	U3	EPSON	SG-8002CA MP
6	4	SN74LVC1G08 SOT23-5	U9-11,U29	TI	SN74LVC1G08DBVR
7	1	FDS9431A SOIC8	U21	FAIRCHILD	FDS9431A
8	1	MT48LC32M16 A2TG-75 TSOP54	U7	MICRON	MT48LC32M16A2P-75
9	1	20MHz OSC003	U19	DIGI-KEY	SG-8002CA-PCC-ND (20.000M)
10	2	SI4411DY SO-8	U18,U23	VISHAY	Si4411DY-T1-E3
11	1	HX1188 ICS007	U26	DIGI-KEY	553-1340-ND
12	1	24MHZ OSC003	U12	EPSON	SG-8002CA-MP

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
13	1	LAN8700 QFN36	U14	SMSC	LAN8700-AEZG
14	1	MAX1233 QFN28	U16	MAXIM	MAX1233
15	1	BF527 M25P16 “U8”	U8	ST MICRO	M25P16-VMW6G
16	1	BF527 M29W320EB “U5”	U5	ST MICRO	M29W320EB70ZE6E
17	1	NAND04 TSOP48	U4	ST MICRO	NAND04GW3B2BN6E
18	1	BF527 XC9536XL “U33”	U33	XILINX	XC9536XL-5VQG44C
19	1	MIC2025-1 SOIC8	U28	DIGI-KEY	576-1057-ND
20	1	12MHZ OSC003	U13	EPSON	SG-8002CA-MP
21	2	74CBTLV3244 TSSOP20	U30,U34	IDT	IDT74CBTLV3244PGG
22	1	50MHZ OSC003	U24	DIGI-KEY	SG-8002CA-PCB-ND (50.000M)
23	1	ADM708SARZ SOIC8	U27	ANALOG DEVICES	ADM708SARZ
24	2	ADP3336ARMZ MSOP8	VR3-4	ANALOG DEVICES	ADP3336ARMZ-REEL7
25	1	ADG752BRTZ SOT23-6	U20	ANALOG DEVICES	ADG752BRTZ-REEL
26	1	ADM3202ARNZ SOIC16	U25	ANALOG DEVICES	ADM3202ARNZ
27	1	ADSPBF527KBC ZENGC1 MBGA28	U2	ANALOG DEVICES	ADSPBF527KBCZENGC1

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
28	2	ADP1864AUJZ SOT23-6	VR1-2	ANALOG DEVICES	ADP1864AUJZ-R7
29	1	ADP1611 MSOP8	VR5	ANALOG DEVICES	ADP1611ARMZ-R7
30	1	PWR 2.5MM_JACK CON005	J6	SWITCH-CRAFT	RAPC712X
31	3	.05 45X2 CON019	J1-3	SAMTEC	SFC-145-T2-F-D-A
32	1	DIP6 SWT017	SW13	CTS	218-6LPST
33	10	DIP4 SWT018	SW1,SW4-5,SW7-11,SW19-20	ITT	TDA04HOSB1
34	1	DB9 9PIN CON038	J4	NORCOMP	191-009-213-L-571
35	3	DIP2 SWT020	SW17-18,SW21	C&K	CKN9064-ND
36	3	IDC 2X1 IDC2X1	P14-16	FCI	90726-402HLF
37	4	IDC 2X1 IDC2X1	JP1-3,JP5	FCI	90726-402HLF
38	1	IDC 3X1 IDC3X1	JP6	FCI	90726-403HLF
39	2	IDC 5X2 IDC5X2	P5,P11	FCI	68737-410HLF
40	2	IDC 10X2 IDC10X2	P9-10	BURG-FCI	54102-T08-10LF
41	2	IDC 17X2 IDC17X2	P6-7	BURG-FCI	54102-T08-17LF
42	1	IDC 20X2 IDC20X2	P8	BURG-FCI	54102-T08-20LF

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
43	6	IDC 2PIN_JUMPER_SHORT	SJ1-2,SJ7-10	DIGI-KEY	S9001-ND
44	1	5A RESETABLE FUS005	F2	MOUSER	650-RGEF500
45	1	ROTARY SWT023	SW2	DIGI-KEY	563-1047-ND
46	1	ROTARY_ENCODER SWT022	SW3	CTS	290UAB0R201B2
47	2	3.5MM DUAL_STEREO CON050	J7-8	SWITCH-CRAFT	35RAPC7JS
48	1	IDC 16x2 IDC16x2	P13	SAMTEC	TSW-116-26-T-D
49	1	USB_MINI-AB 5PIN CON052	P1	MOLEX	56579-0576
50	1	RJ45 8PIN CON_RJ45_12P	J9	DIGI-KEY	380-1022-ND
51	3	MOMENTARY SWT024	SW14-16	PANASONIC	EVQ-Q2K03W
52	1	FPC 16PIN CON056	P12	HIROSE	FH12-16S-1SH(55)
53	1	IDC 9X1 IDC9X1	P2	SAMTEC	SSW-109-01-TM-S
54	1	BATT_HOLDER 24MM CON054	J5	KEYSTONE ELEC	105
55	4	YELLOW LED001	LED1-3,LED6	PANASONIC	LN1461C
56	1	0.01UF 100V 10% 0805	C196	AVX	08051C103KAT2A
57	1	0.22UF 25V 10% 0805	C112	AVX	08053C224KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
58	1	0.1UF 50V 10% 0805	C251	AVX	08055C104KAT
59	2	10K 1/10W 5% 0805	R190-191	VISHAY	CRCW080510K0JNEA
60	2	100 1/10W 5% 0805	R122,R124	VISHAY	CRCW0805100RJNEA
61	16	600 100MHZ 200MA 0603	FER2-16,FER18	DIGI-KEY	490-1014-2-ND
62	3	600 100MHZ 500MA 1206	FER1,FER19-20	STEWARD	HZ1206B601R-10
63	5	1UF 16V 10% 0805	C92,C144,C148, C159,C178	KEMET	C0805C105K4RAC TU
64	1	10 1/10W 5% 0805	R64	VISHAY	CRCW080510R0FKEA
65	2	10UF 16V 20% CAP002	CT5,CT8	PANASONIC	EEE1CA100SR
66	1	10UH 20% IND001	L1	TDK	445-2014-1-ND
67	2	0 1/10W 5% 0805	R58,R188	VISHAY	CRCW08050000Z0EA
68	1	190 100MHZ 5A FER002	FER17	MURATA	DLW5BSN191SQ2
69	2	1A ZHCS1000 SOT23-312	D7,D9	ZETEX	ZHCS1000TA pb-free
70	2	1UF 10V 10% 0805	C164-165	AVX	0805ZC105KAT2A
71	13	10UF 6.3V 10% 0805	C7,C22,C33,C43, C52,C59,C68,C99, C101-102,C186, C254-255	AVX	08056D106KAT2A
72	4	4.7UF 6.3V 10% 0805	C94,C143,C171, C177	AVX	08056D475KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
73	47	0.1UF 10V 10% 0402	C12-19,C27-30, C38-41,C47-50, C56-57,C64-66, C78,C81,C83,C88, C98,C100,C103, C105,C111,C132, C135-136,C146, C157-158,C160-161,C191-194,C249	AVX	0402ZD104KAT2A
74	78	0.01UF 16V 10% 0402	C2,C4-6,C8-11, C20-21,C23-26, C31-32,C34-37, C42,C44-46,C51, C53-55,C58,C60-63,C67,C69-77, C79-80,C82,C84-87,C90-91,C93, C97,C116-117, C121-127,C137-138,C155-156, C163,C166-168, C187-188,C247-248,C250,C252-253	AVX	0402YC103KAT2A
75	65	10K 1/16W 5% 0402	R2-3,R11-14,R16-22,R24-27,R34,R53-55,R59,R65,R69-70, R73-76,R89,R91-93, R104-107,R118-121,R125-126, R129-131,R140, R144,R157-158, R160,R164,R166, R169,R173,R176-178,R184,R196, R198,R213,R301-302,R305	VISHAY	CRCW040210K0FKED
76	3	4.7K 1/16W 5% 0402	R23,R212,R307	VISHAY	CRCW04024K70JNED

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
77	15	0 1/16W 5% 0402	R6,R35,R49,R56, R110,R116,R149, R172,R175,R180-183,R192,R215	PANASONIC	ERJ-2GE0R00X
78	2	1.2K 1/16W 5% 0402	R87-88	PANASONIC	ERJ-2GEJ122X
79	3	22 1/16W 5% 0402	R193-195	PANASONIC	ERJ-2GEJ220X
80	9	33 1/16W 5% 0402	R1,R7-10,R31,R46, R139,R167	VISHAY	CRCW040233R0JNEA
81	2	18PF 50V 5% 0805	C1,C3	AVX	08055A180JAT2A
82	3	100UF 10V 10% C	CT6,CT9-10	AVX	TPSC107K010R0075
83	1	64.9K 1/10W 1% 0805	R145	VISHAY	CRCW080564K9FKEA
84	1	210.0K 1/4W 1% 0805	R146	VISHAY	CRCW0805210KFKEA
85	2	1.5K 1/10W 5% 0603	R71-72	PANASONIC	ERJ-3GEYJ152V
86	5	0.1UF 16V 10% 0603	C169,C174,C176, C195,C246	AVX	0603YC104KAT2A
87	3	1UF 16V 10% 0603	C96,C104,C109	PANASONIC	ECJ-1VB1C105K
88	1	10UF 25V +80/-20% 1210	C244	AVX	1210YD106KAT2A
89	2	68PF 50V 5% 0603	C141,C183	AVX	06035A680JAT2A
90	1	4.7UF 6.3V 20% 0603	C131	PANASONIC	ECJ-1VB0J475M
91	2	470PF 50V 5% 0603	C140,C182	AVX	06033A471JAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
92	3	220UF 6.3V 20% D2E	CT1,CT7,CT11	SANYO	10TPE220ML
93	1	10M 1/10W 5% 0603	R15	VISHAY	CRCW060310M0FNEA
94	5	330 1/10W 5% 0603	R111-113,R115, R123	VISHAY	CRCW0603330RJNEA
95	1	1M 1/10W 5% 0603	R33	VISHAY	CRCW06031M00FNEA
96	6	0 1/10W 5% 0603	R102,R109,R133, R168,R308-309	PHYCOMP	232270296001L
97	10	49.9 1/16W 1% 0603	R60-63,R78-80,R83-85	VISHAY	CRCW060349R9FNEA
98	2	10 1/10W 5% 0603	R127-128	VISHAY	CRCW060310R0JNEA
99	1	47.5K 1/10W 1% 0603	R298	VISHAY	CRCW060347K5FKEA
100	8	100PF 50V 5% 0603	C260-267	AVX	06035A101JAT2A
101	1	12.4K 1/10W 1% 0603	R67	DIGI-KEY	311-12.4KHRTR-ND
102	1	1000PF 50V 5% 0603	C245	PANASONIC	ECJ-1VC1H102J
103	2	75.0 1/10W 1% 0603	R81-82	DALE	CRCW060375R0FKEA
104	2	100 1/16W 5% 0402	R44-45	DIGI-KEY	311-100JRTR-ND
105	2	24.9K 1/10W 1% 0603	R98,R150	DIGI-KEY	311-24.9KHTR-ND
106	4	10UF 10V 10% 0805	C89,C128,C170, C175	PANASONIC	ECJ-2FB1A106K

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
107	1	105.0K 1/16W 1% 0603	R137	PANASONIC	ERJ-3EKF1053V
108	4	0.05 1/2W 1% 1206	R134,R141-143	SEI	CSF 1/2 0.05 1%R
109	2	10UF 16V 10% 1210	C147,C184	AVX	1210YD106KAT2A
110	2	GREEN LED001	LED4,LED7	PANASONIC	LN1361CTR
111	1	RED LED001	LED5	PANASONIC	LN1261CTR
112	2	1000PF 50V 5% 1206	C179-180	AVX	12065A102JAT2A
113	1	255.0K 1/10W 1% 0603	R152	VISHAY	CRCW06032553FK
114	2	80.6K 1/10W 1% 0603	R99,R151	DIGI-KEY	311-80.6KHRCT-ND
115	1	600 100MHZ 1.5A 0805	FER21	DIGI-KEY	240-2390-2-ND
116	4	5A MBRS540T3G SMC	D5,D10-12	ON SEMI	MBRS540T3G
117	3	15KV PGB1010603 0603	D2-4	LIT-TLEFUSE	PGB1010603MR
118	1	VARISTOR V5.5MLA 30A 0603	R37	LIT-TLEFUSE	V5.5MLA0603
119	1	THERM 0.5A 0.4 1206	R36	LIT-TLEFUSE	1206L050-C
120	1	20MA MA3X717E DIO005	D1	PANASONIC	MA3X717E
121	2	2.5UH 30% IND013	L2,L4	COILCRAFT	MSS1038-252NLB

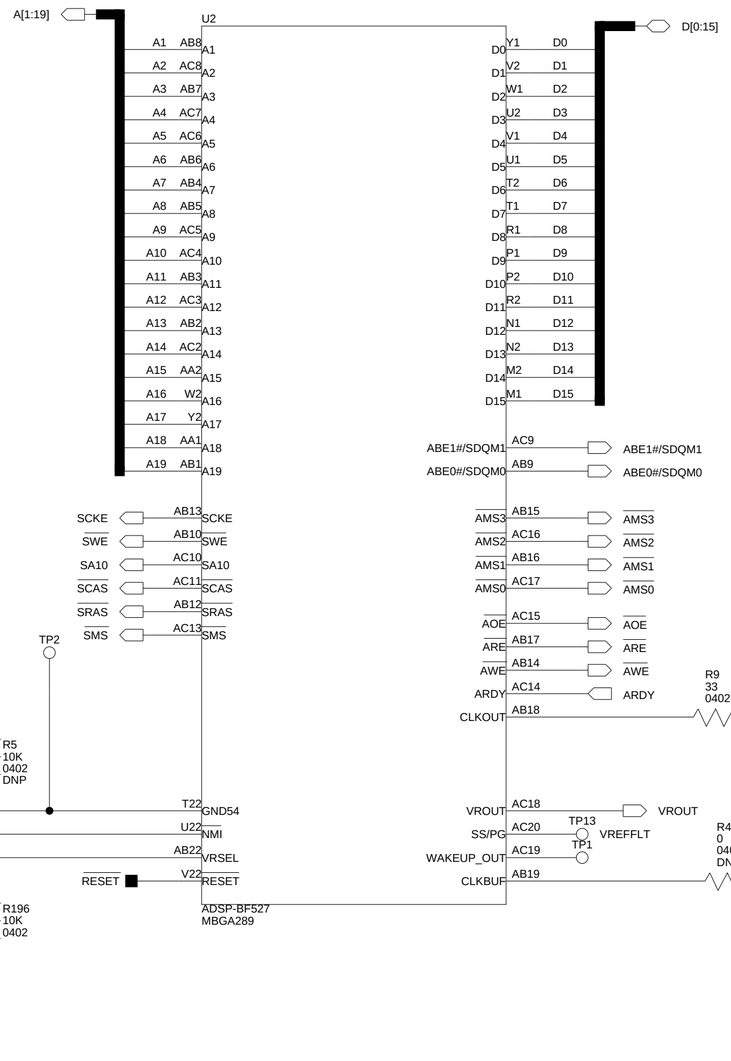
Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
122	2	330.0 1/16W 1% 0402	R68,R77	DIGI-KEY	541-330LCT-ND
123	5	47.0K 1/16W 1% 0402	R38-39,R50-52	ROHM	MCR01MZPF4702
124	3	1.0K 1/16W 1% 0402	R197,R199-200	PANASONIC	ERJ-2RKF1001X
125	2	1000PF 2000V 10% 1206	C133-134	AVX	1206GC102KAT1A
126	2	0.027 1/2W 1% 1206	R101,R103	SUSUMU	RL1632T-R027-F-N
127	4	5.6K 1/16W 0.5% 0402	R40-43	SUSUMU	RR0510P-562-D
128	1	680 1/16W 1% 0402	R47	BC COMPO-NENTS	2312 275 16801
129	1	90.9K 1/16W 5% 0402	R90	DIGI-KEY	541-90.9KLCT-ND
130	1	40.2K 1/16W 5% 0402	R57	DIGI-KEY	541-40.2KLCT-ND
131	4	3.3UF 16V 10% 0805	C113,C118,C120, C129	DIGI-KEY	490-3337-2-ND
132	1	0 1/16W 5% RNS003	RN5	PANASONIC	EXB-2HVR000V
133	4	22UF 10V 10% 1210	C139,C142,C145, C185	DIGI-KEY	490-1876-2-ND
134	1	95K 1/10W 1% 0603	R136	DIGI-KEY	311-95.3KHRTR-ND
135	5	15PF 50V 5% 0402	C119,C130,C197-199	DIGI-KEY	399-1014-2-ND
136	1	8.2UH 20% IND014	L3	COILCRAFT	LPS3010-822ML

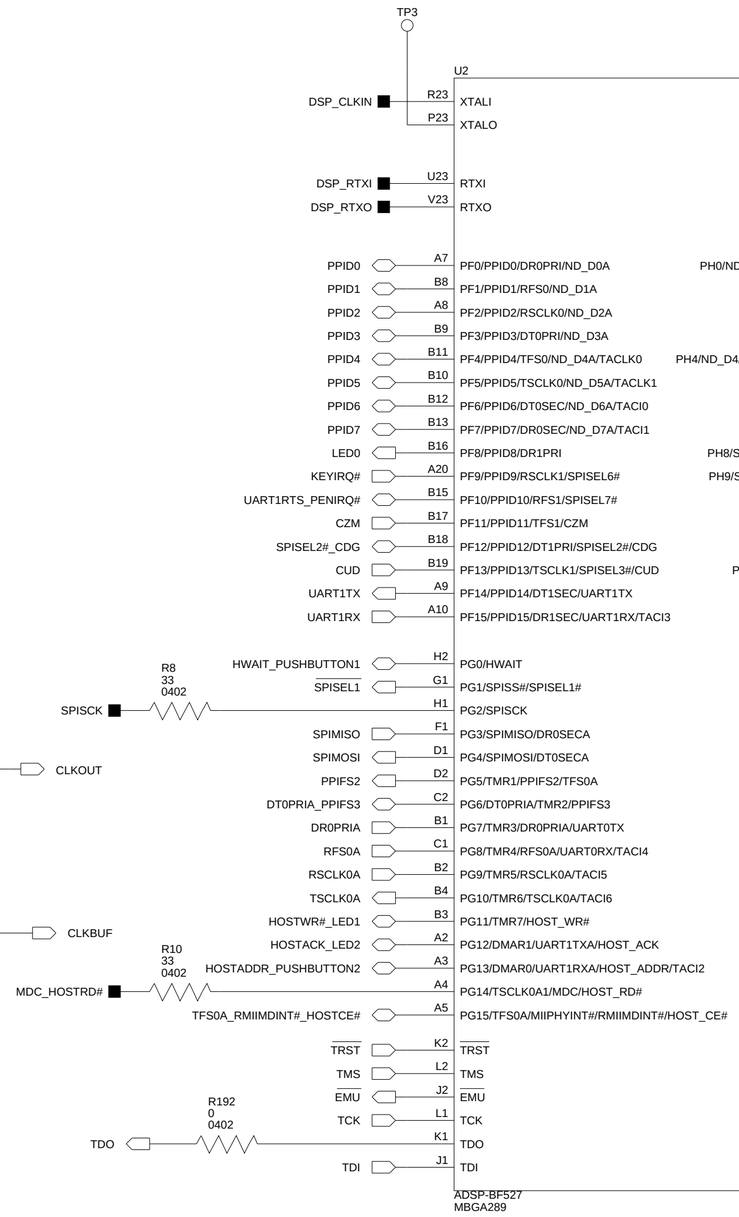
Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
137	1	422K 1/10W 1% 0603	R100	PANASONIC	ERJ-3EKF4223V
138	1	2A DFLS240 POWER_DI12	D13	DIODES INC	DFLS240
139	1	40.2 1/8W 1% 0805	R189	ROHM	MCR10EZPF40R2
140	1	MMSZ12T1G SOD-123	D6	ON SEMI	MMSZ12T1G

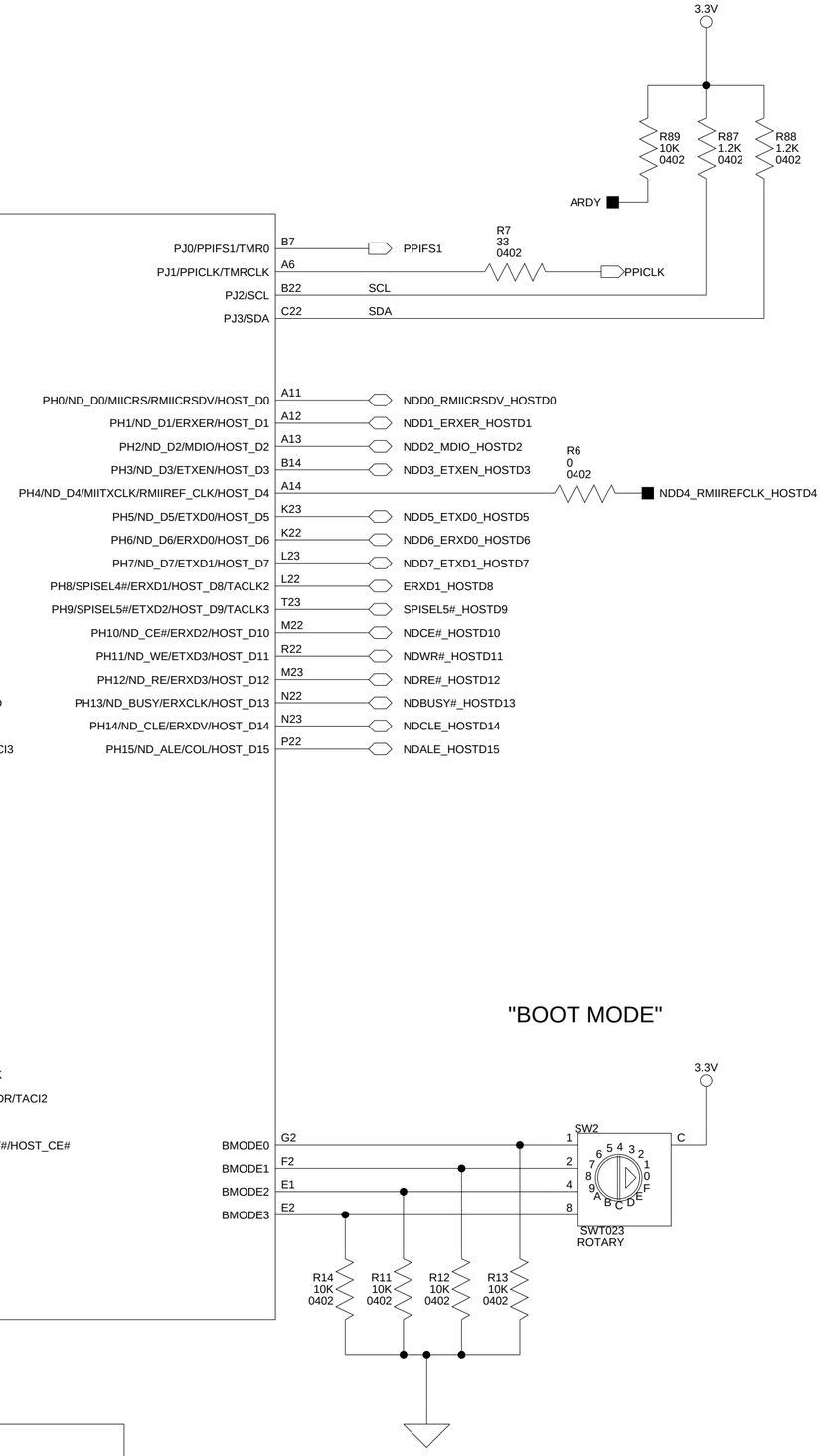
ADSP-BF527 EZ-KIT LITE SCHEMATIC

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

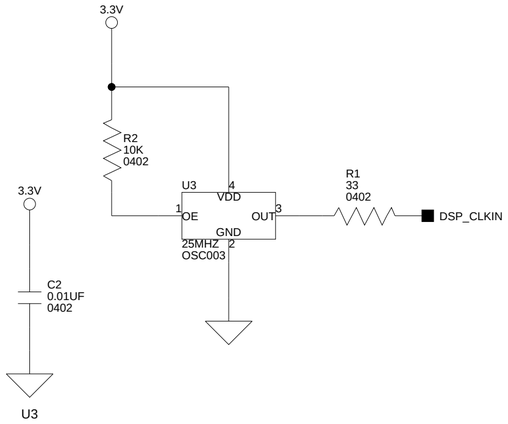
Title	ADSP-527 EZ-KIT Lite TITLE		
Size C	**Board No.** A0208-2006		**Rev** 2.0
Date 4-28-2009_15:57		**Sheet** 1 **of** 13	

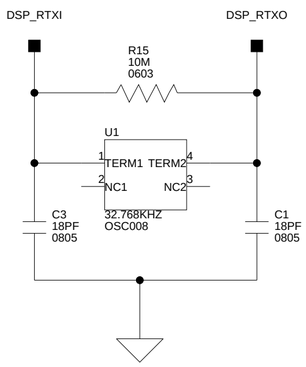




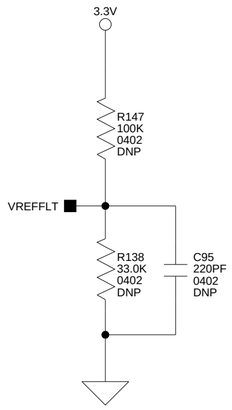


"BOOT MODE"





RTC



SW2: Boot Mode Select Switch

	POSITION	BOOT MODE
Default	0	Reserved
	1	Boot from 8 or 16-bit external flash memory
	2	Boot from 16-bit asynchronous FIFO
	3	Boot from serial SPI memory
	4	Boot from SPI host device
	5	Boot from serial TWI memory
	6	Boot from TWI host
	7	Boot from UART0 host
	8	Boot from UART1Host
	9	Reserved
	A	Boot from SDRAM
	B	Reserved
	C	Reserved
	D	Reserved
	E	Boot from 16-Bit Host DMA
	F	Boot from 8-Bit Host DMA

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	ADSP-527 EZ-KIT Lite DSP EBIU + CONTROL		
Size C	Board No. A0208-2006		Rev 2.0
Date 4-28-2009_15:57		Sheet 2 of 13	

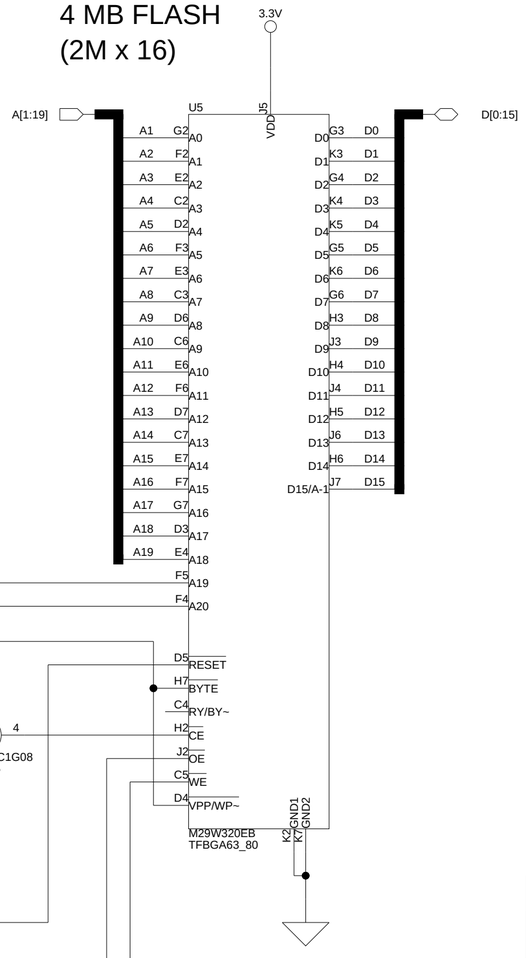
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	ADSP-527 EZ-KIT Lite DSP POWER		
Size C	**Board No.** A0208-2006		**Rev** 2.0
Date 4-28-2009_15:57		**Sheet** 3 **of** 13	

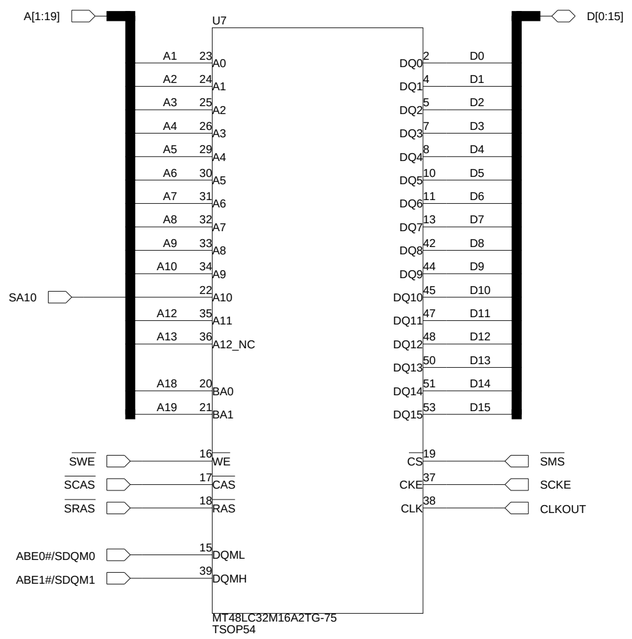
SW7: FLASH Enable

POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION / OFF MODE
SW7.1	DSP (U2)	FLASH (U5)	ON	J2.65 (Expansion Interface)
SW7.2	DSP (U2)	FLASH (U5)	ON	J2.63 (Expansion Interface)
SW7.3	DSP (U2)	FLASH (U5)	ON	J2.61 (Expansion Interface)
SW7.4	DSP (U2)	FLASH (U5)	ON	J2.59 (Expansion Interface)

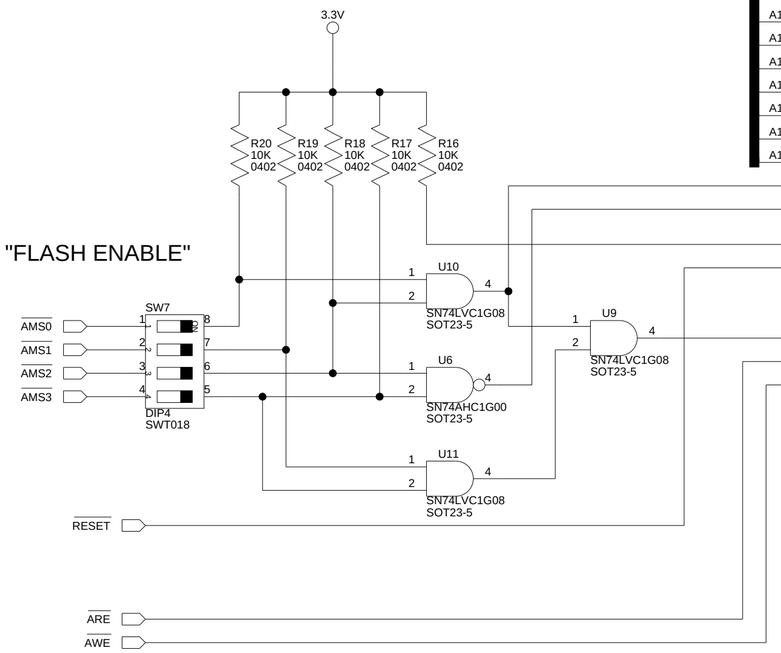
4 MB FLASH (2M x 16)



64MB SDRAM (32M x 16)

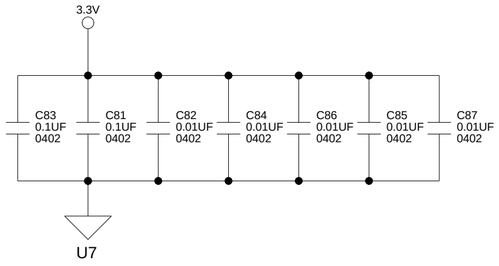


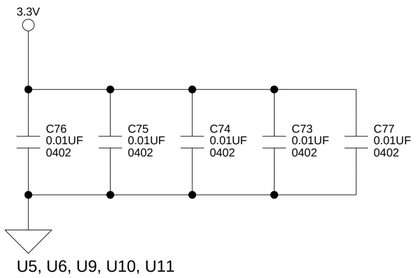
"FLASH ENABLE"



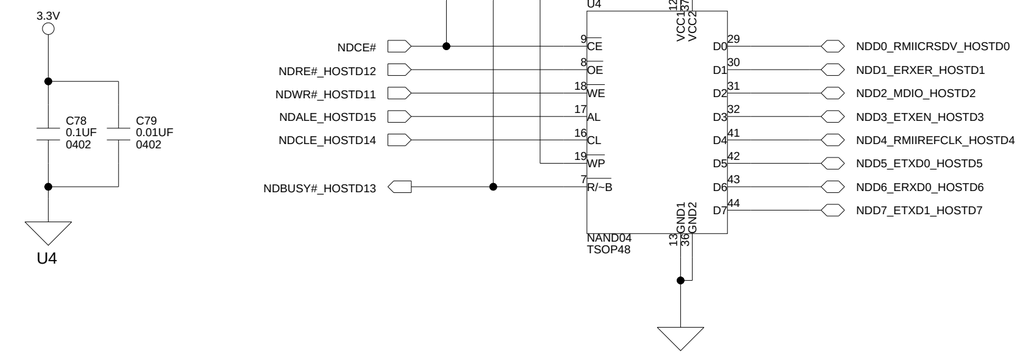
MEMORY MAP

ADDRESS RANGE	SELECT LINE	TYPE
0x2030 0000 - 0x203F FFFF	ASYNC BANK 3	FLASH
0x2020 0000 - 0x202F FFFF	ASYNC BANK 2	FLASH
0x2010 0000 - 0x201F FFFF	ASYNC BANK 1	FLASH
0x2000 0000 - 0x200F FFFF	ASYNC BANK 0	FLASH
0x0000 0000 - 0x03FF FFFF	NONE	SDRAM

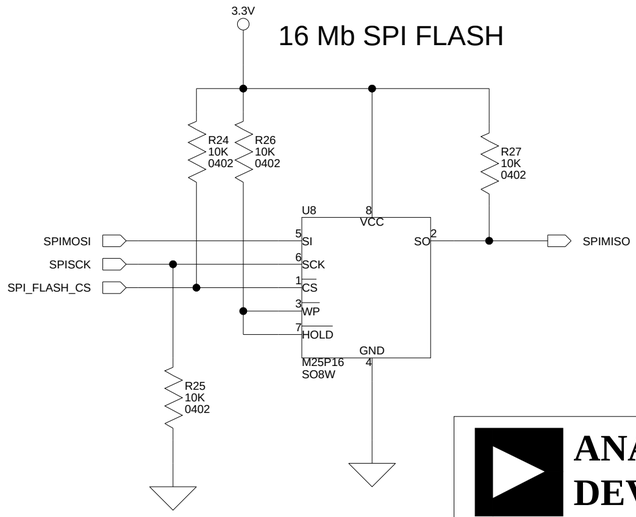




4Gb NAND FLASH

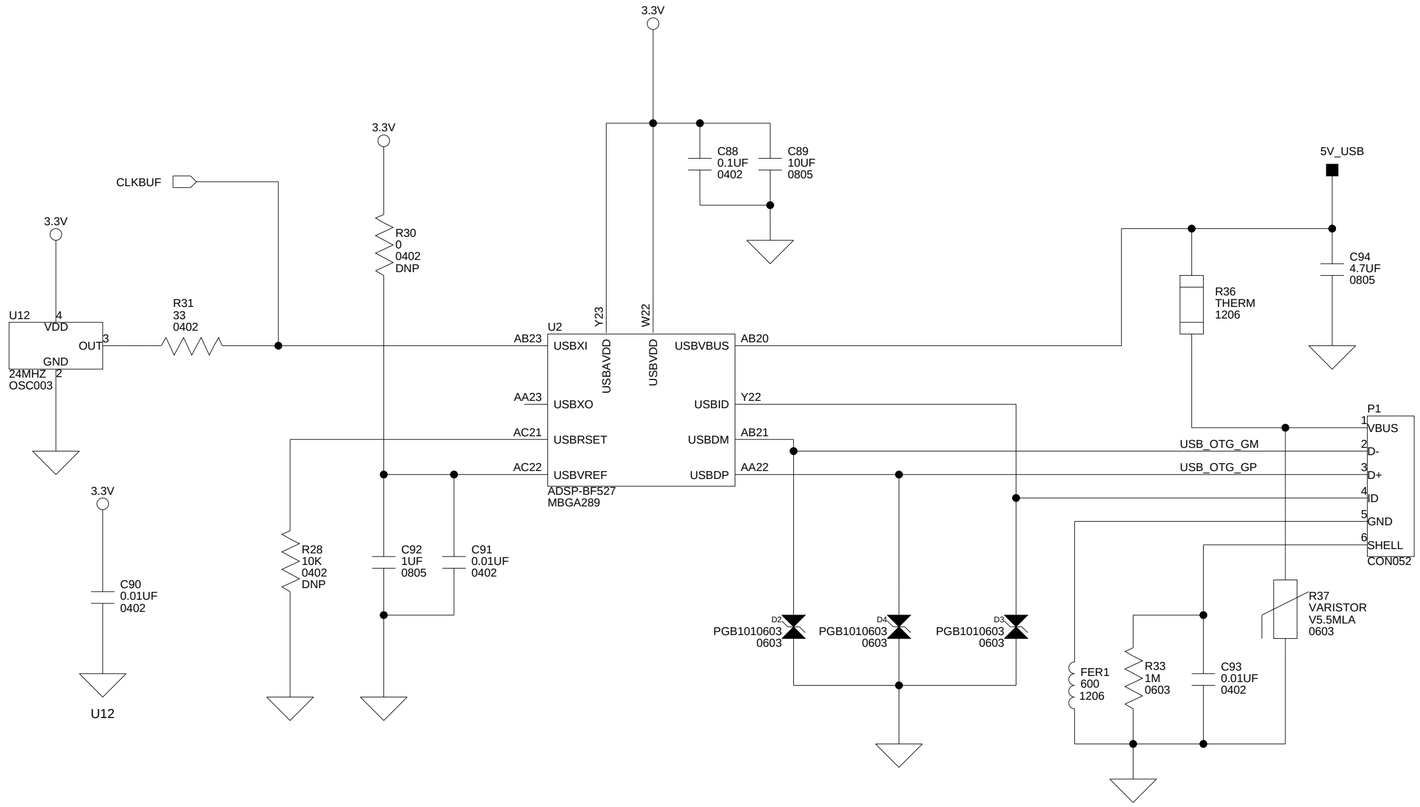


16 Mb SPI FLASH



ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	ADSP-527 EZ-KIT Lite MEMORY	
Size C	**Board No.** A0208-2006	**Rev** 2.0
Date 4-28-2009_15:57	**Sheet** 4 **of** 13	

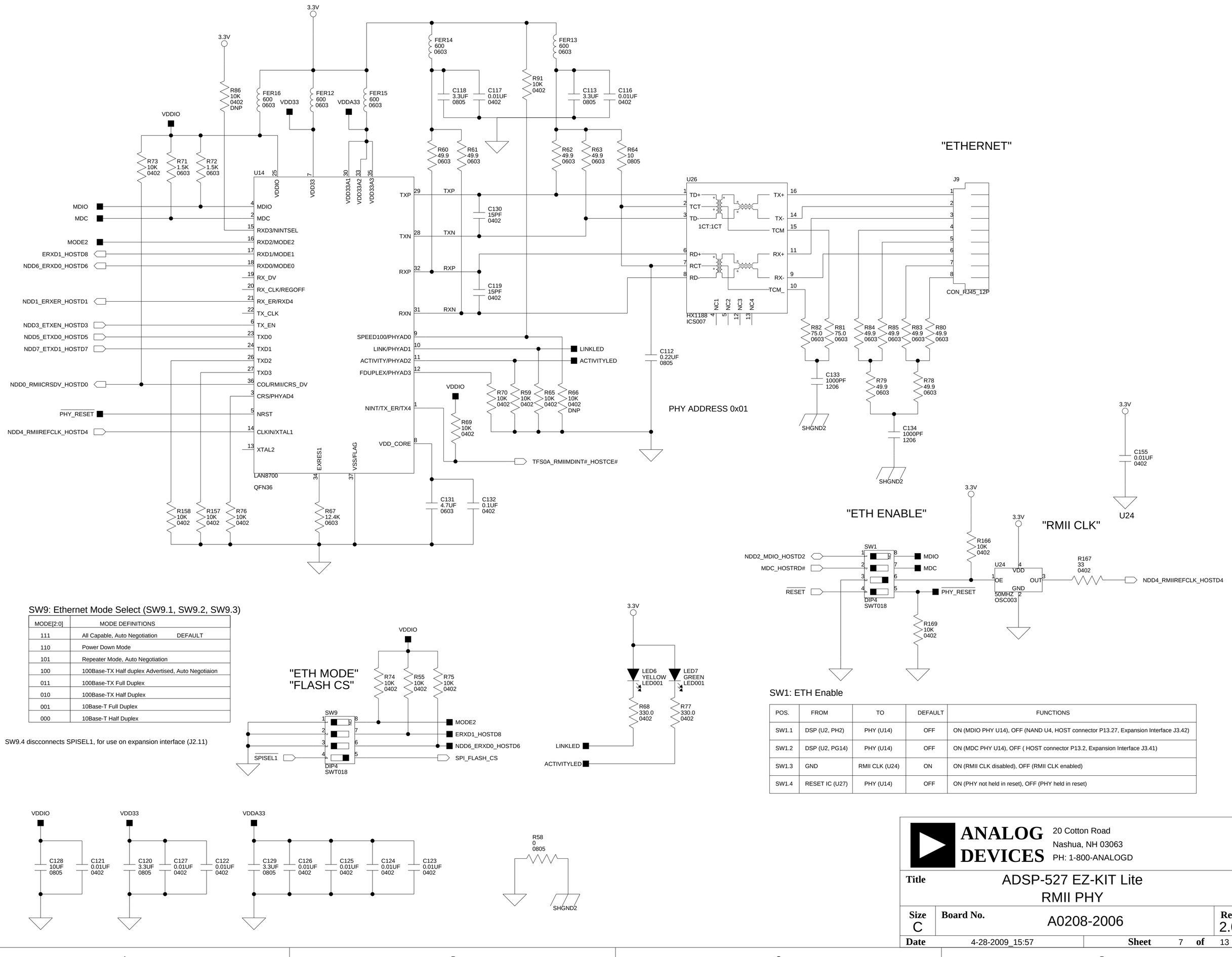
"USB CLK"



"USB OTG"

ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
Title	ADSP-527 EZ-KIT Lite DSP USB OTG		
Size C	**Board No.** A0208-2006		**Rev** 2.0
Date 4-28-2009_15:57		**Sheet** 5 **of** 13	

J7
J8
MIC IN
HP OUT
LINE IN
LINE OUT
SJ10
SHORTING JUMPER DEFAULT=2&3
"MIC GAIN"
R57 40.2K 0402
R90 90.9K 0402
SW4
DIP4 SWT018
C109 1UF 0603
R50 47.0K 0402
C110 220PF 0402 DNP
AGND
SW4: MIC GAIN
POS. | GAIN
1 | 5 (14dB)
2 | 1 (0dB)
3 | 0.5 (-6dB)
4 | NC
3.3V
R109 0 0603
C99 10UF 0805
C98 0.1UF 0402
U2
CVDD
CGND
ALTERNATE FUNCTION / OFF MODE
"MIC/HP LPBK"
"AUDIO MODE"
R54 10K 0402
R160 10K 0402
SW8
MICIN
LHPOUT_RDIV
RHPOUT_RDIV
AUDIO_MODE
SW8 allows the MICIN signal to be looped back, for test purposes, to the Left and Right headphone.
DO NOT switch positions 1 & 2 ON at the same time.
Ensure that JP6 is on 2&3 or OFF when using SW8.
AUDIO CODEC INTERFACE MODE:
SW8.3 ON and SW8.4 OFF = SPI MODE
SW8.3 OFF and SW8.4 ON = TWI MODE
FER3 600 0603
FER4 600 0603
JP6
IDC3X1
"MIC SELECT"
R47 680 0402
C108 220PF 0402 DNP
MICIN_RDIV
MICBIAS_Z
MICIN
MICBIAS
LLINEIN_RDIV
RLINEIN_RDIV
LLINEIN
RLINEIN
FER9 600 0603
FER10 600 0603
AVDD
HPVDD
HPGND
C101 10UF 0805
C100 0.1UF 0402
C102 10UF 0805
C103 0.1UF 0402
CT1 220UF D2E
CT7 220UF D2E
LHPOUT
RHPOUT
CT5 10UF CAP002
CT8 10UF CAP002
LOUT
ROUT
C_CLKOUT
VMID
R308 0 0603
FER5 600 0603
R309 0 0603
FER11 600 0603
R39 47.0K 0402
R51 47.0K 0402
J8
CON050
LHPOUT_RDIV
RHPOUT_RDIV
LOUT_RDIV
ROUT_RDIV
LEFT_LPBK
RIGHT_LPBK
J7
MICIN
MICBIAS
LLINEIN
RLINEIN
LEFT_LPBK
RIGHT_LPBK
FER2 600 0603
FER8 600 0603
R43 5.6K 0402
R42 5.6K 0402
C96 1UF 0603
C104 1UF 0603
R41 5.6K 0402
R40 5.6K 0402
C261 100PF 0603
C260 100PF 0603
C262 100PF 0603
C263 100PF 0603
CODEC_DACLRC
CODEC_DACDAT
CODEC_ADCDAT
CODEC_ADCLRC
BCLK
AUDIO_MODE
CSB
SDIN
SCLK
C_MODE
ADSP-BF527 MBGA289
XTI/MCLK
XTO
R44 100 0402
R45 100 0402
FER6 600 0603
FER7 600 0603
R52 47.0K 0402
R38 47.0K 0402
C264 100PF 0603
C265 100PF 0603
C266 100PF 0603
C267 100PF 0603
"AUDIO CLK"
R53 10K 0402
U13
VDD
OE
GND
OUT
12MHZ OSC003
R46 33 0402
AUDIO_CLK
C97 0.01UF 0402
R163 0 0402 DNP
R164 10K 0402
R172 0 0402
R165 10K 0402 DNP
SPISEL2#_CDG
SPISEL5#_HOSTD9
"SPORT"
"0A"
"ENBL"
SW20
TFS0A_RMIIMDINT#_HOSTCE#
DT0PRIA_PPIFS3
DR0PRIA
RFS0A
SW17
TSCLK0A
RSCLK0A
DIP2 SWT020
SW20 and SW17 disconnect DSP from AUDIO CODEC
"SPI/TWI"
SW19
SPIMOSI
SDA
SPISCK
SCL
AUDIO CODEC MODE INTERFACE:
SPI MODE: ON, OFF, ON, OFF
TWI MODE: OFF, ON, OFF, ON
W1 COPPER
C268 1000PF 0805 DNP
C269 1000PF 0805 DNP
C186 10UF 0805
C105 0.1UF 0402
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD
Title
ADSP-527 EZ-KIT Lite
INTERNAL AUDIO CODEC
Size C
Board No. A0208-2006
Rev 2.0
Date 4-28-2009_15:57
Sheet 6 of 13



SW9: Ethernet Mode Select (SW9.1, SW9.2, SW9.3)

MODE[2:0]	MODE DEFINITIONS
111	All Capable, Auto Negotiation DEFAULT
110	Power Down Mode
101	Repeater Mode, Auto Negotiation
100	100Base-TX Half duplex Advertised, Auto Negotiaion
011	100Base-TX Full Duplex
010	100Base-TX Half Duplex
001	10Base-T Full Duplex
000	10Base-T Half Duplex

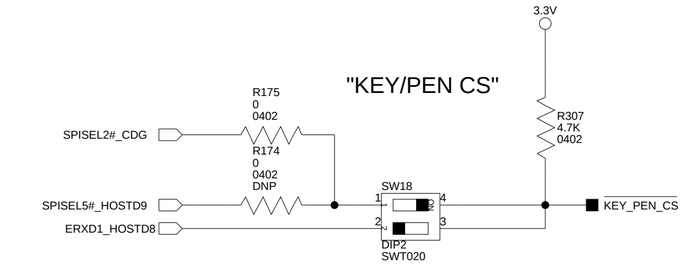
SW9.4 disconnects SPISEL1, for use on expansion interface (J2.11)

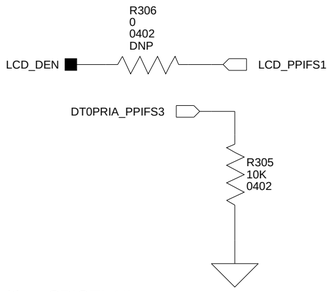
SW1: ETH Enable

POS.	FROM	TO	DEFAULT	FUNCTIONS
SW1.1	DSP (U2, PH2)	PHY (U14)	OFF	ON (MDIO PHY U14), OFF (NAND U4, HOST connector P13.27, Expansion Interface J3.42)
SW1.2	DSP (U2, PG14)	PHY (U14)	OFF	ON (MDC PHY U14), OFF (HOST connector P13.2, Expansion Interface J3.41)
SW1.3	GND	RMII CLK (U24)	ON	ON (RMII CLK disabled), OFF (RMII CLK enabled)
SW1.4	RESET IC (U27)	PHY (U14)	OFF	ON (PHY not held in reset), OFF (PHY held in reset)

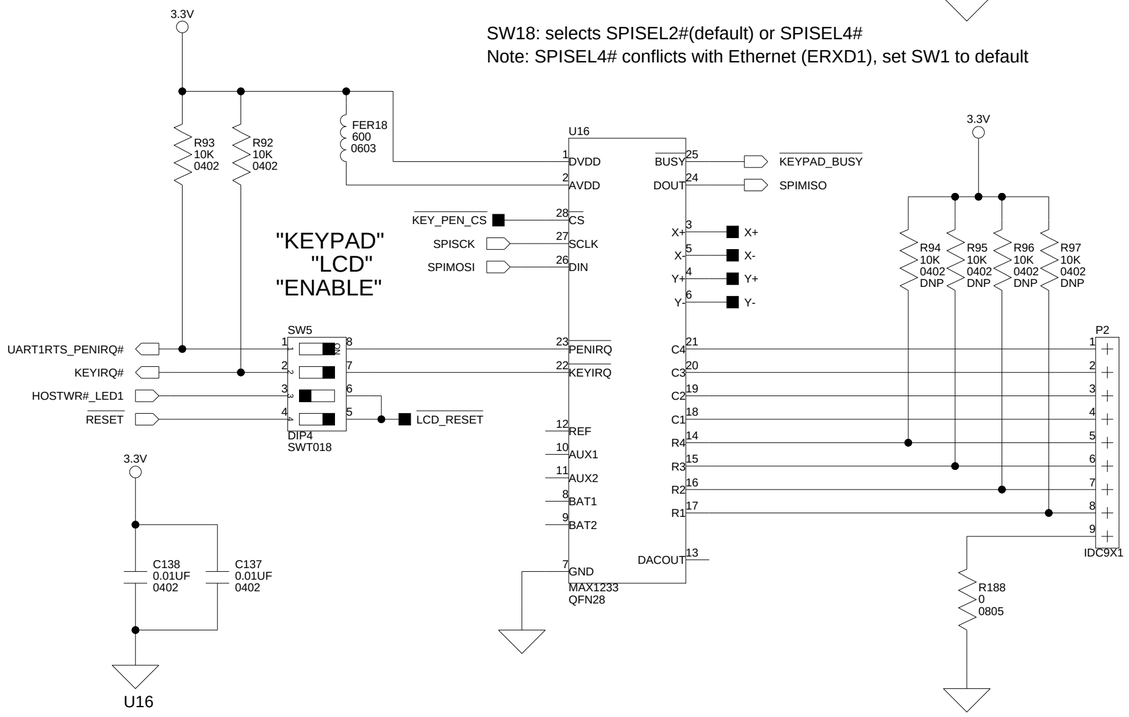
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	ADSP-527 EZ-KIT Lite RMII PHY	
Size C	Board No. A0208-2006	Rev 2.0
Date 4-28-2009_15:57	Sheet 7 of 13	



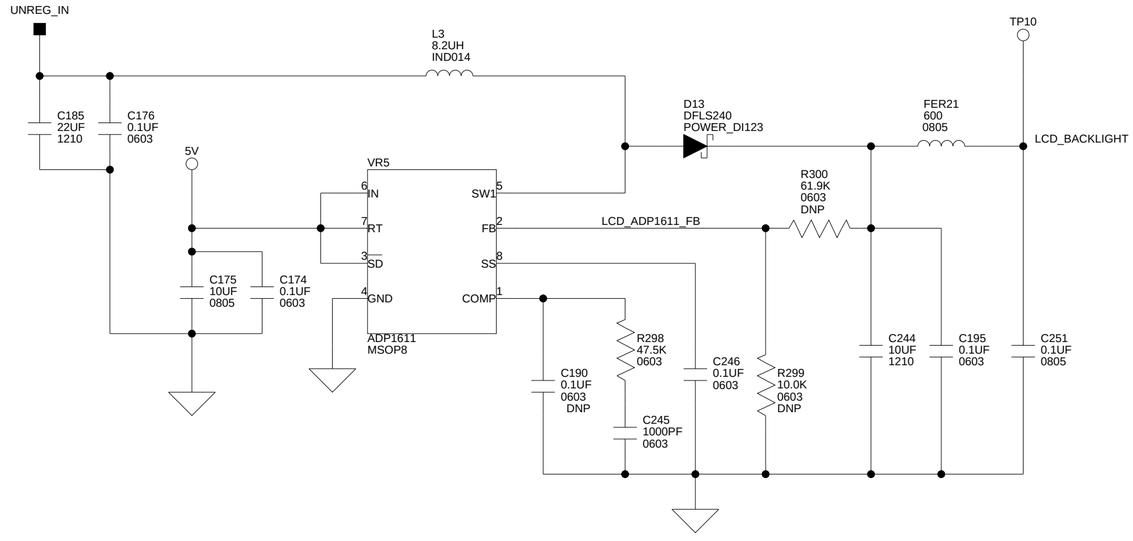


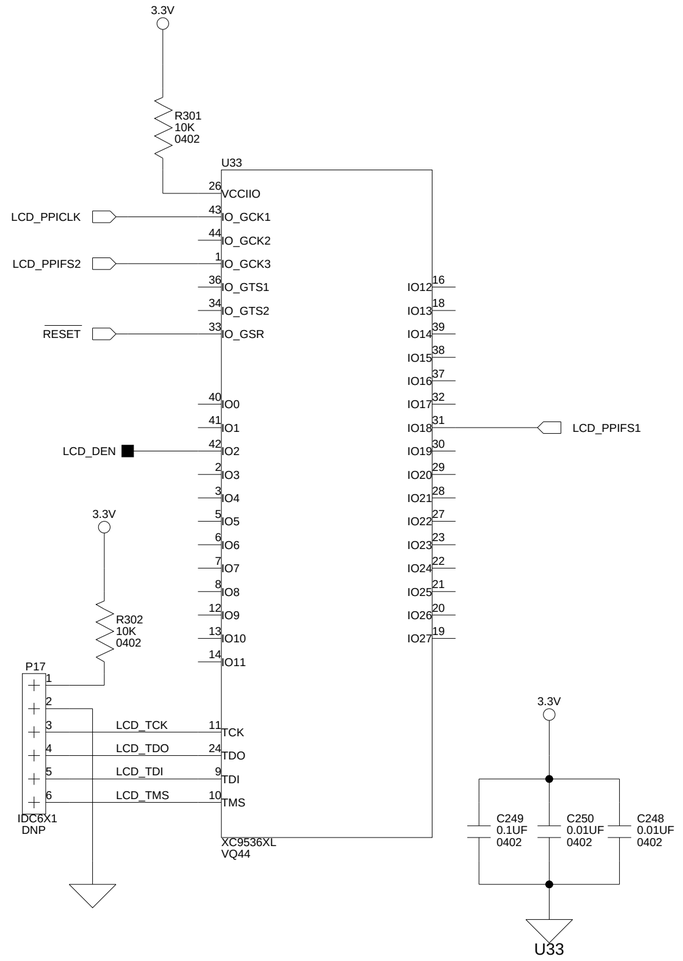
SW18: selects SPISEL2#(default) or SPISEL4#
Note: SPISEL4# conflicts with Ethernet (ERXD1), set SW1 to default

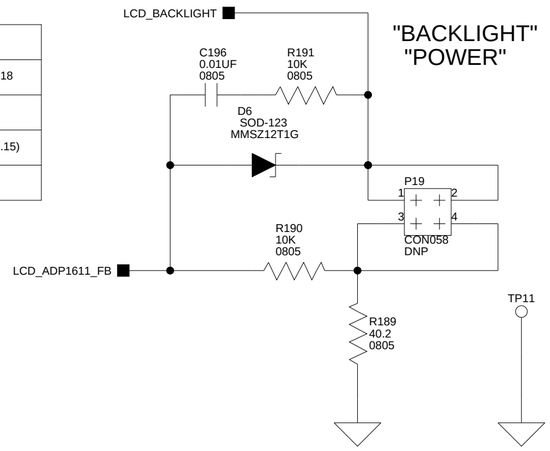


SW5: Keypad LCD enable

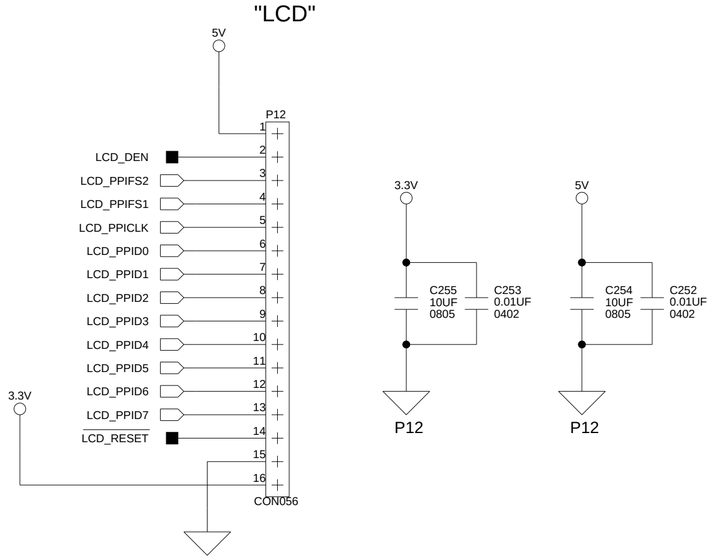
POS.	FROM	TO	DEFAULT	FUNCTIONS
SW1.1	DSP (U2, PF10)	Keypad IC (U16)	ON	OFF (SW10.3 used as GPIO RTS of UART1, expansion interface J2.31, J2.49, SPORT 1 conn P7.7, PPI conn P8.18
SW1.2	DSP (U2, PF9)	Keypad IC (U16)	ON	OFF (Expansion Interface pins: J2.33 J2.48, SPORT 1 conn P7.16, PPI conn P8.17)
SW1.3	DSP (U2, PG11)	LCD conn (P12)	OFF	ON (GPIO control of LCD_RESET), OFF (HOST conn P13.4, LED1, Expansion Interface J1.80, STAMP buffer U34.15)
SW1.4	RESET IC (U27)	LCD conn (P12)	ON	OFF(LCD not connected to board reset)

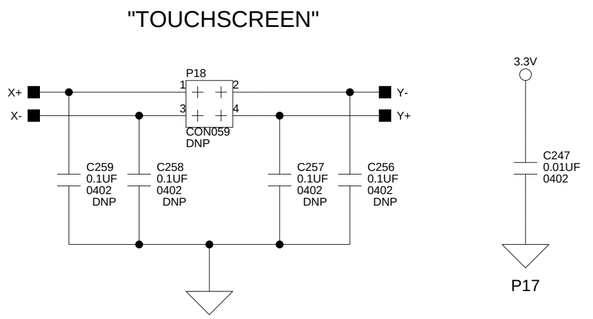




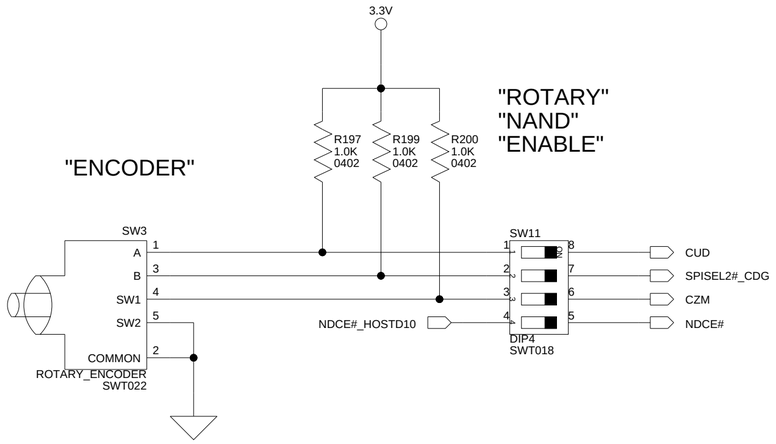


"CPLD JTAG"



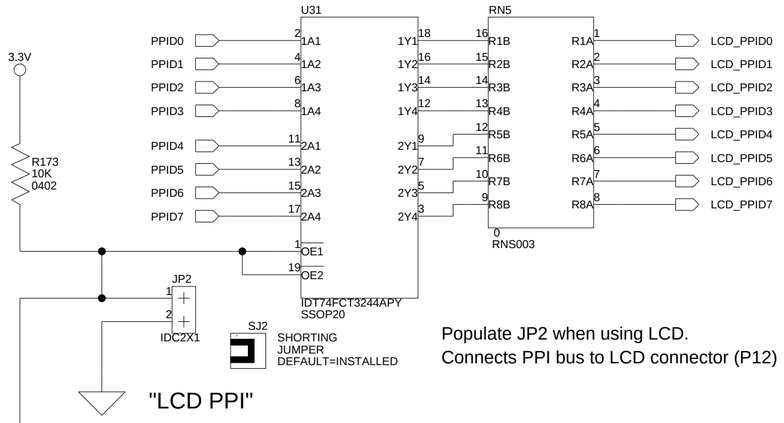


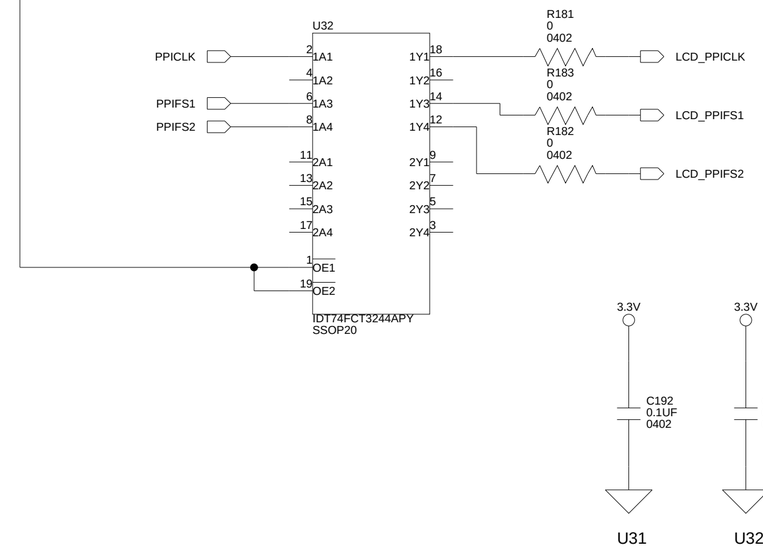
ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	ADSP-527 EZ-KIT Lite LCD	
Size C	**Board No.** A0208-2006	**Rev** 2.0
Date 4-28-2009_15:57	**Sheet** 8 **of** 13	

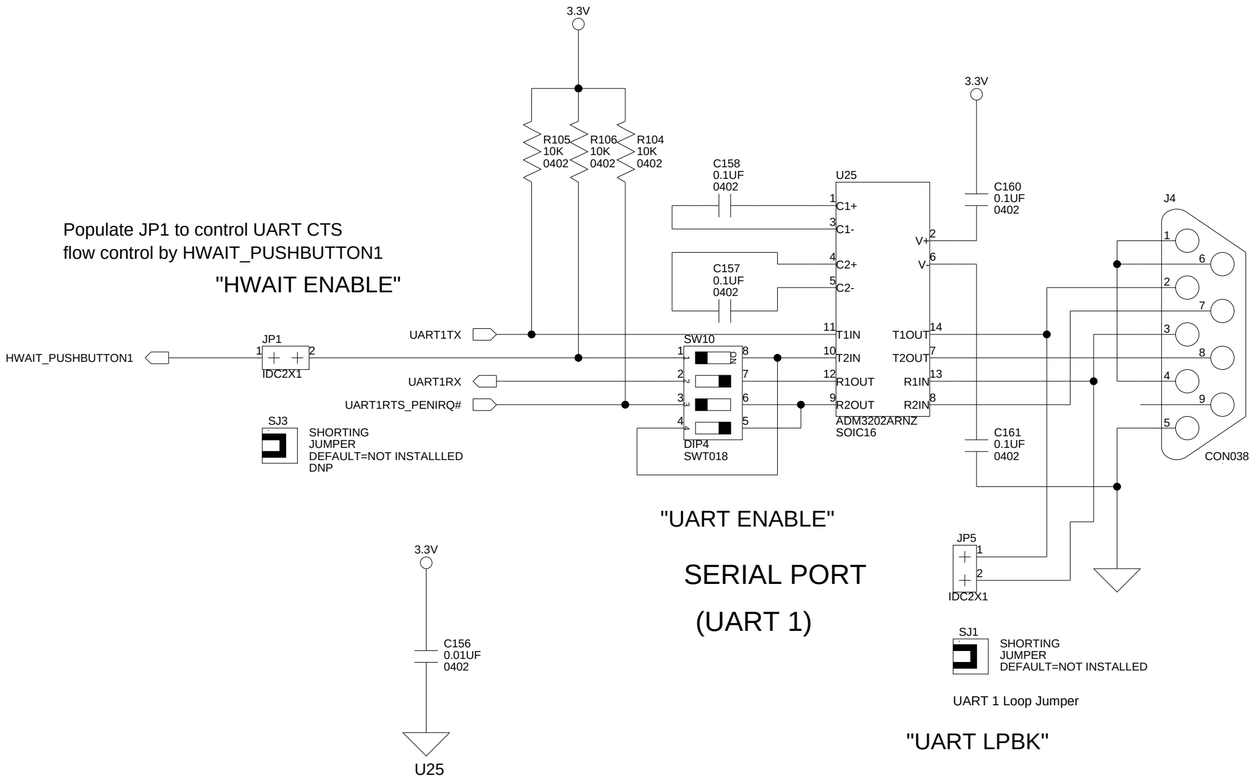


SW11: Rotary NAND enable

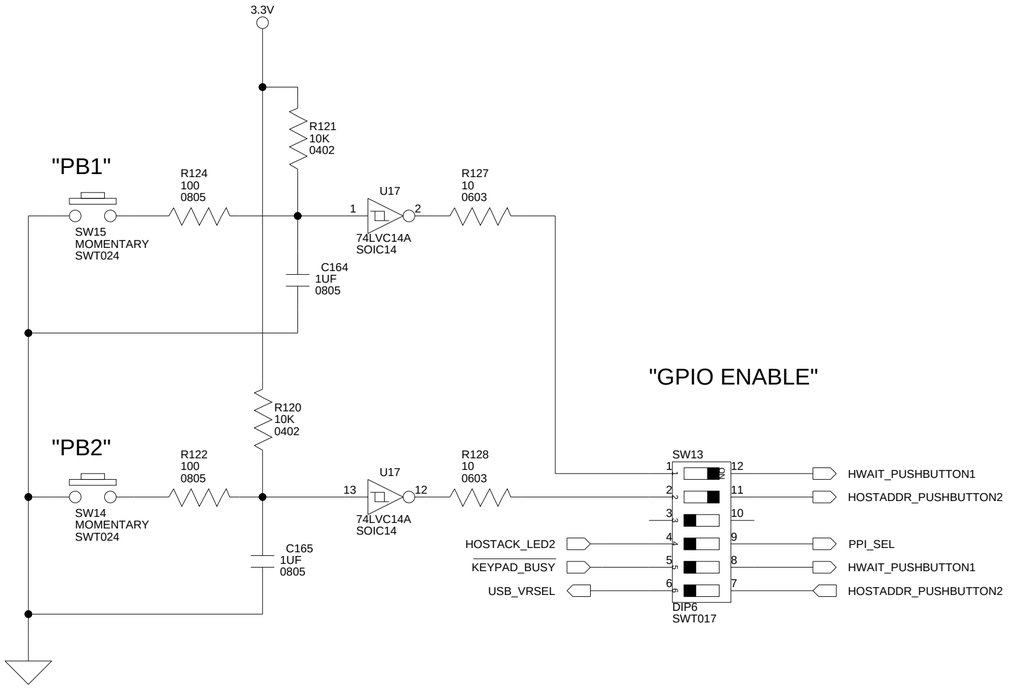
POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION / OFF MODE
SW11.1	Encoder (SW3)	DSP (U2, PF13)	ON	Expansion Interface (J2.34, J2.52) Stamp buffer (U34)
SW11.2	Encoder (SW3)	DSP (U2, PF12)	ON	CS audio codec (U2), CS keypad/touch controller (U16), Expansion Interface (J2.30, J2.51), Stamp buffer (U30)
SW11.3	Encoder (SW3)	DSP (U2, PF11)	ON	Expansion Interface (J2.32, J2.50), Stamp buffer (U34)
SW11.4	DSP (U2, PH10)	NAND (U4)	ON	Host connector (P13.11), Expansion Interface (J3.35)

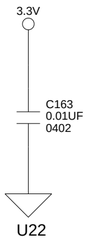


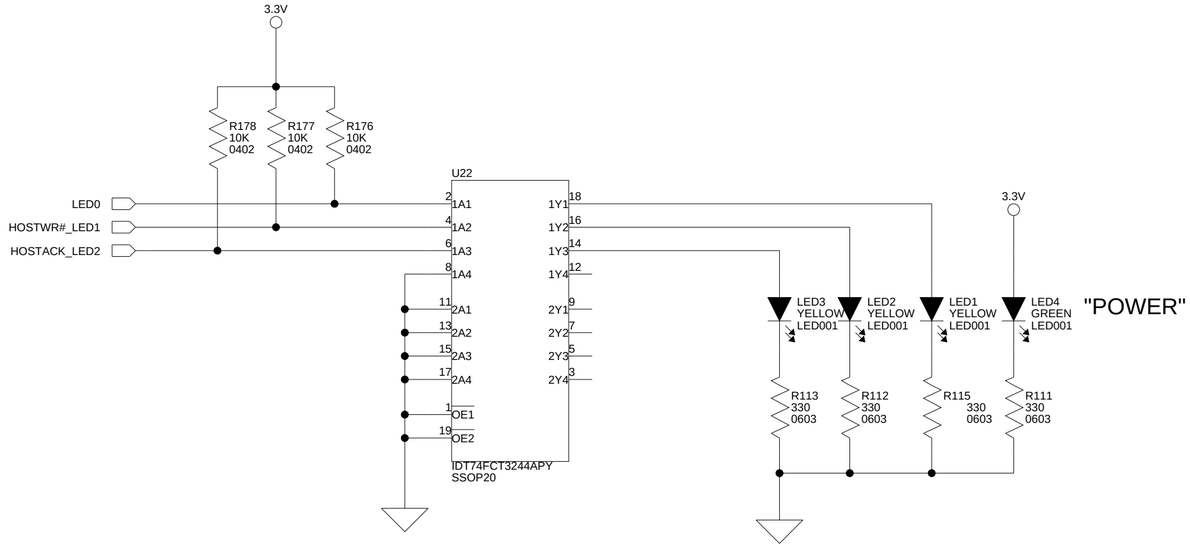




ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
Title	ADSP-527 EZ-KIT Lite ROTARY SWITCH, RS232		
Size C	**Board No.** A0208-2006		**Rev** 2.0
Date 4-28-2009_15:56		**Sheet** 9 **of** 13	

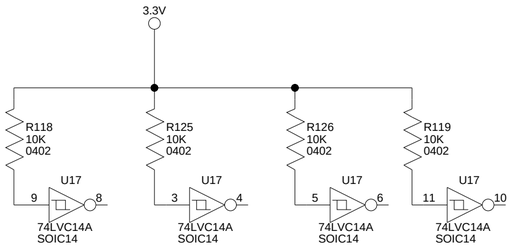


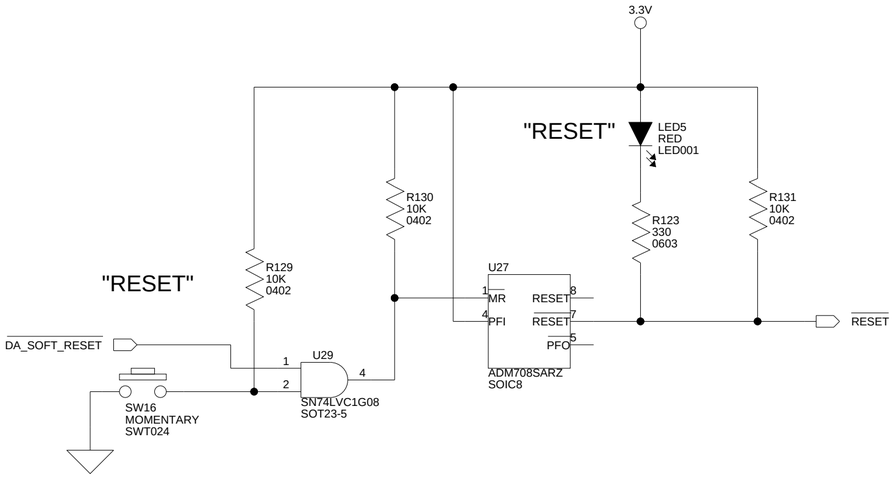


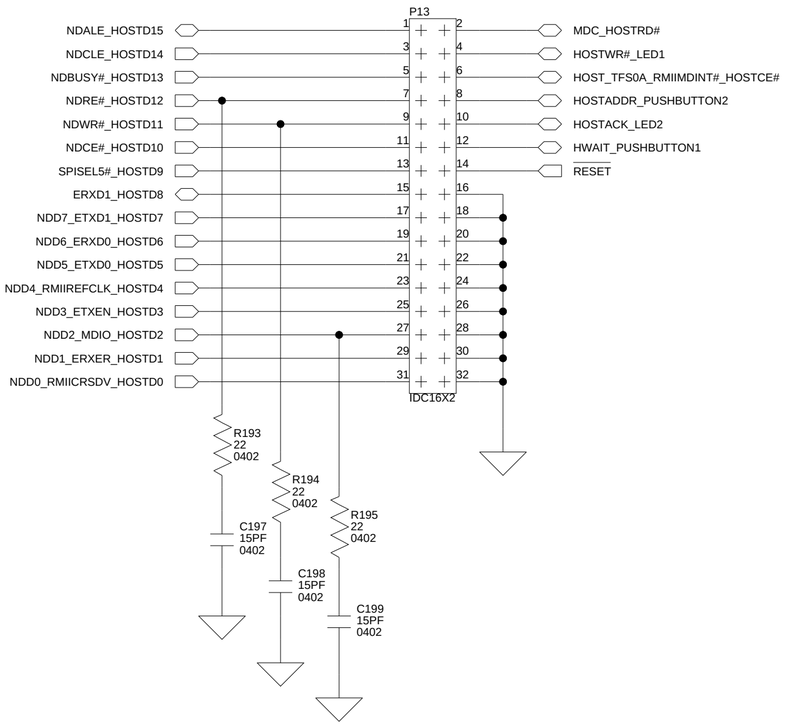


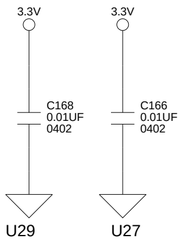
SW13: GPIO enable

POS.	FROM	TO	DEFAULT	FUNCTIONS
SW13.1	push button 1	DSP (U2, PG0)	ON	ON (PB1), OFF (UART 1 CTS U25, HOST connector P13.12, Keypad busy SW13.8, Expansion Interface J1.84)
SW13.2	push button 2	DSP (U2, PG13)	ON	ON (PB2), OFF (HOST connector P13.8, OTG voltage select SW13.7, Expansion Interface J1.85)
SW13.3			OFF	NC
SW13.4	DSP(U2, PG12)	PPI CLK (U20)	OFF	OFF (LED2, Host connector P13.10, Expansion Interface J1.81, STAMP buffer U34), ON (PPI CLK U20)
SW13.5	Keypad BUSY (U16)	DSP(U2, PG0)	OFF	OFF (PB1, UART 1 CTS U25, Host conn P13.12, Expansion Interface J1.84), ON (GPIO Keypad busy U16, SW13.1)
SW13.6	OTG PWR(VR3, U28)	DSP (U2, PG13)	OFF	OFF (HOST connector P13.8, Expansion Interface J1.85), ON (PB2 SW13.11, OTG power VR3, U28)









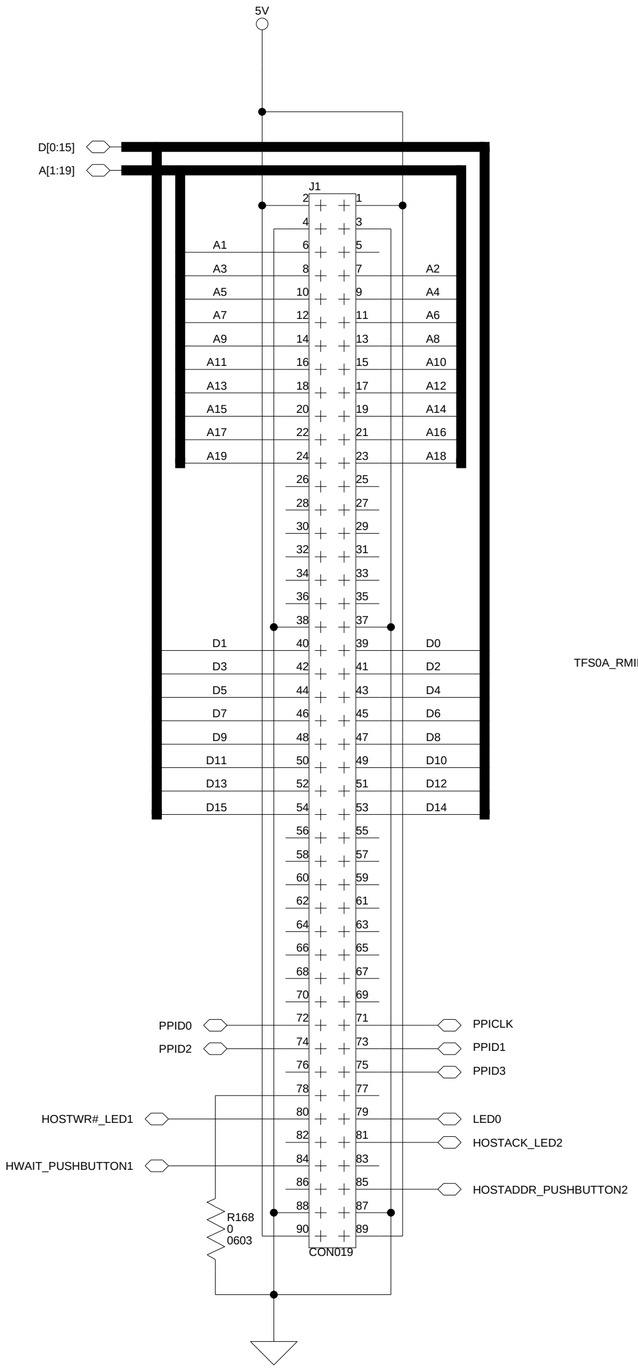
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

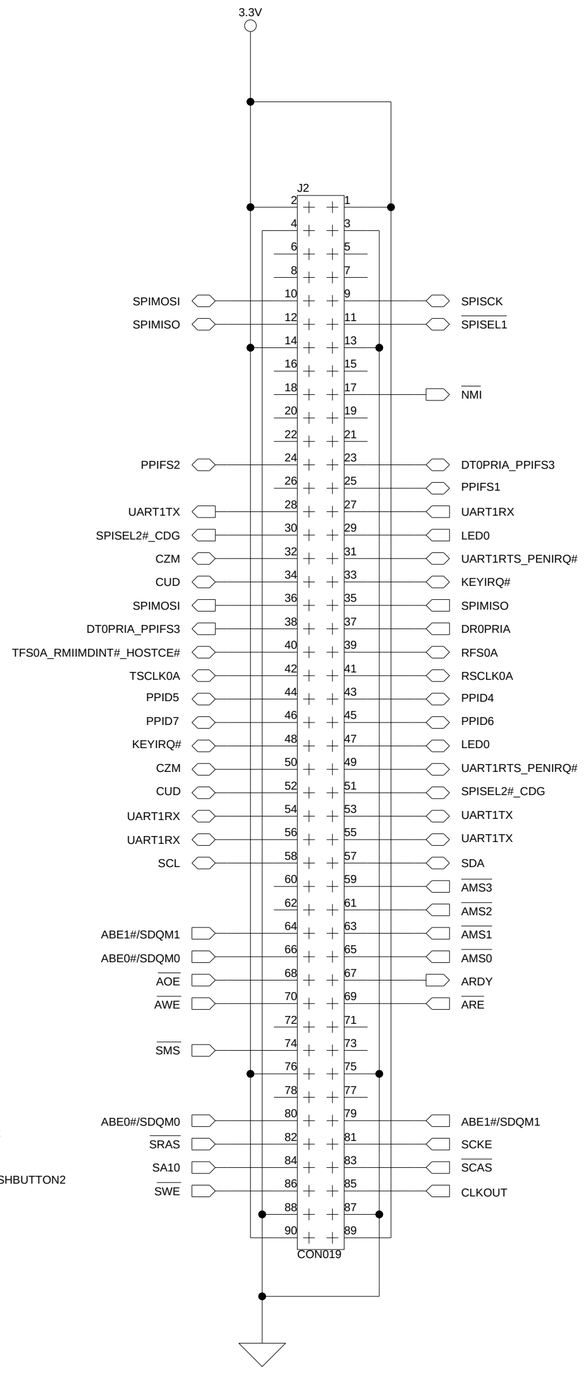
Title ADSP-527 EZ-KIT Lite
LEDS, PUSHBUTTONS, RESET, HOST PORT

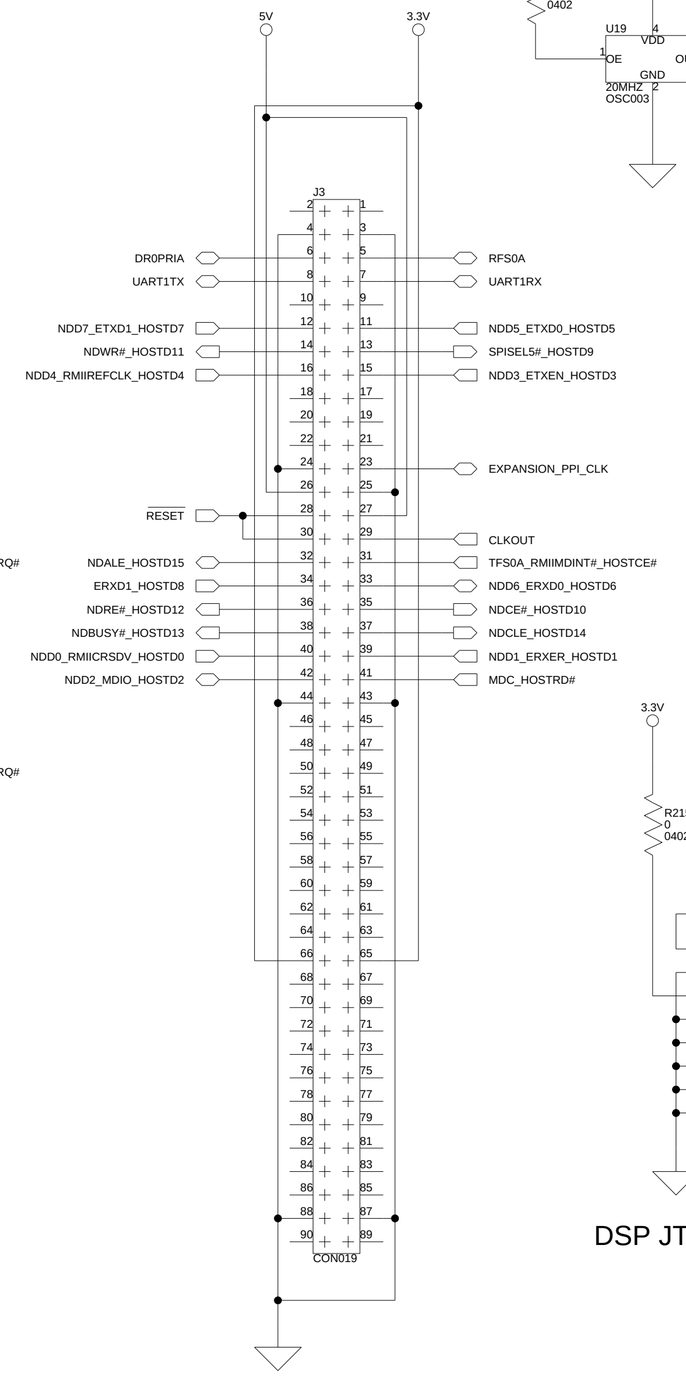
Size	Board No.	Rev
C	A0208-2006	2.0

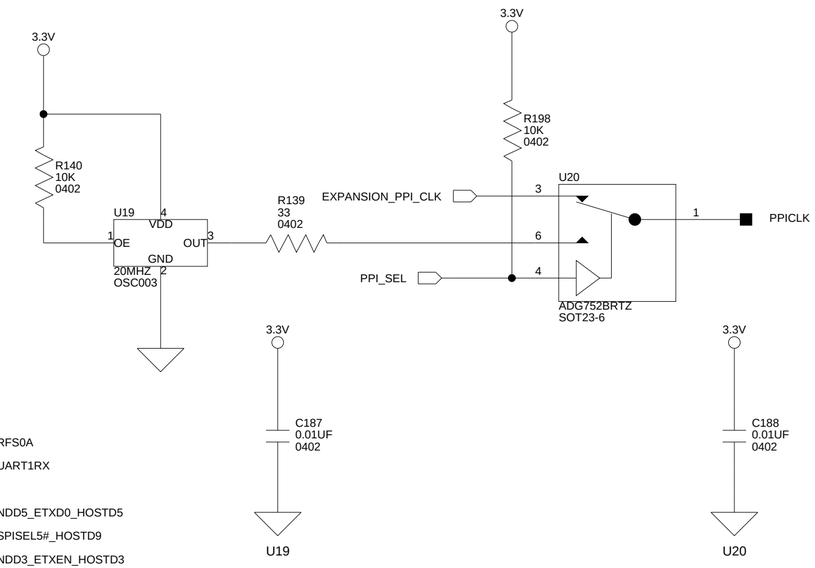
Date	Sheet
4-28-2009_15:57	10 of 13

"EXPANSION INTERFACE = TYPE B"



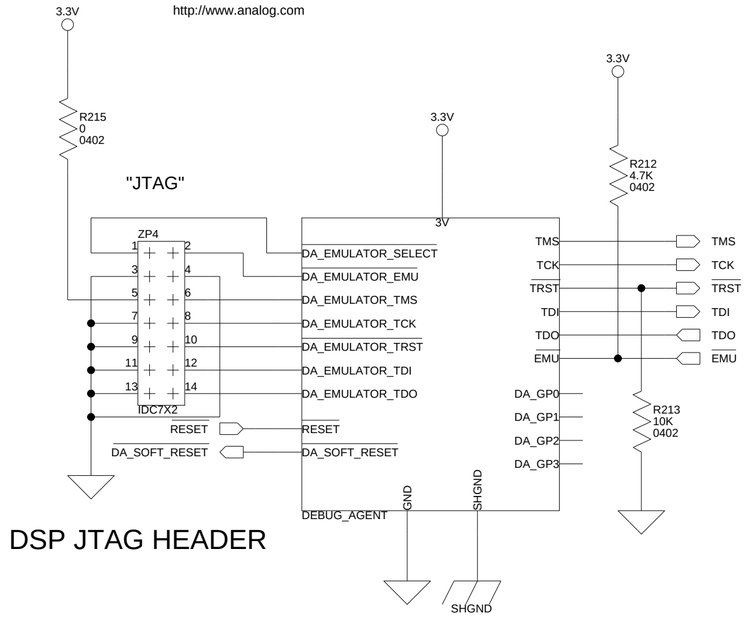






All USB interface circuitry is considered proprietary and has been omitted from this schematic.

When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com



DSP JTAG HEADER

ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
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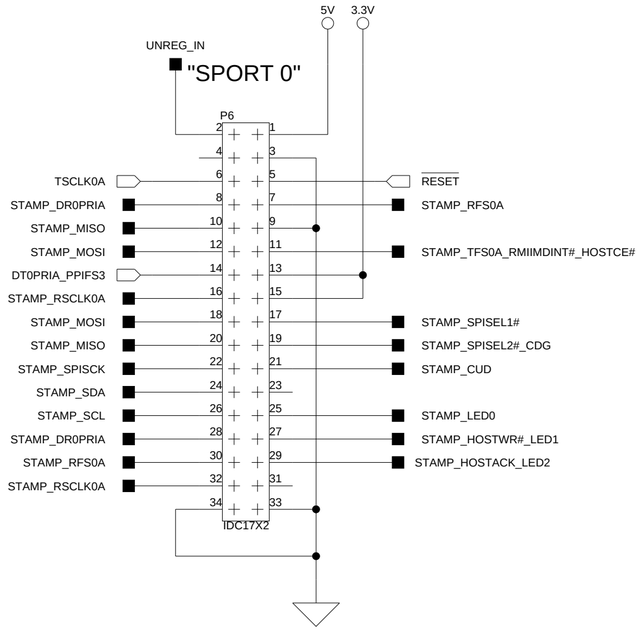
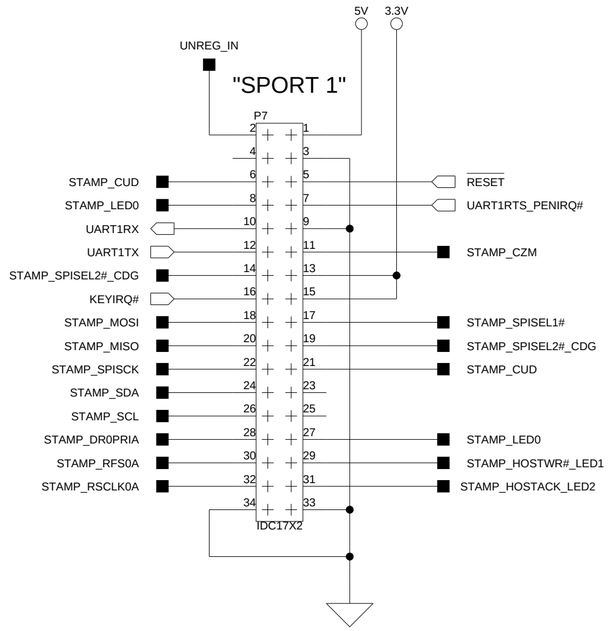
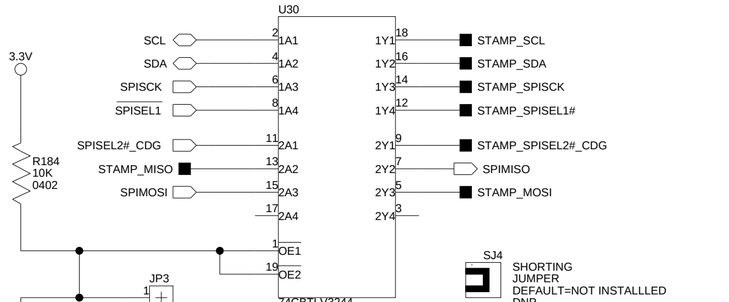
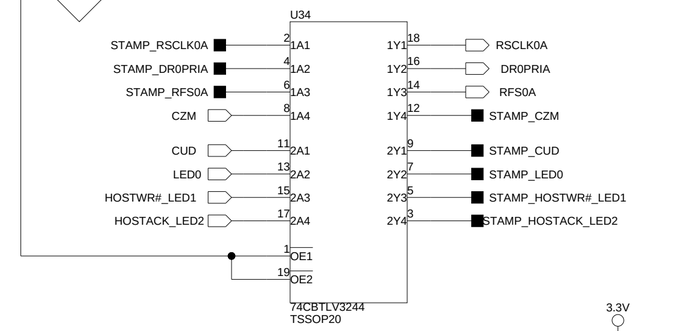
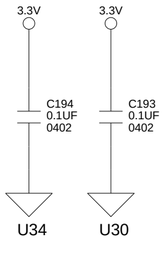
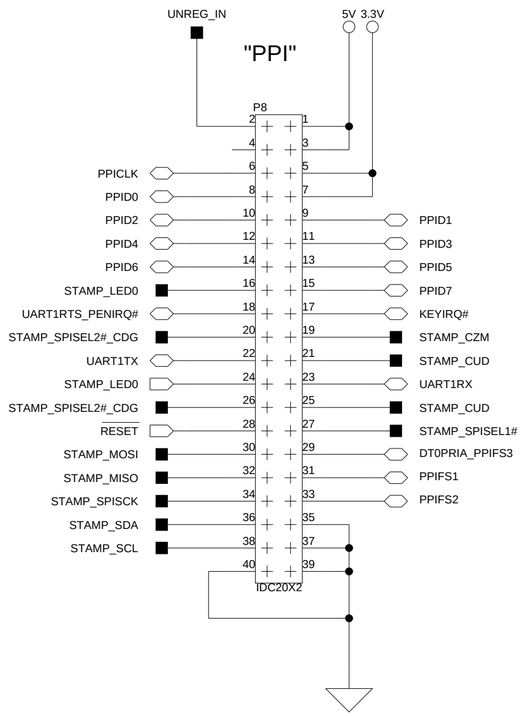


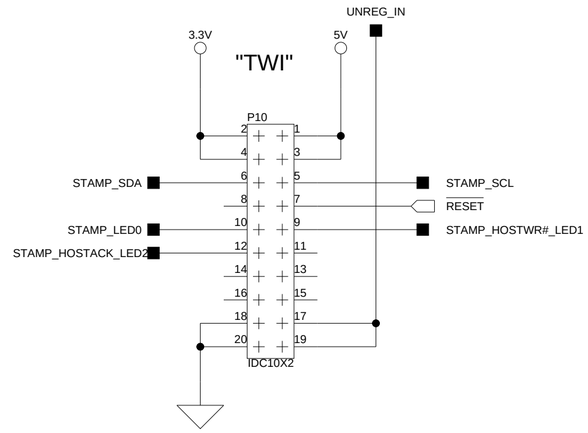


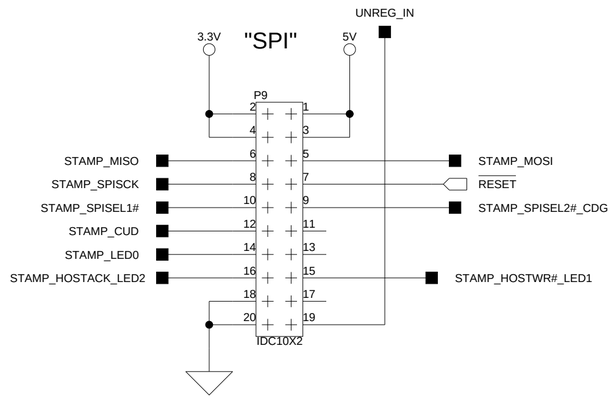


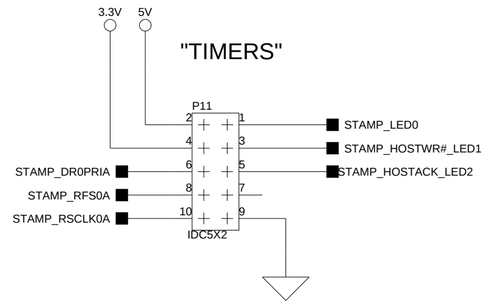


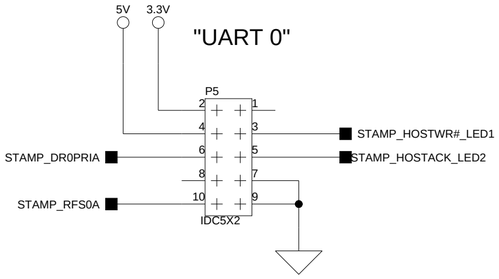




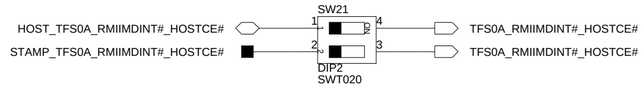








"TFS0A/HOSTCE"
"ENABLE"



SW21 disconnects TFS0A_RMIIMDINT#_HOSTCE#
from SPORT conn P6.11 and HOST conn P13.6

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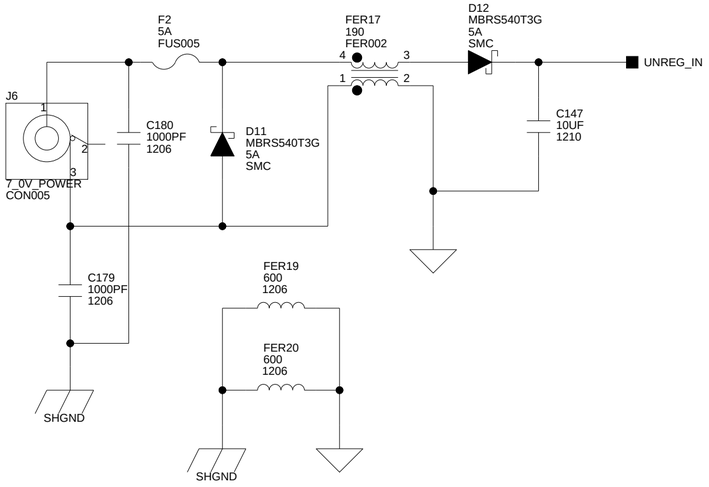
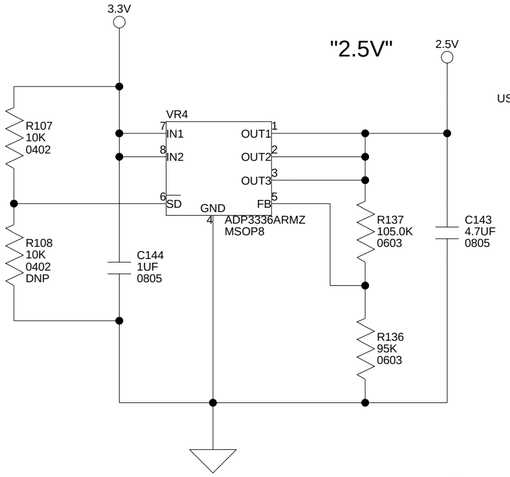
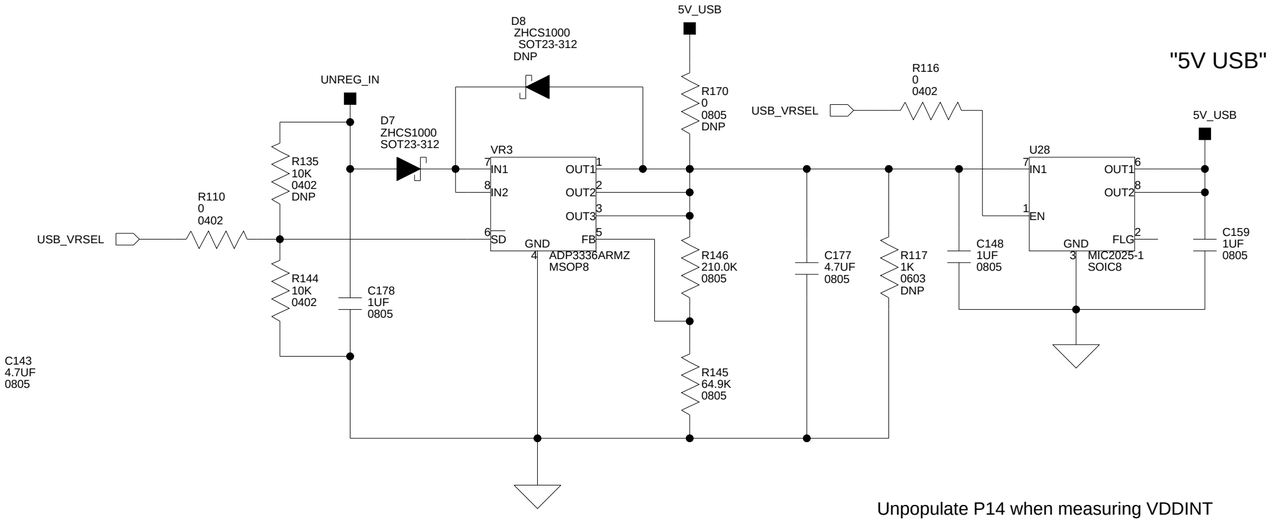
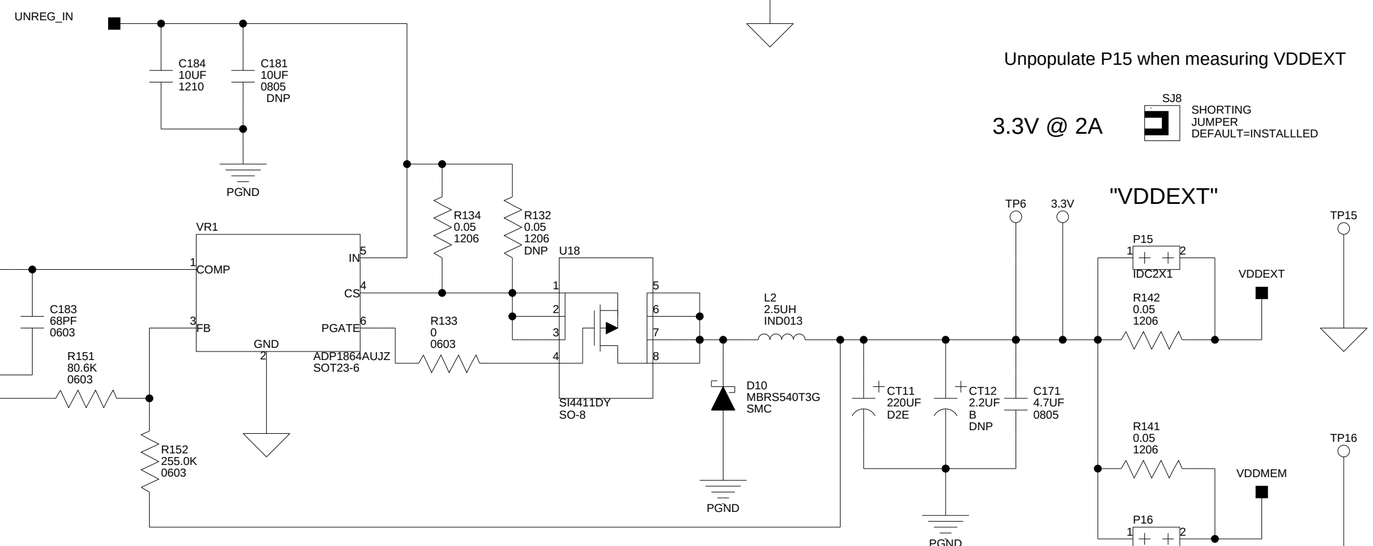






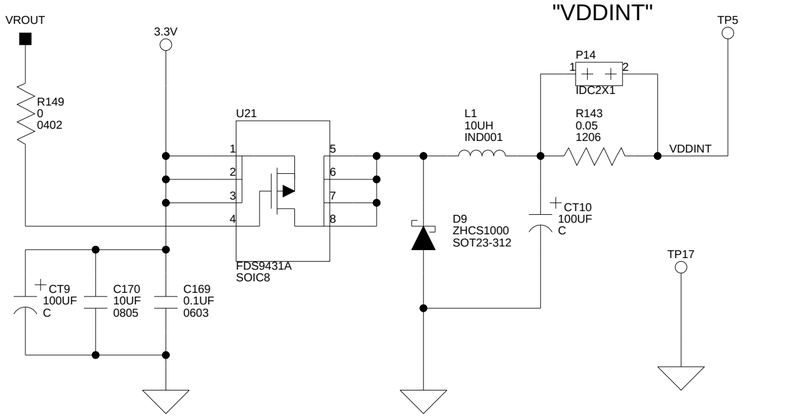
Unpopulate P14 when measuring VDDINT

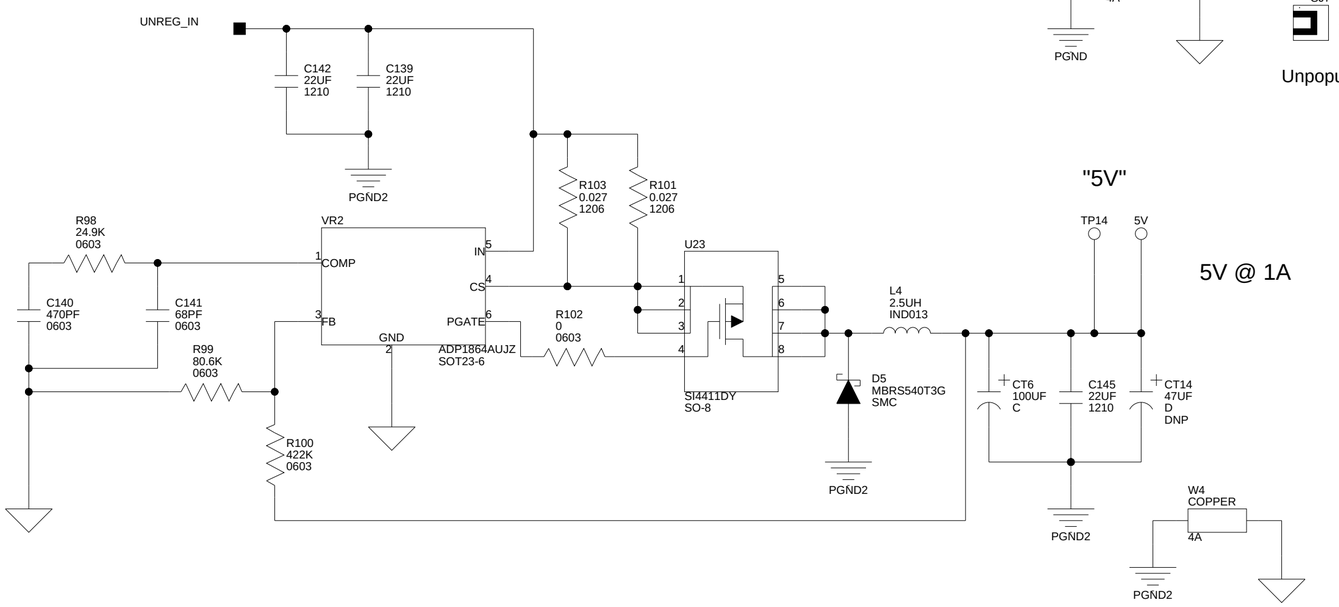


Unpopulate P15 when measuring VDDEXT

3.3V @ 2A

"VDDEXT"





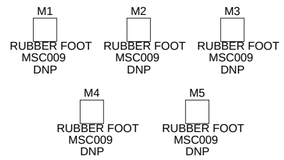
Unpopulate P16 when measuring VDDMEM

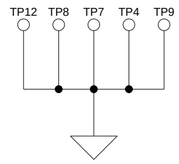
"VDDMEM"

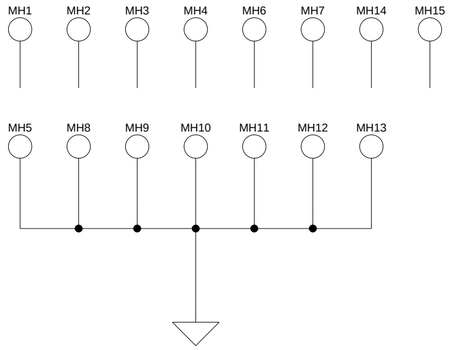
"5V"

5V @ 1A

"GND"







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U

V

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