

Data Sheet

Rev. 2.0 / January 2011

ZSSC3170

Automotive Sensor Signal Conditioner
with LIN and PWM Interface



ZSSC3170

Automotive Sensor Signal Conditioner with LIN and PWM Interface

ZMDI[®]
The Analog Mixed Signal Company



Brief Description

The ZSSC3170 is a CMOS integrated circuit for highly accurate amplification and sensor specific correction of bridge sensor signals. Featuring a maximum analog gain of 420, as well as extended offset compensation capabilities, the ZSSC3170 is adjustable to nearly all resistive bridge sensor types.

Digital compensation of offset, sensitivity, temperature drift, and nonlinearity is accomplished via a 16-bit RISC microcontroller. Conditioning coefficients are stored in an EEPROM certified for automotive applications.

Measured values are provided by one of the digital LIN or PWM interfaces. Each interface can support end-of-line calibration using the sensor output. Noise sensitivity is greatly reduced because the calibration equipment and the ZSSC3170 are mated digitally.

For quick and easy evaluation and support for calibrating prototypes, ZMDI offers the ZSSC3170 SSC Evaluation Kit, which includes evaluation hardware, SSOP20 samples, and software.

Features

- Complies with LIN specifications 1.3 / 2.0 / 2.1
- Configurable LIN publisher frame content
- Data conversion rate of up to 430Hz fully utilizes the maximum LIN channel capacity of 20kbit/s
- PWM high-side and low-side switches, support for LIN communication for end-of-line calibration
- Digital compensation of offset, gain, temperature effects up to 2nd order, and nonlinearity up to 3rd order. Compensation of temperature sensor offset, gain, and nonlinearity up to 2nd order.
- Internal or external temperature reference
- Media temperature sensing by diode or RTD
- Load dump protection of the LIN pin up to $\pm 40V$
- Operating temperature range: -40 to $125^{\circ}C$
- Extended operating temperature range: $\leq 150^{\circ}C$
- Accuracy
 - $\pm 0.25\%$ FSO @ -20 to $85^{\circ}C$
 - $\pm 0.50\%$ FSO @ -40 to $125^{\circ}C$
 - $\pm 1.00\%$ FSO @ -40 to $150^{\circ}C$
- 3 EEPROM words available for optional user data

Benefits

- Measurand and temperature signal available via one output pin
- Compatible with nearly all resistive bridge inputs
- No external trimming components required
- Single-pass calibration minimizes calibration costs
- End-of-line calibration using sensor output
- Optimized for automotive environments with special protection circuitry, excellent electro-magnetic compatibility, and numerous diagnostic features

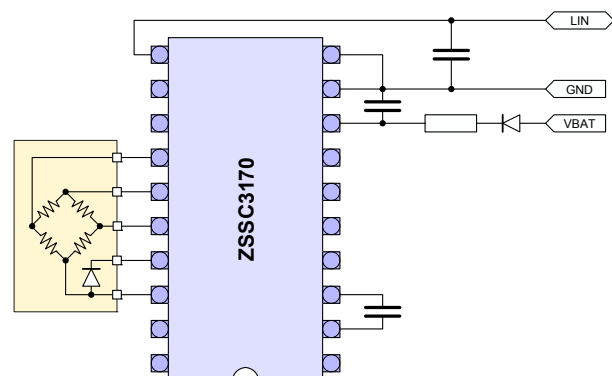
Available Support

- Evaluation Kit
- Application Notes
- Calculation Tools

Physical Characteristics

- Supply voltage: 7 to 18V
- Current consumption in Sleep Mode: $\leq 100\mu A$
- Input span: 1.8 to 267 mV/V
- ADC resolution: 13 to 14 bit
- Output resolution: up to 12-bit (LIN and PWM)
- Package: SSOP20 or die

ZSSC3170 Basic Circuit

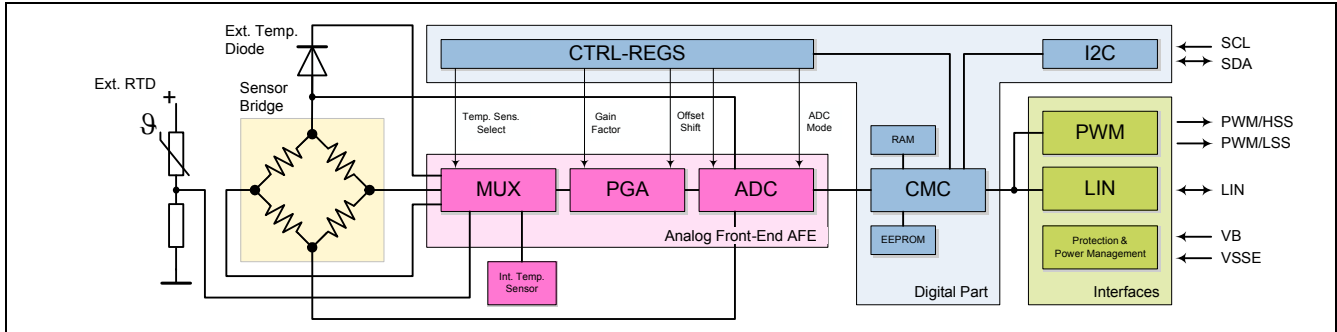


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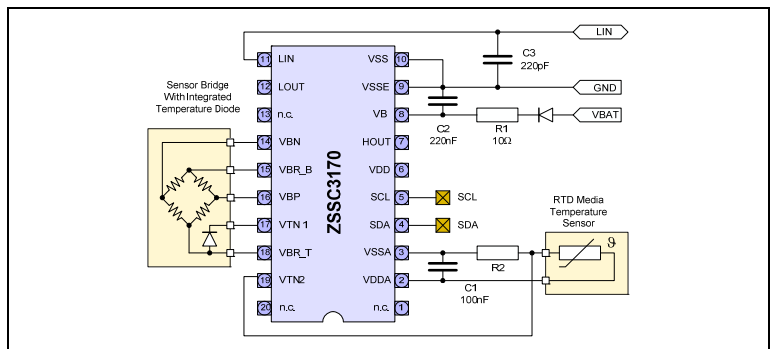
ZSSC3170 Block Diagram



Applications



LIN Pressure Sensor with Temperature Sensor



Ordering Information (Samples)

Product Sales Code	Description	Package
ZSSC3170DE1D	ZSSC3170 Die—Temperature Range -40 to 150°C	Waffle pack
ZSSC3170DA2T	ZSSC3170 SSOP20 (5.3mm)—Temperature Range -40 to 125°C	Tube (66 parts)
ZSSC3170KIT	ZSSC3170 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement, Software, Documentation, 5 SSOP20 Samples	Kit

For a complete set of product options, refer to the data sheet, section 7.

Sales and Further Information

www.zmdi.com

SSC@zmdi.com

Zentrum Mikroelektronik Dresden AG	ZMD America, Inc.	Zentrum Mikroelektronik Dresden AG, Japan Office	ZMD FAR EAST, Ltd.
Grenzstrasse 28 01109 Dresden Germany	8413 Excelsior Drive Suite 200 Madison, WI 53717 USA	2nd Floor, Shinbashi Tokyu Bldg. 4-21-3, Shinbashi, Minato-ku Tokyo, 105-0004 Japan	3F, No. 51, Sec. 2, Keelung Road 11052 Taipei Taiwan
Phone +49 (0)351.8822.7.772 Fax +49 (0)351.8822.8.7772	Phone +1 (608) 829-1987 Fax +1 (631) 549-2882	Phone +81.3.6895.7410 Fax +81.3.6895.7301	Phone +886 2 2377 8189 Fax +886 2 2377 8199

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1 ZSSC3170 Characteristics

1.1 Absolute Maximum Ratings

Parameters are valid without time limit unless otherwise noted.

Table 1.1: Absolute Maximum Ratings

No.	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1.1.1	Supply Voltage - PWM mode ¹ External pin VBAT	VBAT _{PWM}	-18		18	V	To VSSE (external GND) ²
1.1.2	Supply Voltage - PWM mode ¹ Pin VB	VB _{PWM}	-0.3		18	V	To VSSE ²
1.1.3	Supply Voltage - LIN mode ¹ External pin VBAT	VBAT _{LIN}	-18		40	V	To VSS (external GND) ²
1.1.4	Supply Voltage - LIN mode ¹ Pin VB	VB _{LIN}	-0.3		40	V	To VSS ²
1.1.5	Voltage at pin HOUT and LOUT ¹	V _{HOUT} , V _{LOUT}	-18		18	V	To VSSE ²
1.1.6	Voltage at pin LIN ¹	V _{LIN}	-40		40	V	To VSS ²
1.1.7	Analog Supply Voltage ³	VDDA	-0.3		6.5	V	To VSSA
1.1.8	Digital Supply Voltage ³	VDD	-0.3		6.5	V	To VSSA
1.1.9	Voltage at all analog or digital pins ³	V _{AIO} , V _{DIO}	-0.3		VDDA +0.3	V	To VSSA
1.1.10	Storage Temperature	T _{STRG}	-40		150	°C	
1.1.11	Extended Storage Temperature	T _{STRG_EXT}	-40		170	°C	t < 10h

1. Refer to ZSSC3170_HighVoltageProt_Rev*.pdf for detailed specification.

2. Refer to section 3.1 for the application circuit.

3. No measurement in mass production, parameter is guaranteed by design and / or quality monitoring.



1.2 Operating Conditions

Parameters are valid for the entire operating temperature range without time limit unless otherwise noted.

Table 1.2: Operating Conditions

No.	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1.2.1	Supply Voltage ¹	VB	8.2	12	16.5	V	Voltage at pin VB to VSSE
1.2.2	Supply Voltage - LIN mode ¹	VB _{LIN}	7	12	18	V	Voltage at pin VB to VSS
1.2.3	Ambient Temperature	T _{AMB}	-40		125	°C	
1.2.4	Extended Ambient Temperature	T _{AMB_EXT}	125		150	°C	2000h maximum
1.2.5	Ambient Temperature EEPROM Programming	T _{AMB_EEP}	-40		150	°C	See section 1.5
1.2.6	Bridge Resistance ²	R _{BR}	2		25	kΩ	

1. Refer to ZSSC3170_HighVoltageProt_Rev*.pdf for detailed specification.
2. No measurement in mass production, parameter is guaranteed by design and / or quality monitoring.

1.3 Electrical Parameters

If not otherwise specified, all parameter limits are valid within operating conditions defined in section 1.2, and without time limit.

All voltages are related to VSSA, if not otherwise specified.

Note: Refer to the important notes at the end of the table (page 12).

Table 1.3: Electrical Parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1.3.1	Supply Current and Internal Supply Voltages						
1.3.1.1	Supply Current	I _S			7	mA	Excluding bridge supply current; excluding PWM current; oscillator adjusted (typical 2 MHz)
1.3.1.2	Supply Current LIN Sleep Mode	I _{S_LINSLP}		40	100	μA	LIN Sleep Mode without current over LIN wire; PWM output pins not connected; VB _{LIN} = 14.4V for max. value V _{LIN} =VB _{LIN}
1.3.1.3	Internal Supply Voltage (generated internally)	V _{VDA}	4.3	5	6	V	V _{VDA} = V _{VDDA} - V _{VSSA} at R _{BR} ≥ 2kΩ (see 1.2.6)
1.3.1.4	Supply Voltage Sensor Bridge (internally at VDDA and VSSA)	V _{VBR}	V _{VDA} - 0.3V		V _{VDA}		V _{VBR} = V _{VBR_T} - V _{VBR_B} at R _{BR} ≥ 2kΩ (see 1.2.6)

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No.	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1.3.2	Analog Front End (Refer to section 2.3)						
1.3.2.1	Input Voltage Range	V_{IN_SPAN}	1		275	mV/V	Analog gain: 2.8 to 420
1.3.2.2	Maximum Bridge Sensor Offset Compensation	OC			388	% V_{IN_SPAN}	Depending on selected gain (see Table 2.3)
1.3.2.3	Bridge Input Current Difference ¹	I_{IN_DIFF}	-2		2	nA	$T_{AMB} = -25^{\circ}\text{C}$ to 85°C
1.3.2.4	Common Mode Input Voltage Range	V_{IN_CM}	0.29		0.65	V_{VBR}	Dependent on selected gain, XZC off (see Table 2.2); V_{VBR} see 1.3.1.4
1.3.3	Temperature Measurement (Refer to section 2.4)						
1.3.3.1	External Temperature Diode Channel Gain	A_{TSED}	300		1300	ppm FS/mV	
1.3.3.2	External Temperature Diode Bias Current	I_{TSED}	10	20	40	μA	
1.3.3.3	External Temperature Diode Input Range ¹	V_{TSED}	0		1.5	V	Related to V_{VBR_T}
1.3.3.4	External Temperature Resistor Channel Gain	A_{TSER}	1200		4500	ppm FS/ (mV/V)	
1.3.3.5	External Temperature Resistor Input Range ¹	V_{TSER}	0		1.5	V	Related to V_{VBR_T}
1.3.3.6	Internal Temperature Diode Sensitivity	ST_{TSI}	700		2700	ppm FS/K	Raw values, without conditioning calculation

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No.	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1.3.4 Sensor Diagnostic Tasks							
1.3.4.1	Sensor Connection Loss Resistance Threshold	RSCC _{TH}	20		100	kΩ	
1.3.4.2	Maximum Input Capacitance for Sensor Connection Check	CSCC			12	nF	Maximum: 10nF + 20% If Sensor Short Check is enabled, also Sensor Connection Check High-Capacitances Mode must be enabled. (see also 1.3.4.3)
1.3.4.3	Maximum Input Capacitance for Sensor Connection Check; Sensor Short Check and Sensor Aging Check are enabled	CSCC _{SSC/SAC}			1.2	nF	Maximum: 1nF + 20% For using Sensor Short Check and Sensor Aging Check at the same time.
1.3.4.4	Sensor Input Short Resistance Threshold	RSSC _{TH}	50		1000	Ω	
1.3.5 A/D Conversion (refer to section 2.3.3)							
1.3.5.1	ADC Resolution ¹	r _{ADC}			14	Bit	
1.3.5.2	DNL ¹	DNL _{ADC}			0.95	LSB	r _{ADC} = 14-bit, f _{OSC} = 2MHz, best fit, complete AFE, ADC _{INP_R} see 1.3.5.4
1.3.5.3	INL	INL _{ADC}			8	LSB	r _{ADC} = 14-bit, f _{OSC} = 2MHz, best fit, complete AFE, ADC _{INP_R} see 1.3.5.4
1.3.5.4	ADC Input Range	ADC _{INP_R}	10		90	% V _{VBR}	V _{VBR} see 1.3.1.4
1.3.6 PWM Output (Pins HOUT and LOU2)							
1.3.6.1	Output High Level HSS; Pin HOUT	V _{HSS_H}	4			V	I _{SOURCE} = 15mA, V _B ≥ 8.8V to VSSE
1.3.6.2	Output Low Level LSS; Pin LOU2	V _{LSS_L}			0.5V	V	I _{SINK} = 12mA to VSSE
1.3.6.3	Leakage Current Pin LOU2	I _{LEAK_LOU2}			50	μA	Sink; high level at LOU2
1.3.6.4	Rise Time HSS ¹	t _{HSS_RISE}			15	μs	V _{HOUT} = 0.5V→4V
1.3.6.5	Slew Rate HSS ¹	SR _{HSS}			2	V/μs	V _{HOUT} = 0.5V→4V
1.3.6.6	Fall Time LSS ¹	t _{LSS_FALL}			15	μs	V _{LOU2} = 4V→0.5V
1.3.6.7	Slew Rate LSS ¹	SR _{LSS}	-2			V/μs	V _{LOU2} = 4V→0.5V
1.3.6.8	PWM Full-Scale Resolution ¹	r _{PWM_FS}	11			Bit	PWM _{min_min} to PWM _{max_max}
1.3.6.9	Minimum Duty Cycle ¹	PWM _{min}	1		99	%	Adjustable with 8-bit resolution
1.3.6.10	Maximum Duty Cycle ¹	PWM _{max}	1		99	%	Adjustable with 8-bit resolution

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No.	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1.3.7	LIN Interface – Main Parameters² (all voltages related to VSS, R_{VBAT_LIN} = 500 Ω)						
1.3.7.1	Output Low Level Transmitter	V _{LIN_L}	0.6	1.2	2.0	V	
1.3.7.2	Output High Level Transmitter	V _{LIN_H}	0.9		1	VB	Driver off
1.3.7.3	Output Current	I _{LIN_L}	40	90	200	mA	Sink; driver on
1.3.7.4	Pull-Up Resistance	R _{LIN_PU}	20	30	47	kΩ	In series with diode to VB
1.3.7.5	Input Current LIN Recessive, Overvoltage at LIN	I _{LINPASrec}		3	20	μA	-40°C ≤ T _{AMB} ≤ 125°C; V _{LIN} ≥ VB; 7V ≤ VB ≤ 18V; 7V ≤ V _{LIN} ≤ 18V; driver off
				3	50	μA	125°C ≤ T _{AMB} ≤ 150°C; V _{LIN} ≥ VB; 7V ≤ VB ≤ 18V; 7V ≤ V _{LIN} ≤ 18V; driver off
1.3.7.6	Input Current LIN Dominant	I _{LINPASdom}	-1			mA	V _{LIN} = 0V; VB = 12V; driver off
1.3.7.7	Input Current LIN Recessive, Bus no GND	I _{LIN_NOGND}	-1		1	mA	0V ≤ V _{LIN} ≤ 18V; V _{GND} = V _{VB} ; VB = 12V
1.3.7.8	Input Current LIN Bus no VB	I _{LIN_LOSTVB}		3	20	μA	-40°C ≤ T _{AMB} ≤ 125°C; V _{GND} = V _{SUP} = 0V; 0V ≤ V _{LIN} ≤ 18V
				3	50	μA	125°C ≤ T _{AMB} ≤ 150°C; V _{GND} = V _{SUP} = 0V; 0V ≤ V _{LIN} ≤ 18V
1.3.7.9	Slew Rate ²	SR _{LIN}	0.5	1.3	3	V/μs	Rising and falling edges, transmit and receive
1.3.7.10	Input Low Level Receiver	V _{RECL}			0.4	VB	
1.3.7.11	Input High Level Receiver	V _{RECH}	0.6			VB	
1.3.7.12	Input Hysteresis Receiver	V _{RECHYS}	0.08		0.12	VB	V _{RECHYS} = V _{RECH} - V _{RECL}
1.3.7.13	Input Center Point Receiver	V _{BUS_CNT}	0.475	0.5	0.525	VB	V _{BUS_CNT} = (V _{RECL} + V _{RECH})/2
1.3.7.14	Duty Cycle 1	D1	0.396			-	TH _{Rec(max)} = 0.744 * VB; TH _{Dom(max)} = 0.581 * VB; VB = 7.0 to 18V; t _{Bit} = 50μs; D1 = t _{BUS_rec(min)} /(2 * t _{Bit})
1.3.7.15	Duty Cycle 2	D2			0.581	-	TH _{Rec(min)} = 0.422 * VB; TH _{Dom(min)} = 0.284 * VB; VB = 7.6 to 18V; t _{Bit} = 50μs; D1 = t _{BUS_rec(max)} /(2 * t _{Bit})
1.3.7.16	Duty Cycle 3	D3	0.417			-	TH _{Rec(max)} = 0.778 * VB; TH _{Dom(max)} = 0.616 * VB; VB = 7.0 to 18V; t _{Bit} = 96μs; D3 = t _{BUS_rec(min)} /(2 * t _{Bit})

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No.	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1.3.7.17	Duty Cycle 4	D4			0.590	-	$T_{H_{Rec}(min)} = 0.389 * V_B$; $T_{H_{Dom}(min)} = 0.251 * V_B$; $V_B = 7.6$ to $18V$; $t_{Bit} = 96\mu s$; $D4 = t_{BUS_rec(max)} / (2 * t_{Bit})$
1.3.8	System Response						
1.3.8.1	Start-Up Time ¹	t_{START}			30	ms	Until first valid output, $f_{OSC} = 2MHz$
1.3.8.2	Response Time LIN_Mode; Typical LIN Configuration ³	$t_{RESP_LIN_2_14_5}$			3.6	ms	$f_{OSC} = 2.2MHz$; 14-bit resolution; LIN Mode; 100% final value (see Table 2.5)
1.3.8.3	Response Time PWM Mode; Typical PWM Configuration ⁴	$t_{RESP_PWM_2_14_2}$			20	ms	$f_{OSC} = 1.8MHz$; 14-bit resolution; PWM Mode; 100% final value (see Table 2.4)
1.3.8.4	Overall Error AFE ^{5, 6}	F_{AFE_85} F_{AFE_125} F_{AFE_150}			0.25 0.5 1.0	% FS	$T_{AMB}: -20^{\circ}C$ to $85^{\circ}C$ $T_{AMB}: -40^{\circ}C$ to $125^{\circ}C$ $T_{AMB}: -40^{\circ}C$ to $150^{\circ}C$ $f_{OSC} = 2MHz$, XZC off; no sensor related errors; related to digital value
1. No measurement in mass production, parameter is guaranteed by design and/or quality observation. 2. For complete specification see <i>ZSSC3170_LIN_Interface_Description_Rev_*.pdf</i> . 3. 2 Step A/D Conversion (ADCORD=1), 14-bit Resolution (ADCRES=1), Resolution 2nd conversion step 5-bit (ADCMODE=11) 4. 2 Step A/D Conversion (ADCORD=1), 14-bit Resolution (ADCRES=1), Resolution 2nd conversion step 2-bit (ADCMODE=00) 5. Deviation from ideal line including INL, gain, offset & temperature errors. 6. With XZC active: additional total error of max. 25ppm/K at XZC = 31. Error decreases linearly at XZC < 31.							



1.4 Interface Characteristics

Table 1.4: Interface Characteristics

No.	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1.4.1	I²C™ Interface						
1.4.1.1	Input High Level ¹	V _{I2C_IN_H}	0.8			VDDA	
1.4.1.2	Input Low Level ¹	V _{I2C_IN_L}			0.2	VDDA	
1.4.1.3	Output Low Level ¹	V _{I2C_OUT_L}			0.15	VDDA	Open drain, I _{OL} < 2mA
1.4.1.4	SDA Load Capacity ¹	C _{SDA}			400	pF	
1.4.1.5	SCL Clock Frequency ¹	f _{SCL}			400	kHz	
1.4.1.6	Internal Pull-Up Resistor ¹	R _{I2C}	25		100	kΩ	
1.4.2	One Wire Interface at HOUT and LOUT (LIN Protocol)						
1.4.2.1	Input Low Level ¹	V _{OWI_IN_L}			1	V	
1.4.2.2	Input High Level ¹	V _{OWI_IN_H}	4			V	
1.4.2.3	Start Window ¹	t _{START_WIN}			30	ms	At f _{OSC} = 2MHz
1. No measurement in mass production, parameter is guaranteed by design and/or quality observation.							

1.5 EEPROM

Table 1.5: EEPROM

No.	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1.5.1	Write Cycles	n _{EEP_WRI_85}			1000		T _{AMB} < 85°C
		n _{EEP_WRI_150}			100		T _{AMB} < 150°C
1.5.2	Read Cycles	n _{EEP_RD}			8 * 10 ⁸		
1.5.3	Data Retention	t _{EEP_RET}			15	a	100000h@55°C + 27000h@125°C + 3000h@150°C
1.5.4	Programming Time	t _{EEP_WRI}		12		ms	Per written word, at f _{OSC} = 2MHz

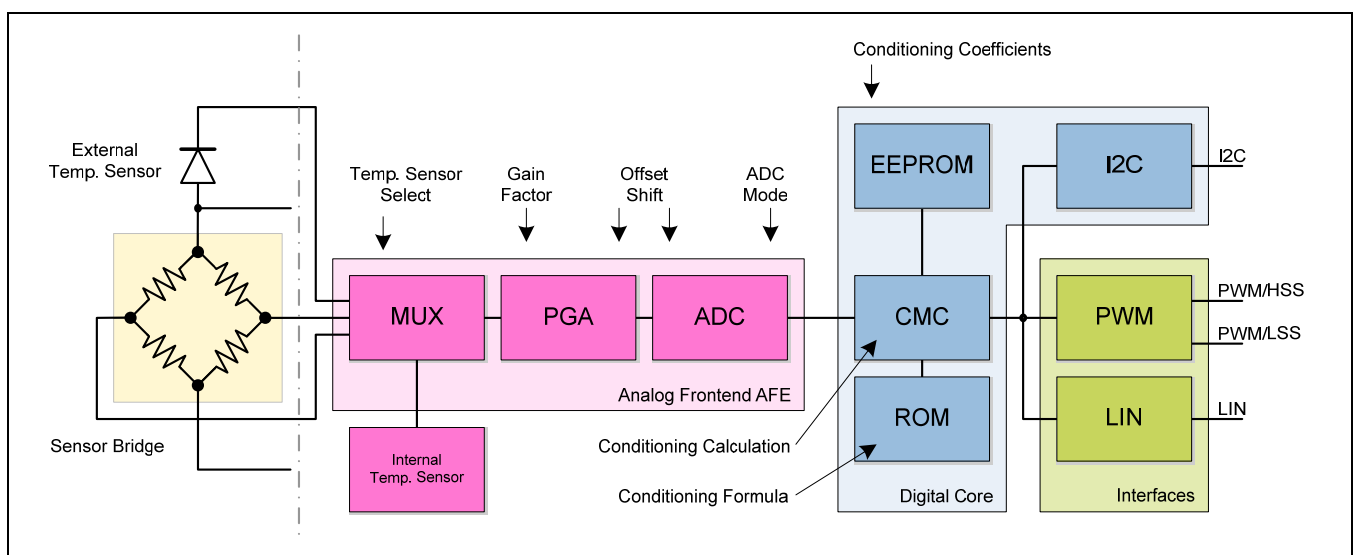


2 Circuit Description

2.1 Signal Flow and Block Diagram

The signal path of the ZSSC3170 consists of the analog front end (AFE), the digital signal processing block and interfaces including protection circuitry. Based on a differential structure, the bridge inputs VBP and VBN are handled by two signal lines each with a dynamic range symmetrical to the Common Mode Potential (Analog Ground equal to $VDDA/2$). Consequently, it is possible to amplify positive and negative input signals within the common mode range of the signal input.

Figure 2.1: Block Diagram of ZSSC3170



The multiplexer (MUX) transmits the signals from either the bridge sensor or the selected temperature sensors to the analog-to-digital converter (ADC) in a defined sequence. The temperature sensor can either be an external or internal diode or an external thermistor (RTD), selected by EEPROM configuration. In LIN mode, temperature output is available. For this temperature measurement the same temperature sensor can be used as for calibration temperature, but also a second temperature sensor input is selectable. The differential signal from the bridge sensor is pre-amplified by the programmable gain amplifier (PGA). The ADC converts bridge sensor and temperature signals into digital values.

The digital signal conditioning takes place in the calibration microcontroller (CMC) using a ROM-resident conditioning formula and sensor-specific coefficients stored in the EEPROM during calibration. The configuration data and the correction parameters can be programmed into the EEPROM by digital communication at the output pins or at the I²C interface. Depending on the programmed output configuration, the corrected sensor signal is output as PWM signal (high-side switch or low-side switch) or as digital value within a LIN frame. During the calibration procedure, the I²C interface can provide measurement values as well.

2.2 Application Modes

For each application, a configuration set must be established (generally prior to calibration) by programming the on-chip EEPROM for the following modes:

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Table 2.1: Application Modes

Bridge Sensor Channel	
Input Voltage Range	Select gain stage of the AFE with respect to the maximum sensor signal span and the zero point of the ADC.
Bridge Sensor Offset Compensation (XZC)	Activate the analog sensor offset compensation if required, e.g. if the sensor offset voltage is close to or larger than the sensor span.
Resolution/Response Time	Select appropriate resolution of the ADC. Settings will influence sampling rate, signal integration time, and therefore sensitivity to noise and disturbances.
Temperature Measurement	
Temperature Measurement for the Correction of the Bridge Signal	Select temperature sensor to calibrate temperature related errors.
Temperature Measurement for the Temperature Output in LIN Mode	Select temperature sensor for temperature measurement.
Output Signal	
Output Mode	Select PWM or LIN according to application requirements.
LIN Mode	Select LIN compatibility to specification package LIN2.1, LIN2.0, or LIN1.3.
PWM Mode	Select switch type high-side switch (HSS) or low-side switch (LSS).



2.3 Analog Front End (AFE)

The analog front end (AFE) consists of the signal multiplexer (MUX), the programmable gain amplifier (PGA) and the analog-to-digital converter (ADC).

2.3.1 Programmable Gain Amplifier (PGA)

Table 2.2 shows the adjustable gains, the corresponding sensor signal spans and the common mode range limits.

Table 2.2: Adjustable Gain Stages, Corresponding Sensor Signal Spans, and Common Mode Ranges

No.	Overall Gain a_{IN}	Maximum Input Voltage Range V_{IN_SPAN} [mV/V] ¹	Gain Amp1	Gain Amp2	Gain Amp3	Input Common Mode Range V_{IN_CM} [%VDDA] ²	
						XZC off	XZC on
1	420	1.8	30	7	2	29 to 65	45 to 55
2	280	2.7	30	4.66	2	29 to 65	45 to 55
3	210	3.6	15	7	2	29 to 65	45 to 55
4	140	5.4	15	4.66	2	29 to 65	45 to 55
5	105	7.1	7.5	7	2	29 to 65	45 to 55
6	70	10.7	7.5	4.66	2	29 to 65	45 to 55
7	52.5	14.3	3.75	7	2	29 to 65	45 to 55
8	35	21.4	3.75	4.66	2	29 to 65	45 to 55
9	26.3	28.5	3.75	3.5	2	29 to 65	45 to 55
10	14	53.75	1	7	2	29 to 65	45 to 55
11	9.3	80	1	4.66	2	29 to 65	45 to 55
12	7	107	1	3.5	2	29 to 65	45 to 55
13	2.8	267	1	1.4	2	32 to 57	not applicable

1. Recommended internal signal range: maximum 75% supply voltage. Range is defined by 75% supply voltage divided by selected gain.
2. At maximum input signal (with XZC: +300% offset).

2.3.2 Offset Compensation

The ZSSC3170 supports two methods of sensor offset compensation:

- Digital offset correction is processed during the digital signal conditioning by the calibration microcontroller (CMC).
- Bridge sensor offset compensation (XZC) is achieved by adding a compensation voltage at the analog signal path that removes coarse offset. XZC is needed for large offset values, which would otherwise overdrive the analog signal path and can be adjusted by 6 EEPROM bits. Depending on the gain adjustment, XZC can handle offset values of up to 300% of the sensor signal range.



Table 2.3: Bridge Sensor Offset Shift Ranges

Overall Gain a_{IN}	Maximum Input Voltage Range V_{IN_SPAN} [mV/V]	Offset Shift per Step [%Full Span]	Approximate Maximum Offset Shift [mV/V]	Approximate Maximum Offset Shift [% V_{IN_SPAN}]
420	1.8	12.5	7.8	388
280	2.7	7.6	7.1	237
210	3.6	12.5	15.5	388
140	5.4	7.6	14.2	237
105	7.1	12.5	31	388
70	10.7	7.6	28	237
52.5	14.3	12.5	62	388
35	21.4	7.6	57	237
26.3	28.5	5.2	52	161
14	53.6	12.5	233	388
10	80	7.6	207	237
7	107	5.2	194	161
2.8	267	0.83	78	26

2.3.3 Analog-to-Digital Converter

The analog-to-digital converter (ADC) is designed in full differential switched capacitor technology with a selectable resolution of 13 or 14-bit. The ADC can operate in first or second order configuration. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency.

- **MSB segment conversion:** In this first step of the A/D conversion the measurement value is being integrated over the complete conversion time ensuring a high degree of noise suppression. To extend the integration phase to the maximum, this fraction of the complete conversion time is selected as long as possible corresponding to the time available.
- **LSB segment conversion:** To achieve a higher resolution, the residual value of the first step is converted in a subsequent step by a second converter. In first order configuration, the second step is skipped (single-step conversion).



Table 2.4: A/D Resolution and Conversion Time in PWM Modes

Mode	A/D Resolution Total [bit]	A/D Resolution MSB Segment Conversion [bit]	A/D Resolution LSB Segment Conversion [bit]	A/D Conversion Mode ADCMODE ¹	PWM Cycle Time (f _{osc} = 1.8MHz) [ms]
PWM / ADC 2 step ¹	14	12	2	00	19.9
	14	11	3	01	10.8
	14	10	4	10	6.3
	14	9	5	11	4.0
	13	11	2	00	10.8
	13	10	3	01	6.3
	13	9	4	10	4.0
	13	8	5	11	2.8
PWM / ADC 1 step	14	14	n/a	n/a	37.5
	13	13	n/a	n/a	19.3

1. See ZSSC3170_FunctionalDescription_Rev_*.pdf for details

Table 2.5: A/D Resolution and Conversion Time in LIN Modes

Mode	A/D Resolution Total [bit]	A/D Resolution MSB Segment Conversion [bit]	A/D Resolution LSB Segment Conversion [bit]	A/D Conversion Mode ADCMODE ¹	Response Time ² in LIN mode (f _{osc} = 2.2MHz) [ms]
LIN / ADC 2 step	14	12	2	00	16.3
	14	11	3	01	8.9
	14	10	4	10	5.2
	14	9	5	11	3.3
	13	11	2	00	8.9
	13	10	3	01	5.2
	13	9	4	10	3.3
	13	8	5	11	2.4
LIN / ADC 1 step	14	14	n/a	n/a	61.5
	13	13	n/a	n/a	31.7

1. See ZSSC3170_FunctionalDescription_Rev_*.pdf for details

2. 100% final value



The following equation describes the conversion result:

$$Z_{\text{ADC}} = 2^r * (V_{\text{ADC_IN}} / V_{\text{ADC_REF}} - \text{RS}_{\text{ADC}})$$

Where

Z_{ADC} :	A/D conversion result
r :	A/D resolution in bits
$V_{\text{ADC_IN}}$:	Differential input voltage of ADC
$V_{\text{ADC_REF}}$:	Differential reference voltage of ADC
RS_{ADC} :	ADC range shift adjustable by EEPROM configuration ($\text{RS}_{\text{ADC}} = 1/16, 1/8, 1/4, 1/2$)

By selecting different values of RS_{ADC} the sensor input signal can be matched to the optimum input voltage range of the ADC. The ADC reference voltage $V_{\text{ADC_REF}}$ is defined as the difference of the bridge supply potentials at pins VBR_T and VBR_B. The theoretical ADC input voltage range $\text{ADC}_{\text{INP_R}}$ is equal to this ADC reference voltage.

A major constraint required for achieving the specified precision as well as the stability and nonlinearity parameters of the AFE is to use a maximum ADC input voltage range of 10% to 90% of $\text{ADC}_{\text{INP_R}}$ within the application. This is of special importance for guarantying the specified parameters for the entire operating temperature range as well as all possible sensor bridge tolerances. The validity of these conditions is not checked by the ZSSC3170's fail-safe functions and therefore must be ensured by the customer-specific configuration.

2.4 Temperature Measurement

The following temperature sensors are supported by ZSSC3170 for both temperature and calibration temperature measurement:

- Internal pn-diode
- External pn-diode; anode to pin VBR_T
- External resistive half-bridge with the thermistor connected in the upper branch

In PWM mode, the conditioning calculation for the bridge sensor signal is based on values of the selected temperature sensor.

In LIN mode, two temperature measurements are executed using either two different sensors or one sensor for both measurements. The temperature output value is the result of a conditioning calculation including offset compensation, gain correction and 2nd order nonlinearity compensation. The conditioning coefficients are stored in the EEPROM.



2.5 System Control and Conditioning Calculation

The system control performs the following tasks:

- Sequencing of the start-up phase
- Control of measurement cycle based on EEPROM configuration data
- 16-bit conditioning calculation for each measurement signal based on EEPROM conditioning coefficients and ROM-resident signal conditioning algorithm
- Processing of communication requests received at the serial interfaces
- Control of calibration mode
- Processing of diagnostic and fail-safe tasks

For a detailed description, refer to the document *ZSSC3170_FunctionalDescription_Rev_*.pdf*.

2.5.1 Operating Modes

Three main modes are implemented in the integrated state machine:

- Normal Operation Mode (NOM) with continuous signal conditioning
- Command Mode (CM) provides access to all internal registers; provides the basis for configuration and calibration of the ZSSC3170
- Diagnostic Mode (DM) indicating detected error conditions

2.5.2 Start-Up Phase

The start-up phase consists of the following time periods:

- Settling of the internal voltage supply represented by the voltage VDDA-VSSA. At the end of this period, the power-on-reset circuit (POR) switches off the reset signal.
- System start, readout of EEPROM, and signature check.
- Processing of the signal conditioning start routine containing bridge sensor signal and temperature measurements, associated auto-zero measurements and the conditioning calculation itself. Within this period the output pins are ready to receive special LIN frames resulting in a switch over to the Command Mode. This start window is active for up to 30ms.

The ZSSC3170 switches into Normal Operation Mode (NOM) after the start window is passed. It proceeds with the cyclic processing of the measurement and conditioning tasks.



2.5.3 Measurement Cycle

Depending on the EEPROM settings, the multiplexer selects the following inputs in a defined sequence:

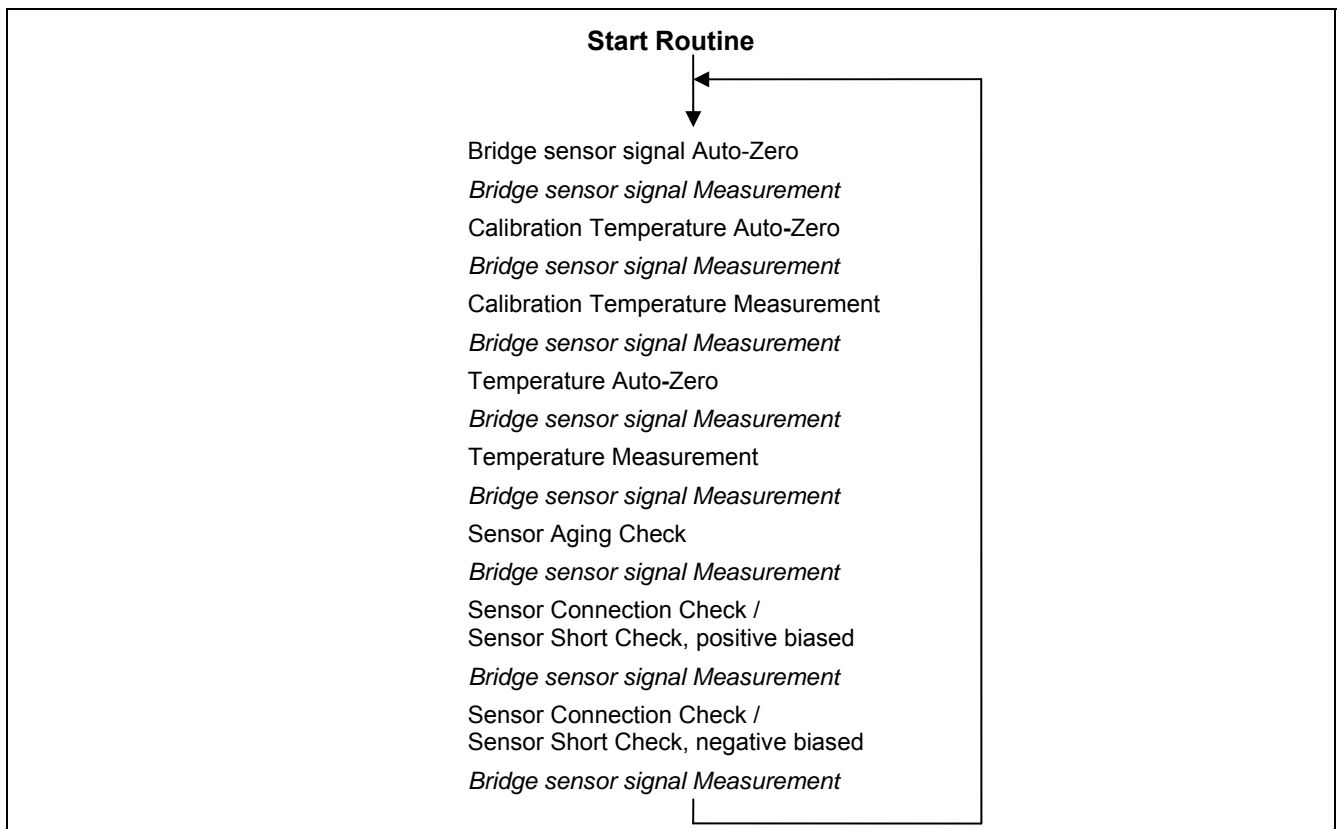
- Pre-amplified sensor bridge signal
- Temperature sensor defined by EEPROM configuration for calibration temperature
- Temperature sensor defined by EEPROM configuration for temperature measurement
- Auto-zero signal
- Diagnostic signals

The CMC controls the complete measurement cycle following a basic flow shown in Figure 2.2.

All necessary measurements for bridge sensor and temperature signal are executed once after power-on within the start-up routine. This initial phase is followed by continuous processing of the complete measurement cycle. The sensor connection check (SCC), sensor short check (SSC), and sensor aging check (SAC) for diagnostic tasks (see section 2.8) are continuously executed within the regular measurement cycle even if the processing of the diagnostic function is disabled by the EEPROM configuration.

For details, refer to *ZSSC3170_FunctionalDescription_Rev_*.pdf*.

Figure 2.2: Measurement Cycle





2.5.4 Conditioning Calculation

After digital auto-zero correction of the bridge sensor measurement value, the interim result is further processed based on the correction formula. Offset and gain with temperature effects up to 2nd order and non-linearity up to 3rd order can be compensated for resulting in a positive 15-bit bridge sensor result value normalized to the range of [0;1].

In LIN mode, the digital measurement value of the temperature is processed based on a proprietary correction formula as well. Offset, gain and non-linearity up to 2nd order can be compensated for yielding a positive 15-bit temperature value normalized to the range of [0;1].

2.6 Signal Outputs

ZSSC3170 provides three signal outputs:

- LIN – LIN Interface revision 2.1/2.0 with compatibility to revision 1.3
- HOUT – PWM high-side switch (HSS)
- LOUT – PWM low-side switch (LSS)

For the respective application, one signal output must be selected and configured as the active output. Idle outputs must be not connected.

To enter the Command Mode, communication can be established at each of the three output pins. A dedicated command must be sent during the start window immediately after power-on (duration $t_{\text{START_WN}}$; see 1.4.2.3). The communication protocol at all pins is based on LIN Data Link Layer. Note that communication at pin HOUT uses inverted signal levels of the LIN frame. In LIN mode, communication at pin LIN is always possible during Normal Operation.

To enable communication within the start window, the output drivers are set to tri-state during this time. The outputs HOUT and LOUT are connected to internal pull resistors to ensure the necessary resistive stage. For the LIN transceiver, an internal pull-up resistor is implemented by default (acc. to LIN specification package, section physical layer).

If not switched into the Command Mode before expiration of the 30ms start window, depending on the configuration, the ZSSC3170 will start to provide a PWM signal or can respond to communication requests of the LIN master.

The function set of the signal outputs is specified in detail in the documents *ZSSC3170_FunctionalDescription_Rev_*.pdf* and *ZSSC3170_LIN_Interface_Description_Rev_*.pdf*.

2.6.1 PWM Outputs HOUT and LOUT

In PWM mode, the output signal is provided at the pins HOUT or LOUT accordingly.

The outputs are protected from short circuit overload by current limiters and time monitoring. Driving the signal lines with slew-rate-limited edges reduces electromagnetic emission. At the pin HOUT, a voltage higher than maximum supply voltage can be tolerated. The notably low leakage current of LOUT is designed to cover the requirements of some unique electronic control units (ECU).



2.6.2 LIN Output

The output of the integrated LIN transceiver at pin LIN is compatible to the LIN revisions 2.1, 2.0 and 1.3. For details, refer to the document *ZSSC3170_LIN_Interface_Description_Rev_*.pdf*. For LIN Physical Layer Conformance Tests, the control pins of the integrated LIN transceiver can be accessed separately in a LIN Conformance Test Mode.

2.7 Digital Test and Calibration Interface

Beyond the digital communication features via the output pins, the ZSSC3170 provides an I²C compatible test and calibration interface with slave functionality. Refer to the document *ZSSC3170_FunctionalDescription_Rev_*.pdf* for a detailed description of the I²C interface.

2.8 Diagnostic and Fail-safe Features, Watchdog and Error Detection

The ZSSC3170 detects various possible failures. An identified failure is indicated by changing to the Diagnostic Mode (DM). With PWM active, the respective output is switched to the resistive mode. In LIN mode, depending on the error classification the respective status bits are activated. A watchdog observes the continuous working of the CMC and the running measurement loop. The operation of the internal clock oscillator is watched by the oscillator failure detection. A check of the sensor bridge for broken or shorted wires is done continuously (the sensor connection check (SCC) and the sensor short check (SSC)). Additionally the common mode voltage of the sensor (CMV) is watched continuously (sensor aging check (SAC)). A check of broken chip (BCC) can be applied in start-up phase after power-on. RAM, ROM, EEPROM, registers, and the arithmetic unit are watched continuously. Refer to the *ZSSC3170_FunctionalDescription_Rev_*.pdf* for a detailed description.

2.9 High Voltage, Reverse Polarity and Short Circuit Protection

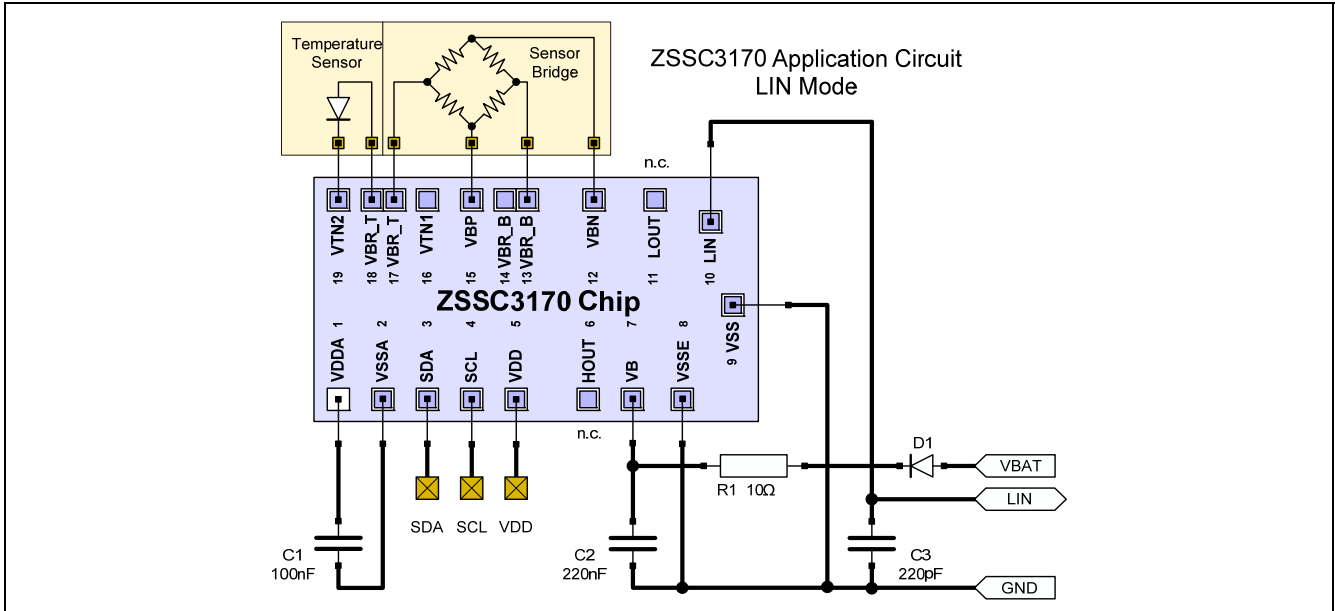
The ZSSC3170 is designed for a direct 12V supply, which can be provided by a vehicle power system. Internal sub-assemblies are supplied and protected by integrated voltage regulators and limiters. Specific protection circuits allow tolerance of permanent reverse polarity at supply and output pins. These functions are described in detail in the document *ZSSC3170_HighVoltageProt_Rev_*.pdf*. When operated in the application circuits shown in section 3, the protection features of the ZSSC3170 are guaranteed without time limit.

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Figure 3.3: Application Circuit in LIN Mode



3.2 Dimensioning of External Components

For application circuits, refer to Figure 3.1, Figure 3.2, and Figure 3.3.

Table 3.1: Dimensioning of External Components for Application Examples

No.	Component	Symbol	Condition	Min	Typ	Max	Unit
3.2.1	Capacitor	C1	All modes		100		nF
3.2.2	Capacitor	C2	HSS		470		nF
3.2.3	Capacitor	C2	LSS, LIN		220		nF
3.2.4	Capacitor	C3	HSS		4.7		nF
3.2.5	Capacitor	C3	LSS		2.2		nF
3.2.6	Capacitor	C3	LIN		220		pF
3.2.7	Resistor	R1	LIN		10		Ω
3.2.8	Resistor	R1	LSS, HSS		27		Ω
3.2.9	Diode	D1	All modes		Standard Si diode		

The capacitor values are examples and must be adapted to the requirements of the specific application, in particular to the EMC requirements. In the LIN application, the voltage drop over the series connection of D1 and R1 must not exceed 1V at maximum supply current. For overvoltage pulses at VBAT, R1 serves as a current limiter.



4 ESD Protection and EMC Specification

All pins have an ESD protection of >2000V according to the Human Body Model (HBM). Additionally the pins VDDE, VSSE, VSS, HOUT and LOUT have an ESD protection of >4000V and the pin LIN has an ESD protection of >8000V (system level).

The level of ESD protection has been tested with devices in SSOP20 packages during the product qualification. The ESD test follows the Human Body Model with 1.5kOhm/100pF based on MIL883, Method 3015.7 (except the LIN pin tests). The ESD test of the LIN pin follows the system level specification with 330Ω/150 pF (according to DIN EN 61000-4-2).

The EMC performance regarding external disturbances as well as EMC emission is documented in *ZSSC3170_HighVoltageProt_Rev_*.pdf*.



5 Pinout and Package

Table 5.1: Pin Definition of ZSSC3170

Pin Die	Pin SSOP20	Name	Description	Remarks
1	2	VDDA	Positive Analog Supply Voltage	Power supply
2	3	VSSA	Negative Analog Supply Voltage	Ground
3	4	SDA	I ² C Clock	Analog I/O, internal pull-up
4	5	SCL	I ² C Data IO	Analog input, internal pull-up
5	6	VDD	Positive Digital Supply Voltage	Power supply
6	7	HOUT	PWM High-Side Switch	High voltage I/O
7	8	VB	Positive External Supply Voltage	High voltage I/O
8	9	VSSE	External Ground (PWM Modes)	High voltage I/O
9	10	VSS	Ground (LIN Mode)	Ground
10	11	LIN	LIN	LIN high voltage I/O
11	12	LOUT	PWM Low-Side Switch	High voltage I/O
12	14	VBN	Negative Input Sensor Bridge	Analog input
13 / 14	15	VBR_B	Negative (Bottom) Bridge Supply Voltage	Analog I/O
15	16	VBP	Positive Input Sensor Bridge	Analog input
16	17	VTN1	Temperature Sensor 1	Analog I/O
17 / 18	18	VBR_T	Positive (Top) Bridge Supply Voltage	Analog I/O
19	19	VTN2	Temperature Sensor 2	Analog I/O

The two-fold implementation of the bridge supply bond pads enables direct bonding from the ZSSC3170 pads to supply pads on the sensor die.

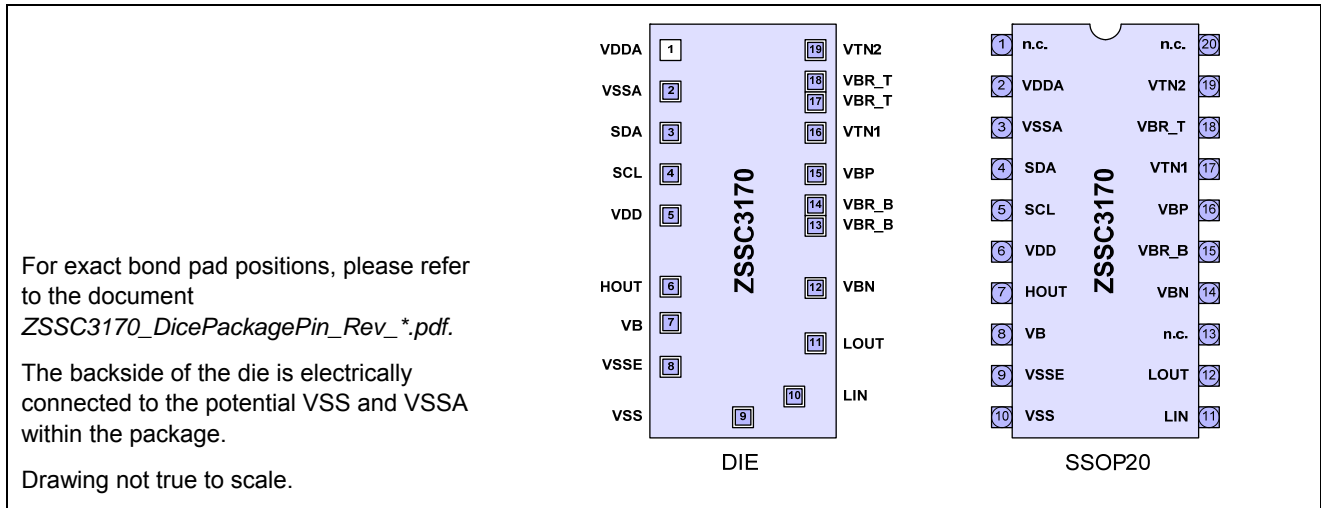
For packaged parts, a SSOP20 Green Package with 5.3mm body and 0.65mm lead pitch is the standard form of delivery.

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Figure 5.1: Pin Configurations for Different Packaging Options



6 Reliability and RoHS Conformity

The ZSSC3170 is qualified according to the AEC-Q100 standard, operating temperature grade 0.

The ZSSC3170 complies with the RoHS directive and does not contain hazardous substances.

The complete RoHS declaration update can be downloaded at www.zmdi.com/quality.

7 Ordering Information

Product Sales Code	Description	Package
ZSSC3170DE1B	ZSSC3170 Die - Temperature Range -40 to 150°C	Wafer
ZSSC3170DE1C	ZSSC3170 Die - Temperature Range -40 to 150°C	Sawn on frame
ZSSC3170DE1D	ZSSC3170 Die - Temperature Range -40 to 150°C	Waffle pack
ZSSC3170DA2T	ZSSC3170 SSOP20 (5.3mm) - Temperature Range -40 to 125°C	Tube (66 parts)
ZSSC3170DA2R	ZSSC3170 SSOP20 (5.3mm) - Temperature Range -40 to 125°C	Reel (2000 parts)
ZSSC3170KIT	ZSSC3170 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement, Software, Documentation, 5 SSOP20 Samples	Kit

8 Related Documents

Document	File Name
Functional Description	ZSSC3170_FunctionalDescription_Rev_*.pdf
High Voltage Protection Description	ZSSC3170_HighVoltageProt_Rev_*.pdf
LIN Interface Description	ZSSC3170_LIN_Interface_Description_Rev_*.pdf
Wafer, Die and Pad Geometry Documentation	ZSSC3170_DicePackagePin_Rev_*.pdf



Visit ZMDI's website www.zmdi.com or contact your nearest sales office for the latest version of these documents.

9 Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front-End
Amp	Amplifier
CM	Command Mode
CMC	Calibration Micro Controller; optimized micro controller architecture for ZMDI signal conditioners
CMV	Common Mode Voltage (of the sensor bridge signal)
DM	Diagnostic Mode
DNL	Differential Nonlinearity
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FSO	Full Scale Output
HSS	High-Side Switch; open-drain output; connects to positive supply when active
I/O	Input/Output
I ² C	Inter-Integrated Circuit; serial two wire data bus, trade mark of Philips Semiconductors
INL	Integral Nonlinearity
LIN	Local Interconnect Network; international communication standard
LSB	Least Significant Bit
LSS	Low-Side Switch; open-drain output; connects to ground when active
MSB	Most Significant Bit
MUX	Multiplexer
NOM	Normal Operation Mode
P	Bridge Sensor Signal; e.g. Pressure
PGA	Programmable Gain Amplifier
POR	Power-On Reset; defined start-up procedure until nominal supply voltage is reached
PWM	Pulse Width Modulation
Rev.	Revision
RISC	Reduced Instruction Set Computing
RoHS	Restrictions of Hazardous Substances
ROM	Read Only Memory

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Term	Description
RTD	Resistance Temperature Detector
SAC	Sensor Aging Check; diagnostic measurement task
SCC	Sensor Connection Check; diagnostic measurement task
SSC	Sensor Short Check; diagnostic measurement task
SSOP	Shrink Small Outline Package
T	Temperature
XZC	Bridge sensor offset compensation (Extended Zero Compensation)

ZSSC3170

Automotive Sensor Signal Conditioner with LIN and PWM Interface



10 Document Revision History

Revision	Date	Description
V1.0	2009-04-05	First Release of Document
V1.3	2010-09-20	Completely revised Data Sheet.
V2.0	2011-01-17	Version Changed from C to D, Second Release of Document, Remark "Preliminary" deleted

Sales and Further Information

www.zmdi.com

SSC@zmdi.com

Zentrum Mikroelektronik Dresden AG

Grenzstrasse 28
01109 Dresden
Germany

Phone +49 (0)351.8822.7.772
Fax +49 (0)351.8822.8.7772

ZMD America, Inc.

8413 Excelsior Drive
Suite 200
Madison, WI 53717
USA

Phone +1 (608) 829-1987
Fax +1 (631) 549-2882

Zentrum Mikroelektronik Dresden AG, Japan Office

2nd Floor, Shinbashi Tokyu Bldg.
4-21-3, Shinbashi, Minato-ku
Tokyo, 105-0004
Japan

Phone +81.3.6895.7410
Fax +81.3.6895.7301

ZMD FAR EAST, Ltd.

3F, No. 51, Sec. 2,
Keelung Road
11052 Taipei
Taiwan

Phone +886 2 2377 8189
Fax +886 2 2377 8199

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