

CY8CKIT-029 PSoC[®] LCD Segment Drive Expansion Board Kit Guide

Doc. # 001-55415 Rev. *G

Cypress Semiconductor 198 Champion Court San Jose, CA 95134-1709 Phone (USA): 800.858.1810 Phone (Intnl): 408.943.2600 http://www.cypress.com



Copyrights

© Cypress Semiconductor Corporation, 2009-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATE-RIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

PSoC[®] Creator[™] is a trademark and PSoC[®] is a registered trademark of Cypress Semiconductor Corp. All other trademarks or registered trademarks referenced herein are property of the respective corporations.

Flash Code Protection

Cypress products meet the specifications contained in their particular Cypress PSoC datasheets. Cypress believes that its family of PSoC products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

Contents



1.	Introdu	lotion	5
	1.1	Kit Contents	5
	1.2	PSoC Creator	5
	1.3	Getting Started	6
	1.4	Additional Learning Resources	6
	1.5	Document History	6
	1.6	Document Conventions	6
2.	Installa	tion	7
	2.1	CD Installation	7
	2.2	Install Hardware	8
	2.3	Install Software	8
	2.4	Verify Kit version	8
3.	Kit Ope	eration	9
	3.1	Introduction	9
	3.2	Programming a PSoC 3 Device	9
	3.3	Hardware Connections	12
	3.4	Verify the Output	13
4.	Hardwa	are	15
	4.1	System Block Diagram	15
	4.2	Functional Description	16
		4.2.1 LCD Glass Details	16
		4.2.1.1 Pixel Mapping Table	16
	4.0	4.2.1.2 Glass Specification	1/
	4.3	Port Options with CY8CKIT-001 DVK	17
	4.4		19
5.	Code E	xamples	21
	5.1	Code Example 1: LCD_Seg_Example1_Battery_Meter	21
		5.1.1 Project Description	21
		5.1.2 Running the Code Example	21
		5.1.3 Hardware Connections	21
		5.1.4 Verifying Output	21
		5.1.5 PSOC Creator Project Details	22
		5.1.5.1 LCD_Sey	22
		5153 VR	∠r 28
	52	Code Example 2: I CD Seg Example 2: StopWatch	20 29
	0.2	5.2.1 Project Description	
		5.2.2 Running the Code Example	30
		U	



5.2.3	Hardwa	are Connections	
5.2.4	Verifying	g the Output	
5.2.5	PSoC C	Creator Project Details	
	5.2.5.1	LCD_Seg	
	5.2.5.2	Real Time Clock (RTC)	
	5.2.5.3	Status Register	
	5.2.5.4	Sw_Sample_Clock	
	5.2.5.5	Clock SW	

A. Appendix

41

- A 1	Schematic	41
A 2	Board Lavout	42
7.12	A 2.1 PDCR-09571 Top View	42
	A.2.2 PDCR-09571 Bottom View	
A.3	BOM	



The CY8CKIT-029 PSoC[®] LCD Segment Drive Expansion Board Kit (EBK) is an expansion board that is used with CY8CKIT-001. It allows you to evaluate PSoC's LCD drive capability by designing your own projects with the easy-to-use LCD segment component in Cypress's PSoC Creator[™] or altering the code examples provided with this kit.

The CY8CKIT-029 PSoC LCD Segment Drive EBK is based on the PSoC family of devices. PSoC is a programmable system-on-chip platform for 8-, 16-, and 32-bit applications. It combines precision analog and digital logic with a high-performance 8051 single cycle per instruction pipeline processor, achieving 10 times the performance of previous 8051 processors. With PSoC, you can create the exact combination of peripherals and integrated proprietary IP to meet the needs of your applications. You are no longer constrained by a catalog.

1.1 Kit Contents

This kit contains:

- PSoC LCD Segment Drive Expansion Board
- Quick Start Guide
- Kit CD

Inspect the contents of the kit; if you do not find any part, contact your nearest Cypress sales office for help.

1.2 **PSoC Creator**

Cypress's PSoC Creator software is a state-of-the-art, easy-to-use software development Integrated Development Environment (IDE). It introduces a hardware and software co-design environment based on classical schematic entry and revolutionary embedded design methodology.

With PSoC Creator, you can:

- Create and share user defined, custom peripherals using hierarchical schematic design.
- Automatically place and route select components and integrate simple glue logic normally residing in discrete muxes.
- Trade-off hardware and software design considerations allowing you to focus on what matters and get to market faster.

PSoC Creator also enables you to tap into an entire tools ecosystem with integrated compiler tool chains, RTOS solutions, and production programmers to support both PSoC 3 and PSoC 5.



1.3 Getting Started

To get started, see Chapter 3 for a description of the kit operation and how to program the PSoC 3 device. A code example is used to explain how to use the PSoC LCD segment drive expansion board with the CY8CKIT-001 DVK. Chapter 4 provides details of the hardware. Chapter 5 guides you to create simple code examples. The Appendix section provides the schematics and bill of materials (BOM) associated with the expansion board.

1.4 Additional Learning Resources

Visit http://www.cypress.com for additional learning resources in the form of datasheets, technical reference manual, and application notes.

1.5 Document History

Revision	Release Date	Description of Change				
**	09/02/2009	Initial version of the guide				
*A	10/13/2009	DT Updates				
*В	11/02/2009	Jpdated Schematic in Appendix				
*C	12/08/2009	Updated Figure 5-3, Figure 5-15, and Note in section 5.2.5.5 Clock_SW				
*D	02/16/2011	Updated Figures as per the latest software				
*E	05/24/2011	Fixed template styles				
*F	08/17/2011	Updated Figures 5-4, Figure 5-5, Figure 5-9, Figure 5-17, Figure 5-18.				
*G	12/02/2011	Jpdated kit installation location in section 2.1				

1.6 Document Conventions

Convention	Usage			
Courier New	Displays file locations, user entered text, and source code:			
Courier new	C:\cd\icc\			
Italias	Displays file names and reference documentation:			
Italics	Read about the sourcefile.hex file in the PSoC Designer User Guide.			
[Bracketed, Bold]	Displays keyboard commands in procedures: [Enter] or [Ctrl] [C]			
File > Open	Represents menu paths: File > Open > New Project			
Bold	Displays commands, menu paths, and icon names in procedures: Click the File icon and then click Open .			
Timos Now Roman	Displays an equation:			
Times new Roman	2 + 2 = 4			
Text in gray boxes	Describes Cautions or unique functionality of the product.			





2.1 CD Installation

Follow these steps to install the CY8CKIT-029 PSoC LCD Segment Drive EBK software:

1. Insert the kit CD into the CD drive of your computer. The CD is designed to auto-run and the PSoC LCD Segment Drive EBK menu appears.

Figure 2-1. CY8CKIT-029 Kit Menu



Note If auto-run does not execute, double-click cyautorun.exe in the root directory of the CD.



2. Use Windows Explorer to browse documents inside the PSoC LCD Segment Drive EBK folder.



Note After the installation is complete, the kit contents are found at the following location:

C:\Program Files\Cypress\CY8CKIT-029A\2.0

2.2 Install Hardware

No hardware installation is required for this kit.

2.3 Install Software

When installing the PSoC LCD segment drive EBK, the installer checks if the prerequisite software is installed in your system. These include PSoC Creator, PSoC Programmer, Windows Installer, .NET, Acrobat Reader, and KEIL Complier. If these applications are not installed, the installer prompts you to download and install them.

The following software are provided in the CD:

- 1. PSoC Creator
- PSoC Programmer 3.12.4 or later Note When installing PSoC Programmer, select Typical on the Installation Type page.
- 3. Code Examples (provided in the Firmware folder)

2.4 Verify Kit version

To know the kit revision, look for the white sticker on the back of the kit box. If the revision reads CY8CKIT-029A Rev **, then congratulations, you own the latest version.

You can purchase our latest kits at www.cypress.com/go/CY8CKIT-029.





3.1 Introduction

The CY8CKIT-029 PSoC LCD Segment Drive EBK code examples are designed using a display with many segments (8 common lines by 16 segment lines giving 128 segments).

Code Example 1: LCD_Seg_Example1_Battery_Meter

This example demonstrates the battery charge indicator along with the 14-segment display of the LCD glass by implementing a battery meter.

Code Example 2: LCD_Seg_Example2_StopWatch

This example implements a stopwatch using the RTC component in PSoC Creator. The hours, minutes, and seconds (HH:MM:SS) are displayed on the 14-segment LCD display.

See Code Examples on page 21 for more information.

3.2 Programming a PSoC 3 Device

The code examples are provided in the documentation section of the kit CD. This section provides details on programming the PSoC 3 device.

To program the 'Battery Meter' example to the PSoC 3 silicon, follow these steps:

- 1. Place the PSoC 3 processor module on the CY8CKIT-001 DVK.
- 2. Power the DVK using either battery connections or a wall power unit.
- 3. Connect the MiniProg3 JTAG cable to the JTAG connector, both on MiniProg3 and the PSoC 3 processor module. Connect the MiniProg3 to a host PC USB high-speed port using a USB cable.

The connections for steps 1 to 3 are shown in Figure 3-1.





Figure 3-1. PSoC 3 Processor Module, Power, and MiniProg3 Connection with CY8CKIT-001 DVK

Note See the *PSoC Development Kit Board Guide* for details on connecting and programming PSoC devices.

4. Click on the code example, *LCD_Seg_Example1_Battery_Meter*, located in **Examples and Kits** on the Start Page of PSoC Creator.

Start Page

PSoC® Creator ™

PSoC Creator Start Page
Quick Start Guide
Intro to PSoC
Intro to PSoC Creator
PSoC Creator Training
Help Tutorials
My First Five PSoC 3 Designs

Examples and Kits
Find Example Project...

Kits
PSoC LCD Segment Drive EBK - CY8CKIT-029A
DLCD_Seg_Example1_Battery_Meter.cywrk
LCD_Seg_Example2_StopWatch.cywrk

Figure 3-2. Start Page



- 5. Create a folder in the desired location and click **OK**. The project opens in PSoC Creator and is saved in that folder.
- 6. Build the project by selecting the **Build** option.

igure 3-3. Build Project					
LCD_Seg_Example1_Battery_Meter - PSoC Creator 2.0					
<u>File E</u> dit <u>Y</u> iew <u>D</u> ebug Project	<u>Build</u> <u>T</u> ools <u>W</u> indow <u>H</u> elp				
1 🔁 🔁 着 🖆 🖬 🖉 🖻 🕽 🖓	Build LCD_Seg_Example1_Battery_Meter Shift+F6				
	Clean LCD_Seg_Example1_Battery_Meter				
Workspace Explorer	Clean_and Build LCD_Seg_Example1_Battery_Meter				

7. Click the **Program** icon.

Figu	Figure 3-4. Program Option							
🗒 LO	CD_Seg	g_Exar	nple1_8	lattery_l	deter	- PSoC	Creator :	2.0
Eile	<u>E</u> dit	⊻iew	<u>D</u> ebug	Project	<u>B</u> uild	<u>T</u> ools	<u>W</u> indow	Help
: 🗂	<u>°</u> 6	i 💕 🛛				1X	50	- 1 🗈
	- 🚠 🗧	» 嘴	🎇 🎘	Ŧ				
Works	pace Ex	plorer	_		•	д X	Start	Page
ត្រូ 🔍	2		Prog	gram (Ctrl-	-F5)			

8. The project is programmed successfully, as shown in Figure 3-5.

Figure 3-5. Programming Successful

The link step is up to date, no work needs to be done.
Build Succeeded
Programming started for device: 'PSoC3 CY8C3866AXI-040'.
Device ID Check
Erasing
Programming User NVL Arrays
Programming of Flash Starting
Protecting
Verify Checksum
Device 'PSoC3 CY8C3866AXI-040' was successfuly programmed
I

9. Reset the device by pressing the switch SW4 on the DVK; see Figure 3-6.





3.3 Hardware Connections

Connect the PSoC LCD segment drive board to Port A of the CY8CKIT-001 DVK.

Figure 3-7. Board Connected to Port A



Connect the analog input from the potentiometer (VR slot in CY8CKIT-001 DVK) to P0_2 on the DVK.



Figure 3-8. VR Connected to P0_2 on CY8CKIT-001 DVK



Power the VR by setting jumper J11 to the 'ON' position.

Figure 3-9. Jumper J11 in ON Position on CY8CKIT-001 DVK



The remaining jumper settings on the DVK are in the default state. See the *PSoC Development Kit Board Guide* for the default setting of jumpers.

3.4 Verify the Output

Vary the VR (potentiometer) and note the change in status displayed on the LCD.

Figure 3-10. Verifying Output of Battery Meter Project



Note The best viewing angle is from 6 o'clock, according to the LCD glass characteristics.

Kit Operation



4. Hardware



4.1 System Block Diagram

The PSoC LCD Segment Drive EBK consists of only three blocks.

- LCD glass (Golden View Display LCD, GV13956A-TPP)
- I2C EEPROM (ST, M24C02-W)
- 40-pin (20x2) connector (Sullins Connector Solutions, S2111E-20-ND)

Figure 4-1. System Block Diagram



This board includes a custom LCD glass with maximum 128 segments. The glass has 24 pins (8 common and 16 segments lines) that are routed to the 20x2 pin connector and connected to the configured I/O pins of PSoC 3.

I2C EEPROM is a 'No Load' component on the board. It is used to store information about the EBK board number, so PSoC can recognize the board. ST M24C02-W is the 2-Kbit EEPROM with operating voltage in the range 2.5 V to 5.5 V.

40-pin (20×2) connector helps to connect the configured PSoC 3 I/O pins to the LCD glass pins. From the 40 pins available, only 24 are used by the kit. All unused pins are left floating.



4.2 Functional Description

4.2.1 LCD Glass Details

Figure 4-2 shows the image of the LCD glass and Table 4-1 lists the segment details. The LCD glass provides visual feedback.

Figure 4-2. LCD Glass



Table 4-1. LCD Glass Segment Details

Label	Description			
А	Battery charge indicator bars			
В	Wireless symbol			
С	Alarm display			
D	7-segment numeric section			
E	Medical symbol			
F	14-segment alpha numeric section			

4.2.1.1 Pixel Mapping Table

	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15
COM7	T7	S1	S2	COL1	S3	S4	S5	COL2	T1	T4	T2	T3	COL3	COL4	T5	T6
COM6	1A	1J	2A	2J	ЗA	3J	4A	4J	5A	5J	6A	6J	10D	9D	8D	7D
COM5	1P	1K	2P	2K	3P	3K	4P	4K	5P	5K	6P	6K	10C	9C	8C	7C
COM4	1F	1B	2F	2B	3F	3B	4F	4B	5F	5B	6F	6B	10E	9E	8E	7E
COM3	1G	1L	2G	2L	3G	3L	4G	4L	5G	5L	6G	6L	10G	9G	8G	7G
COM2	1E	1C	2E	2C	3E	3C	4E	4C	5E	5C	6E	6C	10B	9B	8B	7B
COM1	1M	1R	2M	2R	3M	3R	4M	4R	5M	5R	6M	6R	10F	9F	8F	7F
COM0	1N	1D	2N	2D	3N	3D	4N	4D	5N	5D	6N	6D	10A	9A	8A	7A



The following figure shows the segment lettering information for all LCD segments.

Figure 4-3. Segment Lettering Information



14-Segment and 7-Segment Lettering Information:



Note Pixel mapping table is also available on the back of the CY8CKIT-029 PSoC LCD Segment Drive EBK.

- 4.2.1.2 Glass Specification
 - Display type: TN
 - Viewing direction: 6 o'clock
 - Drive method:1/8 Duty, 1/4 BIAS
 - Operating voltage: 3.0 V
 - Polarizer mode: Reflective/Positive
 - Operating temperature: 0 °C ~ +50 °C.
 - Storage temperature: -10 °C ~ +60 °C.

4.3 Port Options with CY8CKIT-001 DVK

The LCD segment drive board connects to the CY8CKIT-001 PSoC DVK through the 20x2 pin connector. It connects through one of the following ports: Port A, Port A Prime, or Port B. Table 4-2 shows the pin assignment for all three ports along with the segment LCD pins (common and segments lines) assignment. Figure 3-7 shows the LCD segment board connection to port A of the DVK.

CYPRESS

Pin	Port A	Port A'	Port B	PSoC EBK
1	P3_7	P6_7	P1_7	SEG15
2	P3_6	P6_6	P1_6	SEG14
3	P3_5	P6_5	P1_5	SEG13
4	P3_4	P6_4	P1_4	SEG12
5	P3_3	P6_3	P1_3	SEG11
6	P3_2	P6_2	P1_2	SEG10
7	P3_1	P6_1	P1_1	SEG9
8	P3_0	P6_0	P1_0	SEG8
9	GND	GND	GND	GND
10	RESRV 11	RESRV 8	RESRV 3	NC
11	P5_7	P2_7	P2_7	SEG7
12	P5_6	P2_6	P2_6	SEG6
13	P5_5	P2_5	P2_5	SEG5
14	P5_4	P2_4	P2_4	SEG4
15	P5_3	P2_3	P2_3	SEG3
16	P5_2	P2_2	P2_2	SEG2
17	P5_1	P2_1	P2_1	SEG1
18	P5_0	P2_0	P2_0	SEG0
19	GND	GND	GND	GND
20	RESRV 10	RESRV 7	RESRV 2	NC
21	P4_7	P0_7	P0_7	COM0
22	P4_6	P0_6	P0_6	COM1
23	P4_5	P0_5	P0_5	COM2
24	P4_4	P0_4	P0_4	COM3
25	P4_3	P0_3	P0_3	COM4
26	P4_2	P0_2	P0_2	COM5
27	P4_1	P0_1	P0_1	COM6
28	P4_0	P0_0	P0_0	COM7

GND

RESRV 6

P7_7

P7_6

P7_5

P7_4

P7_3

P7 2

P7_1

P7_0

GND

RESRV 5

GND

RESRV 1

P12_3

P12_2

P12_1

P12_0

V3_3

VADJ

GND

V5_0

VIN

GND

GND

NC

NC

NC

SDA

SCL

V3_3

NC

GND

NC

NC

GND

Table 4-2. Port Pin Connections

GND

RESRV 9

P12_3

P12_2

P12_1

P12_0

V3_3

VADJ

GND

V5_0

VIN

GND

29

30

31

32 33

34

35

36

37

38

39

40



Jumper Settings of CY8CKIT-001 DVK to Use Port A' and Port B:

Both Port A' and Port B uses the Port 2 pins for segment lines. Switch the jumper J12 to the 'OFF' position; this switches off the power to the character LCD, which is connected to Port 2 of the CY8CKIT-001 DVK.





PSoC 3 provides serial wire debugging (SWD) with SWD on GPIO pins option. The port pins used for SWD are P1_0 (SWDIO) and P1_1 (SWDCK). Port B uses the P1_0 and P1_1 for Seg9 and Seg8 signals, respectively. Therefore, the debugging option is not available when using Port B. PSoC Creator allows routing P1_1 and P1_0 to be used as GPIO pins when debugging is disabled. To disable debugging, follow these steps:

- 1. Open the design wide resource file (with extension '.cydwr').
- 2. Click the **System** tab.
- 3. In the Debugging option, clear the **Enable** check box; select **Debug ports disabled** in the Debug Port Select (DPS) option. See Figure 4-5 for these settings.

Figure 4-5	. Disable	Debugging
------------	-----------	-----------

Start Page *LCD_Segeter.cydwr TopDesign.cysch		→ 4 Þ ×
Seset LEExpand Collapse		
Option	Туре	Value
Configuration		
□ Programming\Debugging		
- Debug Port Select (DPS)	ENUM	Debug ports disabled 🗸 🗸
- Enable	BOOL	
Require XRES Pin	BOOL	
Use Optional XRES	BOOL	
Voltage Configuration		

4.4 **Power Supply**

The kit is powered from the CY8CKIT-001 DVK through the 40-pin (2×20) connector.

Hardware







5.1 Code Example 1: LCD_Seg_Example1_Battery_Meter

This code example demonstrates the battery charge indicator along with the 14-segment display of the LCD glass by implementing a battery meter. The battery meter is used to graphically display the battery charge level; the 14-segment display is used to relay messages related to the battery charge (full, medium, and low).

5.1.1 Project Description

The potentiometer on the DVK is used to increase and decrease the battery meter on the segment LCD. The four segments (S2, S3, S4, S5, see Figure 4-3) have four voltage levels (1.25 V, 2.50 V, 3.75 V, and 5 V) to define the switching on/off of the battery meter. This is accomplished using count values from the Delta-Sigma ADC available on PSoC 3. Based on the battery meter, 'Full', 'Medium', and 'Low' are displayed on the 14-segment LCD display.





5.1.2 Running the Code Example

Follow the steps described in Programming a PSoC 3 Device on page 9 to program the PSoC 3 device with the Battery Meter code example.

5.1.3 Hardware Connections

See Hardware Connections on page 12 for details on hardware connections.

5.1.4 Verifying Output

Vary the VR (potentiometer) and note the status changes displayed on the LCD.







5.1.5 PSoC Creator Project Details

PSoC Creator offers a flexible software tool to create and configure the programmable peripherals. Figure 5-3. PSoC Creator Top Level Design For Battery Meter Project

	ADC_De	ISig	
VR 🛛 🚽		5	LCD_Seg Segment LCD
	4	-	

5.1.5.1 LCD_Seg

The LCD_Seg is the core component in this code example. There is a single segment LCD component selected to handle all displays on the LCD glass panel. This component defines all segment assignments for the glass. The component presents a grid containing an entry for each addressable element in the glass. An element can be a pixel in the matrix characters, a segment of one of the segment displays, or a specific icon (symbol) built into the display. Each element is considered a pixel and is individually addressed at its mapped location and turned on or off using the component pixel handling API calls.

There are also helper functions that can be defined. Each helper is specifically designed to allow handling of the different types of characters in the display. Thus, segments of a segment character are grouped and addressed collectively by a single helper. Each helper has a set of component API calls that are placed in the code to write digits or characters to the target display areas.

Each icon is turned on or off using a write pixel API call. The matrix display characters are set using a write string API call. The segment displays are written one character at a time using a write character or write digit API call.

In the basic configuration, the bias voltage is selected to set the contrast level. The contrast level can also be adjusted dynamically, by using the API call provided by the segment LCD component. The higher the bias level set in the call to the API the higher the contrast. The API allows a selection between 0 and 127 with 127 corresponding to the maximum contrast level. The frame rate is selected to be the maximum rate before the characters in the display begin to reduce in contrast.

The segment LCD component in this code example is used to control the switching on/off of the segments of battery charge indicator (S1, S2, S3, S4, and S5) and also the 14-segment display message. The component provides all analog and digital signals necessary to drive 128 segments liquid crystal display using eight common lines and sixteen segment drive lines.



Figure 5-4. Segment LCD Configuration: Basic Tab

Configure 'SegLCD'	? 🛛
Name: LCD_Seg	
Basic Configuration Driver	Power Settings Display Helpers Custom Characters Built-in 4 D
Number of common lines	8
Number of segment lines	16
Enable Ganging Commons	
Bias type	1/4
Waveform type	Type A Standard 💙
Frame rate, Hz	100
Driver Power Mode	No Sleep 🔽
Bias voltage, V	2.891 • 3.0V • 5.5V
Datasheet	OK Apply Cancel

Figure 5-5. Segment LCD Configuration: Driver Power Settings

Configure	'SegLCD'					? 🛛
Name: Basic	LCD_Seg	Driver Po	ower Settings	Display Helpe	ers Custom Character	s Built-in 4 ▷
Glass S	iize, sq cm vanced		10	\$		
High © [C	n Drive Time, µs Default Step Custom Step [[s 2.27 0.04	Value 79.49	\$		
High D Low D Low D	Drive Strength trive Time, μs trive Strength		seg=1x com=2x 2.27 seg=0.06x com=	✓0.12x ✓		
Datas	heet			OK	Apply	Cancel



Basic (onfiguration	n Driver Po	wer Settings	Display H	elners (istom Charac	ters Built-i	n
elpers				Selec	ted Helpers			
Segme 4 Segm 6 Segm argraph 1atrix	nt ent rand Dial] Helpe	r_14Segment r_Bar_0	0		
Helper f	unction con	figuration						
	Mura	bor of our bolo	e ca	ootod piuol po				
A		а А	A	A	A	*		
E P.J	KBEP	KBEPI	KBEPI	KBEPI	KBEPU	кв		
U.S.			41 Lai					
E M M	DOCH	NRCEMN	DOEMN	BOEMN	DODUNI			
EMIN	RCEM	ARCEMN	RCEMM	RCEMM	RCEMPI			
D	- X X	D X X D	D	D X X D	D.			
Pixel Ma	apping Table	9						
	Com7	Com6	Com5	Com4	Com3	Com2	Com1	Com0
Seg0	PIX7	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0
Seg1	S1	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0
Seg2	S2	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1
Seg3	PIX31	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1
Seg4	\$3	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2
Seg5	S4	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2
Seg6	S5	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3
Seg7	PIX63	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3
Seg8	PIX71	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4
Seg9	PIX79	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4
Seg10	PIX87	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5
Seg11	PIX95	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5
Seg12	PIX103	PIX102	PIX101	PIX100	PIX99	PIX98	PIX97	PIX96
eg13	PIX111	PIX110	PIX109	PIX108	PIX107	PIX106	PIX105	PIX104
1000007	PIX119	PIX118	PIX117	PIX116	PIX115	PIX114	PIX113	PIX112
jeg14	PIX127	PIX126	PIX125	PIX124	PIX123	PIX122	PIX121	PIX120
eg14 eg15								
eg14 leg15								
ieg14 ieg15								
ieg14 ieg15								

Figure 5-6. Six Character Helper for 16-Segment Display



Helpers 7 Segment 14 Segmer 16 Segmer Bargraph a Matrix Helper fur	t nt and Dial nction cont			Selec	ted Helpers			
7 Segment 14 Segmer 16 Segmer Bargraph a Matrix Helper fur	t nt and Dial nction cont		c		1.10			
16 Segmer Bargraph a Matrix Helper fur	nt and Dial nction cont		CONTRACTOR OF STREET	Helpe	r_145egment_ r Bar 0	_U		
Bargraph a Matrix Helper fur	and Dial							
Helper fur	nction con		4					
	nedorr con	figuration						
		ngurauon		101 10	1			
	Num	ber of symbols.	5 Sel	ected pixel na	me			
100 100 10								
SSS	SSS							
1 2 3	3 4 5							
1								
Pixel Map	ping Table							
	Com7	Com6	Com5	Com4	Com3	Com2	Com1	Com0
Seg0	PIX7	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0
Seg1	S1	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0
Seg2	S2	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1
Seg3	PIX31	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1
Seq4	\$3	H14SEG2	H14SEG2	H14SEG2	H14SEG2	UNIXEEDO		
						H143EGZ	H14SEG2	H14SEG2
Seg5	S4	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2 H14SEG2	H14SEG2 H14SEG2
Seg5 Seg6	S4 S5	H14SEG2 H14SEG3	H14SEG2 H14SEG3	H14SEG2 H14SEG3	H14SEG2 H14SEG3	H14SEG2 H14SEG2	H14SEG2 H14SEG2 H14SEG3	H14SEG2 H14SEG2 H14SEG3
Seg5 Seg6 Seg7	S4 S5 PIX63	H14SEG2 H14SEG3 H14SEG3	H14SEG2 H14SEG3 H14SEG3	H14SEG2 H14SEG3 H14SEG3	H14SEG2 H14SEG3 H14SEG3	H14SEG2 H14SEG2 H14SEG3 H14SEG3	H14SEG2 H14SEG2 H14SEG3 H14SEG3	H14SEG2 H14SEG2 H14SEG3 H14SEG3
Seg5 Seg6 Seg7 Seg8	S4 S5 PIX63 PIX71	H14SEG2 H14SEG3 H14SEG3 H14SEG4	H14SEG2 H14SEG3 H14SEG3 H14SEG4	H14SEG2 H14SEG3 H14SEG3 H14SEG4	H14SEG2 H14SEG3 H14SEG3 H14SEG4	H14SEG2 H14SEG3 H14SEG3 H14SEG4	H14SEG2 H14SEG2 H14SEG3 H14SEG3 H14SEG4	H14SEG2 H14SEG2 H14SEG3 H14SEG3 H14SEG4
Seg5 Seg6 Seg7 Seg8 Seg9	S4 S5 PIX63 PIX71 PIX79	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4	H14SEG2 H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4	H14SEG2 H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4
Seg5 Seg6 Seg7 Seg8 Seg9 Seg10	S4 S5 PIX63 PIX71 PIX79 PIX87	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5	H143EG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5	H14SEG2 H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5	H14SEG2 H14SEG3 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5
Seg5 Seg6 Seg7 Seg8 Seg9 Seg10 Seg11	S4 S5 PIX63 PIX71 PIX79 PIX87 PIX85	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5	H143EG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5	H14SEG2 H14SEG3 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5	H14SEG2 H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5
Seg5 Seg6 Seg7 Seg8 Seg9 Seg10 Seg11 Seg12	S4 S5 PIX63 PIX71 PIX79 PIX87 PIX87 PIX95 PIX103	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX102	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX101	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 PIX100	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX99	H145EG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX98	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX97	H14SEG2 H14SEG3 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX96
Seg5 Seg6 Seg7 Seg8 Seg9 Seg10 Seg11 Seg12 Seg13	S4 S5 PIX63 PIX71 PIX79 PIX87 PIX87 PIX95 PIX103 PIX111	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX102 PIX110	H14SEG3 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX101 PIX103	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX100 PIX108	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX99 PIX107	H143EG2 H148EG3 H148EG3 H148EG3 H148EG4 H148EG5 H148EG5 PIX98 PIX106	H14SEG2 H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX97 PIX105	H14SEG2 H14SEG3 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX96 PIX104
Seg5 Seg6 Seg7 Seg8 Seg9 Seg10 Seg11 Seg12 Seg13 Seg14	S4 S5 PIX63 PIX71 PIX79 PIX87 PIX87 PIX87 PIX103 PIX111 PIX119	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX102 PIX110 PIX118	H14SEG3 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX101 PIX109 PIX117	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX100 PIX108 PIX116	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX99 PIX107 PIX115	H143EG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX98 PIX106 PIX114	H14SEG2 H14SEG3 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX97 PIX105 PIX113	H14SEG2 H14SEG3 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX96 PIX104 PIX112
Seg5 Seg6 Seg7 Seg8 Seg9 Seg10 Seg11 Seg12 Seg13 Seg14 Seg15	S4 S5 PIX63 PIX71 PIX79 PIX87 PIX95 PIX103 PIX103 PIX111 PIX119 PIX127	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX102 PIX110 PIX118 PIX126	H14SEG3 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX101 PIX109 PIX107 PIX125	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX100 PIX100 PIX108 PIX116 PIX124	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX99 PIX107 PIX107 PIX123	H143EG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX98 PIX106 PIX114 PIX122	H14SEG2 H14SEG3 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX97 PIX105 PIX113 PIX121	H14SEG2 H14SEG3 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX96 PIX104 PIX112 PIX120
Seg5 Seg6 Seg7 Seg8 Seg9 Seg10 Seg11 Seg12 Seg13 Seg14 Seg15	S4 S5 PIX63 PIX71 PIX79 PIX87 PIX95 PIX103 PIX111 PIX119 PIX127	H14SEG2 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX102 PIX110 PIX118 PIX126	H14SEG2 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX101 PIX109 PIX117 PIX125	H14SEG2 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX100 PIX108 PIX108 PIX116 PIX124	H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX99 PIX107 PIX115 PIX123	H143EG2 H14SEG3 H14SEG3 H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX98 PIX106 PIX114 PIX122	H14SEG2 H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX97 PIX105 PIX113 PIX121	H14SEG2 H14SEG2 H14SEG3 H14SEG3 H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX96 PIX104 PIX112 PIX120

Figure 5-7. Bar Graph Helper for 5 Battery Indicator Segments

Notes

- For details of parameters see the component datasheets.
- The figure only shows the tabs within the component that need to be changed, other tabs such as the Built In tab, have the default setting. This is valid for all components of both code examples.



The segment naming in the LCD glass (Golden View Display LCD, GV13956A-TPP) and SegLCD component in PSoC Creator are different.

#	Segment in Golden View Display LCD, GV13956A-TPP	SegLCD Component in PSoC Creator
1	А	А
2	В	В
3	С	C
4	D	D
5	E	E
6	F	F
7	G	G
8	Р	Н
9	J	I
10	К	J
11	L	К
12	R	L
13	Ν	М
14	М	N

Table 5-1.	Segment	Naming in	LCD
------------	---------	-----------	-----

The same is depicted symbolically in Figure 5-8

Figure 5-8. Segment Naming in LCD







5.1.5.2 ADC_DelSig

The ADC is used to sample an input voltage, take the voltage from the potentiometer, and control the battery charge indication on the LCD segments.

Figure 5-9.	ADC_DelS	ig Compone	ent Configuratio	n: Configure Tab
-------------	----------	------------	------------------	------------------

Configure 'ADC_DelSig'	?×
Name: ADC_DelSig	
Configure Built-in	۹ ۵
Config 1 Common	
Comment : Default Config	
Config Name : CFG1 ADC_DelSig_CFG1	
Sampling	
Conversion Mode 3 - Multi Sample (Tur 😪 🛛 # Configs 👖 🤤	
Resolution 16 vits	
Conversion Rate 10000 🗢 SPS Range [489 - 11725 SPS]	
Clock Frequency 2620.000 kHz	
Input Options	
Input Mode 🔿 Differential 💿 Single	
Input Range Vssa to Vdda	
Buffer Gain 1 💌 Buffer Mode Rail to Rail 💌	
Reference	
Vref Internal Vdda/4 🛛 1.2500 🗘 Volts (Vdd)	
Datasheet OK Apply Can	cel



5.1.5.3 VR

The VR pin is used to read the analog value from the potentiometer. The Pin Drive mode is configured as High-Z, which is the default value. Figure 5-10 and Figure 5-11 show the port pin setting.

Figure 5-10. VR Configuration: Type Tab



Figure 5-11. VR Configuration: General Tab

Configure 'cy_pins'		? 🔀
Name: VR	Reset Built-in	4 Þ
Number of Pins: 1 [All Pins] └─⊠ VR_0	Type General Input Output Drive Mode Initial High Impedance Analog Minimu	State: 0) v um Supply Voltage:
Data Sheet		Cancel



5.2 Code Example 2: LCD_Seg_Example2_StopWatch

5.2.1 Project Description

This code example implements a stopwatch using the RTC component in PSoC Creator. The values hours, minutes, and seconds (HH:MM:SS) are displayed on the 14-segment display of the LCD.

Figure 5-12. StopWatch Project Flowchart





5.2.2 Running the Code Example

To program the PSoC 3 device with the StopWatch code example,

- 1. Follow steps 1 to 3 in Programming a PSoC 3 Device on page 9.
- 2. Click the code example, *LCD_Seg_Example2_StopWatch*, from Examples and Kits in the Start Page of PSoC Creator.
- 3. Follow the steps 5-10 in Programming a PSoC 3 Device on page 9 to complete programming.

5.2.3 Hardware Connections

- 1. Connect the LCD segment drive board to Port A of the DVK, as shown in Figure 3-7.
- 2. Connect the input from the mechanical switch SW1 of DVK to port pin P0_2 on the DVK, as shown in Figure 5-13.



Figure 5-13. Connect Switch SW1 to P0_2 on CY8CKIT-001 DVK

The remaining jumper settings on the DVK have the default state. See the *PSoC Development Kit Board Guide* for default setting of the jumpers.

5.2.4 Verifying the Output

On power up, the LCD segment displays HH.MM.SS as 00.00.00 on the 14-segment display of the LCD.

Figure 5-14. LCD Display





The mechanical switch SW1 on the DVK is used to start, stop, and reset the stopwatch. The switch sequence is shown Figure 5-15.

Figure 5-15. Switch SW1 Starts RTC



Pressing SW1 the first time starts the stopwatch and the values HH.MM.SS from the RTC are displayed on the LCD. The stopwatch increments every second. The second press stops the stopwatch and the value at which the watch stopped (HH.MM.SS) is displayed on the LCD. The third press of the switch resets the display to 00.00.00 (HH.MM.SS).



5.2.5 PSoC Creator Project Details

Figure 5-16. PSoC Creator Top Level Design for StopWatch Project



5.2.5.1 LCD_Seg

The LCD_Seg is the core component used in this project. It displays the time (HH:MM:SS) on the 14-segment display section. The component provides all analog and digital signals necessary to drive 128 segments LCD using eight common lines and sixteen segment drive lines.

Figure 5-17. Segment LCD Configuration: Basic Tab

Configure 'SegLCD'		?×
Name: LCD_Seg		
Basic Configuration Driver P	ower Settings Display Helpers Custom Characters Built-in	۹ ۵
Number of common lines	8	
Number of segment lines	16	
Enable Ganging Commons		
Bias type	1/4 💌	
Waveform type	Type A Standard 💌	
Frame rate, Hz	100 💌	
Driver Power Mode	No Sleep 💌	
Bias voltage, V	2.891 • 3.0V • 5.5V	
Datasheet	OK Apply Cance	



5 S	5	5
Configure 'SegLCD'		? 🗙
Name: LCD_Seg		
Basic Configuration	Driver Power Settings Display He	lpers Custom Characters Built-in 4 D
Glass Size, sq.cm	10	
Advanced		
High Drive Time, μs		
Default Step 2	2.27 Value	
Custom Step	.04 🗢 79.49 🗢	
High Drive Strength	seg=1x com=2x 💉	
Low Drive Time, µs	2.27	
Low Drive Strength	seg=0.06x com=0.12x 💉	
Datasheet	ОК	Apply Cancel

Figure 5-18. Segment LCD Configuration: Driver Power Settings



Bacic (me: LCD_Seg							
Holooro	-oringaradio		wer becangs	Coloo		ascom enarae	cors baile i	
Helpers Selected Helpers 7 Segment Helper_14Segment_0 14 Segment Helper_Bar_0 16 Segment (a)								
Helper f	unction con	iguration						
	🗙 Num	ber of symbols:	6 Sel	ected pixel na	me			
F P J	К В F Р.	A A J K B F P J	A K B F P J	A K B F P J	A K B F P J I	∢ в		
EMN	RCEM	I G NRCEMN	RCEMN	RCEMN	RCEMN	र २ c		
			D	D	D	N.		
Pixel Ma	apping Table							
	Com7	Com6	Com5	Com4	Com3	Com2	Com1	ComO
Seg0	PIX7	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0
Seg1	PIX15	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0
Seg2	PIX23	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1
Seg3	COL1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1
Seg4	PIX39	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2
Sec5	PIX47	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2
oego	PIX55	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3
Seg6		H14SEC3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3
Seg6 Seg7	COL2	11143EG3					UNICECT	H14SEG4
Seg6 Seg7 Seg8	COL2 PIX71	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H143EG4	H14SEG4
Seg6 Seg7 Seg8 Seg9	COL2 PIX71 PIX79	H14SEG4 H14SEG4	H14SEG4 H14SEG4	H14SEG4 H14SEG4	H14SEG4 H14SEG4	H14SEG4 H14SEG4	H14SEG4	
Seg6 Seg7 Seg8 Seg9 Seg10	COL2 PIX71 PIX79 PIX87	H14SEG4 H14SEG4 H14SEG5	H14SEG4 H14SEG4 H14SEG5	H14SEG4 H14SEG4 H14SEG5	H14SEG4 H14SEG4 H14SEG5	H14SEG4 H14SEG4 H14SEG5	H14SEG4 H14SEG4	H14SEG5
Seg6 Seg7 Seg8 Seg9 Seg10 Seg11	COL2 PIX71 PIX79 PIX87 PIX85	H14SEG4 H14SEG4 H14SEG5 H14SEG5	H14SEG4 H14SEG4 H14SEG5 H14SEG5	H14SEG4 H14SEG4 H14SEG5 H14SEG5	H14SEG4 H14SEG4 H14SEG5 H14SEG5	H14SEG4 H14SEG4 H14SEG5 H14SEG5	H14SEG4 H14SEG4 H14SEG5 H14SEG5	H14SEG5 H14SEG5
Seg6 Seg7 Seg8 Seg9 Seg10 Seg11 Seg12	COL2 PIX71 PIX79 PIX87 PIX95 PIX103	H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX102	H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX101	H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX100	H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX99	H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX98	H14SEG4 H14SEG5 H14SEG5 PIX97	H14SEG5 H14SEG5 PIX96
Seg6 Seg7 Seg8 Seg9 Seg10 Seg11 Seg12 Seg13	COL2 PIX71 PIX79 PIX87 PIX87 PIX95 PIX103 PIX111	H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX102 PIX110	H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX101 PIX109	H14SEG4 H14SEG5 H14SEG5 PIX100 PIX108	H14SEG4 H14SEG5 H14SEG5 PIX99 PIX107	H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX98 PIX106	H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX97 PIX105	H14SEG5 H14SEG5 PIX96 PIX104
Seg6 Seg7 Seg8 Seg9 Seg10 Seg11 Seg12 Seg13 Seg14	COL2 PIX71 PIX79 PIX87 PIX95 PIX103 PIX111 PIX119	H14SEG3 H14SEG4 H14SEG5 H14SEG5 PIX102 PIX100 PIX110 PIX118	H14SEG4 H14SEG5 H14SEG5 PIX101 PIX109 PIX117	H14SEG4 H14SEG5 H14SEG5 PIX100 PIX108 PIX116	H14SEG4 H14SEG5 H14SEG5 PIX99 PIX107 PIX115	H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX98 PIX106 PIX114	H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX97 PIX105 PIX113	H14SEG5 H14SEG5 PIX96 PIX104 PIX112
Seg6 Seg7 Seg8 Seg9 Seg10 Seg11 Seg12 Seg13 Seg14 Seg15	COL2 PIX71 PIX79 PIX87 PIX95 PIX103 PIX111 PIX119 PIX127	H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX102 PIX110 PIX118 PIX126	H14SEG4 H14SEG5 H14SEG5 PIX101 PIX109 PIX117 PIX125	H14SEG4 H14SEG5 H14SEG5 H14SEG5 PIX100 PIX108 PIX116 PIX124	H14SEG4 H14SEG5 H14SEG5 PIX99 PIX107 PIX115 PIX123	H14SEG4 H14SEG5 H14SEG5 PIX98 PIX106 PIX114 PIX122	H14SEG4 H14SEG5 H14SEG5 PIX97 PIX105 PIX113 PIX121	H14SEG5 H14SEG5 PIX96 PIX104 PIX112 PIX120
Seg6 Seg7 Seg8 Seg9 Seg10 Seg11 Seg12 Seg13 Seg14 Seg15	COL2 PIX71 PIX79 PIX87 PIX95 PIX103 PIX111 PIX119 PIX127	H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX102 PIX110 PIX118 PIX126	H14SEG4 H14SEG5 H14SEG5 PIX101 PIX109 PIX117 PIX125	H14SEG4 H14SEG4 H14SEG5 PIX100 PIX108 PIX108 PIX116 PIX124	H14SEG4 H14SEG5 H14SEG5 PIX99 PIX107 PIX115 PIX123	H14SEG4 H14SEG4 H14SEG5 H14SEG5 PIX98 PIX106 PIX114 PIX122	H145EG4 H145EG5 H145EG5 PIX97 PIX105 PIX105 PIX113 PIX121	H14SEG5 H14SEG5 PIX96 PIX104 PIX112 PIX120

Figure 5-19. Six Character Helper for 16-Segment Display



The segment naming in the LCD glass (Golden View Display LCD, GV13956A-TPP) and SegLCD component in PSoC Creator are different.

#	Segment in Golden View Display LCD, GV13956A-TPP	SegLCD component in PSoC Creator
1	A	A
2	В	В
3	C	С
4	D	D
5	E	E
6	F	F
7	G	G
8	Р	Н
9	J	I
10	К	J
11	L	К
12	R	L
13	N	Μ
14	М	Ν

Table 5-2.	Segment	Naming in	LCD
------------	---------	-----------	-----

The same is depicted symbolically in Figure 5-20

Figure 5-20. Segment Naming in LCD







Basic C	Configuratio	n Driver Po	wer Settings	Display H	lelpers C	ustom Charac	ters Built-i	n
Helpers				Selec	ted Helpers			
7 Segme 14 Segm 16 Segm Bargraph Matrix	nt ent ent and Dial	5] Helpe	r_14Segment r_Bar_0	0		
Helper f	unction con X Nurr	figuration ber of symbols:	2 Sel	ected pixel na	me			
C C O O L L 1 2 Pixel Ma	apping Table	3						
1 11011110	Com7	Com6	Com5	Com4	Com3	Com2	Com1	Com0
Seg0	PIX7	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0
Seq1	PIX15	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0	H14SEG0
Seg2	PIX23	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1
Seg3	COL1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1	H14SEG1
Seg4	PIX39	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2
Seg5	PIX47	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2	H14SEG2
Seg6	PIX55	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3
Seg7	COL2	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3	H14SEG3
Seg8	PIX71	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4
Seg9	PIX79	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4	H14SEG4
Seg10	PIX87	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5
Sea11	PIX95	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5	H14SEG5
	PIX103	PIX102	PIX101	PIX100	PIX99	PIX98	PIX97	PIX96
Seg12	PIX111	PIX110	PIX109	PIX108	PIX107	PIX106	PIX105	PIX104
Seg12 Seg13	PIX119	PIX118	PIX117	PIX116	PIX115	PIX114	PIX113	PIX112
Seg12 Seg13 Seg14	DIV107	PIX126	PIX125	PIX124	PIX123	PIX122	PIX121	PIX120
Seg12 Seg13 Seg14 Seg15	PIA(2)							

Figure 5-21. Bar Graph Helper for Two Dots between 14-Segment Display Section



5.2.5.2 Real Time Clock (RTC)

The RTC is minimally configured to use Sunday as the start of the week. The firmware enables the RTC with hours, minutes, and seconds set to zero. When you press SW1, the RTC starts incrementing the time every second, SS from 0 to 59, then MM to 0 to 59, and hours from 0 to 24; thereafter it resets. If you press SW1 again, the RTC stops; on the third press, the RTC is reset to initial condition of hours, minutes, and seconds set to zero.

Figure 5-22.	RTC Com	ponent Basic	Configuration
	1110 000	portion baolo	ooningaradon

Configure 'RTC'	? 🗙
Name: FTC Basic Configuration Built-in	4 ⊳
Enable Daylight Savings Time Functionality	
Start of week Sunday	
Data Sheet OK Apply Cance	*

5.2.5.3 Status Register

Status register is used to store the status of the switch that is read in the firmware.

-igure 5-23.	Status F	Register	Configuration:	Configure	Tab

Configure 'CyStatusReg'	? 🔀
Name: Switch_Input	
Configure Built-in	4 ۵
Inputs 1 ModeMask Bit Mode Set All Sticky 0 Transparent Set All Transparent	
Datasheet OK Apply C	Cancel



5.2.5.4 Sw_Sample_Clock

The clock component of PSoC Creator is used to sample the switch at the frequency of 500 Hz.

Figure 5-24.	Clock Component	Configuration:	Configure Clock Tab
--------------	------------------------	----------------	---------------------

Configure 'cy	_clock'				? 🛛
Name: Sw	/_Sample_Clock				
Configur	e Clock Advance	ed Built-in			4 ⊳
Clock Type:	💿 New	🔘 Existing			
Source:	PLL_OUT <i>(24.0</i> 4	00 MHz)			~
Specify:	 Frequency 	500	Hz 🗸		1
	🔘 Divider				
Summary API Gene Uses Cloo Name: PI Enabled: Frequenc, Accuracy By default, all o Resources edi	rated: Yes ck: Tree Resource ck: Info L_OUT Yes y: 24.000 MHz : ±1 clocks are marked as tor.	: Yes : 'start on reset'	'. The setting	can be change	id in the Design Wide
Datasheet		ОК		Apply	Cancel

5.2.5.5 Clock_SW

This is a digital port component used to read the pin status. It is configured as "Input" port. The drive mode of the pin is configured to Resistive Pull Up mode because the switch input is a Active High input.

Figure 5-25. Switch Pin Configuration: General Tab

Configure 'cy_pins'		? 🛛
Name: Control_SW	set Built-in	4 Þ
Number of Pins: 1		
[All Pins]	Type General Input O Drive Mode Resistive Pull Up	Initial State: Low (0)
Datasheet	ОК Арр	ly Cancel



Note Pin assignment in both code examples is according to Port A of the DVK. Open the code example and change the pin assignment in PSoC Creator (.cydwr file) for Port A' or Port B according to Table 4-2. The pin assignment for code example 1 is shown in Figure 5-26.

Start Page TopDesign.cysch LCD_Seg_Eeter.cydwr						→ 4 Þ ×
	Alias	Name	Pin	L	Lock	Туре
	VR	VR	P1[7]	~		Analog
		LCD_Seg_Com[7]	P0[0]	~		Digital Output
		LCD_Seg_Com[6]	P0[1]	~		Digital Output
		LCD_Seg_Com[5]	P0[2]	~		Digital Output
And And And And And And And And And		LCD_Seg_Com[4]	P0[3]	~		Digital Output
100, Seg. Seg. 9 [1] P2(5) Ved 33 [19/		LCD_Seg_Com[3]	P0[4]	~		Digital Output
(40) Seg Seg (2) (73) (41) (50) Seg Carr(4)		LCD_Seg_Com[2]	P0[5]	~		Digital Output
4 Pr2(4) 120 SC. Pr2(1) 22 LCD Sc.		LCD_Seg_Com[1]	P0[6]	~		Digital Output
5 Pr2(8) (22.50x Pr2(8) (21.50x Pr2(8) (21.50x LCD_Sing_Sing(12) (01.50x Pr2(8) (21.50x Pr2(8) (21.50x		LCD_Seg_Com[0]	P0[7]	~		Digital Output
LCD Seg Seg 13 7 P013 P013 P013 00		LCD_Seg_Seg[15]	P6[7]	~		Digital Output
LCD Seg Seg 10 2 P0(7) P12(2 67		LCD_Seg_Seg[14]	P6[6]	~		Digital Output
Web Wed Wed Ed 151 Ind 557 108 557		LCD_Seg_Seg[13]	P6[5]	~		Digital Output
		LCD_Seg_Seg[12]	P6[4]	~		Digital Output
Vied CY8C3866AXI-040 ***		LCD_Seg_Seg[11]	P6[3]	~		Digital Output
ve page 100-TQFP ne d		LCD_Seg_Seg[10]	P6[2]	~		Digital Output
17 Pilt nr. 22		LCD_Seg_Seg[9]	P6[1]	~		Digital Output
9 P\$3 nc 92		LCD_Seg_Seg[8]	P6[0]	~		Digital Output
CERSE OP PIG SNO 10, JFAC TWS XFA, 304± 3/ PSQ 3 39 CERSE PIN SNO OK JFAC TOK XFA, 304± 3/ PSQ 3 35		LCD_Seg_Seg[7]	P2[7]	~		Digital Output
22 P1(2) XVES 102 120 121 121 121 121 121 121 121 121		LCD_Seg_Seg[6]	P2[6]	~		Digital Output
24 PP(4)/FAC TO: E C C C C C C C C C C C C C C C C C C		LCD_Seg_Seg[5]	P2[5]	~		Digital Output
		LCD_Seg_Seg[4]	P2[4]	~		Digital Output
prov. Side and a second		LCD_Seg_Seg[3]	P2[3]	~		Digital Output
3 3 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8		LCD_Seg_Seg[2]	P2[2]	~		Digital Output
		LCD_Seg_Seg[1]	P2[1]	~		Digital Output
		LCD_Seg_Seg[0]	P2[0]	~		Digital Output
🔗 🖗 Pins 🕑 Clocks 🖋 Interrupts 👫 DMA 🦻 System 🖺 Directives						4 Þ

Figure 5-26. Pin Connection Mapping for Port A'

Note The pins for VR and SW1 must be reassigned to any other free GPIO when using Port A' and Port B. This is because P0_2 pin used in both code examples for VR and SW1, is used for common lines.

Code Examples



A. Appendix



A.1 Schematic





A.2 Board Layout

A.2.1 PDCR-09571 Top View



A.2.2 PDCR-09571 Bottom View

							-			1.0	-		11.2			1	1.7	1.0	10	20	21	199		-	
PIN		14				•	1			10	11	12	13	1.	1.5	1.0	11	10	1.8	20	21	66	63	24	
çêm	Cim.	_			_		_		11		-	OULI	- 10			or 1	n.	-	12	10	0013	COLA	- 15	- 10	
COMP		CORD							64	^u	-	U.	-	**	- 44	4		- 54	-	44	-				
çtan			-0888							-				-							140	16	- 86	ж.	
-				088					N.	19	. 25			-				88.	•		140	1.		8	
0864					0000				-89	11	- 28	2	1.8	8	-	4		8	-		116	-	- 25	16	
-0000						C063			15	15	*	16		- 25		46	*	86		86	148				
-	-						000			-			-38					-			197				
ON								CERE	-18	10		-	-	-				-	-		184		84.	78	
		-	_				-		-	-			-	-	-	-							-		******

Note See the Hardware folder in Kit CD for Schematic and Layout PDF files.



A.3 BOM

Item	Qty.	Reference	Description	Manufacturer Name	Manufacturing Part Number						
1			РСВ	Cypress	PDCR-09571 REV**						
2	1	LCD1	LCD Glass	Golden View Display	GV13956A-TPP						
3	1	J1	CONN HEADER.100 DUAL R/A 40POS	Sullins Connector Solutions	S2111E-20-ND						
No Load											
4	6	R1, R2, R3, R4, R5, R6	RES 10 KΩ 1/16W 5% 0402 SMD	Panasonic - ECG	ERJ-2GEJ103X						
5	1	U1	IC SRL EEPROM I2C 2 KBIT SO-8	STMicroelectronics	M24C02-RMN6TP						
Install at the bottom of PCB as close to the corners as possible											
6	4	N/A	BUMPER WHITE.500X.23 SQUARE	Richco Plastic Co	RBS-3R						

