



## STB40NF10L

N-channel 100V - 0.028Ω - 40A - D<sup>2</sup>PAK  
Low gate charge STripFET™ II Power MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB40NF10L	100V	<0.033Ω	40A

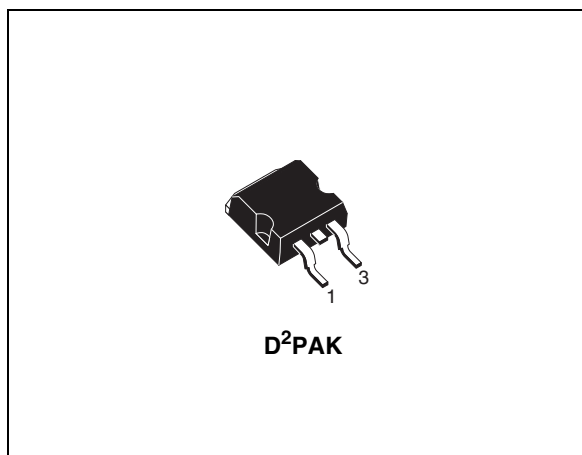
- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

### Description

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STB40NF10L	B40NF10L	D <sup>2</sup> PAK	Tape & reel

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	100	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	100	V
$V_{GS}$	Gate- source voltage	$\pm 15$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	40	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	25	A
$I_{DM}^{(1)}$	Drain current (pulsed)	160	A
$P_{tot}$	Total dissipation at $T_C = 25^\circ\text{C}$	150	W
	Derating Factor	1	W/°C
$E_{AS}^{(2)}$	Single pulse avalanche energy	430	mJ
$T_{stg}$	Storage temperature	-65 to 175	°C
$T_j$	Max. operating junction temperature		

1. Pulse width limited by safe operating area.

2. Starting  $T_j = 25^\circ\text{C}$ ,  $I_D = 20\text{A}$ ,  $V_{DD} = 40\text{V}$

**Table 2. Thermal data**

$R_{thj-case}$	Thermal resistance junction-case max	1	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	°C/W
$T_J$	Maximum lead temperature for soldering purpose	300	°C

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating},$ $T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 20A$ $V_{GS} = 5V, I_D = 20A$		0.028 0.030	0.033 0.036	$\Omega$ $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 20A$		25		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$		2300		pF
$C_{oss}$	Output capacitance			290		pF
$C_{rss}$	Reverse transfer capacitance			125		pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50V, I_D = 20A$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see <a href="#">Figure 13</a> )		25		ns
$t_r$	Rise time			82		ns
$t_{d(off)}$	Turn-off delay time			64		ns
$t_f$	Fall time			24		ns
$Q_g$	Total gate charge	$V_{DD} = 80V, I_D = 40A,$ $V_{GS} = 4.5V, R_G = 4.7\Omega$ (see <a href="#">Figure 14</a> )		46	64	nC
$Q_{gs}$	Gate-source charge			12		nC
$Q_{gd}$	Gate-drain charge			22		nC

1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

**Table 5. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				40 160	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 40A, V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 40A, di/dt = 100A/\mu s,$ $V_{DD} = 30V, T_j = 150^\circ C$ (see <a href="#">Figure 15</a> )		110 467 8		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

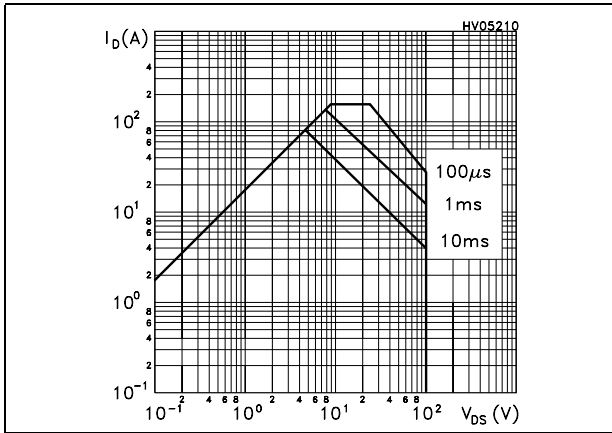


Figure 2. Thermal impedance

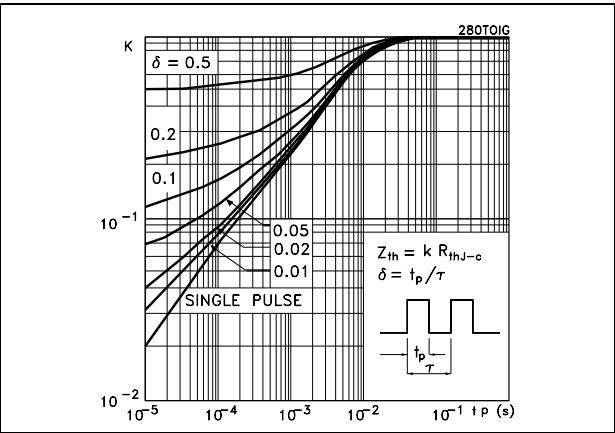


Figure 3. Output characteristics

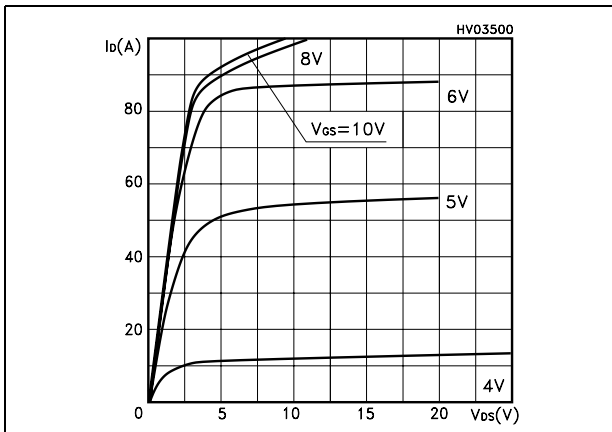


Figure 4. Transfer characteristics

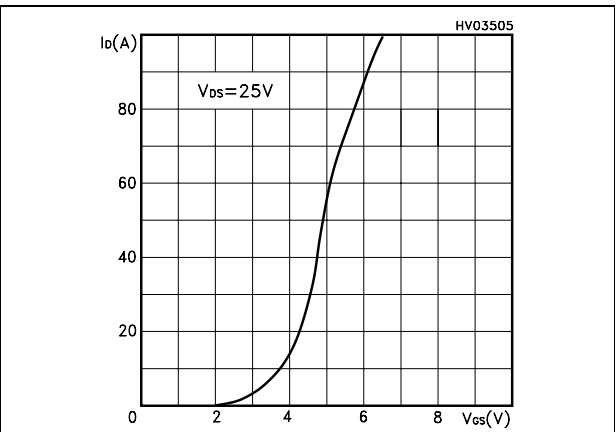


Figure 5. Transconductance

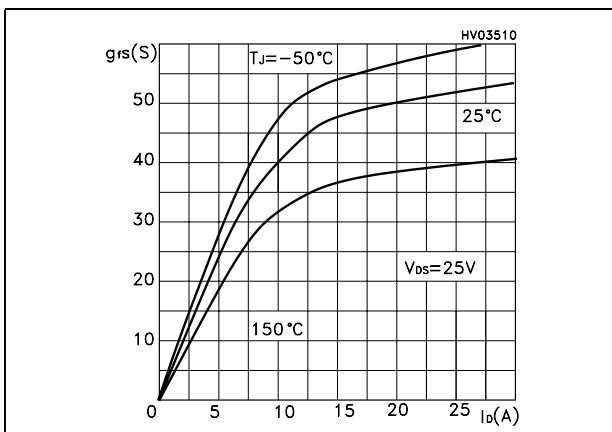


Figure 6. Static drain-source on resistance

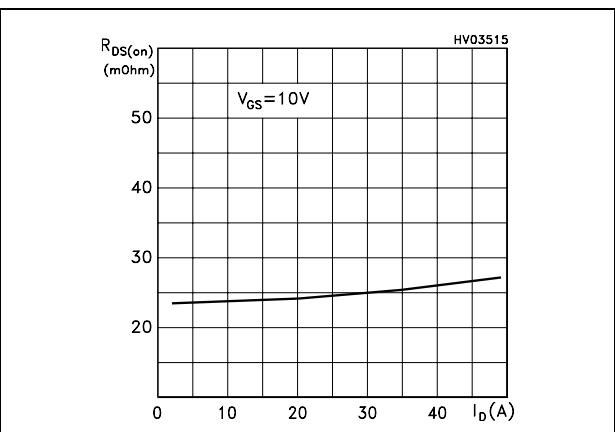


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

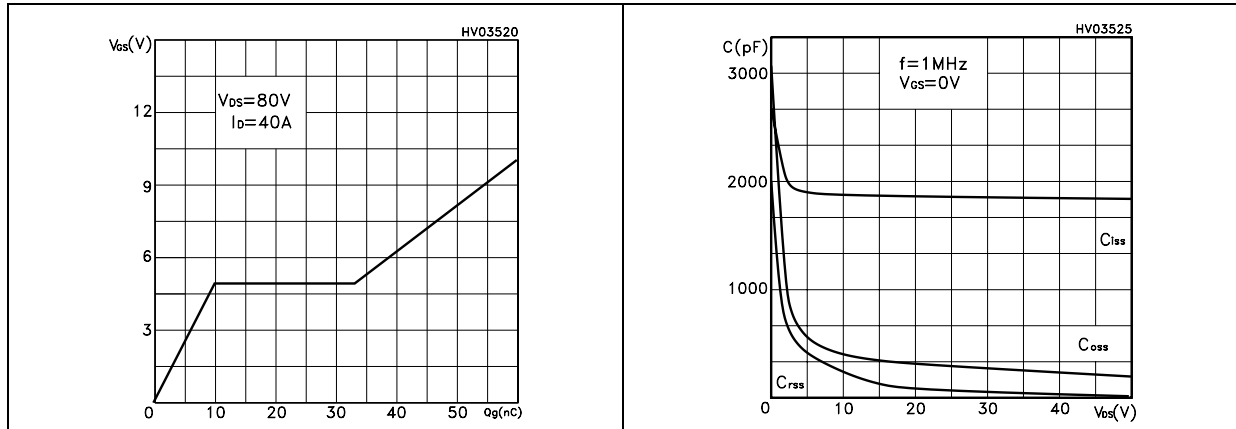


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

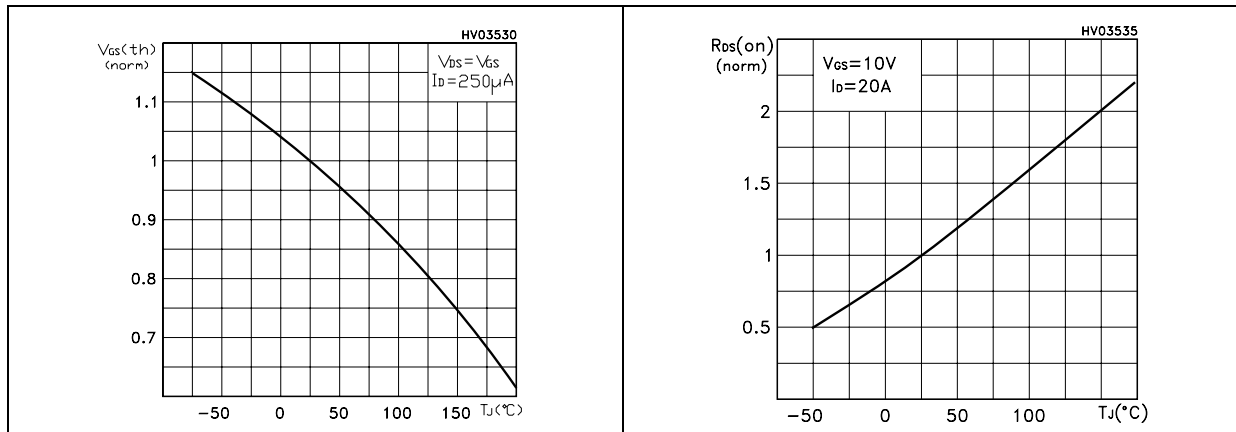
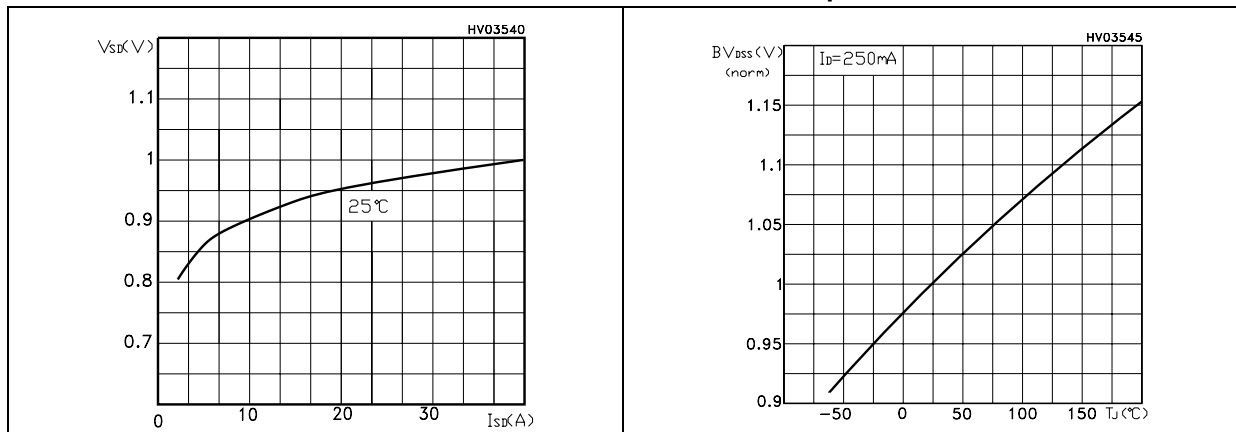


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

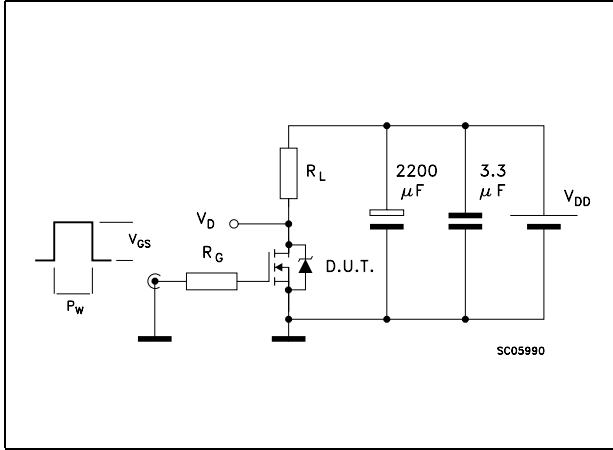


Figure 14. Gate charge test circuit

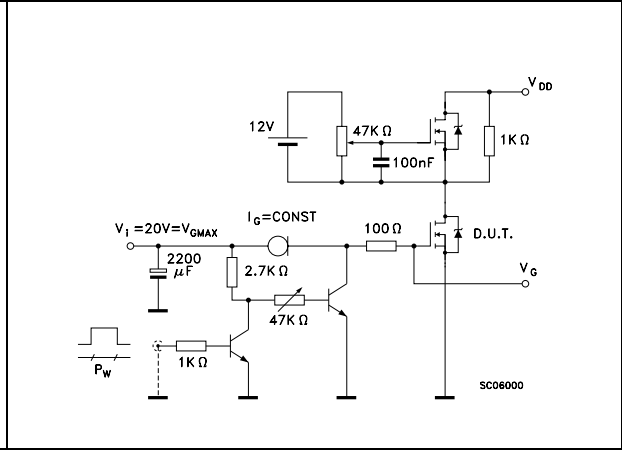


Figure 15. Test circuit for inductive load switching and diode recovery times



Figure 16. Unclamped Inductive load test circuit



Figure 17. Unclamped inductive waveform



Figure 18. Switching time waveform



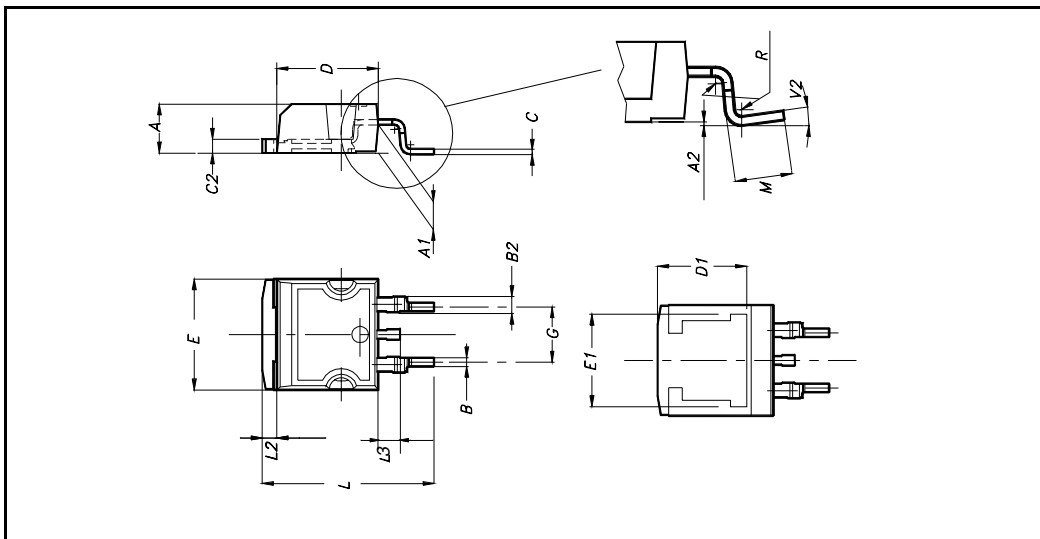


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

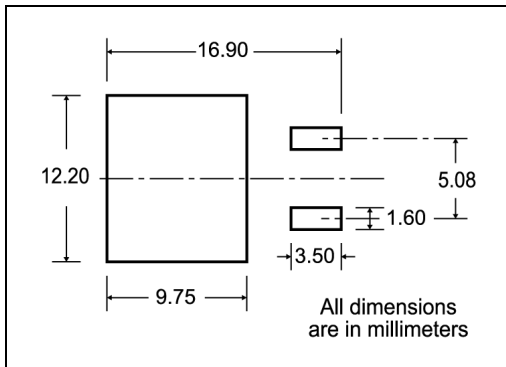
**D<sup>2</sup>PAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



# 5 Packing mechanical data

## D<sup>2</sup>PAK FOOTPRINT



## TAPE AND REEL SHIPMENT

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

\* on sales type

## 6 Revision history

**Table 6. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
21-Jun-2004	1	First release
26-Jun-2006	2	New template, no content change

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