REV 1.2

TECHNICAL DESCRIPTION

Fastrax IT520 OEM GPS Receiver

This document describes the electrical connectivity and electrical functionality of the Fastrax IT520 OEM GPS Receiver.

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Fastrax Ltd.

Fastrax

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CHANGE LOG

Rev.	Notes	Date
1.0	Initial documentation	2010-02-01
1.1	Minor modifications in text.	2010-02-01
1.2	BOM and PCB layer info for application board added. Active antenna gain requirement modified in table 1.	2010-09-10

CONTENTS

COMPLEMENTARY READING

The following Fastrax reference documents are complementary reading for this document. All operating and firmware related documentation is also available at ***www.fastraxgps.com***

Ref. #	Document name
1	IT500 brochure
2	Fastrax 500 Series NMEA protocol specification
3	Module Soldering Profile

1 GENERAL DESCRIPTION

1.1 General

The Fastrax IT520 is a GPS module, which provides receiver functionality using the low power, ultra-high performance MediaTek MT3329 chip (also previously launched as Fastrax IT500, *ref 1*). The module has tiny form factor 10.4mm x 14.0mm, height is 2.3mm nominal. The IT520 receiver provides low power operation and very fast TTFF. Extreme weak signal acquisition and tracking capability meet the most demanding performance expectations and enable even indoor operation. The module will be available in two variants:

- IT520 (with two UART ports)
- IT520U (with USB 2.0 interface)

The Fastrax IT520 module provides complete signal processing from antenna to host port data output (*ref 2*). MTK Binary protocol can be used to push predicted ephemeris data into the IT520 receiver in AGPS applications. With IT520U module variant one of the serial ports is replaced with USB 2.0 interface,

The Fastrax IT520 module requires a power supply VDD and a backup supply voltage VDD_B for non-volatile RAM & RTC blocks, and GPS antenna input signal. The IT520 module interfaces to the customer's application via serial port. Other I/O signals include PPS timing signal, Fix valid indicator signal and active Antenna Bias Supervisor status signals (2 outputs). Serial data and all I/O signal levels are 2.8V CMOS compatible and inputs are 3.6V tolerable.

The antenna input supports passive and active antennas and provides also an internally generated and current limited antenna bias supply with Antenna Bias Supervisor state outputs.

A control input is reserved for future firmware support, which can be used to set the module in low power standby state while keeping the VDD supply active.

This document describes the electrical connectivity and main functionality of the IT520 module.

1.2 Block diagram

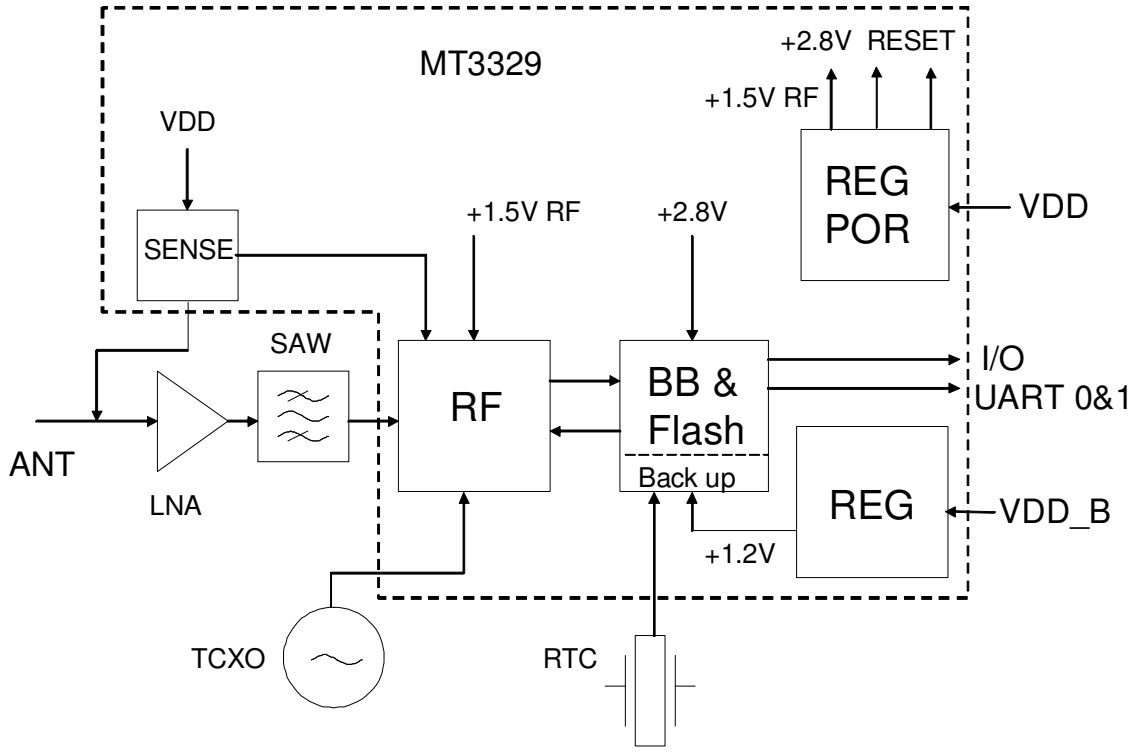


Figure 1 Block diagram

1.3 Frequency plan

Clock frequencies generated internally at the Fastrax IT520 receiver:

- 32768 Hz real time clock (RTC)
- 16.368 MHz master clock (TCXO)
- 3142.656 MHz and 1571.328 MHz local oscillator of the RF down-converter

2 SPECIFICATIONS

2.1 General

Table 1 General Specifications

Receiver	GPS L1 C/A-code, SPS
Channels	22 tracking / 66 acquisition
Update rate	1 Hz default (fix rate configurable up to 10Hz)
Supply voltage, VDD	+3.0V…+4.2 V
Back up supply voltage, VDD_B	+2.0V…+4.2 V (preferably active all the time)
USB supply voltage, VDD_USB	+3.0… +3.6V (available only on IT520U).
Power consumption, VDD	75 mW typical @ 3.0V (without Antenna bias)
Power consumption, VDD_B	15 uW typical @ 3.0V (during Back up state)
Power consumption, Standby mode	3mW typical @ 3.0V
Power consumption, VDD_USB	7 mW typical @ 3.3V during operation (IT520U)
Antenna net gain range	+6…+25dB (including cable loss)
Antenna bias voltage	Same as VDD
Antenna bias current	3mA…30mA (internally limited to 30 mA typ.)
Storage temperature	-40ºC…+85ºC
Operating temperature	-40ºC…+85ºC
Serial port configuration (default)	Port 0: NMEA (IT520U: USB 2.0); Port 1: RTCM
Serial data format	8 bits, no parity, 1 stop bit
Serial data speed (default)	NMEA: 9600 baud
I/O signal levels	2.8V CMOS compatible: low state 0.0…0.8V; high state 2.0…2.8V. Inputs are +3.6V tolerable. Note: FOUT_32K output is 1.2V CMOS compatible.
I/O signal drive capability	+/- 4mA typ.

2.2 Absolute maximum ratings

Table 2 Absolute maximum ratings

Item	Min	Max	unit
Operating and storage temperature	-40	+85	ºC
Power dissipation	-	500	mW
Supply voltage, VDD	-0.3	+4.2	V
Supply voltage, VDD_B	-0.3	+4.2	V
Supply voltage, VDD_USB	-0.3	+3.6	V
Current output on antenna input	0	+50	mA
Input voltage on any input connection	-0.3	+3.6	V
Input voltage at BU_BATT	-0.3	+1.8	V
RF input level (out of band > ±50 MHz)	-	+15	dBm

3 OPERATION

3.1 Operating modes

After power up the receiver boots from the internal flash memory for normal operation. Modes of operation:

- Tracking/navigating mode
- Low power tracking/navigating mode
- Standby state
- Backup state

3.2 Tracking/Navigating mode

In tracking/navigating mode the Fastrax IT520 receiver module will search for satellites and collects almanac data. Once the receiver has collected almanac data (this takes about 12 minutes from Factory Cold Start) and stored it in internal Flash memory, it will automatically enter Low Power Tracking mode. The VDD power consumption in table 1 is measured in Low Power Tracking/Navigating mode.

3.3 Low Power Tracking/Navigating mode

In Low power tracking/navigating mode the receiver continues normal navigation but does not collect further Almanacs data (ephemeris data is collected whenever new satellites become visible). Therefore the current consumption is reduced to level of 75 mW typ..

3.4 Standby state

The Standby state is a firmware option (default). In Standby state the IT520 receiver will power down internally the RF-part including antenna bias of the ANT input and puts the processor in standby state. RTC oscillator is running and RAM content is maintained over the Standby state. The current consumption is greatly reduced from Low Power Tracking/Navigating mode, but remains higher than in Backup state (see table 1). The Standby state is initiated by falling edge at STANDBY signal. The module can be waked up from Standby state by rising edge at the STANDBY signal.

3.5 Backup state

When the main supply VDD is removed from the Fastrax IT520 while keeping back up supply VDD_B active, the module enters Backup state. In this state, the module sustains GPS time estimate by the RTC oscillator. Also, satellite ephemeris data is stored in battery backup RAM in order to enable fastest possible TTFF when VDD is powered back again.

During Backup state all outputs are at low state but all inputs can remain at low or high state.

Any user configuration settings are valid as long as the backup supply is active. When the VDD_B is powered off, the configuration is reset to factory configuration on next power up.

3.6 Default firmware configuration

Fastrax IT520 default firmware configuration:

1. Port 0: NMEA 9600 baud
2. Port 1: RTCM input, 9600 baud
3. NMEA output: GGA, RMC, GSV, GSA (all 1 sec interval)
4. DGPS/SBAS: Disabled, can be enabled with NMEA command (*ref 2*).
5. Datum: WGS84

4 CONNECTIVITY

4.1 Connection assignments

The I/O connections are available as soldering pads on the bottom side of the module. These pads are also used to attach the module on the motherboard in application. All unconnected I/O should be left open (floating) unless instructed to use pull external up or pull down.

Table 3 Connections

Contact	Signal name	I/O	Alternative signal name	Signal description
1	ANT	I/O	-	Antenna signal input 50 ohm; Antenna bias voltage output, filtered from VDD supply.
2	GND	-	-	Ground
3	GND	-	-	Ground
4	GND	-	-	Ground
5	GND	-	-	Ground
6	VS_AA	O	-	Antenna Bias supply voltage. High= Bias voltage OK; Low= Bias voltage short circuit.
7	FOUT_32K	O	-	Reserved for future usage; option for clock 32768Hz output 1.2V CMOS.
8	VDD_B	S	-	Back up power supply +2.0... 4.2V
9	VDD	S	-	Power supply +3.0V... 4.2V.
10	BU_BATT	Analog 1.08 to 1.4V	-	Optional connection to external backup Super Capacitor, nominal voltage 1.29V. Suggestion is to leave open and use VDD_B.
11	GND	-	-	Ground
12	FIX_VALID	O		Valid fix indicator.
13	VDD_USB	S	-	Power supply +3.3V for IT520U USB. Leave open for IT520.
14	STANDBY	I	-	Control input for Standby state. Pulled up with internal 75 kohm typ. Leave open if not used.
15	RXD1	I	-	UART 1 async. input. Internally pulled up with 75 kohm typ.

16	TXD1	O	-	UART 1 async. output
17	GND	-	-	Ground
18	RXD0	I	USB_D-	UART 0 async. input, internally pulled up with 75 kohm typ, or USB_D- (only IT520U)
19	TXD0	O	USB_D+	UART 0 async. output or USB_D+ (only IT520U)
20	PPS	O	-	1PPS signal output.
21	GND	-	-	Ground
22	ANT_OK	O	-	Active antenna status indicator. High=bias >3mA (typ,); Low=bias <3mA (typ.)
23	GND	-	-	Ground
24	XRESET	I	-	Asynchronous system reset input, active when low. Internally pulled up with 75 kohm typ.
Contact	**Signal name**	**I/O**	**Alternative signal name**	**Signal description**

4.2 Power supply

The Fastrax IT520 module requires two separate power supplies: VDD_B for non-volatile back up block (RTC/RAM) and the VDD for digital and RF parts. IT520U module variant requires additional supply VDD_USB +3.3V for the USB driver (+5V is available from USB host, use external regulator for +3.3V supply). I/O block has internal +2.8V regulator and thus I/O signals are 2.8V CMOS compatible. VDD can be switched off when navigation is not needed but if possible keep the backup supply VDD_B active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF.

Back up supply VDD_B draws typically 5 uA current in back up state. During navigation VDD_B current typically peaks up to 55 uA and is in average 30-40 uA.

Main power supply VDD current varies according to the processor load and satellite acquisition. Maximum VDD peak current is about 40 mA during acquisition.

NOTE

Backup supply VDD_B has to be active whenever main supply VDD is active.

4.3 Reset

The reset input XRESET is an active low asynchronous reset. The processor boots after the low-to-high transition. At power up or power down the reset is forced internally when the VDD is below 2.8 V. The XRESET input is internally pulled high with 75 kohm resistor (typ.) and for normal operation the input can be left unconnected (floating).

4.4 STANDBY control input

STANDBY control input is reserved to firmware support for standby functionality. High state = Tracking/Navigation mode; Low state = Standby state (navigation stopped). The input is pulled high with 75 kohm typ. during Tracking/Navigation mode (and pulled to low state during Standby state). Typical current drain from VDD supply is 1mA during Standby state.

NOTE

If not used, leave STANDBY not connected (floating).

4.5 Antenna input

The module supports passive and active antennas. The antenna input impedance is 50 ohms. During Tracking/Navigating mode, the input provides also a bias supply (internally filtered from VDD). When the navigation is stopped (e.g. in Reset, Backup or Standby states), the antenna bias is switched off internally.

NOTE

Passive antennas with a short-circuit to GND should be DC blocked externally with a 18pF…1nF serial capacitor.

NOTE

With passive antenna keep the cable loss at minimum (<1dB).

4.6 Active GPS antenna

The customer may use an external active GPS antenna in case the antenna is placed further away from the module. It is suggested the active antenna has a net gain *including cable loss* in the range +6 dB…+25 dB.

Antenna input provides also internal Antenna Bias Supervisor and current limiter. If more current is drawn, for example in case of antenna short circuit >30mA (typ.), the fault is indicated by Antenna Bias Supervisor outputs. Also, if the active antenna is removed or antenna cable is cut,

the state is indicated respectively. The antenna status indicator output states are described in table below.

Table 1. Antenna Bias Supervisor output signals.

Signal	Antenna Bias OK (bias 3…30mA)	Antenna short (bias >30mA)	Antenna open or passive antenna (bias <3mA)
ANT_OK	High	High	Low
VS_AA	High	Low	High

NOTE

VS_AA output level is at VDD (max 4.2V). Thus use a series resistor (> 1kohm) at VS_AA output to limit current at external 3.3V CMOS inputs.

The internal Antenna bias supply has some internal impedance that will cause a drop in supplied bias voltage, which depends on load current at external active antenna. Typical voltage drop from VDD is 0.2V at 15mA and 0.7V at 25mA active antenna current. If higher bias current is required, it can be provided by an external LC-circuit connected to the Antenna input.

4.7 UART

The device supports UART communication via Port 0 and Port 1. With the standard firmware the Port 0 is configured by default to NMEA protocol with 9600 baud and Port 1 to RTCM protocol (input only) with 9600 baud. For supported messages see NMEA manual for Fastrax IT500 series (*ref 2*).

The default configuration for Ports can be changed by commands via NMEA (*ref 2*). Any custom configuration stays active as long as the backup supply VDD_B is active.

I/O levels form the serial ports are 2.8V CMOS compatible, not RS232 compatible. Inputs are 3.6V tolerable. Use an external level converter to provide RS232 levels when needed.

4.8 USB

The Fastrax IT520U module variant has a built-in USB 2.0 interface. The USB interface will use the same pins as UART0 of the IT520. With IT520U the USB power supply VDD_USB (+3.3V) has to be active. Do not connect USB +5V supply to VDD_USB; instead use external +3.3V regulator powered from USB +5V supply.

NOTE

The Main Power supply VDD has to be switched on simultaneously or before the USB power supply VDD_USB.

Use external +3.3V regulator powered from USB +5V supply.

4.9 PPS

The pulse-per-second (PPS) output provides an output for timing purposes. There is a 100ms pulse once per second synchronized to UTC second at rising edge when the receiver has a valid position fix available.

4.10 FIX_VALID

FIX_VALID signal indicates if there is a valid GPS fix available. When there is no valid fix available, this signal is at constant low state ('0'). When a valid fix is available, this signal is toggling between low and high state at 0.5Hz and 50% duty cycle (1sec high, 1sec low).

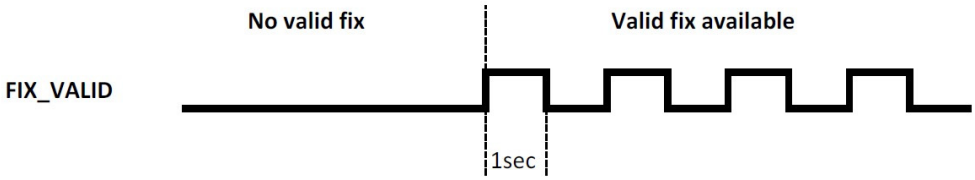


Figure 1. FIX_VALID output operation.

4.11 BU_BATT

The BU_BATT is optional connection for external back up super capacitor, e,g, 1F. The nominal charge voltage is 1.29V, which is internally generated from VDD_B supply. Charge current is 5mA max (VDD_B active) and load current during backup is 3uA typ. (VDD_B off).

The BU_BATT usage is not suggested method for back up super capacitor connectivity, since the backup capacity is lower due to lower voltage range 1.08… 1.29V. In contrast the suggested method is to connect a rechargeable battery to VDD_B and to charge it via a schottky diode from the 3… 3.3V VDD supply, which gives much more discharge capacity. See application circuit diagram for reference.

4.12 Mechanical dimensions and contact numbering

Module size is 10.4mm (width) x 14.0mm (length) x 2.3mm (height 2.6mm max). General tolerance is ±0.3mm. The dimensions are compatible with Fastrax IT321 module (but pin out and signal assignments differ).

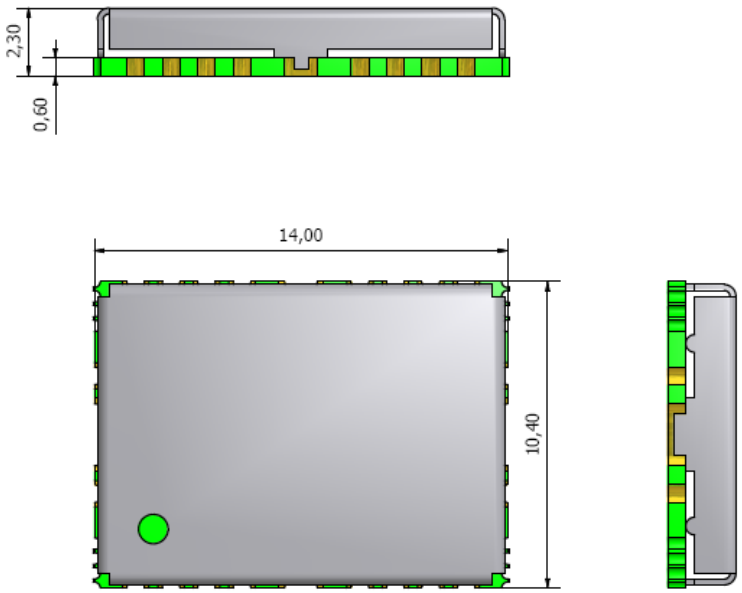


Figure 2 Dimensions

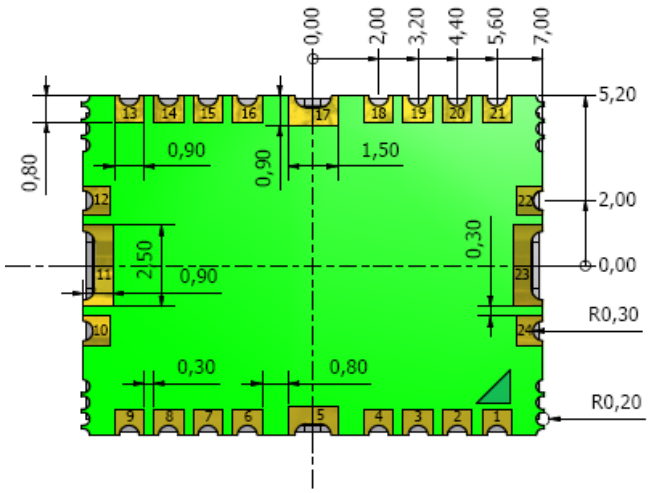


Figure 3 I/O pad numbering and dimensions, bottom view.

4.13 Suggested pad layout and pin out

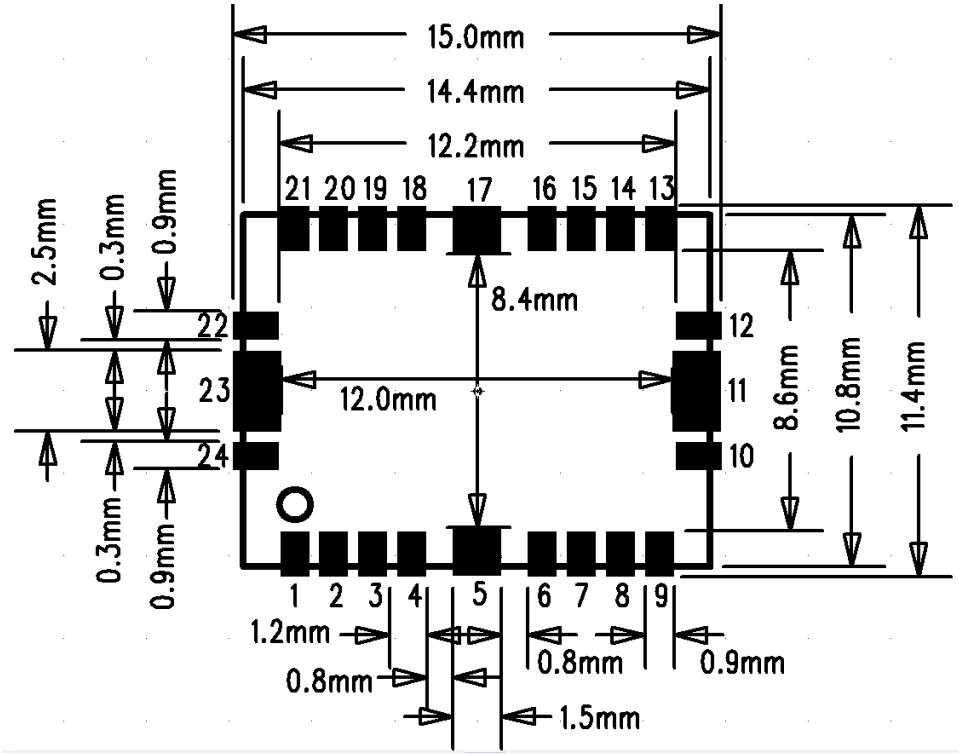


Figure 4 Suggested pad layout, occupied area and pin out, top view.

5 MANUFACTURING

5.1 Assembly and soldering

The IT520 module is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. Suggested solder paste stencil height is 150um minimum to ensure sufficient solder volume. If required paste mask pad openings can be increased to ensure proper soldering and solder wetting over pads.

Use pre-heating at 150… 180 ºC for 60… 120 sec. Suggested peak reflow temperature is 235… 245ºC (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260ºC. For details see Fastrax document 'Soldering Profile' (*ref 3*).

5.2 Moisture sensitivity

Note that the IT520 is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be repacked or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

Moisture barrier bag self life is 1 year; thus it is suggested to assemble modules prior self life expiration. If the moisture barrier bad self life is exceeded, the modules must be baked prior usage; contact Fastrax support for details.

5.3 Marking

Module marking includes type and batch codes and serial number.

Type code is e.g. **IT520-130N-ITX-3541,** where

- **IT520** is module type
- **130** is firmware revision 1.3.0 and **N** is incremental firmware release revision
- **ITX** is firmware configuration code
- **3541** is BOM (Bill-of-Materials) revision code

Batch code is e.g.**100208,** where

- **1** is factory code
- **0** is last digit of the year (e.g. 2010)
- **02** is month (e.g. February)
- **08** is incremental number of the production batch during the month

Serial number is unique for each module having 10 digits including tester code, last two digits of the year, julian date code and incremental number.

5.4 Tape and reel

One reel contains 500 modules. The same reel is used for Fastrax IT321 and IT520 modules.

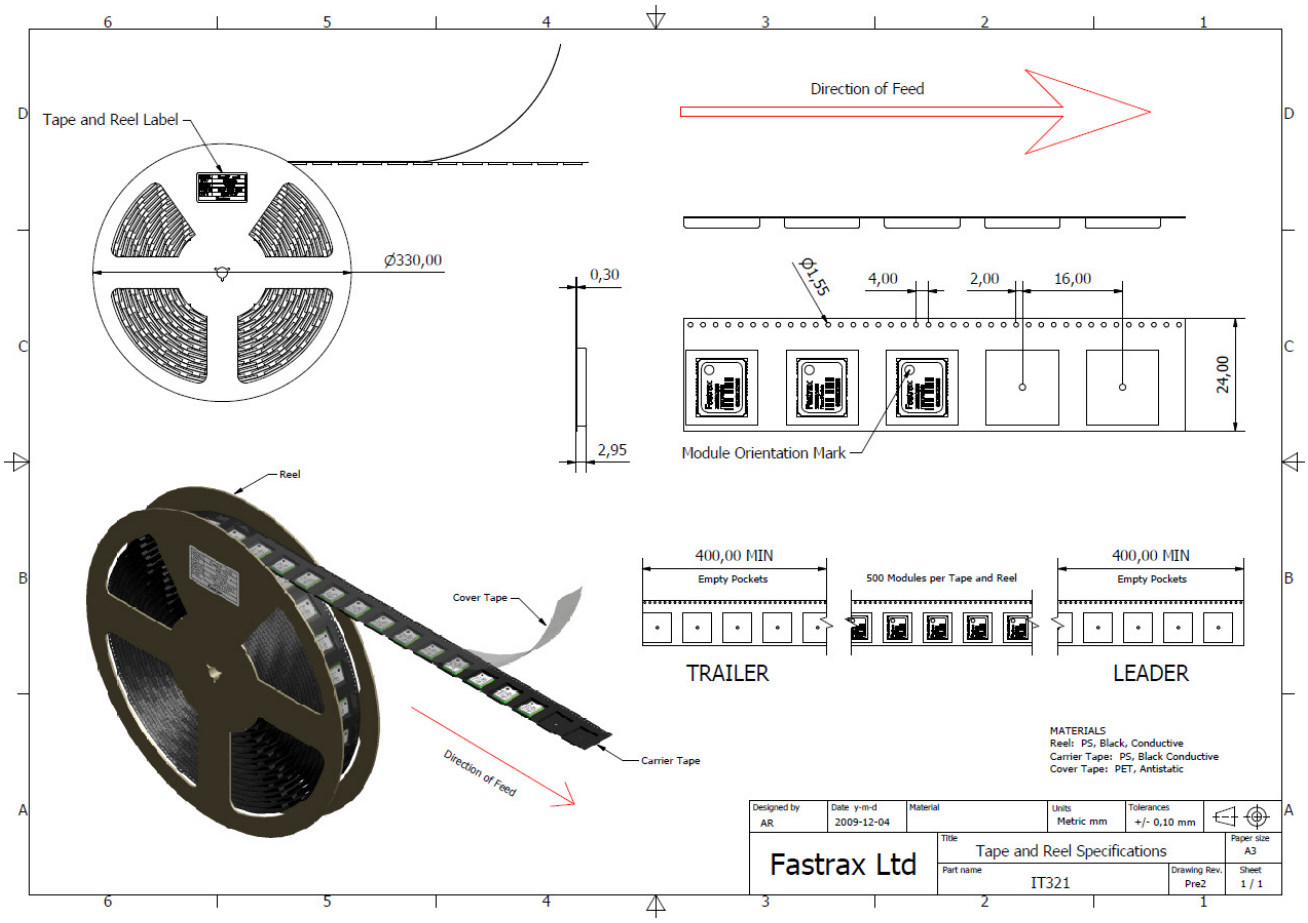


Figure 5 Tape and reel specification

6 REFERENCE DESIGN

The reference design gives a guideline for the applications using the IT520 GPS module. In itself it is not a finished product, but an example that performs correctly.

In the following two chapters the reader is exposed to design rules that should be followed, when designing an IT520 in to the application. By following the rules an optimal design with no unexpected behavior caused by the PCB layout itself can be created. These guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques and high speed logic.

6.1 Minimum Application Circuit Diagram

The Minimum Application supports communication through the UART Port 0 (NMEA protocol). Other required signals are the antenna input ANT, supply voltage for VDD and VDD_B, and GND.

The module is powered to VDD from an external +3.3V supply. The re-chargeable LiMn battery BT1 provides Backup state supply to VDD_B. When main supply VDD is active, the battery is charged and VDD_B power is provided via D1 and R1 is used to limit the BT1 charge current.

The backup supply can be provided also from a coin cell battery but then use a series diode to block out any charge current to the battery. Also any available power supply with suitable voltage range, which is active all the time, is acceptable for VDD_B supply,

All digital signals are routed away from the module through series resistors (R2…R4). In this way the local oscillator (LO) signal leakage, which is present in the I/O signals, is decoupled. Although the LO leakage is very small at the IO contacts of the module, it may still interfere the GPS reception, especially when the antenna is located very near to these signal routes. Place these series resistors close to the module with short traces.

For the same reason capacitors C1 and C2 power de-coupling capacitors should be connected very close to the module with short traces to I/O contacts and to ground plane.

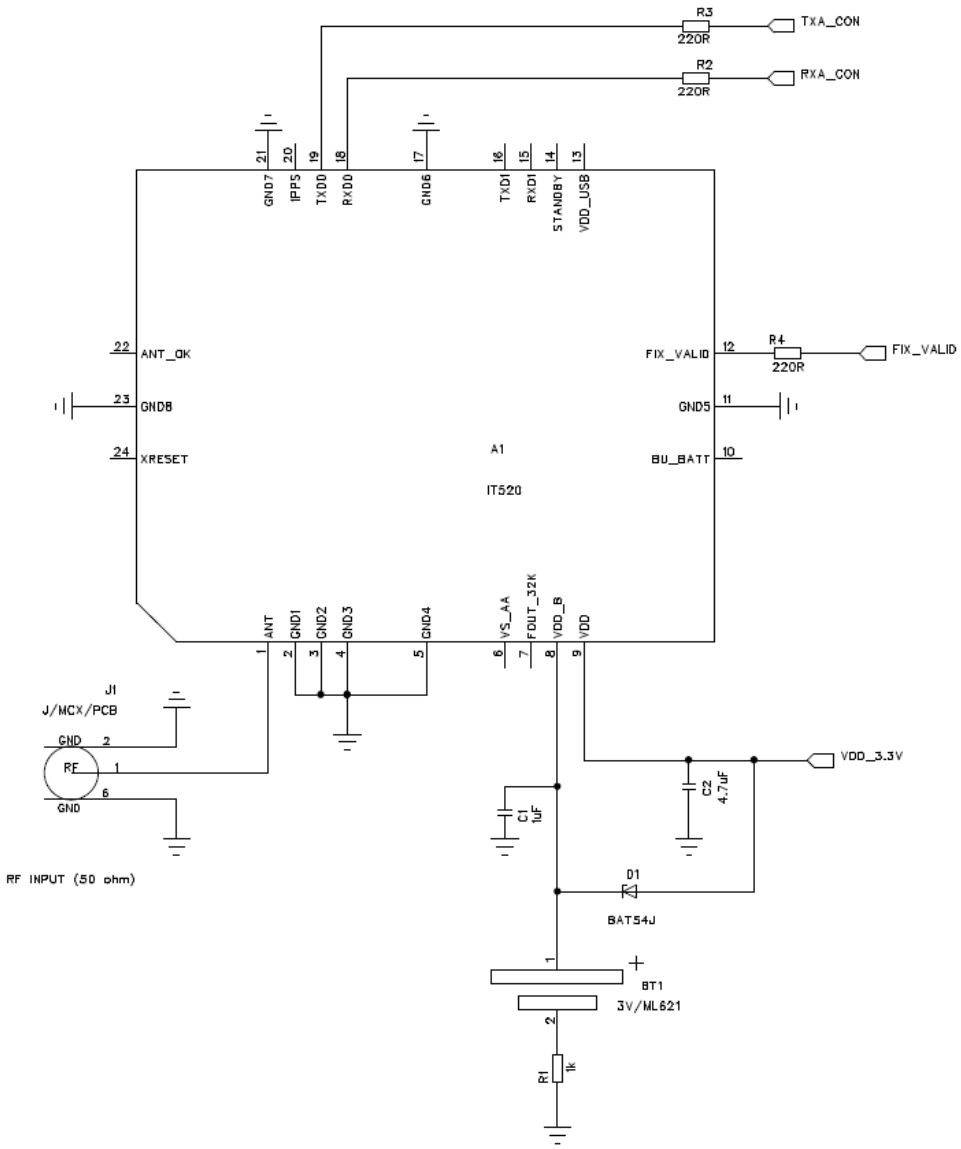


Figure 2. Minimum Application Circuit Diagram

Note that there is a DC bias voltage present at the RF input, when the module is operating in Navigating mode. If a passive antenna with short-circuit to GND is used, an external series DC block capacitor (18pF…1nF) must be used for the ANT signal line.

6.2 PCB layout issues

The suggested 4-layer PCB build up is presented in the following table.

Table 2. Suggested PCB build up.

Layer	Description
1	Signal + Ground with copper keep-out below IT520
2	Ground plane
3	Signal + Ground or VDD plane
4	Signal (short traces) + Ground

Routing signals on top layer directly under the module should be avoided. This area should be dedicated to keep-out to both traces and to ground (copper), except for via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be also minimized.

For a multi-layer PCB the first inner layer below the IT520 is suggested to be dedicated for the ground plane. Below this ground layer other layers with signal traces are allowed. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should placed very near to the IT520 module. In this way the risk for the local oscillator leakage is minimized. For the same reason by-pass capacitors C4 and C5 should be connected very close to the module with short traces to IO contacts and to the ground plane. Place the GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the IT520 to ground plane with short traces to via holes, which are connected to the ground plane. Use preferably two via holes for each GND pad.

The RF input should be routed clearly away from other signals. This minimizes the possibility of interference. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate and on the height between the signal trace and the first ground plane. With FR-4 material the width of the trace shall be two times the substrate height.

A board space free of any traces should be covered with copper areas (GND). In this way, a solid RF ground is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend during the PCB manufacturing or reflow soldering. Bending may cause soldering failures.

7 IT520 APPLICATION BOARD

The Fastrax IT520 Application Board provides the IT520 connectivity to the Fastrax Evaluation Kit or to other evaluation purposes. It provides a single PCB board equipped with the IT520 module, a 3.0V regulator, a battery for back up supply, an MCX antenna connector and a 2x20 pin Card Terminal connector. Assembly option is provided to support IT520U USB variant.

7.1 Card Terminal I/O-connector

The following signals are available at the 40-pin Card Terminal I/O connector J2. The same pin numbering applies also to the Fastrax Evaluation Kit pin header J4. I/O signal levels are CMOS 2.8V compatible and inputs are 3.6V tolerable unless stated otherwise.

Table 4 IT520 Application Board connectivity

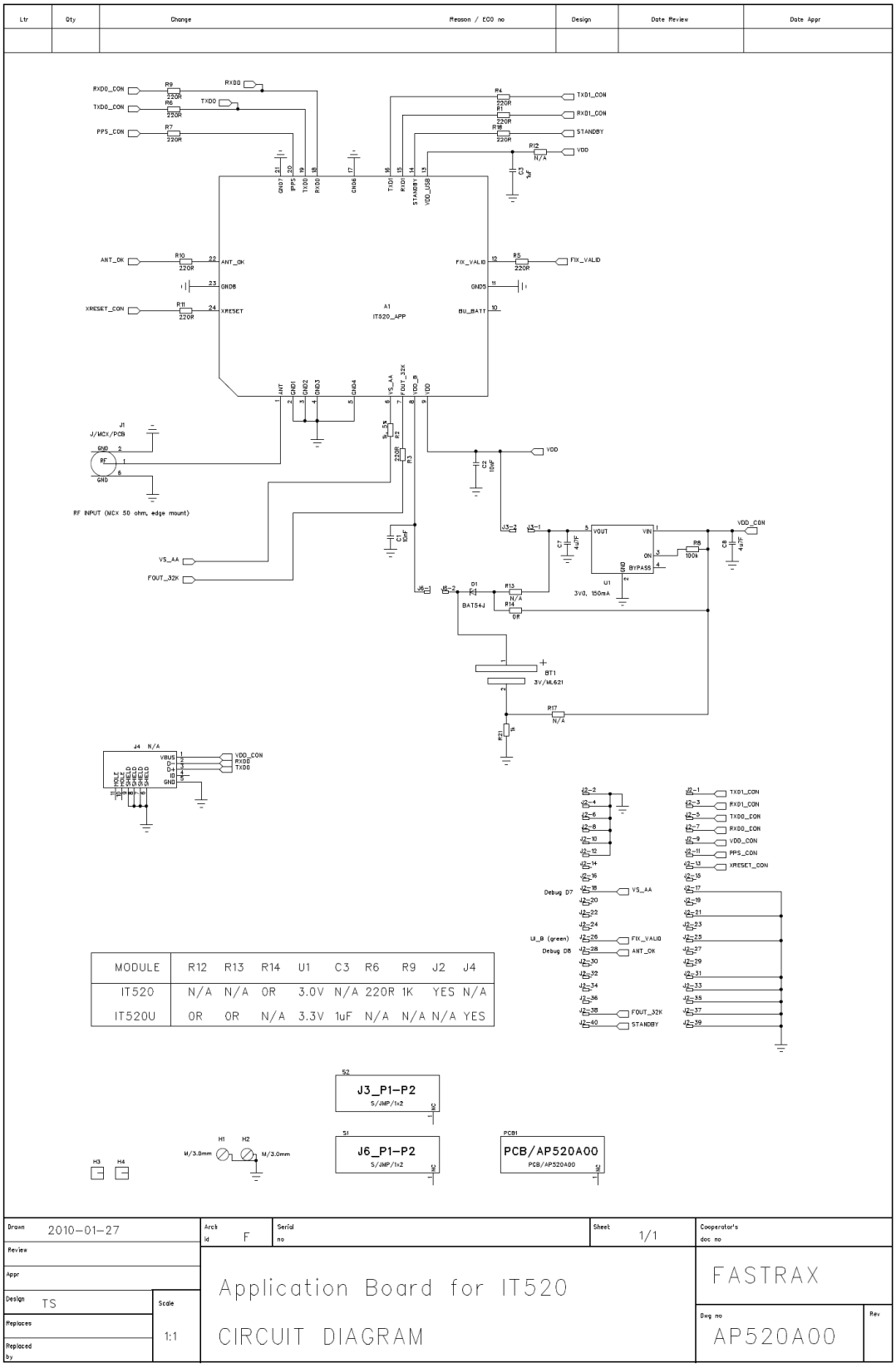
Pin	Signal name	I/O	Alternative GPIO name	Interface to Fastrax Evaluation Kit
1	TXD1_CON	O	-	UART 1 async. output
2	GND	-	-	Ground
3	RXD1_CON	I	-	UART 1 async. input
4	GND	-	-	Ground
5	TXD0_CON	O	-	UART 0 async. output
6	GND	-	-	Ground
7	RXD0_CON	I	-	UART 0 async. input
8	GND	-	-	Ground
9	VDD_CON	S	-	Power supply input +3.3V
10	GND	-	-	Ground
11	PPS_CON	O	-	1PPS signal output
12	GND	-	-	Ground
13	XRESET_CON	I	-	Active low async. system reset
14	-	-	-	Not connected
15	-	-	-	Not connected
16	-	-	-	Not connected
17	GND	-	-	Ground
18	VS_AA	O	-	Antenna Bias Supply (Debug indicator E7)

19	-	-	-	Not connected
20	-	-	-	Not connected
21	GND	-	-	Ground
22	-	-	-	Not connected
23	-	-	-	Not connected
24	-	-	-	Not connected
25	GND	-	-	Ground
26	FIX_VALID	O	-	Fix Valid indicator (UI indicator B, green)
27	-	-	-	Not connected
28	ANT_OK	O	-	Antenna Bias Current indicator (Debug E8)
29	-	-		Not connected
30	-	-	-	-
31	GND	-	-	Ground
32	-	-	-	Not connected
33	GND	-	-	Ground
34	-	-	-	Not connected
35	GND	-	-	Ground
36	-	-	-	-
37	GND	-	-	Ground
38	FOUT_32K	O	-	Option for 32768Hz clock output, 1.2V CMOS
39	GND	-	-	Ground
40	STANDBY	I	-	Option for Standby state control input
Pin	**Signal name**	**I/O**	**Alternative GPIO name**	**Interface to Fastrax Evaluation Kit**

7.2 Bill of materials, PCB rev A

Item	Qty	Reference	TECHNICALDESCRIPTION
1	1	BT1	PANASONIC ML621/F9D, 3V 5mAh
2	1	C1	10nF 16V 10% X7R 0402
3	1	C2	10nF 50V 10% X7R 0402
4	2	C7-8	4,7uF 6,3V X5R 0805 +-20%
5	1	D1	Diode 75V 225mA, BAT54J
6	1	A1	IT520 MODULE, rev A00
7	2	J3 J6	1x2 pin-header, straight, 2,54mm
8	1	J2	EDGE MOUNT SOCKET STRIP 40 PINS
9	1	J1	50 Ohm male MCX connector PCB
10	1	PCB1	Application board for IT520 rev. A
11	1	R14	Resistor chip, 0R 0402
12	1	R8	100k 5% 0402 63mW
13	1	R21	Resistor chip, 1k 5% 0402 63mW
14	1	R2	Resistor chip, 1k 5% 0402 63mW
15	8	R3-7 R10-11 R18	220R 5% 0402 63mW
16	2	R1 R9	Resistor chip, 220R 5% 0402 63mW
17	1	S2	Jumper, Pitch, 2.54mm, Red colour
18	1	S1	Jumper, Pitch, 2.54mm, Red colour
19	1	U1	Reg. 3V0, 150mA

7.3 Circuit drawing, rev A



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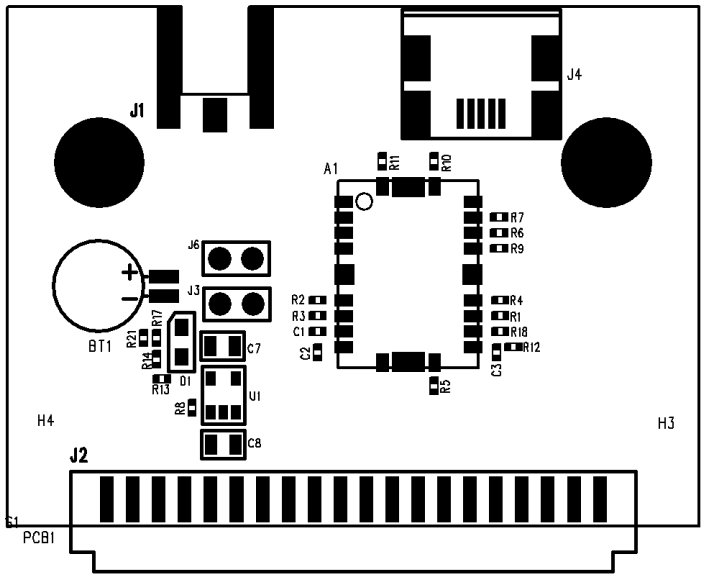
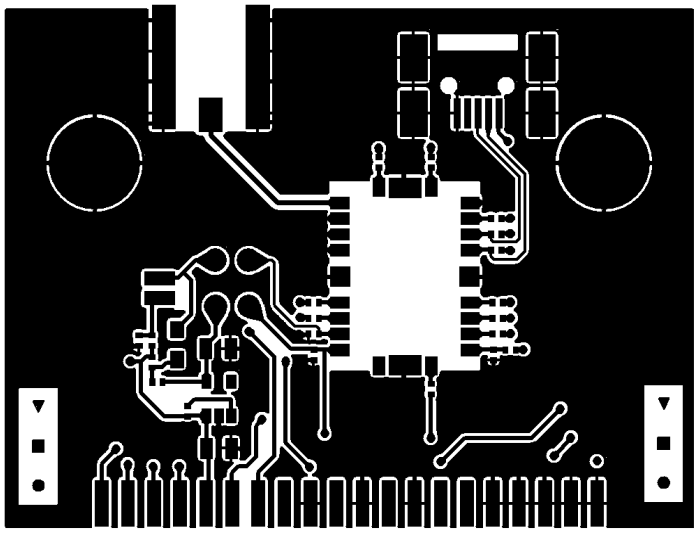
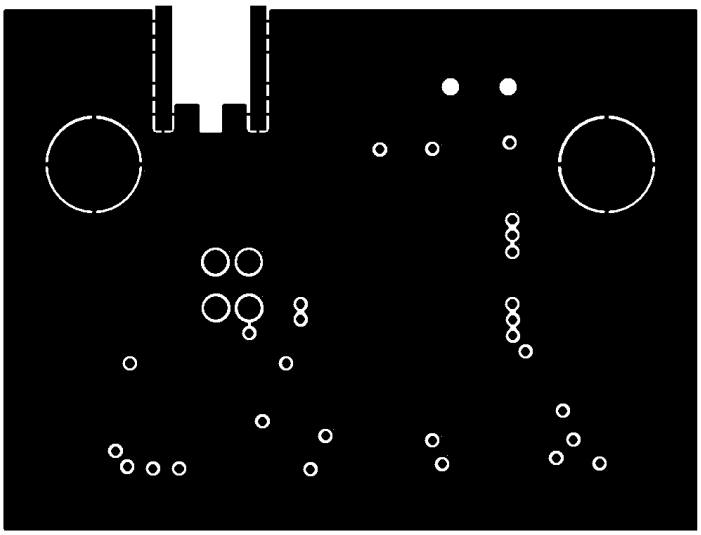
7.4 Assembly drawing, Top side, rev A



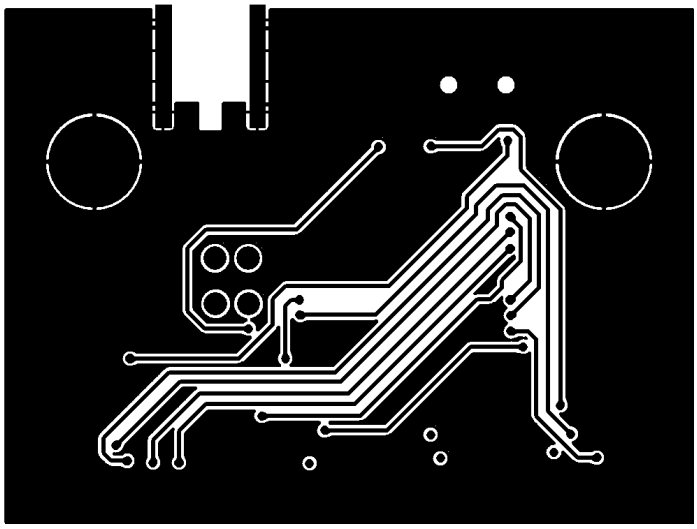
7.5 Artwork, layer 1 (Top), rev A



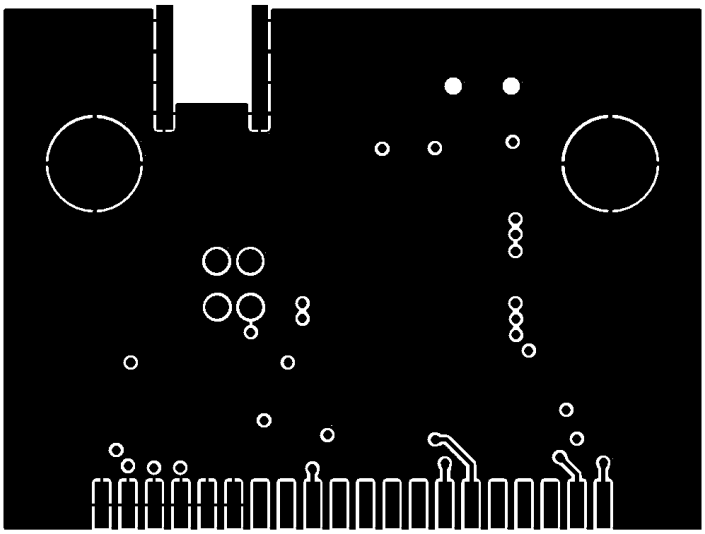
7.6 Artwork, layer 2, rev A



7.7 Artwork, layer 3, rev A



7.8 Artwork, layer 4 (Bottom), rev A



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