Data Sheet | November 29, 2011 | FN2906.8

8.5MHz, Ultra-Low Noise Precision Operational Amplifier

The HA-5127 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Intersil D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (10V/μs) wideband capability.

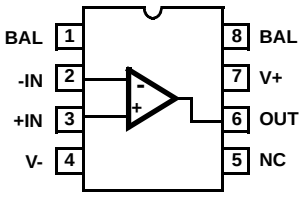
This amplifier's impressive list of features include low V_{OS} (10μV), wide unity gain-bandwidth (8.5MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range ($\pm$5V to $\pm$15V) while consuming only 140mW of power.

Using the HA-5127 allows designers to minimize errors while maximizing speed and bandwidth.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5127's qualities include instrumentation amplifiers, pulse amplifiers, audio preamplifiers, and signal conditioning circuits. This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37. For the military grade product, refer to the HA-5127/883 data sheet.

Pinout

HA-5127
(CERDIP, SOIC)
TOP VIEW



Features

- Slew Rate 10V/μs
- Unity Gain Bandwidth 8.5MHz
- Low Noise . . . . . 3nV/$\sqrt{Hz}$ at 1kHz
- Low V_{OS} 10μV
- High CMRR 126dB
- High Gain 1800V/mV
- Pb-Free Available (RoHS Compliant)

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Ordering Information

PART NUMBER (Note 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA7-5127A-5 (Note 4)	HA7- 5127A-5	0 to +75	8 Ld CERDIP	F8.3A
HA9P5127-5 (Note 4)	5127 5	0 to +75	8 Ld SOIC	M8.15
HA9P5127-5Z (Note 1)	5127 5Z	0 to +75	8 Ld SOIC (Pb-free)	M8.15
HA9P5127-5ZX96 (Notes 1, 2)	5127 5Z	8 Ld SOIC (Pb-free)		M8.15

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Please refer to TB347 for details on reel specifications.
3. For Moisture Sensitivity Level (MSL), please see device information page for HA-5127, HA-5127A. For more information on MSL please see techbrief TB363.
4. Not recommended for new designs.

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 7) 0.7V
Output Current . . . . . Full Short Circuit Protection

Operating Conditions

Temperature Range
HA5127/27A-5 . . . . . 0°C to +75°C

Thermal Information

Thermal Resistance (Typical, Note 6)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	115	28
SOIC Package	157	N/A

Maximum Junction Temperature (Ceramic Package, Note 5) . . +175°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Maximum power dissipation, including output load must be designed to maintain the maximum junction temperature below +175°C for Hermetic packages, and below +150°C for the plastic packages.
6. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.

Electrical Specifications

V_{SUPPLY} = ±15V, C_L < 50pF, R_S < 100Ω. **Boldface limits apply over the operating temperature range, 0°C to +75°C.**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5127A			HA-5127			UNITS
			MIN (Note 13)	TYP	MAX (Note 13)	MIN (Note 13)	TYP	MAX (Note 13)	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	10	25	-	30	-	µV
		Full	-	30	**60**	-	70	**300**	µV
Average Offset Voltage Drift		Full	-	0.2	**0.6**	-	0.4	**1.8**	µV/°C
Bias Current		25	-	±10	±40	-	±15	±80	nA
		Full	-	±20	±**60**	-	±35	±**150**	nA
Offset Current		25	-	7	35	-	12	75	nA
		Full	-	15	**50**	-	30	**135**	nA
Common Mode Range		Full	±**10.3**	±11.5	-	±10.3	±11.5	-	V
Differential Input Resistance (Note 8)		25	1.5	6	-	0.8	4	-	MΩ
Input Noise Voltage (Note 9)	0.1Hz to 10Hz	25	-	0.08	0.18	-	0.09	0.25	μV_{P-P}
Input Noise Voltage Density	f = 10Hz	25	-	3.5	8.0	-	3.8	8.0	nV/√Hz
	f = 100Hz		-	3.1	4.5	-	3.3	4.5	nV/√Hz
	f = 1000Hz		-	3.0	3.8	-	3.2	3.8	nV/√Hz
Input Noise Current Density	f = 10Hz	25	-	1.7	4.0	-	1.7	-	pA/√Hz
	f = 100Hz		-	1.0	2.3	-	1.0	-	pA/√Hz
	f = 1000Hz		-	0.4	0.6	-	0.4	0.6	pA/√Hz
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2kΩ	25	1000	1800	-	700	1500	-	V/mV
		Full	**600**	1200	-	300	800	-	V/mV
Common Mode Rejection Ratio	V_{CM} = ±10V	Full	**114**	126	-	100	120	-	dB
Minimum Stable Gain		25	1	-	-	1	-	-	V/V
Unity-Gain-Bandwidth		25	5	8.5	-	5	8.5	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 600Ω	25	±10.0	±11.5	-	±10.0	±11.5	-	V
	R_L = 2kΩ	Full	±**11.7**	±13.8	-	±11.5	±13.5	-	V
Full Power Bandwidth (Note 10)		25	111	160	-	111	160	-	kHz
Output Resistance	Open Loop	25	-	70	-	-	70	-	Ω
Output Current		25	16.5	25	-	16.5	25	-	mA

Electrical Specifications $V_{SUPPLY} = \pm15V$, $C_L < 50pF$, $R_S < 100\Omega$. **Boldface limits apply over the operating temperature range, 0°C to +75°C. (Continued)**

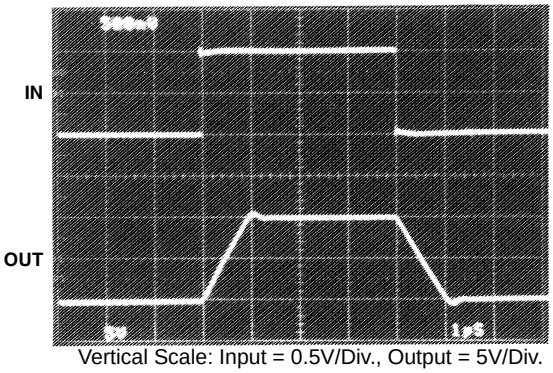
PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5127A			HA-5127			UNITS
			MIN (Note 13)	TYP	MAX (Note 13)	MIN (Note 13)	TYP	MAX (Note 13)	
TRANSIENT RESPONSE (Note 11)									
Rise Time		25	-	-	150	-	-	150	ns
Slew Rate	$V_{OUT} = 10V$	25	7	10	-	7	10	-	V/µs
Settling Time (Note 12)		25	-	1.5	-	-	1.5	-	µs
Overshoot		25	-	20	40	-	20	40	%
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	3.5	-	-	3.5	-	mA
		Full	-	-	**4.0**	-	-	**4.0**	mA
Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$	Full	-	2	**4**	-	16	**51**	µV/V

NOTES:

8. This parameter value is based upon design calculations.
9. Refer to Typical Performance Curves.
10. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
11. Refer to “Test Circuits and Waveforms” on page 3.
12. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -1$.
13. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

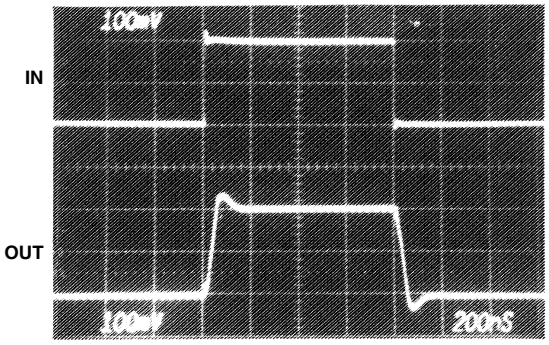
Test Circuits and Waveforms

FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUITS



Vertical Scale: Input = 0.5V/Div., Output = 5V/Div.
Horizontal Scale: 1µs/Div.

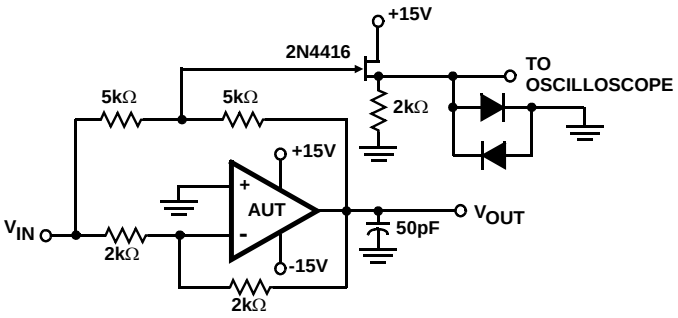
LARGE SIGNAL RESPONSE



Vertical Scale: 100mV/Div.
Horizontal Scale: 200ns/Div.

SMALL SIGNAL RESPONSE

Test Circuits and Waveforms (Continued)

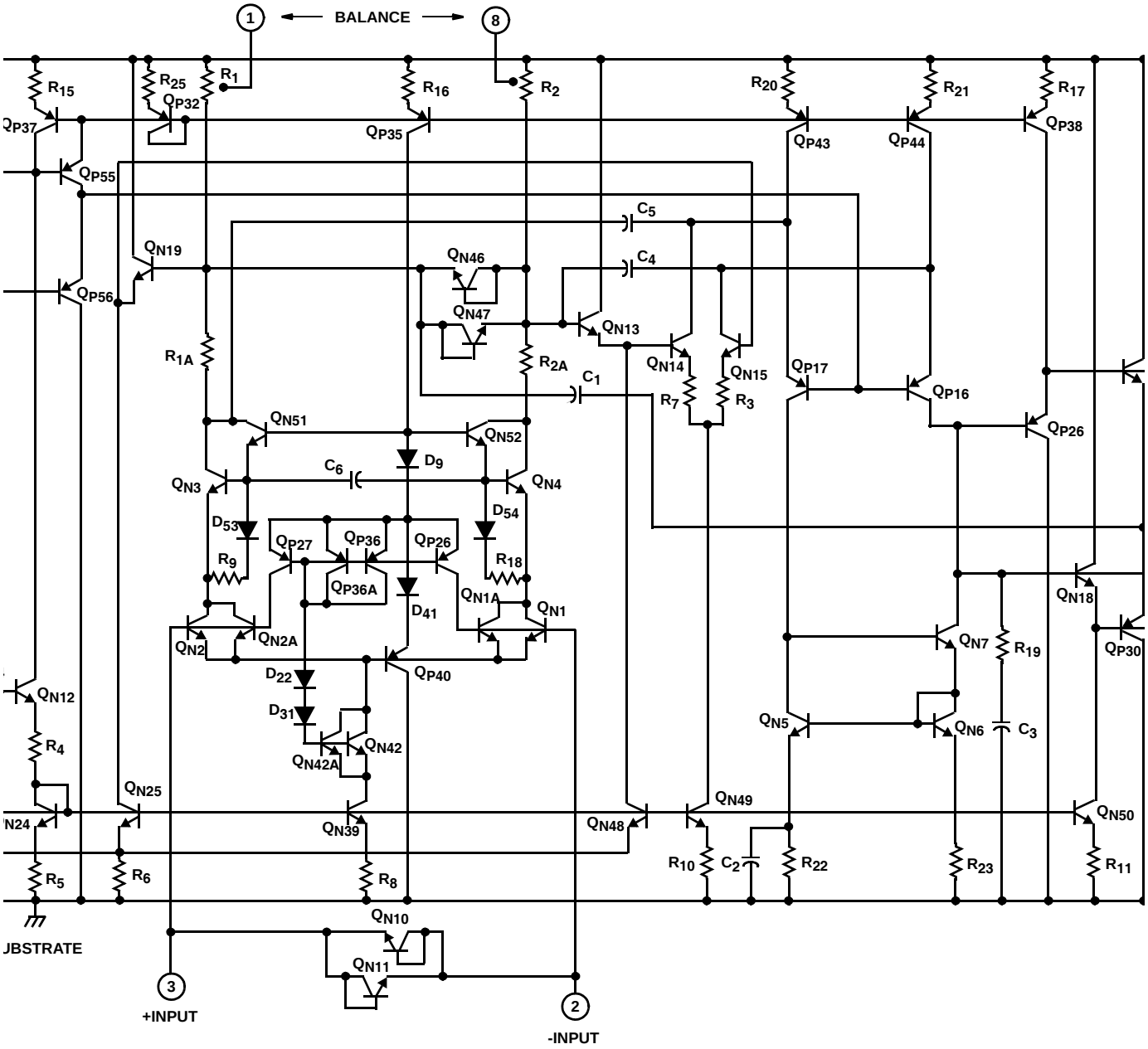


NOTES:

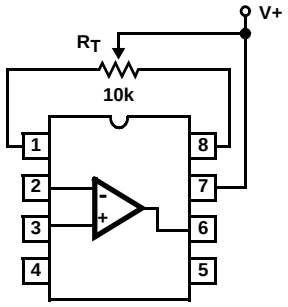
14. A_V = -1.
15. Feedback and summing resistors should be 0.1% matched.
16. Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Schematic Diagram



Application Information



NOTE: Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±4mV with $R_T = 10k\Omega$.

FIGURE 3. SUGGESTED OFFSET VOLTAGE ADJUSTMENT

Low resistances are preferred for low noise applications as a 1kΩ resistor has 4nV/$\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

FIGURE 4. SUGGESTED STABILITY CIRCUITS

Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

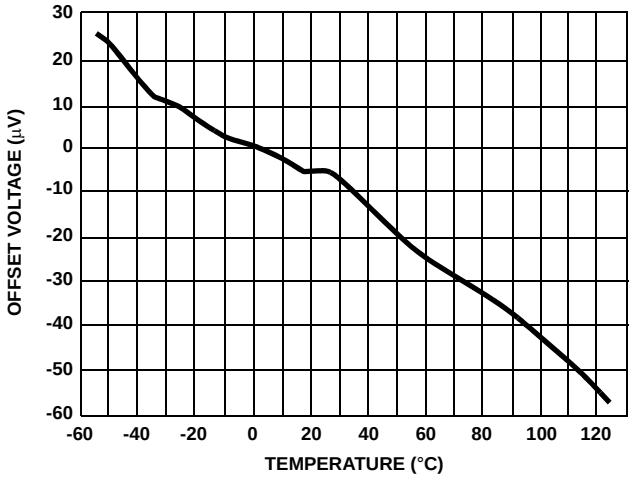


FIGURE 5. TYPICAL OFFSET VOLTAGE DRIFT vs TEMPERATURE

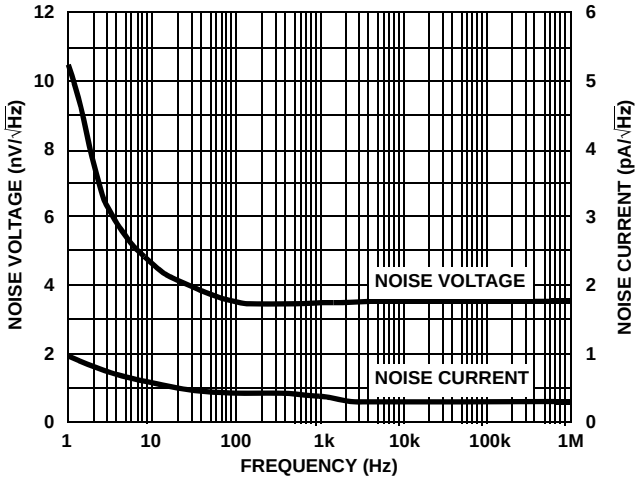


FIGURE 6. NOISE CHARACTERISTICS

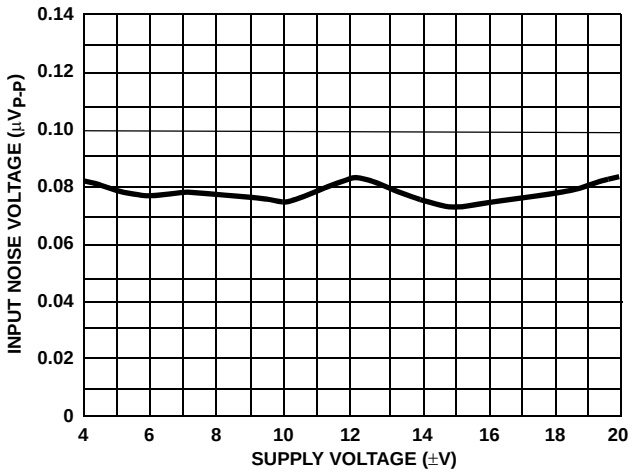


FIGURE 7. NOISE vs SUPPLY VOLTAGE

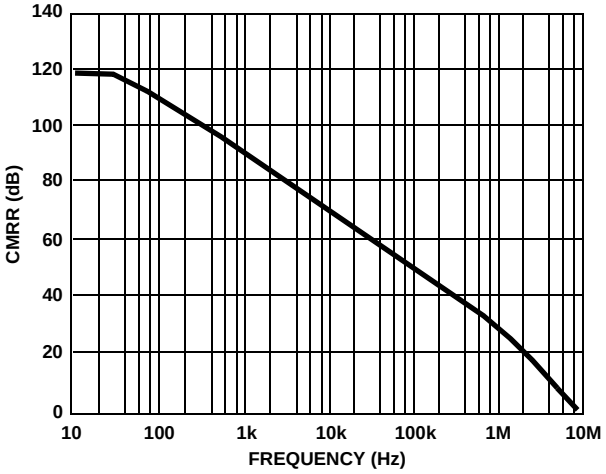


FIGURE 8. CMRR vs FREQUENCY

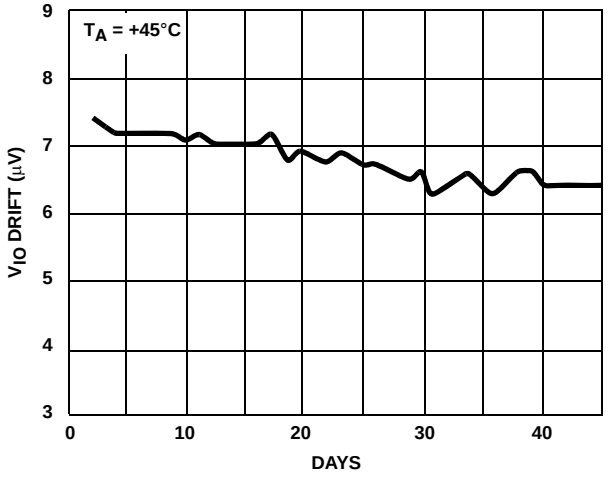


FIGURE 9. OFFSET VOLTAGE DRIFT vs TIME

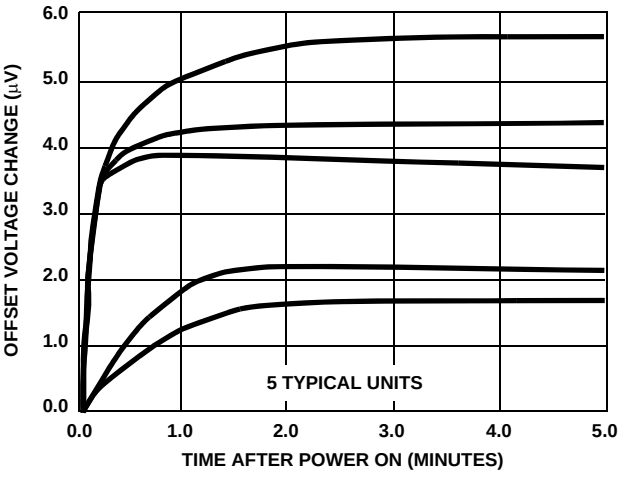


FIGURE 10. OFFSET VOLTAGE WARM UP DRIFT

Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V **(Continued)**

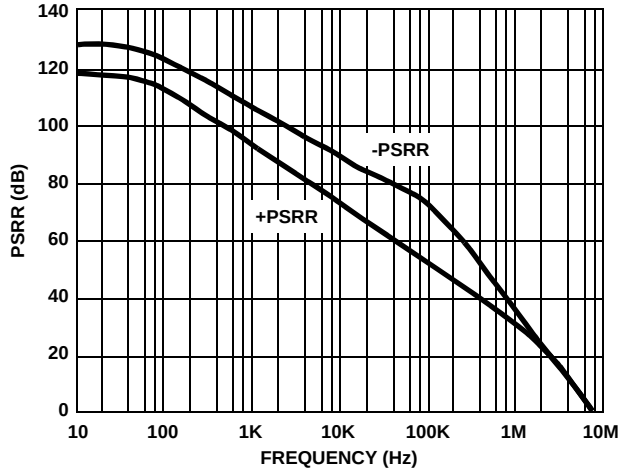


FIGURE 11. PSRR vs FREQUENCY

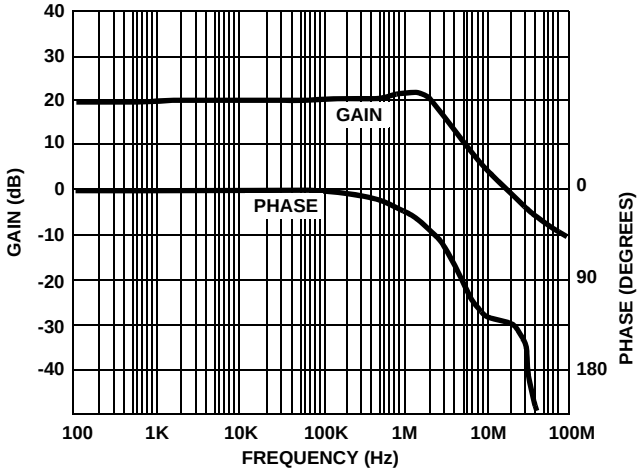


FIGURE 12. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

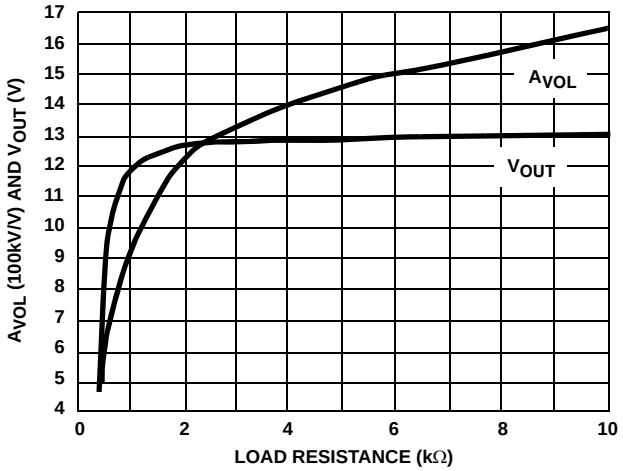


FIGURE 13. A_{VOL} AND V_{OUT} vs LOAD RESISTANCE

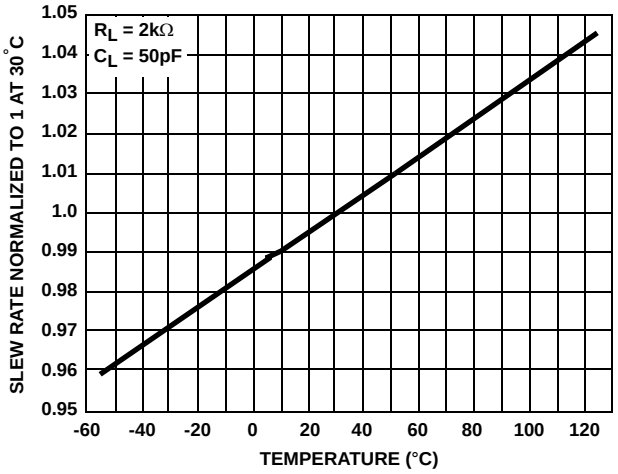


FIGURE 14. NORMALIZED SLEW RATE vs TEMPERATURE

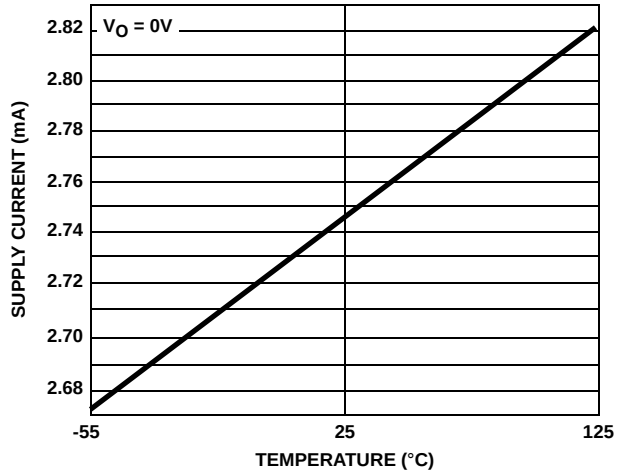


FIGURE 15. SUPPLY CURRENT vs TEMPERATURE

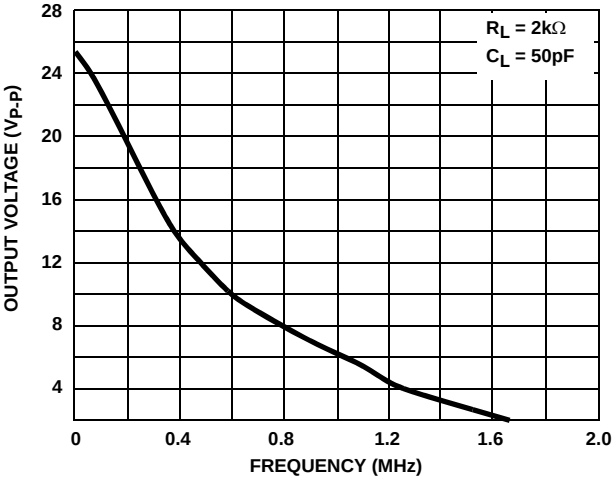


FIGURE 16. MAX UNDISTORTED SINEWAVE OUTPUT vs FREQUENCY

Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V **(Continued)**

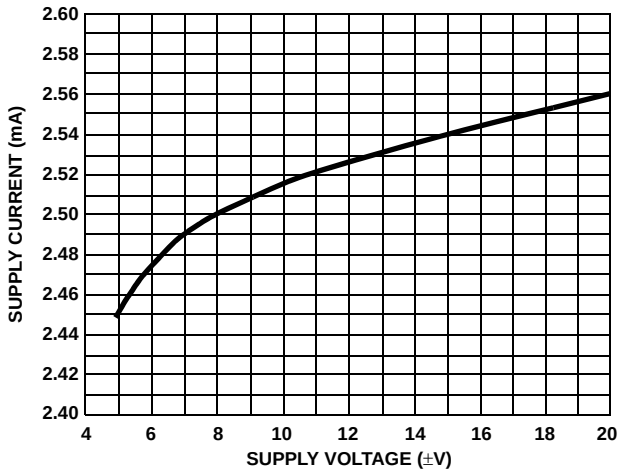


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

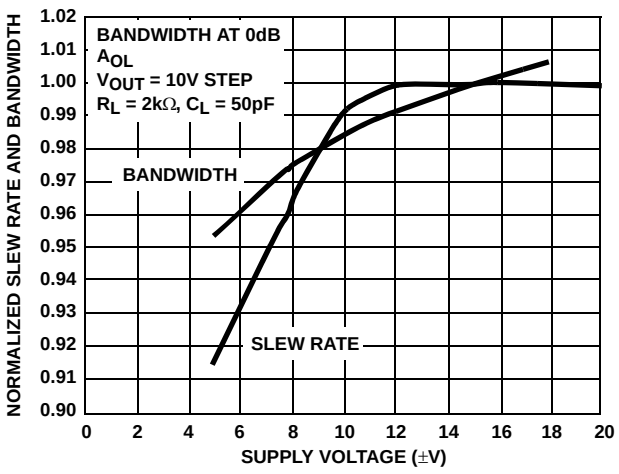


FIGURE 18. BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE

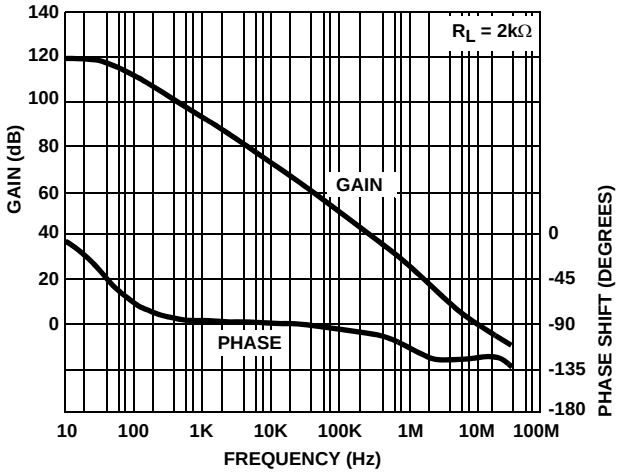


FIGURE 19. OPEN LOOP GAIN AND PHASE

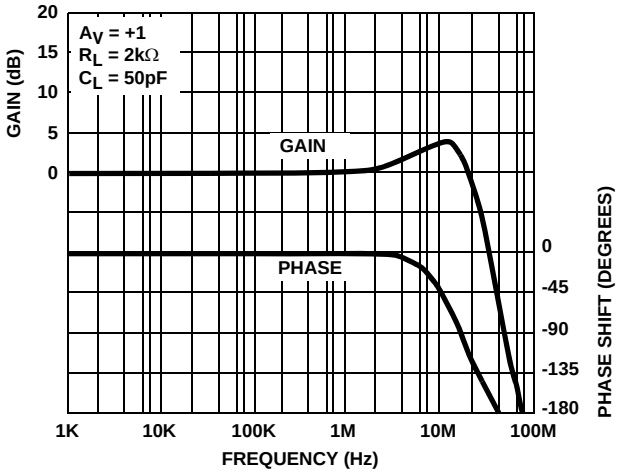
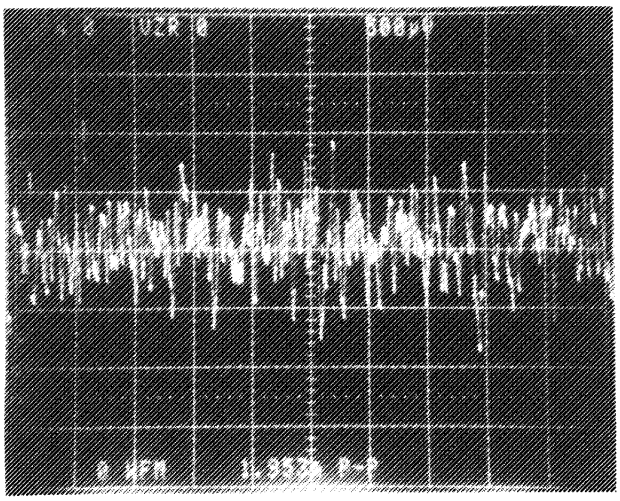


FIGURE 20. CLOSED LOOP GAIN AND PHASE

Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V **(Continued)**



Horizontal Scale = 1s/Div.
Vertical Scale = 0.002µV/Div.
A_{CL} = 25,000V/V, E_N = 0.08μV_{P-P} RTI

FIGURE 21. PEAK-TO-PEAK NOISE VOLTAGE (0.1Hz TO 10Hz)

Die Characteristics

DIE DIMENSIONS:

104 mils x 65 mils x 19 mils
2650µm x 1650µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

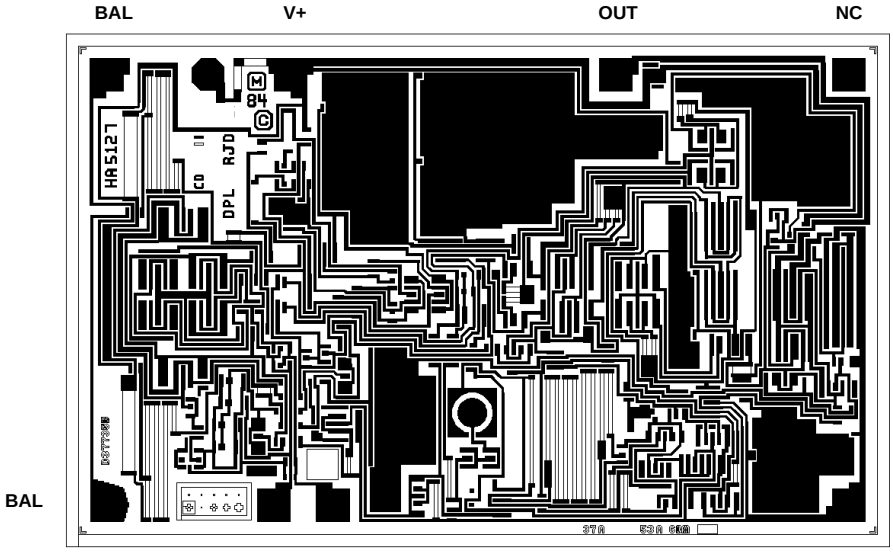
63

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5127

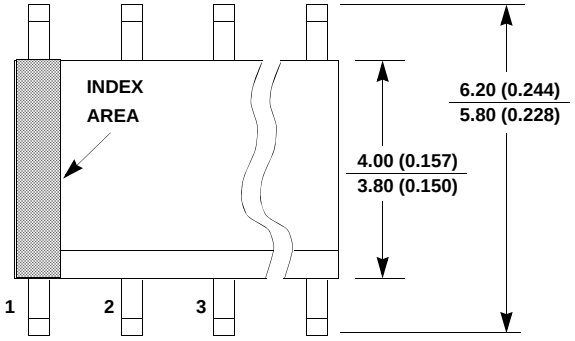


Package Outline Drawing

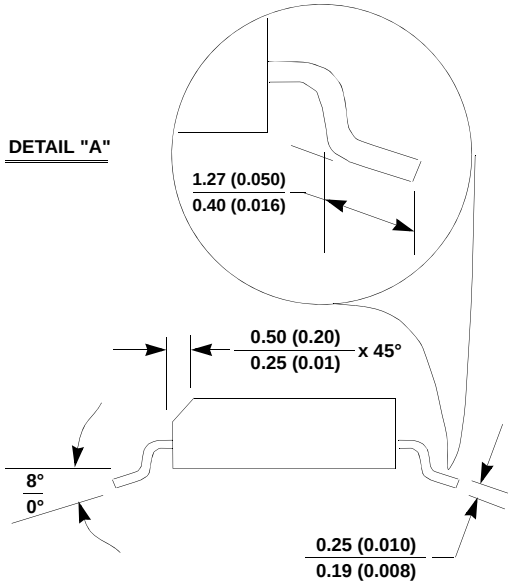
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

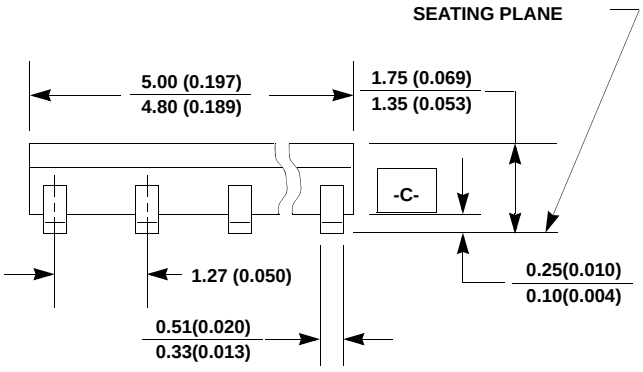
Rev 3, 3/11



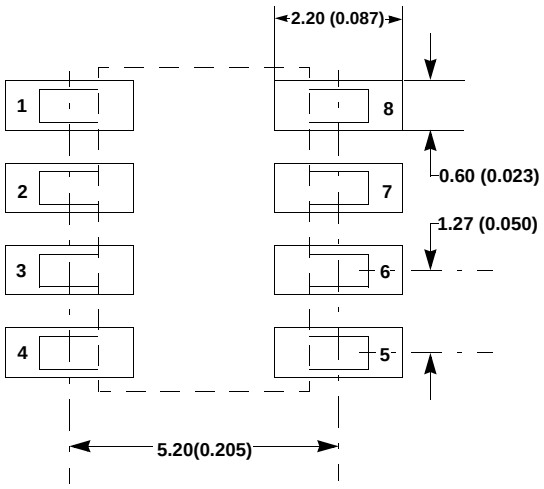
TOP VIEW



SIDE VIEW “B”



SIDE VIEW “A”

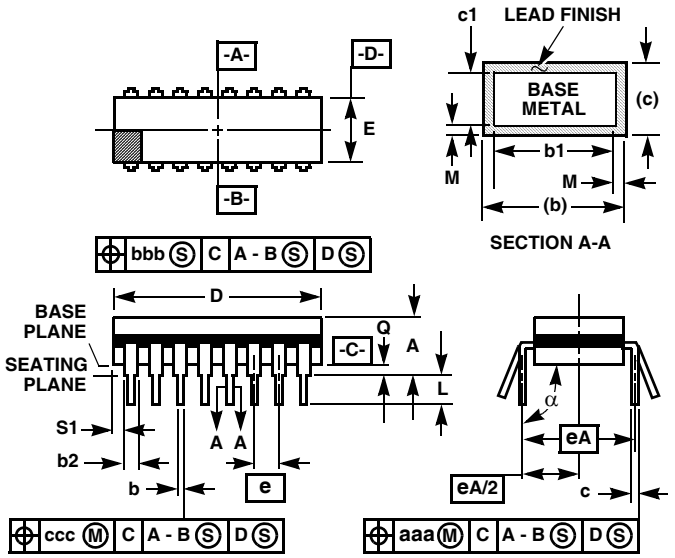


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

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