| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Drawing updated to reflect current requirements. - ro | 01-07-10 | R. MONNIN |

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| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | A | | | | | | | | | | | | | | | | | | | |
| SHEET | 15 | | | | | | | | | | | | | | | | | | | |

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| REV STATUS | REV | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |

PMIC N/A

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95-05-08

REVISION LEVEL
A

**DEFENSE SUPPLY CENTER COLUMBUS**
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**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL-LINEAR, ANALOG-TO-DIGITAL CONVERTER, 12-BIT, MONOLITHIC

SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-90632** |

SHEET 1 OF 15

DSCC FORM 2233
APR 97

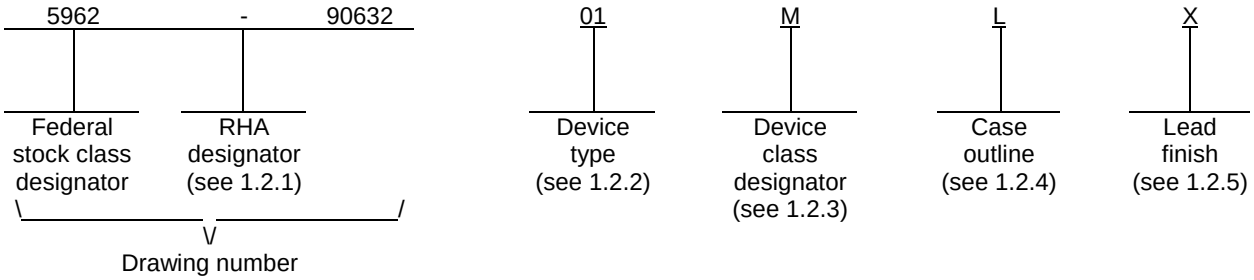
5962-E515-01

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | AD7870T | 12-bit analog-to-digital converter |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| L | GDIP3-T24 or CDIP4-T24 | 24 | Dual-in-line |
| 3 | CQCC1-N28 | 28 | Square leadless chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Positive supply voltage ($V_{DD}$) to AGND .....-0.3 V dc to +7.0 V dc
Negative supply voltage ($V_{SS}$) to AGND .....+0.3 V dc to -7.0 V dc
AGND to DGND .....-0.3 V dc to $V_{DD}$ +0.3 V dc
Analog input range ($V_{IN}$) to AGND .....-15 V dc to +15 V dc
Reference output voltage (REF OUT) to AGND .....0 V dc to $V_{DD}$
Digital input voltage to DGND .....-0.3 V dc to $V_{DD}$ +0.3 V dc
Digital output voltage to DGND .....-0.3 V dc to $V_{DD}$ +0.3 V dc
Power dissipation ($P_D$), $T_A$ = +75°C .....450 mW 2/
Lead temperature (soldering, 10 seconds) .....+300°C
Storage temperature range .....-65°C to +150°C
Thermal resistance, junction–to-case ($\theta_{JC}$) .....See MIL-STD-1835
Thermal resistance, junction–to-ambient ($\theta_{JA}$) .....120°C/W

1.4 Recommended operating conditions.

Positive supply voltage range ($V_{DD}$) .....+4.75 V dc to +5.25 V dc
Negative supply voltage range ($V_{SS}$) .....-4.75 V dc to -5.25 V dc
Analog input range .....-3.0 V dc to +3.0 V dc
Ambient operating temperature range ($T_A$) .....-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Above $T_A$ = +75°C, derate 10 mW/°C.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Resolution for which no missing codes are guaranteed | RES | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V | 1,2,3 | 01 | 12 | | BITS |
| Integral linearity error | ILE | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V | 1,2,3 | 01 | | ±1 | LSB |
| Differential linearity error | DLE | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V | 1,2,3 | 01 | | ±1 | LSB |
| Bipolar zero error | BZE | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V | 1,2,3 | 01 | | ±5 | LSB |
| Positive full scale error 3/ | PFSE | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V | 1,2,3 | 01 | | ±5 | LSB |
| Negative full scale error 3/ | NFSE | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V | 1,2,3 | 01 | | ±5 | LSB |
| Signal to noise ratio 4/ | SNR | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V, $V_{IN}$ = 10 kHz sine wave, $f_{SAMPLE}$ = 100 kHz | 4,5,6 | 01 | 69 | | dB |
| Total harmonic distortion | THD | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V, $V_{IN}$ = 10 kHz sine wave, $f_{SAMPLE}$ = 100 kHz | 4,5,6 | 01 | | -78 | dB |
| Peak harmonic | PH | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V, $V_{IN}$ = 10 kHz sine wave, $f_{SAMPLE}$ = 100 kHz | 4,5,6 | 01 | | -78 | dB |
| Intermodulation distortion 2nd and 3rd order terms | IMD | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V, $f_a$ = 9 kHz, $f_b$ = 9.5 kHz, $f_{SAMPLE}$ = 50 kHz | 4,5,6 | 01 | | -78 | dB |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Track / hold acquisition time 5/ | $t_{ACQ}$ | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V | 4,5,6 | 01 | | 2 | µs |
| Analog input voltage | $V_{IN}$ | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V | 1,2,3 | 01 | | ±3 | V |
| Analog input current | $I_{IN}$ | $V_{DD}$ = +5.25 V, $V_{SS}$ = -5.25 V | 1,2,3 | 01 | | ±500 | µA |
| Voltage reference output | $V_{REF}$ | $V_{DD}$ = +5 V, $V_{SS}$ = -5 V | 1 | 01 | 2.99 | 3.01 | V |
| Voltage reference output temperature coefficient | dREF/ dT | $V_{DD}$ = +5 V, $V_{SS}$ = -5 V | 2,3 | 01 | | +60 | ppm/°C |
| Reference load sensitivity | ΔREF | $I_{IN}$ = 0 to 500 µA, $V_{DD}$ = +5 V, $V_{SS}$ = -5 V, reference load not changed during conversion | 1,2,3 | 01 | | ±1 | mV |
| Digital input capacitance 5/ | $C_{IN}$ | $V_{DD}$ = +5 V, $V_{SS}$ = -5 V | 4 | 01 | | 10 | pF |
| Floating state output capacitance 5/ | $C_{OUT}$ | $V_{DD}$ = +5 V, $V_{SS}$ = -5 V | 4 | 01 | | 15 | pF |
| Digital input high voltage | $V_{INH}$ | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V | 7,8 | 01 | 2.4 | | V |
| Digital input low voltage | $V_{INL}$ | $V_{DD}$ = +4.75 V, $V_{SS}$ = -5.25 V | 7,8 | 01 | | 0.8 | V |
| Digital input current | $I_{IN}$ | $V_{DD}$ = +5.25 V, $V_{SS}$ = -5.25 V | 1,2,3 | 01 | | ±10 | µA |
| Digital output high voltage | $V_{OH}$ | $I_{SOURCE}$ = 40 µA, $V_{DD}$ = +4.75 V, $V_{SS}$ = -5 V | 1,2,3 | 01 | 4 | | V |
| Digital output low voltage | $V_{OL}$ | $I_{SINK}$ = 1.6 mA, $V_{DD}$ = +4.75 V, $V_{SS}$ = -5 V | 1,2,3 | 01 | | 0.4 | V |
| Floating state leakage current | $I_{LKG}$ | $V_{DD}$ = +5.25 V, $V_{SS}$ = -5.25 V, DB11- DB0 | 1,2,3 | 01 | | ±10 | µA |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Positive supply current | $I_{DD}$ | $V_{DD}$ = +5.25 V, $V_{SS}$ = -5.25 V | 1,2,3 | 01 | | 13 | mA |
| Negative supply current | $I_{SS}$ | $V_{DD}$ = +5.25 V, $V_{SS}$ = -5.25 V | 1,2,3 | 01 | | 6 | mA |
| Conversion time | $t_{CONV}$ | $V_{DD}$ = +5 V, $V_{SS}$ = -5 V, external clock = 2.5 MHz | 9,10,11 | 01 | | 8 | µs |
| | | $V_{DD}$ = +5 V, $V_{SS}$ = -5 V, internal clock | | | 6.5 | 9 | |
| $\overline{\text{CONVST}}$ pulse width | $t_1$ | 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 50 | | ns |
| $\overline{\text{CS}}$ to $\overline{\text{RD}}$ setup | $t_2$ | Mode 1, 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 0 | | ns |
| $\overline{\text{RD}}$ pulse width | $t_3$ | 6/, 7/, 8/ | 9,10,11 | 01 | 75 | | ns |
| $\overline{\text{CS}}$ to $\overline{\text{RD}}$ hold | $t_4$ | Mode 1, 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 0 | | ns |
| $\overline{\text{RD}}$ to $\overline{\text{INT}}$ delay | $t_5$ | 5/, 6/, 7/, 8/ | 9,10,11 | 01 | | 70 | ns |
| Data access time after $\overline{\text{RD}}$ | $t_6$ | 6/, 7/, 8/, 9/ | 9,10,11 | 01 | | 70 | ns |
| Bus relinquish time after $\overline{\text{RD}}$ | $t_7$ | 6/, 7/, 8/, 10/ | 9,10,11 | 01 | 5 | 50 | ns |
| HBEN to $\overline{\text{RD}}$ setup | $t_8$ | 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 0 | | ns |
| HBEN to $\overline{\text{RD}}$ hold | $t_9$ | 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 0 | | ns |
| $\overline{\text{SSTRB}}$ to SCLK falling edge setup | $t_{10}$ | 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 100 | | ns |
| SCLK cycle | $t_{11}$ | 5/, 6/, 7/, 8/, 11/ | 9,10,11 | 01 | 370 | | ns |
| SCLK to valid data delay | t12 | 5/, 6/, 7/, 8/, 12/ | 9,10,11 | 01 | | 150 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| SCLK rising edge to $\overline{SSTRB}$ | $t_{13}$ | 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 20 | 100 | ns |
| Bus relinquish time after SCLK | $t_{14}$ | 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 10 | 100 | ns |
| $\overline{CS}$ to $\overline{RD}$ setup | $t_{15}$ | Mode 2, 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 60 | | ns |
| $\overline{CS}$ to $\overline{BUSY}$ propagation delay | $t_{16}$ | 5/, 6/, 7/, 8/ | 9,10,11 | 01 | | 120 | ns |
| Data setup prior to $\overline{BUSY}$ | $t_{17}$ | 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 200 | | ns |
| $\overline{CS}$ to $\overline{RD}$ hold | $t_{18}$ | Mode 2, 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 0 | | ns |
| HBEN to $\overline{CS}$ setup | $t_{19}$ | 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 0 | | ns |
| HBEN to $\overline{CS}$ hold | $t_{20}$ | 5/, 6/, 7/, 8/ | 9,10,11 | 01 | 0 | | ns |
| Functional test | FT | See 4.4.1b | 7,8 | 01 | | | |

1/ $V_{DD}$ = +5 V, $V_{SS}$ = -5 V, AGND = DGND = 0 V, unless otherwise stated.

2/ $f_{CLK}$ = 2.5 MHz.

3/ Measured with respect to internal reference and includes bipolar offset error.

4/ SNR calculation includes distortion and noise components.

5/ Measured only at initial design characterization and after design or process changes which might affect this parameter. These limits are guaranteed even though they are not tested.

6/ All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

7/ Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and $\overline{SSTRB}$ and a 2 kΩ pull-up on SCLK. The capacitance on all three outputs is 35 pF.

8/ See figures 3 and 4.

9/ Test $t_6$ is measured loaded and defined as the time required for an output to cross 0.8 V or 2.4 V.

10/ Test $t_7$ is measured loaded and defined as the time required for the data lines to change 0.5 V.

11/ SCLK mark/space ratio measured from a voltage level of 1.6 V is 40/60 to 60/40.

12/ SDATA will drive higher capacitive loads but this will add the $t_{12}$ since it increases the external RC time circuit (4.7 kΩ || $C_L$) and hence the time to reach 2.4 V.

| Device type | 01 | |
|---|---|---|
| Case outlines | L | 3 |
| Terminal number | Terminal symbol | |
| 1 | $\overline{RD}$ | NC |
| 2 | $\overline{BUSY}$ / $\overline{INT}$ | $\overline{RD}$ |
| 3 | CLK | $\overline{BUSY}$ / $\overline{INT}$ |
| 4 | DB11 / HBEN | CLK |
| 5 | DB10 / $\overline{SSTRB}$ | DB11 / HBEN |
| 6 | DB9 / SCLK | DB10 / $\overline{SSTRB}$ |
| 7 | DB8 / SDATA | DB9 / SCLK |
| 8 | DB7 / LOW | NC |
| 9 | DB6 / LOW | DB8 / SDATA |
| 10 | DB5 / LOW | DB7 / LOW |
| 11 | DB4 / LOW | DB6 / LOW |
| 12 | DGND | DB5 / LOW |
| 13 | DB3 / DB11 | DB4 / LOW |
| 14 | DB2 / DB10 | DGND |
| 15 | DB1 / DB9 | NC |
| 16 | DB0 / DB8 | DB3 / DB11 |
| 17 | $V_{DD}$ | DB2 / DB10 |
| 18 | AGND | DB1 / DB9 |
| 19 | REF OUT | DB0 / DB8 |
| 20 | $V_{IN}$ | $V_{DD}$ |
| 21 | $V_{SS}$ | AGND |
| 22 | 12/ $\overline{8}$ /CLK | NC |
| 23 | $\overline{CONVST}$ | REF OUT |
| 24 | $\overline{CS}$ | $V_{IN}$ |
| 25 | --- | $V_{SS}$ |
| 26 | --- | 12/ $\overline{8}$ /CLK |
| 27 | --- | $\overline{CONVST}$ |
| 28 | --- | $\overline{CS}$ |

FIGURE 1. Terminal connections.

| 12/ $\overline{8}$ / CLOCK | DB11/ HBEN | DB10/ $\overline{\text{SSTRB}}$ | DB9/ SCLK | DB8/ SDATA | DB7/ LOW | DB6/ LOW | DB5/ LOW | DB4/ LOW | DB3/ DB11 | DB2/ DB10 | DB1/ DB9 | DB0/ DB8 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HI 1/ | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| LOW 2/ or –5 V | HI | $\overline{\text{SSTRB}}$ | SCLK | SDATA | LOW | LOW | LOW | LOW | DB11 (MSB) | DB10 | DB9 | DB8 |
| LOW 2/ or –5 V | LOW | $\overline{\text{SSTRB}}$ | SCLK | SDATA | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DBO (LSB) |

1/ A single 12-bit parallel word for 16-bit data buses.

2/ A two-byte format for 8-bit data buses. HBEN controls the byte-formatted data. Whereas, $\overline{\text{SSTRB}}$ , SCLK, and SDATA control the serial data output format.

FIGURE 2. Truth table.

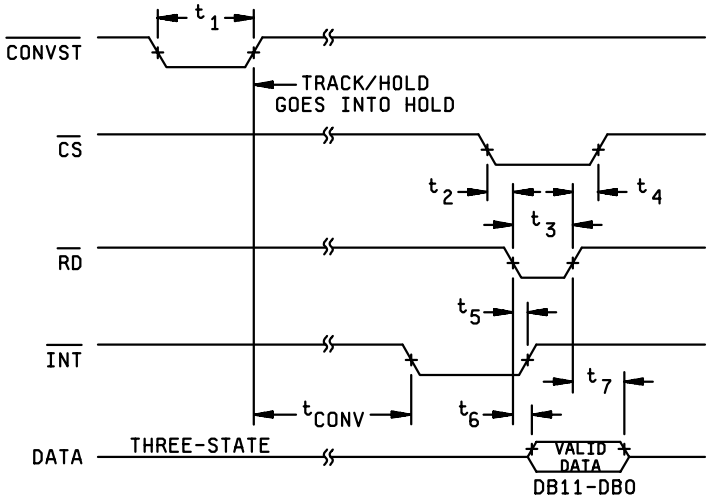
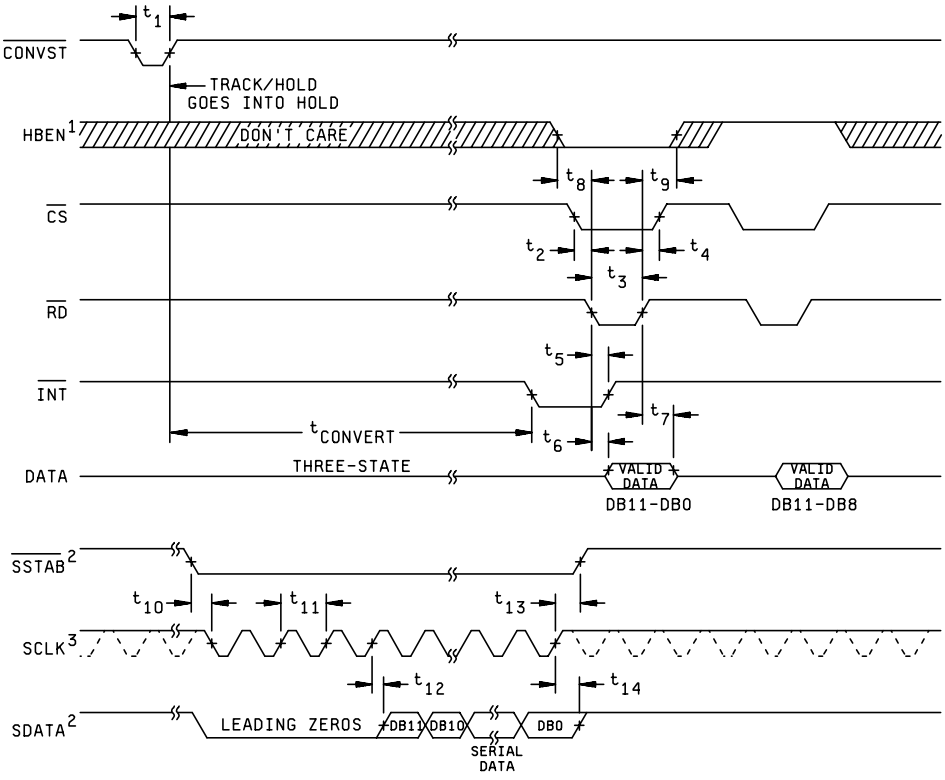



FIGURE 3. Mode 1 timing diagram , (12-bit parallel read).




NOTES:

1. Times $t_2$, $t_3$, $t_4$, $t_8$, and $t_9$ are the same for a high byte read as for a low byte read.
2. External 4.7 kΩ pull-up resistor.
3. External 2 kΩ pull-up resistor, continuous SCLK (dashed line) when 12/ $\overline{8}$ / CLK = -5 V, noncontinuous when 12/ $\overline{8}$ / CLK = 0 V.

FIGURE 3. Mode 1 timing diagram – continued, (byte or serial read).

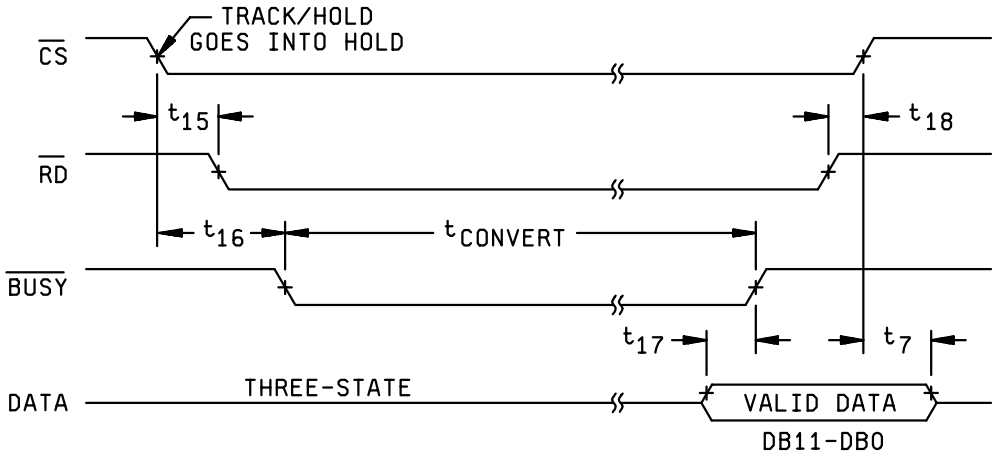
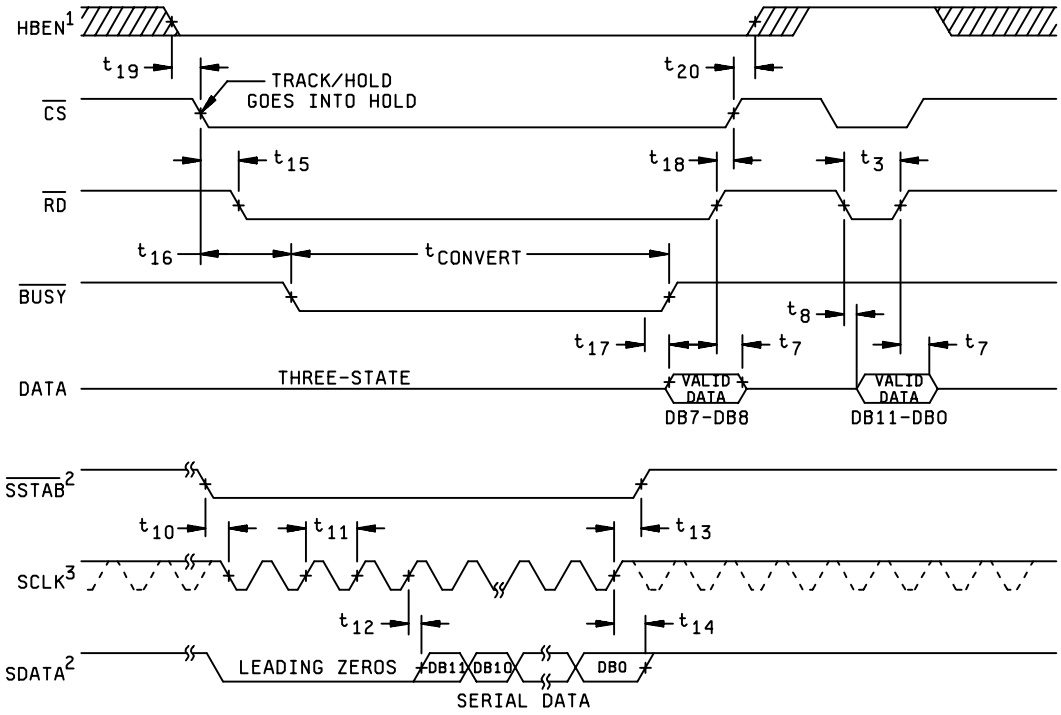



FIGURE 3. Mode 2 timing diagram , (12-bit parallel read).




NOTES:

1. Times $t_{15}$, $t_{16}$, and $t_{20}$ are the same for a high byte read as for a low byte read.
2. External 4.7 kΩ pull-up resistor.
3. External 2 kΩ pull-up resistor, continuous SCLK (dashed line) when 12/ $\overline{8}$ / CLK = -5 V, noncontinuous when 12/ $\overline{8}$ / CLK = 0 V.

FIGURE 3. Mode 2 timing diagram – continued, (byte or serial read).

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

TABLE II. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | 1 | 1 | 1 |
| Final electrical parameters (see 4.2) | 1,2,3,4,5,6, 1/ 7,8,9,10,11 | 1,2,3,4,5, 1/ 6,7,8,9,10,11 | 1,2,3,4,5, 1/ 6,7,8,9,10,11 |
| Group A test requirements (see 4.4) | 1,2,3,4,5,6, 7,8,9,10,11 | 1,2,3,4,5,6, 7,8,9,10,11 | 1,2,3,4,5,6, 7,8,9,10,11 |
| Group C end-point electrical parameters (see 4.4) | 1 | 1 | 1,2,3,4,5,6, 9,10,11 |
| Group D end-point electrical parameters (see 4.4) | 1 | 1 | 1 |
| Group E end-point electrical parameters (see 4.4) | --- | --- | --- |

1/ PDA applies to subgroup 1.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, Q and V subgroups 7 and 8 tests shall be sufficient to verify the truth table.

c. Parameters specified in table I herein with note 5/ shall be tested on initial release or design. Sample size shall be 15, 0 failures allowed.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-07-10

Approved sources of supply for SMD 5962-90632 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9063201MLA | 24355 | AD7870TQ/883B |
| 5962-9063201M3A | 24355 | AD7870TE/883B |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 24355 | Analog Devices<br>Route 1 Industrial Park<br>P.O. Box 9106<br>Norwood, MA 02062<br>Point of contact: Bay F-1<br>Raheen Ind. Estate<br>Limerick, Ireland |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.