Micropower 18V CMOS RRIO Op Amp

Preliminary Technical Data

AD8548

FEATURES

Micropower at high voltage (18 V): 18 µA typical
Single-supply operation: 2.7 V to 18 V
Dual-supply operation: ±1.35 V to ±9 V
Low input bias current: 20 pA
Gain bandwidth: 200 kHz
Unity-gain stable
Excellent electromagnetic interference immunity

APPLICATIONS

Portable operating systems
Current monitors
4 mA to 20 mA loop drivers
Buffer/level shifting
Multipole filters
Remote/wireless sensors
Low power transimpedance amplifiers

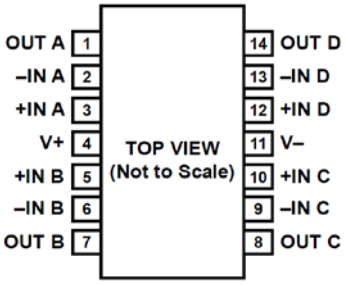
GENERAL DESCRIPTION

The AD8548 is a Quad, micropower, rail-to-rail input/output amplifier optimized for low power and wide operating supply voltage range applications.

The AD8548 operates from 2.7 V up to 18 V with a typical quiescent supply current of 18 µA. The AD8548 also has high immunity to electromagnetic interference.

The combination of low supply current, low offset voltage, very low input bias current, wide supply range, and rail-to-rail input and output make the AD8548 ideal for current monitoring and current loops in process and motor control applications. The combination of precision specifications makes this device ideal for dc gain and buffering of sensor front ends or high impedance input sources in wireless or remote sensors or transmitters.

PIN CONFIGURATION



14-Lead SOIC_N (R Suffix)

Table 1. Micropower Op Amps

Supply Voltage	5 V	12 V to 16 V	36 V
Single	AD8500 ADA4505-1 AD8505 AD8541 AD8603	AD8663	
Dual	AD8502 ADA4505-2 AD8506 AD8542 AD8607	AD8667 OP281	OP295 ADA4062-2
Quad	AD8504 ADA4505-4 AD8508 AD8544 AD8609	AD8669 OP481	OP495 ADA4062-4

Rev. PrA

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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V_{SY} = 2.7 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 2.7 V			4	mV
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +85°C			tbd	mV
		V_{CM} = 0 V to 2.7 V; −40°C ≤ T_A ≤ +85°C			tbd	mV
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +125°C			tbd	mV
		V_{CM} = 0 V to 2.7 V; −40°C ≤ T_A ≤ +125°C			tbd	mV
Input Bias Current	I_B			1	10	pA
		−40°C ≤ T_A ≤ +125°C			2.6	nA
Input Offset Current	I_{OS}				20	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	79	95		dB
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +85°C	70			dB
		V_{CM} = 0 V to 2.7 V; −40°C ≤ T_A ≤ +85°C	64			dB
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +125°C	63			dB
		V_{CM} = 0 V to 2.7 V; −40°C ≤ T_A ≤ +125°C	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 2.2 V	94	105		dB
		−40°C ≤ T_A ≤ +85°C	75			dB
		−40°C ≤ T_A ≤ +125°C	65			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
Input Resistance	R_{IN}			10		GΩ
Input Capacitance, Differential Mode	C_{INDM}			3.5		pF
Input Capacitance, Common Mode	C_{INCM}			3.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C	2.69			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C			10	mV
Short-Circuit Current	I_{SC}			±4		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		20		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 18 V	105	125		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		18	22	µA
		−40°C ≤ T_A ≤ +125°C			33	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		38		V/ms
Settling Time to 0.1%	t_s	V_{IN} = 1 V step, R_L = 100 kΩ, C_L = 10 pF		14		µs
Gain Bandwidth Product	GBP	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		170		kHz
Phase Margin	Φ_M	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		69		Degrees
Channel Separation	CS	f = 10 kHz, R_L = 1 MΩ		105		dB
EMI Rejection Ratio of IN+	EMIRR	V_{IN} = 100 mV_{PEAK}; f = 400 MHz, 900 MHz, 1800 MHz, 2400 MHz		90		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		6		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		60		nV/√Hz
		f = 10 kHz		56		nV/√Hz

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ELECTRICAL CHARACTERISTICS—10 V OPERATION

V_{SY} = 10 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 10 V			4	mV
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +85°C			tbd	mV
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +125°C			tbd	mV
Input Bias Current	I_B			2	15	pA
		−40°C ≤ T_A ≤ +125°C			2.6	nA
Input Offset Current	I_{OS}				30	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		10	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 10 V	90	105		dB
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +85°C	72			dB
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +125°C	64			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 9.5 V	105	120		dB
		−40°C ≤ T_A ≤ +85°C	95			dB
		−40°C ≤ T_A ≤ +125°C	67			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
Input Resistance	R_{IN}			10		GΩ
Input Capacitance, Differential Mode	C_{INDM}			3.5		pF
Input Capacitance, Common Mode	C_{INCM}			3.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C	9.98			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C			20	mV
Short-Circuit Current	I_{SC}			±11		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 18 V	105	125		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		18	22	µA
		−40°C ≤ T_A ≤ +125°C			33	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		60		V/ms
Settling Time to 0.1%	t_s	V_{IN} = 1 V step, R_L = 100 kΩ, C_L = 10 pF		13		µs
Gain Bandwidth Product	GBP	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		200		kHz
Phase Margin	Φ_M	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		60		Degrees
Channel Separation	CS	f = 10 kHz, R_L = 1 MΩ		105		dB
EMI Rejection Ratio of IN+	EMIRR	V_{IN} = 100 mV_{PEAK}; f = 400 MHz, 900 MHz, 1800 MHz, 2400 MHz		90		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		50		nV/√Hz
		f = 10 kHz		45		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ELECTRICAL CHARACTERISTICS—18 V OPERATION

V_{SY} = 18 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 18 V			4	V
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +85°C			tbd	mV
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +85°C			tbd	mV
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +125°C			tbd	mV
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +125°C			tbd	mV
Input Bias Current	I_B			5	20	pA
		−40°C ≤ T_A ≤ +125°C			2.9	nA
Input Offset Current	I_{OS}				40	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		18	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 18 V	95	110		dB
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +85°C	83			dB
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +85°C	74			dB
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +125°C	80			dB
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +125°C	67			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 17.5 V	110	120		dB
		−40°C ≤ T_A ≤ +85°C	105			dB
		−40°C ≤ T_A ≤ +125°C	73			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
Input Resistance	R_{IN}			10		GΩ
Input Capacitance, Differential Mode	C_{INDM}			3.5		pF
Input Capacitance, Common Mode	C_{INCM}			10.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C	17.97			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C			30	mV
Short-Circuit Current	I_{SC}			±12		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 18 V	105	125		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		18	22	µA
		−40°C ≤ T_A ≤ +125°C			33	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		70		V/ms
Settling Time to 0.1%	t_s	V_{IN} = 1 V step, R_L = 100 kΩ, C_L = 10 pF		12		µs
Gain Bandwidth Product	GBP	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		200		kHz
Phase Margin	Φ_M	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		60		Degrees
Channel Separation	CS	f = 10 kHz, R_L = 1 MΩ		105		dB
EMI Rejection Ratio of IN+	EMIRR	V_{IN} = 100 mV_{PEAK}; f = 400 MHz, 900 MHz, 1800 MHz, 2400 MHz		90		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		50		nV/√Hz
		f = 10 kHz		45		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	20.5 V
Input Voltage	(V–) – 300 mV to (V+) + 300 mV
Input Current[1]	±10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Temperature Range	
Storage	−65°C to +150°C
Operating	−40°C to +125°C
Junction	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages using a standard 4-layer board.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead SOIC (R-14)	142	45	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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