Low Power, Precision Analog Microcontroller, Dual Sigma-Delta ADCs, Flash/EE, ARM7TDMI

ADuC7060

FEATURES

Analog input/output
- Dual (24-bit) ADCs
- Single-ended and differential inputs
- Programmable ADC output rate (4 Hz to 8 kHz)
- Programmable digital filters
- Built-in system calibration
- Low power operation mode
  - Primary (24-bit) ADC channel
    - Up to 5 input channels
    - PGA (1 to 512) input stage
    - Selectable input range: ±2.34 mV to ±1.2 V
    - 30 nV rms noise
  - Auxiliary (24-bit) ADC: up to 8 buffered input channels
- On-chip precision reference (±10 ppm/°C)
- Programmable sensor excitation current sources
  - 200 µA to 2 mA current source range
- Single 14-bit voltage output DAC

Microcontroller
- ARM7TDMI core, 16-/32-bit RISC architecture
- JTAG port supports code download and debug
- Multiple clocking options

Memory
- 32 kB (16 kB × 16) Flash/EE memory, including 2 kB kernel
- 4 kB (1 kB × 32) SRAM

Tools
- In-circuit download, JTAG based debug
- Low cost, QuickStart™ development system

Communications interfaces

SPI interface (5 Mbps)
- 4-byte receive and transmit FIFOs

UART serial I/O and I^2C (master/slave)

On-chip peripherals
- 4× and 2× general-purpose (capture/compare) timers
- Wakeup timer
- Watchdog timer

Vectored interrupt controller for FIQ and IRQ
- 8 priority levels for each interrupt type
- Interrupt on edge or level external pin inputs

16-bit, 6-channel PWM

General-purpose inputs/outputs
- Up to 14 GPIO pins that are fully 3.3 V compliant

Power
- AVDD/DVDD specified for 2.5 V (+5%)
- All inputs/outputs fully 3.3 V compliant
- Active mode: 2.6 mA (@1 MHz, both ADCs active)
- 10 mA (@10 MHz, both ADCs active)

Packages and temperature range
- Fully specified for −40°C to +125°C operation
- 48-lead LFCSP and LQFP

Derivatives

48-lead LQFP and 48-lead LFCSP, dual ADCs (ADuC7060)

APPLICATIONS

Industrial automation and process control

Intelligent, precision sensing systems, 4 mA to 20 mA loop-based smart sensors

GENERAL DESCRIPTION

The ADuC7060 is a fully integrated, 8 kSPS, 24-bit data acquisition system incorporating high performance multichannel sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), 16-bit/32-bit ARM7TDMI® MCU, and Flash/EE memory on a single chip.

The ADCs consists of a 5-channel primary ADC and up to an 8-channel auxiliary ADC. The ADCs operate in single-ended or differential input modes. A single channel buffered voltage output DAC is available on-chip. The DAC output range is programmable to one of two voltage ranges.

The devices operate from an on-chip oscillator and a PLL generating an internal high frequency clock up to 10.24 MHz. The microcontroller core is an ARM7TDMI, 16-bit/32-bit RISC machine offering up to 10 MIPS peak performance; 4 kB of SRAM and 32 kB of nonvolatile Flash/EE memory are provided on-chip. The ARM7TDMI core views all memory and registers as a single linear array.

The ADuC7060 contains four timers. Timer1 is a wake-up timer with the ability to bring the part out of power saving mode. Timer2 can be configured as a watchdog timer. A 16-bit PWM with six output channels is also provided.

The ADuC7060 contains an advanced interrupt controller. The vectored interrupt controller (VIC) allows every interrupt to be assigned a priority level. It also supports nested interrupts to a maximum level of eight per IRQ and FIQ. When IRQ and FIQ interrupt sources are combined, a total of 16 nested interrupt levels are supported. On-chip factory firmware supports in-circuit serial download via the UART serial interface ports and nonintrusive emulation via the JTAG interface.

The parts operate from 2.375 V to 2.625 V over an industrial temperature range of −40°C to +125°C.

Rev. 0

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REVISION HISTORY

4/09—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

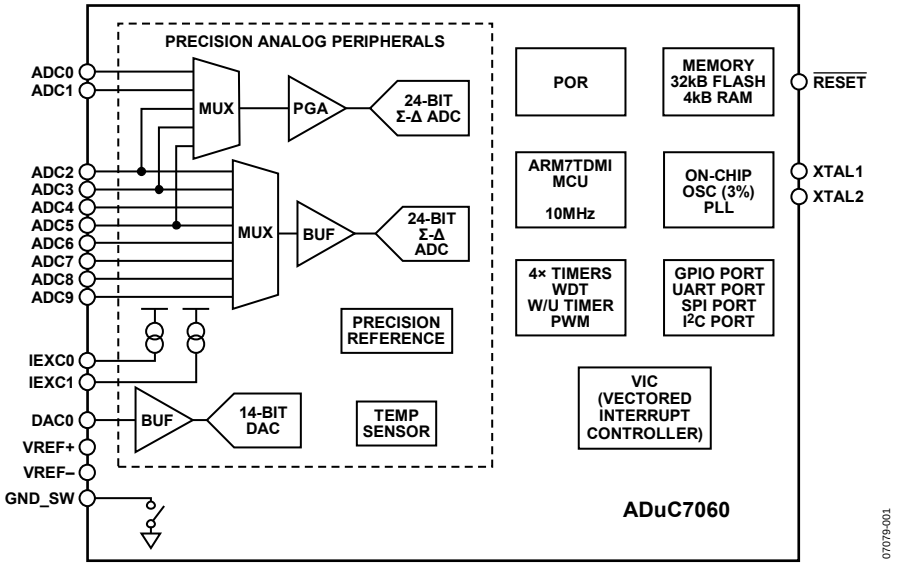


Figure 1.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = 2.5 V ± 5%, VREF+ = 1.2 V, VREF− = GND internal reference, f_{CORE} = 10.24 MHz driven from an external 32.768 kHz watch crystal or on-chip precision oscillator, all specifications T_A = −40°C to +125°C, unless otherwise noted. Output noise specifications can be found in Table 36 (ADC auxiliary channel) and Table 34 (primary ADC).

Table 1. ADuC7060 Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPECIFICATIONS	For all ADC specifications, assume normal operating mode unless specifically stated otherwise				
Conversion Rate[1]	Chop off, ADC normal operating mode	50		8000	Hz
	Chop on, ADC normal operating mode	4		2600	Hz
	Chop on, ADC low power mode	1		650	Hz
Main Channel					
No Missing Codes[1]	Chop off (f_{ADC} ≤ 1 kHz)	24			Bits
	Chop on (f_{ADC} ≤ 666 Hz)	24			Bits
Integral Nonlinearity[1, 2]	Gain = 4		±15		ppm of FSR
Offset Error[3, 4]	Chop off, offset error is in the order of the noise for the programmed gain and update rate following calibration		±8		µV
Offset Error[1, 3, 4]	Chop on		±0.5		µV
Offset Error Drift vs. Temperature[5]	Chop off (with gain ≤ 64)		650/PGA_GAIN		nV/°C
Offset Error Drift vs. Temperature[5]	Chop on (with gain ≤ 64)		10		nV/°C
Full Scale Error[1, 6, 7, 8]	Normal mode		±0.5		mV
Full Scale Error[1, 6, 7, 8]	Low power mode		±1.0		mV
Gain Drift v Temperature[9]			5		ppm/°C
PGA Gain Mismatch Error			±0.1		%
Power Supply Rejection	Chop on, ADC = 1 V, (gain = 1)		65		dB
	Chop on, ADC = 7.8 mV, (gain = 128)		113		dB
	Chop off, ADC = 1 V, (gain = 1)		65		dB
Auxiliary Channel					
No Missing Codes[1]	Chop off (f_{ADC} ≤ 1 kHz)	24			Bits
	Chop on (f_{ADC} ≤ 666 Hz)	24			Bits
Integral Nonlinearity[1]				±20	ppm of FSR
Offset Error[4]	Chop off		±30		µV
Offset Error[1, 4]	Chop on		±0.5		µV
Offset Error Drift vs. Temperature[5]	Chop off		200		nV/°C
Offset Error Drift vs. Temperature[5]	Chop on		10		nV/°C
Full-Scale Error[1, 6, 7, 8]	Normal mode		±0.5		mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Full-Scale Error[1, 6, 8]	Low power mode		±1.0		mV
Gain Drift vs. Temperature[9]			3		ppm/°C
Power Supply Rejection	Chop on, ADC = 1 V		65		dB
	Chop off, ADC = 1 V		65		dB
ADC SPECIFICATIONS: ANALOG INPUT	Internal V_{REF} = 1.2 V				
Main Channel					
Absolute Input Voltage Range	Applies to both VIN+ and VIN−	0.1		V_{DD} − 0.7	V
Input Voltage Range	Gain = 1[1]		1.2		V
	Gain = 2[10]		600		mV
	Gain = 4[10]		300		mV
	Gain = 8		150		mV
	Gain = 16		75		mV
	Gain = 32		37.5		mV
	Gain = 64		18.75		mV
	Gain = 128		9.375		mV
Input Leakage Current[1]	ADC0 and ADC1		10		nA
	ADC2, ADC3, ADC4, and ADC5		15		nA
	ADC6, ADC7, ADC8, and ADC9		15		nA
Common-Mode Rejection DC[1]					
On ADC	ADC = 7.8 mV	113			dB
	ADC = 1 V[1]		95		dB
Common-Mode Rejection 50 Hz/60 Hz[1]	50 Hz/60 Hz ± 1 Hz, 16.6 Hz and 50 Hz update rate, chop on				
	ADC = 7.8 mV, range ± 20 mV	95			dB
	ADC = 1 V, range ± 1.2 V	90			dB
Normal-Mode Rejection 50 Hz/60 Hz[1]					
On ADC	50 Hz/60 Hz ± 1 Hz, 16.6 Hz f_{ADC}, chop on	75			dB
	50 Hz/60 Hz ± 1 Hz, 16.6 Hz f_{ADC}, chop off	67			dB
Auxiliary Channel					
Absolute Input Voltage Range[1]	Buffer enabled	0.1		AVDD − 0.1	V
	Buffer disabled	AGND		AVDD	
Input Voltage Range	Range-based reference source		0 − 1.2		V
Common-Mode Rejection DC[1]					
On ADC	ADC = 1 V[1]		87		dB
Common-Mode Rejection 50 Hz/60 Hz[1]	50 Hz/60 Hz ± 1 Hz, 16.6 Hz and 50 Hz update rate, chop on				
	ADC = 1 V, range ± 1.2 V	90			dB
Normal-Mode Rejection 50 Hz/60 Hz[1]					
On ADC	50 Hz/60 Hz ± 1 Hz, 16.6 Hz f_{ADC}, chop on	75			dB
	50 Hz/60 Hz ± 1 Hz, 16.6 Hz f_{ADC}, chop off	67			dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VOLTAGE REFERENCE					
ADC Precision Reference					
Internal V_{REF}			1.2		V
Initial Accuracy	Measured at T_A = 25°C	−0.06		+0.06	%
Reference Temperature Coefficient[1, 11]		−20	±10	+20	ppm/°C
Power Supply Rejection[1]			70		dB
External Reference Input Range[12]		0.1		AVDD	V
V_{REF} Divide-by-2 Initial Error[1]			0.1		%
DAC CHANNEL SPECIFICATIONS	R_L = 5 kΩ, C_L = 100 pF				
Voltage Range			0 – V_{REF}		V
			0 – AVDD		V
12-BIT MODE					
DC Specifications[13]					
Resolution		12			Bits
Relative Accuracy			±2		LSB
Differential Nonlinearity	Guaranteed monotonic		±0.2	±1	LSB
Offset Error	1.2 V internal reference		±2	±15	mV
Gain Error	V_{REF} range (reference = 1.2 V)			±1	%
	AVDD range			±1	%
Gain Error Mismatch				0.1	% of full scale on DAC
16-BIT MODE[1]					
DC Specifications[14]					
Resolution		14			Bits
Relative Accuracy	For 14-bit resolution		±3		LSB
Differential Nonlinearity	Guaranteed monotonic (14 bits)		±0.5	±1	LSB
Offset Error	1.2 V internal reference		±2	±15	mV
Gain Error	V_{REF} range (reference = 1.2 V)		±1		%
	AVDD range		±1		%
Gain Error Mismatch			0.1		% of full scale on DAC
DAC AC CHARACTERISTICS					
Voltage Output Settling Time			10		µs
Digital-to-Analog Glitch Energy	1 LSB change at major carry (where maximum number of bits simultaneously change in the DAC0DAT register)		±20		nV-sec
TEMPERATURE SENSOR[1, 15]	After user calibration				
Accuracy	MCU in power down or standby mode		±4		°C
Thermal Impedance	48-lead LFCSP		27		°C/W
	48-lead LQFP		55		°C/W
POWER-ON RESET (POR)					
POR Trip Level	Refers to voltage at DVDD pin				
	Power-on level		2.0		V
	Power-down level		2.25		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ Timeout from POR	Maximum supply ramp between 1.8 V to 2.25 V; after POR trip, DVDD must reach 2.25 V within this time limit			128	ms
EXCITATION CURRENT SOURCES					
Output Current	Available from each current source	200	1000		µA
Initial Tolerance at 25°C			±5		%
Drift[1]			0.06		%/°C
Initial Current Matching at 25°C	Matching between both current sources		±0.5		%
Drift Matching[1]			20		ppm/°C
Line Regulation (AVDD)[1]	AVDD = 2.5 V ± 5%		0.2		%/V
Output Compliance[1]		AVDD − 0.7 V		AGND − 30 mV	V
WATCHDOG TIMER (WDT)					
Timeout Period[1]	32.768 kHz clock, 256 prescale	0.008		512	sec
Timeout Step Size			7.8		ms
FLASH/EE MEMORY[1]					
Endurance[16]		10,000			Cycles
Data Retention[17]		20			Years
DIGITAL INPUTS	All digital inputs except NTRST				
Input Leakage Current	Input (high) = DVDD		±1	±10	µA
Input Pull-Up Current	Input (low) = 0 V	10	20	80	µA
Input Capacitance			10		pF
Input Leakage Current	NTRST only: input (low) = 0 V		±1	±10	µA
Input Pull-Down Current	NTRST only: input (high) = DVDD	30	55	100	µA
LOGIC INPUTS[1]	All logic inputs				
Input Low Voltage (VINL)				0.4	V
Input High Voltage (VINH)		2.0			V
CRYSTAL OSCILLATOR[1]					
Logic Inputs, XTAL1 Only					
Input Low Voltage (VINL)				0.8	V
Input High Voltage (VINH)		1.7			V
XTAL1 Capacitance			12		pF
XTAL2 Capacitance			12		pF
ON-CHIP OSCILLATORS					
Oscillator			32,768		kHz
Accuracy		−3		+3	%
MCU CLOCK RATE	Eight programmable core clock selections within this range: binary divisions 1, 2, 4, 8 . . . 64, 128	0.160	2.56	10.24	MHz
MCU START-UP TIME					
At Power-On	Includes kernel power-on execution time		134		ms
After Reset Event	Includes kernel power-on execution time		5		ms
From MCU Power-Down					
PLL On					
Wakeup from Interrupt	CD = 0		4.8		µs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PLL Off					
Wakeup from Interrupt	CD = 0		66		μs
Internal PLL Lock Time			1		ms
POWER REQUIREMENTS					
Power Supply Voltages					
DVDD (±5%)		2.375	2.5	2.625	V
AVDD (±5%)		2.375	2.5	2.625	V
Power Consumption					
I_{DD} (MCU Normal Mode)[18]	MCU clock rate = 10.24 MHz, ADC on		6	10	mA
	MCU clock rate = 1.28 MHz, ADC on, DAC off			2.8	mA
I_{DD} (MCU Powered Down)[1]	Full temperature range		55	350	μA
	Reduced temperature range −40°C to +85°C		55	120	μA
I_{DD} (Primary ADC)	PGA enabled, normal mode/low power mode		0.8/0.3		mA
I_{DD} (Auxiliary ADC)	Normal mode/low power mode		0.3/0.1		mA

[1] These numbers are not production tested but are guaranteed by design and/or characterization data at production release.
[2] Valid for primary ADC gain setting of PGA = 4 to 64.
[3] Tested at gain range = 4 after initial offset calibration.
[4] Measured with an internal short. A system zero-scale calibration removes this error.
[5] Measured with an internal short.
[6] These numbers do not include internal reference temperature drift.
[7] Factory calibrated at gain = 1.
[8] System calibration at a specific gain range removes the error at this gain range.
[9] Measured using an external reference.
[10] Limited by the minimum absolute input voltage range.
[11] Measured using the box method.
[12] References up to AVDD are accommodated by setting ADC0CON Bit 12.
[13] Reference DAC linearity is calculated using a reduced code range of 171 to 4095.
[14] Reference DAC linearity is calculated using a reduced code range of 2731 to 65,535.
[15] Die temperature.
[16] Endurance is qualified to 10,000 cycles as per JEDEC Std. 22 Method A117 and measured at −40°C, +25°C, and +125°C. Typical endurance at 25°C is 170,000 cycles.
[17] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Std. 22 Method A117. Retention lifetime derates with junction temperature.
[18] Typical additional supply current consumed during Flash/EE memory program and erase cycles is 7 mA and 5 mA, respectively.

TIMING SPECIFICATIONS

I²C Timing

Table 2. I²C Timing in Standard Mode (100 kHz)

		Slave		Master	
Parameter	**Description**	**Min**	**Max**	**Typ**	**Unit**
t_L	SCLOCK low pulse width[1]	4.7			µs
t_H	SCLOCK high pulse width[1]	4.0			ns
t_{SHD}	Start condition hold time	4.0			µs
t_{DSU}	Data setup time	250			ns
t_{DHD}	Data hold time	0	3.45		µs
t_{RSU}	Setup time for repeated start	4.7			µs
t_{PSU}	Stop condition setup time	4.0			µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7			µs
t_R	Rise time for both CLOCK and SDATA		1		µs
t_F	Fall time for both CLOCK and SDATA		300		ns

[1] t_{HCLK} depends on the clock divider or CD bits in PLLCON MMR. $t_{HCLK} = t_{UCLK}/2^{CD}$.

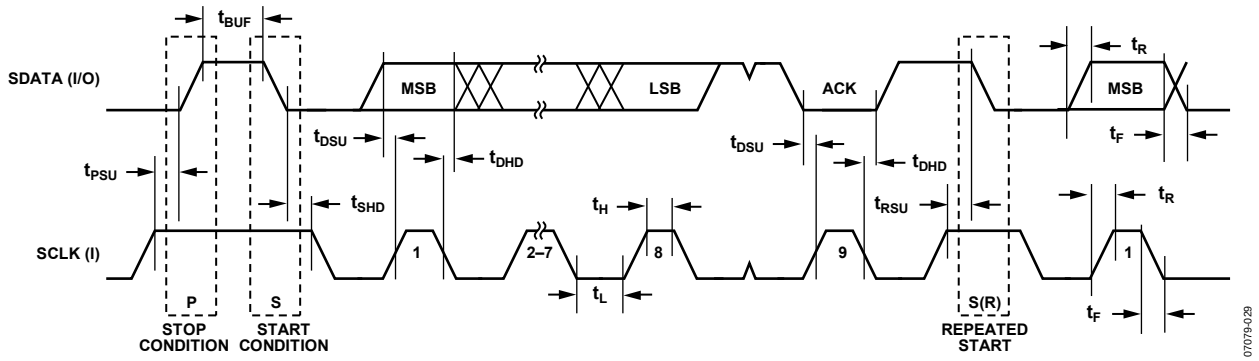


Figure 2. I²C Compatible Interface Timing

SPI Timing

Table 3. SPI Master Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLOCK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLOCK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLOCK edge			25	ns
t_{DSU}	Data input setup time before SCLOCK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLOCK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		30	40	ns
t_{DR}	Data output rise time		30	40	ns
t_{SR}	SCLOCK rise time		30	40	ns
t_{SF}	SCLOCK fall time		30	40	ns

[1] t_{HCLK} depends on the clock divider or CD bits in PLLCON MMR. $t_{HCLK} = t_{UCLK}/2^{CD}$.
[2] t_{UCLK} = 97.6 ns. It corresponds to the 10.24 MHz internal clock from the PLL before the clock divider.

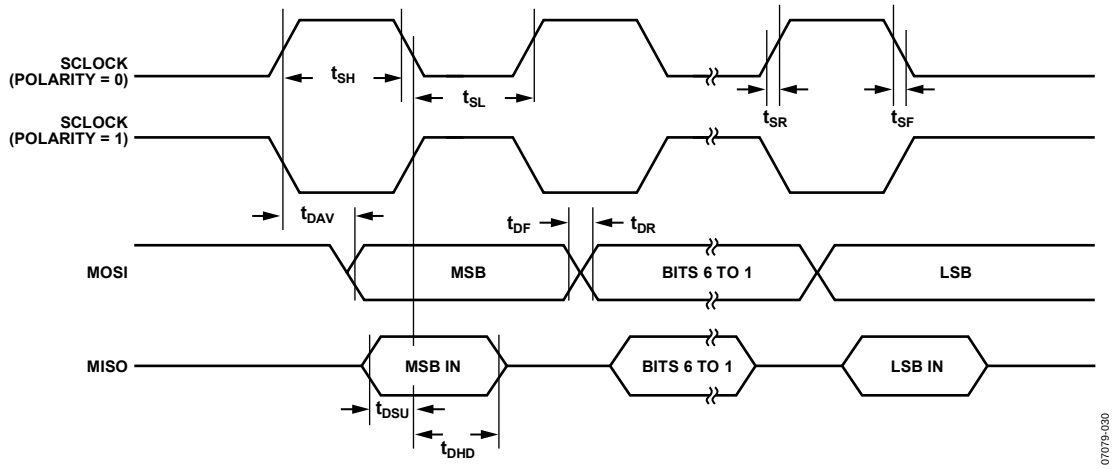


Figure 3. SPI Master Mode Timing (Phase Mode = 1)

Table 4. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLOCK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLOCK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLOCK edge			25	ns
t_{DOSU}	Data output setup before SCLOCK edge			90	ns
t_{DSU}	Data input setup time before SCLOCK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLOCK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		30	40	ns
t_{DR}	Data output rise time		30	40	ns
t_{SR}	SCLOCK rise time		30	40	ns
t_{SF}	SCLOCK fall time		30	40	ns

[1] t_{HCLK} depends on the clock divider or CD bits in PLLCON MMR. $t_{HCLK} = t_{UCLK}/2^{CD}$.
[2] t_{UCLK} = 97.6 ns. It corresponds to the 10.24 MHz internal clock from the PLL before the clock divider.

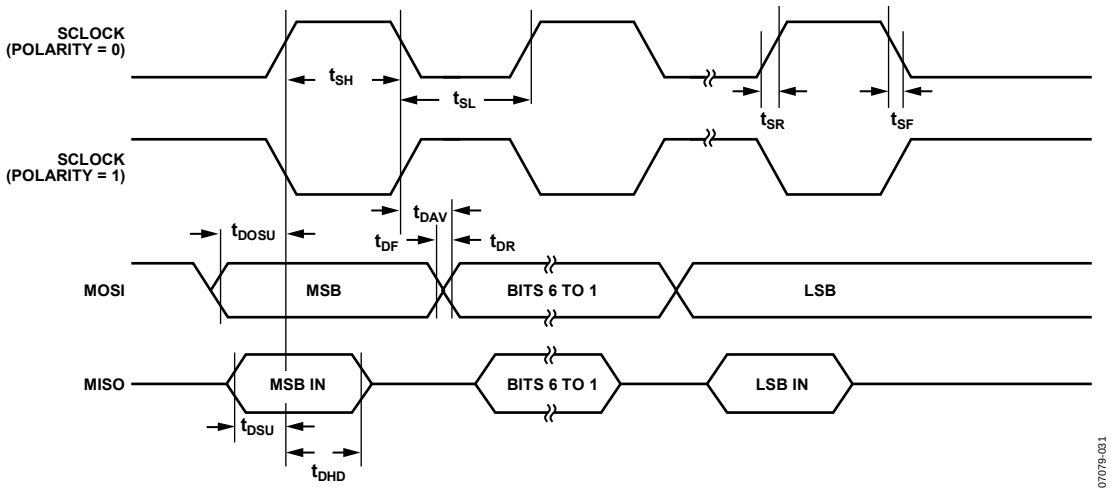


Figure 4. SPI Master Mode Timing (Phase Mode = 0)

Table 5. SPI Slave Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLOCK edge[1]	$(2 \times t_{HCLK}) + (2 \times t_{UCLK})$			ns
t_{SL}	SCLOCK low pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{SH}	SCLOCK high pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{DAV}	Data output valid after SCLOCK edge			40	ns
t_{DSU}	Data input setup time before SCLOCK edge[1]	$1 \times t_{UCLK}$			ns
t_{DHD}	Data input hold time after SCLOCK edge[1]	$2 \times t_{UCLK}$			ns
t_{DF}	Data output fall time		30	40	ns
t_{DR}	Data output rise time		30	40	ns
t_{SR}	SCLOCK rise time	1			ns
t_{SF}	SCLOCK fall time	1			ns
t_{SFS}	$\overline{CS}$ high after SCLOCK edge	0			ns

[1] t_{UCLK} =97.6 ns. It corresponds to the 10.24 MHz internal clock from the PLL before the clock divider.
[2] t_{HCLK} depends on the clock divider or CD bits in PLLCON MMR. $t_{HCLK} = t_{UCLK}/2^{CD}$.

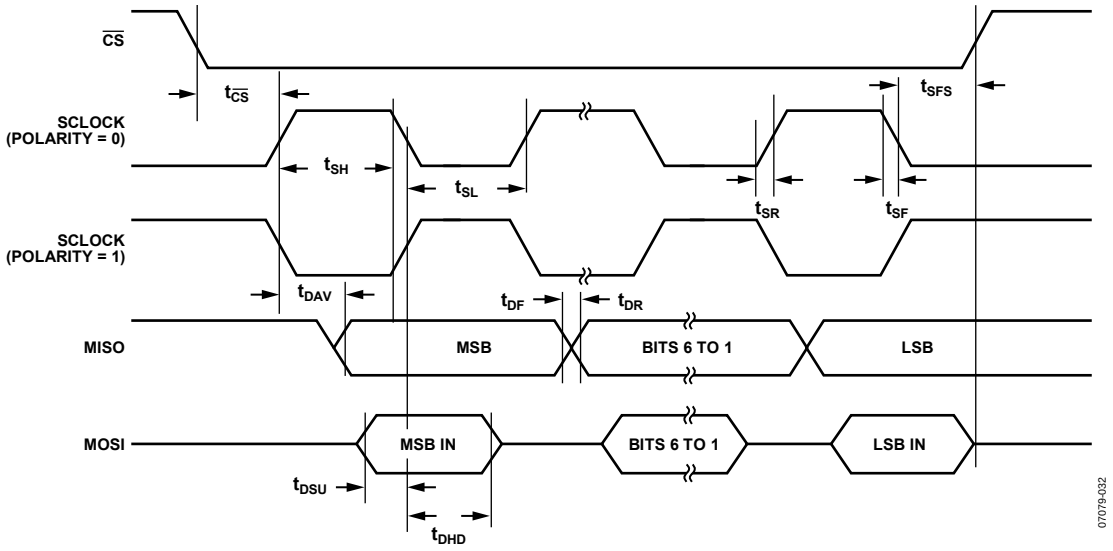


Figure 5. SPI Slave Mode Timing (Phase Mode = 1)

Table 6. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLOCK edge[1]	$(2 \times t_{HCLK}) + (2 \times t_{UCLK})$			ns
t_{SL}	SCLOCK low pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{SH}	SCLOCK high pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{DAV}	Data output valid after SCLOCK edge			40	ns
t_{DSU}	Data input setup time before SCLOCK edge[1]	$1 \times t_{UCLK}$			ns
t_{DHD}	Data input hold time after SCLOCK edge[1]	$2 \times t_{UCLK}$			ns
t_{DF}	Data output fall time		30	40	ns
t_{DR}	Data output rise time		30	40	ns
t_{SR}	SCLOCK rise time	1			ns
t_{SF}	SCLOCK fall time	1			ns
t_{DOCS}	Data output valid after $\overline{CS}$ edge			10	ns
t_{SFS}	$\overline{CS}$ high after SCLOCK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.
[2] t_{HCLK} depends on the clock divider or CD bits in PLLCON MMR. $t_{HCLK} = t_{UCLK}/2^{CD}$.

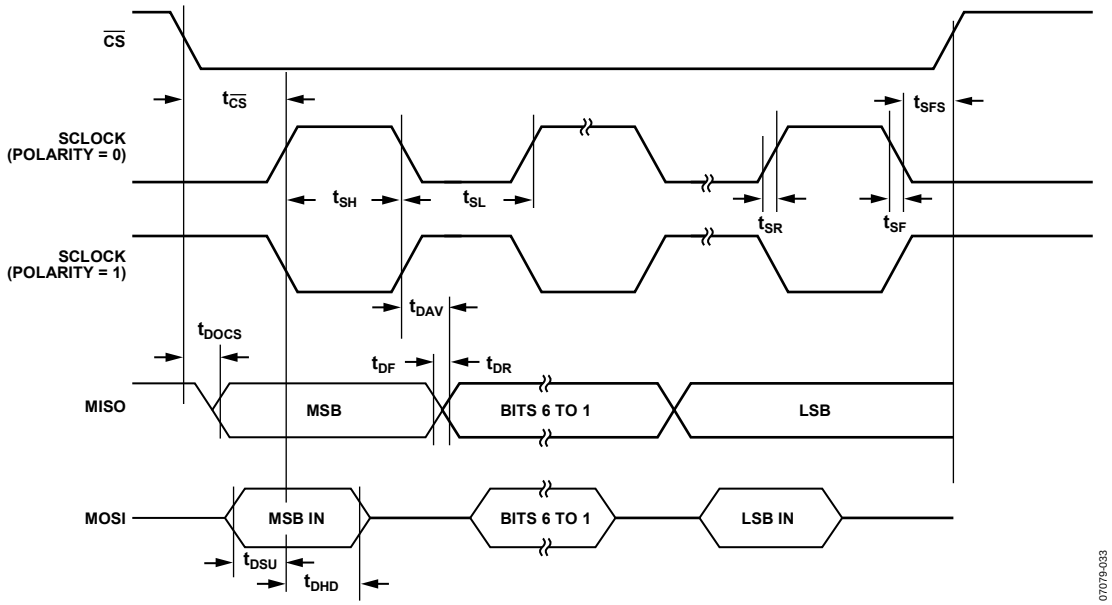


Figure 6. SPI Slave Mode Timing (Phase Mode = 0)

ABSOLUTE MAXIMUM RATINGS

T_A = −40°C to +125°C, unless otherwise noted.

Table 7.

Parameter	Rating
AGND to DGND to AVDD to DVDD	−0.3 V to +0.3 V
Digital I/O Voltage to DGND	−0.3 V to DVDD + 0.3 V
VREF± to AGND	−0.3 V to AVDD + 0.3 V
ADC Inputs to AGND	−0.3 V to AVDD + 0.3 V
ESD (Human Body Model) Rating	
All Pins	±2 kV
Storage Temperature	125°C
Junction Temperature	
Transient	150°C
Continuous	130°C
Lead Temperature	
Soldering Reflow (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

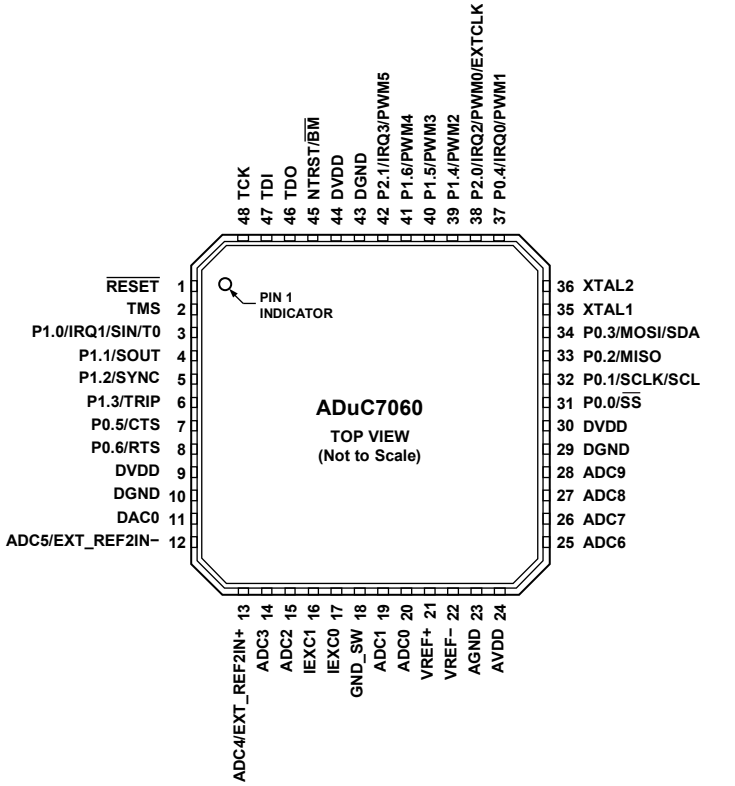


Figure 7. 48-Lead LQFP and 48-Lead LFCSP_VQ Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
0	EP		Exposed Paddle. The LFCSP_VQ only has an exposed paddle that must be left unconnected. This does not apply to the LQFP.
1	$\overline{\text{RESET}}$	I	Reset. Input pin, active low. An external 1 kΩ pull-up resistor is recommended with this pin.
2	TMS	I	JTAG Test Mode Select. Input pin. Used for debug and download. An external pull-up resistor (~100 kΩ) should be added to this pin.
3	P1.0/IRQ1/SIN/T0	I/O	General-Purpose Input and Output P1.0/External Interrupt Request 1/Serial Input Pin/Timer0 input. This pin is a multifunction input/output pin offering four functions.
4	P1.1/SOUT	I/O	General-Purpose Input and General-Purpose Output P1.1/Serial Output. This is a dual function input/output pin.
5	P1.2/SYNC	I/O	General-Purpose Input and General-Purpose Output P1.2/PWM External Sync Input. This is a dual function input/output pin.
6	P1.3/TRIP	I/O	General-Purpose Input and General-Purpose Output P1.3/PWM External Trip Input. This is a dual function input/output pin.
7	P0.5/CTS	I/O	General-Purpose Input and General-Purpose Output P0.5/Clear-to-Send Signal in UART Mode.
8	P0.6/RTS	I/O	General-Purpose Input and General-Purpose Output P0.6/Request-to-Send Signal in UART Mode.
9	DVDD	S	Digital Supply Pin.
10	DGND	S	Digital Ground.
11	DAC0	O	DAC Output. Analog output pin.
12	ADC5/EXT_REF2IN–	I	Single-Ended or Differential Analog Input 5/External Reference Negative Input. This is a dual function analog input pin. The ADC5 serves as the analog input for the auxiliary ADC. The EXT_REF2IN– serves as the external reference negative input by ADC for the auxiliary channel.

Pin No.	Mnemonic	Type[1]	Description
13	ADC4/EXT_REF2IN+	I	Multifunction Analog Input Pin. This pin can be used for the single-ended or differential Analog Input 4, which is the analog input for the auxiliary ADC, or it can be used for the external reference positive input for the auxiliary channel.
14	ADC3	I	Single-Ended or Differential Analog Input 3. Analog input for the primary and auxiliary ADCs.
15	ADC2	I	Single-Ended or Differential Analog Input 2. Analog input for the primary and auxiliary ADCs.
16	IEXC1	O	Programmable Current Source. Analog output pin.
17	IEXC0	O	Programmable Current Source. Analog output pin.
18	GND_SW	I	Switch to Internal Analog Ground Reference. When this input pin is not used, connect it directly to the AGND system ground.
19	ADC1	I	Positive Differential Input for Primary ADC. Analog input pin.
20	ADC0	I	Negative Differential Input for Primary ADC. Analog input pin.
21	VREF+	I	External Reference Positive Input for the Primary Channel. Analog input pin.
22	VREF−	I	External Reference Negative Input for the Primary Channel. Analog input pin.
23	AGND	S	Analog Ground.
24	AVDD	S	Analog Supply Pin.
25	ADC6	I	Analog Input 6 for Auxiliary ADC. Single-ended or differential Analog Input 6. Analog input for the auxiliary ADC.
26	ADC7	I	Analog Input 7 for Auxiliary ADC. Single-ended or differential Analog Input 7. Analog input for the auxiliary ADC.
27	ADC8	I	Analog Input 8 for Auxiliary ADC. Single-ended or differential Analog Input 8. Analog input for the auxiliary ADC.
28	ADC9	I	Analog Input 9 for Auxiliary ADC. Single-ended or differential Analog Input 9. Analog input for the auxiliary ADC.
29	DGND	S	Digital Ground.
30	DVDD	S	Digital Supply Pin.
31	P0.0/$\overline{SS}$	I/O	General-Purpose Input and General-Purpose Output P0.0/SPI Slave Select Pin. Active low. This is a dual function input/output pin.
32	P0.1/SCLK/SCL	I/O	General-Purpose Input and General-Purpose Output P0.1/SPI Clock Pin/I²C® Clock Pin. This is a triple function input/output pin.
33	P0.2/MISO	I/O	General-Purpose Input and General-Purpose Output P0.2/SPI Master Input Slave Output. This is a dual function input/output pin.
34	P0.3/MOSI/SDA	I/O	General-Purpose Input and General-Purpose Output P0.3/SPI Master Output Slave Input/I²C Data Pin. This is a triple function input/output pin.
35	XTAL1	O	External Crystal Oscillator Output Pin.
36	XTAL2	I	External Crystal Oscillator Input Pin.
37	P0.4/IRQ0/PWM1	I/O	General-Purpose Input and General-Purpose Output P0.4/External Interrupt Request 0/PWM1 Output. This is a triple function input/output pin.
38	P2.0/IRQ2/PWM0/EXTCLK	I/O	General-Purpose Input and General-Purpose Output P2.0/External Interrupt Request 2/PWM0 Output/External Clock Input. This is a triple function input/output pin.
39	P1.4/PWM2	I/O	General-Purpose Input and General-Purpose Output P1.4/PWM2 Output. This is a dual function input/output pin.
40	P1.5/PWM3	I/O	General-Purpose Input and General-Purpose Output P1.5/PWM3 Output. This is a dual function input/output pin.
41	P1.6/PWM4	I/O	General-Purpose Input and General-Purpose Output P1.6/PWM4 Output. This is a dual function input/output pin.
42	P2.1/IRQ3/PWM5	I/O	General-Purpose Input and General-Purpose Output P2.1/External Interrupt Request 3/PWM5 Output. This is a triple function input/output pin.
43	DGND	S	Digital Ground.
44	DVDD	S	Digital Supply Pin.
45	NTRST/$\overline{BM}$	I	JTAG Reset/Boot Mode. Input pin used for debug and download only and boot mode ($\overline{BM}$). The ADuC7060 enters serial download mode if $\overline{BM}$ is low at reset and executes code if $\overline{BM}$ is pulled high at reset through a 4.7 kΩ resistor.

Pin No.	Mnemonic	Type[1]	Description
46	TDO	O	JTAG Data Out. Output pin used for debug and download only.
47	TDI	I	JTAG Data In. Input pin used for debug and download only. Add an external pull-up resistor (~100 kΩ) to this pin.
48	TCK	I	JTAG Clock Pin. Input pin used for debug and download only. Add an external pull-up resistor (~100 kΩ) to this pin.

[1] I = input, O = output, S = supply.

TERMINOLOGY

Conversion Rate

The conversion rate specifies the rate at which an output result is available from the ADC, once the ADC has settled.

The sigma-delta (Σ-Δ) conversion techniques used on this part mean that while the ADC front-end signal is oversampled at a relatively high sample rate, a subsequent digital filter is used to decimate the output giving a valid 24-bit data conversion result at output rates from 1 Hz to 8 kHz.

Note that, when software switches from one input to another (on the same ADC), the digital filter must first be cleared and then allowed to average a new result. Depending on the configuration of the ADC and the type of filter, this can take multiple conversion cycles.

Integral Nonlinearity (INL)

INL is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

No Missing Codes

No missing codes is a measure of the differential nonlinearity of the ADC. The error is expressed in bits and specifies the number of codes (ADC results) as 2N bits, where N is no missing codes guaranteed to occur through the full ADC input range.

Offset Error

Offset error is the deviation of the first code transition ADC input voltage from the ideal first code transition.

Offset Error Drift

Offset error drift is the variation in absolute offset error with respect to temperature. This error is expressed as least significant bits per degree Celsius.

Gain Error

Gain error is a measure of the span error of the ADC. It is a measure of the difference between the measured and the ideal span between any two points in the transfer function.

Output Noise

The output noise is specified as the standard deviation (or 1 × Sigma) of ADC output codes distribution collected when the ADC input voltage is at a dc voltage. It is expressed as micro root mean square. The output, or root mean square (rms) noise, can be used to calculate the effective resolution of the ADC as defined by the following equation:

$$Effective\ Resolution = \log2(Full\text{-}Scale\ Range/rms\ Noise)\ \text{bits}$$

The peak-to-peak noise is defined as the deviation of codes that fall within 6.6 × Sigma of the distribution of ADC output codes collected when the ADC input voltage is at dc. The peak-to-peak noise is, therefore, calculated as

$$6.6 \times rms\ Noise$$

The peak-to-peak noise can be used to calculate the ADC (noise free code) resolution for which there is no code flicker within a 6.6-Sigma limit as defined by the following equation:

$$Noise\ Free\ Code\ Resolution = \log2\left(\frac{Full - Scale\ Range}{Peak - to - Peak\ Noise}\right)\ \text{bits}$$

Data Sheet Acronyms

ADC analog-to-digital converter
ARM advanced RISC machine
JTAG joint test action group
LSB least significant byte/bit
LVF low voltage flag
MCU microcontroller
MMR memory mapped register
MSB most significant byte/bit
PID protected identifier
POR power-on reset
PSM power supply monitor
rms root mean square

OVERVIEW OF THE ARM7TDMI CORE

The ARM7 core is a 32-bit, reduced instruction set computer (RISC), developed by ARM® Ltd. The ARM7TDMI is a von Neumann-based architecture, meaning that it uses a single 32-bit bus for instruction and data. The length of the data can be 8, 16, or 32 bits and the length of the instruction word is either 16 bits or 32 bits, depending on the mode in which the core is operating.

The ARM7TDMI is an ARM7 core with four additional features, as listed in Table 9.

Table 9. ARM7TDMI

Feature	Description
T	Support for the Thumb® (16-bit) instruction set
D	Support for debug
M	Enhanced multiplier
I	Includes the EmbeddedICE™ module to support embedded system debugging

THUMB MODE (T)

An ARM instruction is 32 bits long. The ARM7TDMI processor supports a second instruction set compressed into 16 bits, the Thumb instruction set. Faster code execution from 16-bit memory and greater code density is achieved by using the Thumb instruction set, making the ARM7TDMI core particularly suited for embedded applications.

However, the Thumb mode has three limitations.

- Relative to ARM, the Thumb code usually requires more instructions to perform the same task. Therefore, ARM code is best for maximizing the performance of time-critical code in most applications.
- The Thumb instruction set does not include some instructions that are needed for exception handling, so ARM code can be required for exception handling.
- When an interrupt occurs, the core vectors to the interrupt location in memory and executes the code present at that address. The first command is required to be in ARM code.

MULTIPLIER (M)

The ARM7TDMI instruction set includes an enhanced multiplier, with four extra instructions to perform 32-bit by 32-bit multiplication with a 64-bit result, and 32-bit by 32-bit multiplication-accumulation (MAC) with a 64-bit result.

EMBEDDED ICE (I)

The EmbeddedICE module provides integrated on-chip debug support for the ARM7TDMI. The EmbeddedICE module contains the breakpoint and watchpoint registers that allow nonintrusive user code debugging. These registers are controlled through the JTAG test port. When a breakpoint or watchpoint is encountered, the processor halts and enters the debug state. When in a debug state, the processor registers can be interrogated, as can the Flash/EE, SRAM, and memory mapped registers.

ARM7 Exceptions

The ARM7 supports five types of exceptions, with a privileged processing mode associated with each type. The five types of exceptions are as follows:

Type 1: normal interrupt or IRQ. This is provided to service general-purpose interrupt handling of internal and external events. Note, that the ADuC7060 supports eight configurable priority levels for all IRQ sources.

Type 2: fast interrupt or FIQ. This is provided to service data transfer or a communication channel with low latency. FIQ has priority over IRQ. Note, that the ADuC7060 supports eight configurable priority levels for all FIQ sources.

Type 3: memory abort (prefetch and data).

Type 4: attempted execution of an undefined instruction.

Type 5: software interrupts (SWI) instruction that can be used to make a call to an operating system.

Typically, the programmer defines interrupts as IRQ, but for higher priority interrupts, the programmer can define interrupts as the FIQ type.

The priority of these exceptions and vector addresses are listed in Table 10.

Table 10. Exception Priorities and Vector Addresses

Priority	Exception	Address
1	Hardware reset	0x00
2	Memory abort (data)	0x10
3	FIQ	0x1C
4	IRQ	0x18
5	Memory abort (prefetch)	0x0C
6	Software interrupt[1]	0x08
6	Undefined instruction[1]	0x04

[1] A software interrupt and an undefined instruction exception have the same priority and are mutually exclusive.

The list of exceptions in Table 10 are located from 0x00 to 0x1C, with a reserved location at 0x14.

ARM REGISTERS

The ARM7TDMI has 16 standard registers. R0 to R12 are for data manipulation, R13 is the stack pointer, R14 is the link register, and R15 is the program counter that indicates the instruction currently being executed. The link register contains the address from which the user has branched (when using the branch and link command) or the command during which an exception occurred.

The stack pointer contains the current location of the stack. Generally, on an ARM7TDMI, the stack starts at the top of the available RAM area and descends using the area as required. A separate stack is defined for each of the exceptions. The size of each stack is user configurable and is dependent on the target application. When programming using high level languages, such as C, it is necessary to ensure that the stack does not overflow. This is dependent on the performance of the compiler that is used.

When an exception occurs, some of the standard registers are replaced with registers specific to the exception mode. All exception modes have replacement banked registers for the stack pointer (R13) and the link register (R14) as represented in Figure 8. The FIQ mode has more registers (R8 to R12) supporting faster interrupt processing. With the increased number of noncritical registers, the interrupt can be processed without the need to save or restore these registers, thereby reducing the response time of the interrupt handling process.

More information relative to the programmer's model and the ARM7TDMI core architecture can be found in ARM7TDMI technical and ARM architecture manuals available directly from ARM Ltd.

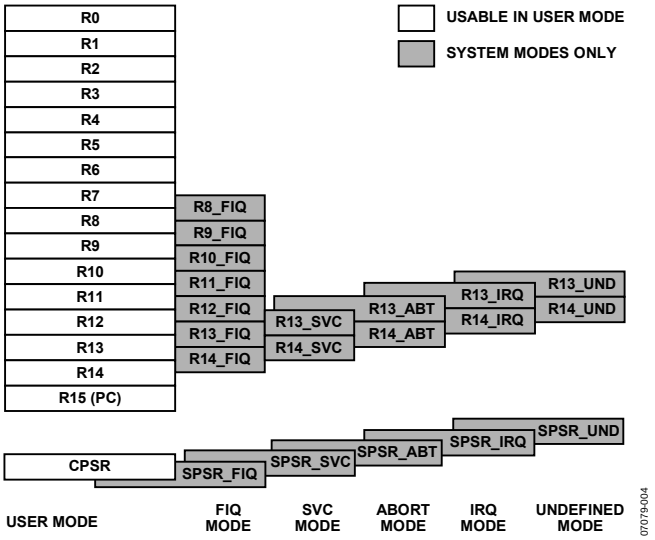


Figure 8. Register Organization

INTERRUPT LATENCY

The worst-case latency for an FIQ consists of the longest time the request can take to pass through the synchronizer, plus the time for the longest instruction to complete (the longest instruction is an LDM) that loads all the registers including the PC, plus the time for the data abort entry, plus the time for FIQ entry. At the end of this time, the ARM7TDMI is executing the instruction at 0x1C (FIQ interrupt vector address). The maximum total time is 50 processor cycles, or just over 4.88 µs in a system using a continuous 10.24 MHz processor clock. The maximum IRQ latency calculation is similar but must allow for the FIQ having higher priority, which can delay entry into the IRQ handling routine for an arbitrary length of time. This time can be reduced to 42 cycles if the LDM command is not used; some compilers have an option to compile without using this command. Another option is to run the part in Thumb mode where this is reduced to 22 cycles.

The minimum latency for FIQ or IRQ interrupts is five cycles. This consists of the shortest time the request can take through the synchronizer plus the time to enter the exception mode.

Note that the ARM7TDMI initially (first instruction) runs in ARM (32-bit) mode when an exception occurs. The user can immediately switch from ARM mode to Thumb mode if required, for example, when executing interrupt service routines.

MEMORY ORGANIZATION

The ARM7, a von Neumann architecture MCU core sees memory as a linear array of 232-byte locations. As shown in Figure 9, the ADuC7060 maps this into four distinct user areas, namely: a memory area that can be remapped, an SRAM area, a Flash/EE area, and a memory mapped register (MMR) area.

The first 30 kB of this memory space is used as an area into which the on-chip Flash/EE or SRAM can be remapped. Any access, either reading or writing, to an area not defined in the memory map results in a data abort exception.

Memory Format

The ADuC7060 memory organization is configured in little endian format: the least significant byte is located in the lowest byte address and the most significant byte in the highest byte address. See Figure 10 for details.

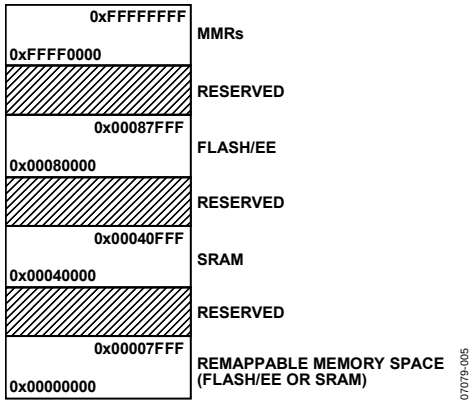


Figure 9. Memory Map

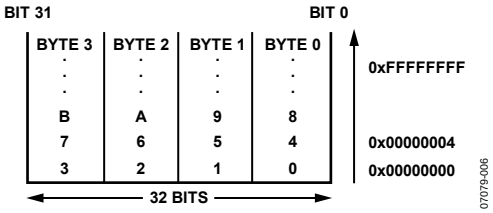


Figure 10. Little Endian Format

SRAM

The ADuC7060 features 4 kB of SRAM, organized as 1024 × 32 bits, that is, 1024 words located at 0x40000. The RAM space can be used as data memory as well as volatile program space.

ARM code can run directly from SRAM at full clock speed given that the SRAM array is configured as a 32-bit wide memory array. SRAM is read/writable in 8-, 16-, and 32-bit segments.

Remap

The ARM exception vectors are all situated at the bottom of the memory array, from Address 0x00000000 to Address 0x00000020.

By default, after a reset, the Flash/EE memory is logically mapped to Address 0x00000000. It is possible to logically remap the SRAM to Address 0x00000000 by setting Bit 0 of the remap MMR located at 0xFFFF0220. To revert Flash/EE to 0x00000000, Bit 0 of remap is cleared.

It is sometimes desirable to remap RAM to 0x00000000 to optimize the interrupt latency of the ADuC7060 because code can run in full 32-bit ARM mode and at maximum core speed. Note that, when an exception occurs, the core defaults to ARM mode.

Remap Operation

When a reset occurs on the ADuC7060, execution starts automatically in the factory programmed internal configuration code. This so-called kernel is hidden and cannot be accessed by user code. If the ADuC7060 is in normal mode, it executes the power-on configuration routine of the kernel and then jumps to the reset vector, Address 0x00000000, to execute the user's reset exception routine. Because the Flash/EE is mirrored at the bottom of the memory array at reset, the reset routine must always be written in Flash/EE.

The remap command must be executed from the absolute Flash/EE address and not from the mirrored, remapped segment of memory, because this may be replaced by SRAM. If a remap operation is executed while operating code from the mirrored location, prefetch/data aborts can occur or the user can observe abnormal program operation. Any kind of reset logically remaps the Flash/EE memory to the bottom of the memory array.

Remap Register

Name: Remap

Address: 0xFFFF0220

Default value: 0x0000

Access: Read and write

Function: This 8-bit register allows user code to remap either RAM or Flash/EE space into the bottom of the ARM memory space starting at Address 0x00000000.

Table 11. REMAP MMR Bit Designations

Bit	Description
7:1	Reserved. These bits are reserved and should be written as 0 by user code.
0	Remap bit. Set by user to remap the SRAM to 0x00000000. Cleared automatically after reset to remap the Flash/EE memory to 0x00000000.

FLASH/EE CONTROL INTERFACE

Serial and JTAG programming use the Flash/EE control interface, which includes the eight MMRs outlined in this section.

FEESTA Register

FEESTA is a read-only register that reflects the status of the flash control interface as described in Table 12.

Name: FEESTA

Address: 0xFFFF0E00

Default value: 0x0020

Access: Read

Table 12. FEESTA MMR Bit Designations

Bit	Description
15:6	Reserved.
5	Reserved.
4	Reserved.
3	Flash interrupt status bit. Set automatically when an interrupt occurs, that is, when a command is complete and the Flash/EE interrupt enable bit in the FEEMOD register is set. Cleared when reading the FEESTA register.
2	Flash/EE controller busy. Set automatically when the controller is busy. Cleared automatically when the controller is not busy.
1	Command fail. Set automatically when a command completes unsuccessfully. Cleared automatically when reading the FEESTA register.
0	Command pass. Set by the MicroConverter® when a command completes successfully. Cleared automatically when reading the FEESTA register.

FEEMOD Register

FEEMOD sets the operating mode of the flash control interface. Table 13 shows FEEMOD MMR bit designations.

Name: FEEMOD

Address: 0xFFFF0E04

Default value: 0x0000

Access: Read and write

Table 13. FEEMOD MMR Bit Designations

Bit	Description
15:9	Reserved.
8	Reserved. Always set this bit to 0.
7:5	Reserved. Always set these bits to 0 except when writing keys.
4	Flash/EE interrupt enable. Set by user to enable the Flash/EE interrupt. The interrupt occurs when a command is complete. Cleared by user to disable the Flash/EE interrupt.
3	Erase/write command protection. Set by user to enable the erase and write commands. Cleared to protect the Flash against the erase/write command.
2:0	Reserved. Always set these bits to 0.

FEECON Register

FEECON is an 8-bit command register. The commands are described in Table 14.

Name: FEECON

Address: 0xFFFF0E08

Default value: 0x07

Access: Read and write

Table 14. Command Codes in FEECON

Code	Command	Description
0x00[1]	Null	Idle state.
0x01[1]	Single read	Load FEEDAT with the 16-bit data. Indexed by FEEADR.
0x02[1]	Single write	Write FEEDAT at the address pointed by FEEADR. This operation takes 50 µs.
0x03[1]	Erase/write	Erase the page indexed by FEEADR and write FEEDAT at the location pointed by FEEADR. This operation takes approximately 24 ms.
0x04[1]	Single verify	Compare the contents of the location pointed to by FEEADR to the data in FEEDAT. The result of the comparison is returned in FEESTA Bit 1.
0x05[1]	Single erase	Erase the page indexed by FEEADR.
0x06[1]	Mass erase	Erase 30 kB of user space. The 2 kB of kernel are protected. To prevent accidental execution, a command sequence is required to execute this instruction. See the Command Sequence for Executing a Mass Erase section.
0x07	Reserved	Reserved.
0x08	Reserved	Reserved.
0x09	Reserved	Reserved.
0x0A	Reserved	Reserved.
0x0B	Signature	This command results in a 24-bit LFSR-based signature being generated and loaded into FEESIGN MMR. This operation takes 16,389 clock cycles.
0x0C	Protect	This command can run only once. The value of FEEPRO is saved and removed only with a mass erase (0x06) or the key.
0x0D	Reserved	Reserved.
0x0E	Reserved	Reserved.
0x0F	Ping	No operation; interrupt generated.

[1] The FEECON register always reads 0x07 immediately after execution of any of these commands.

FEEDAT Register

FEEDAT is a 16-bit data register. This register holds the data value for flash read and write commands.

Name: FEEDAT

Address: 0xFFFF0E0C

Default value: 0xXXXX

Access: Read and write

FEEADR Register

FEEADR is a 16-bit address register used for accessing individual pages of the 32 kB flash block. The valid address range for a user is: 0x0000 to 0x77FF. This represents the 30 kB flash user memory space. A read or write access outside this boundary causes a data abort exception to occur.

Name: FEEADR

Address: 0xFFFF0E10

Default value: 0x0000

Access: Read and write

FEESIGN Register

The FEESIGN register is a 24-bit MMR. This register is updated with the 24-bit signature value after the signature command has been executed. This value is the result of the linear feedback shift register (LFSR) operation initiated by the signature command.

Name: FEESIGN

Address: 0xFFFF0E18

Default value: 0xFFFFFF

Access: Read

FEEPRO Register

FEEPRO MMR provides protection following a subsequent reset of the MMR. It requires a software key (see Table 15).

Name: FEEPRO

Address: 0xFFFF0E1C

Default value: 0x00000000

Access: Read and write

FEEHIDE Register

FEEHIDE MMR provides immediate protection. It does not require any software key. Note that the protection settings in FEEHIDE are cleared by a reset (see Table 15).

Name: FEEHIDE

Address: 0xFFFF0E20

Default value: 0xFFFFFFFF

Access: Read and write

Table 15. FEEPRO and FEEHIDE MMR Bit Designations

Bit	Description
31	Read protection. Cleared by user to protect all code. No JTAG read accesses for protected pages if this bit is set. Set by the user to allow reading the code via JTAG.
30	Protection for Page 59 (0x00087600 to 0x000877FF). Set by user to allow writing to Page 59. Cleared to protect Page 59.
29	Protection for Page 58 (0x00087400 to 0x000875FF). Set by the user to allow writing to Page 58. Cleared to protect Page 58.
28:0	Write protection for Page 57 to Page 0. Each bit represents two pages. Each page is 512 bytes in size. Bit 0 is protection for Page 0 and Page 1 (0x00080000 to 0x000803FF). Set by the user to allow writing Page 0 and Page 1. Cleared to protect Page 0 and Page 1. Bit 1 is protection for Page 2 and Page 3 (0x00080400 to 0x000807FF. Set by the user to allow writing Page 2 and Page 3. Cleared to protect Page 2 and Page 3. … … Bit 27 is protection for Page 54 and Page 55 (0x00087000 to 0x000873FF). Set by the user to allow writing to Page 54 and Page 55. Cleared to protect Page 54 and Page 55. Bit 28 is protection for Page 56 and Page 57 (0x00087400 to 0x000877FF). Set by the user to allow writing to Page 56 and Page 57. Cleared to protect Page 56 and Page 57.

Command Sequence for Executing a Mass Erase

```
FEEDAT = 0x3CFF;
FEEADR = 0x77C3;
FEEMOD = FEEMOD|0x8;   //Erase key enable
FEECON = 0x06;         //Mass erase command
```

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers, except the core registers, reside in the MMR area. All shaded locations shown in Figure 11 are unoccupied or reserved locations and should not be accessed by user software. Figure 11 shows the full MMR memory map.

The access time for reading from or writing to an MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: advanced high performance bus (AHB) used for system modules and advanced peripheral bus (APB) used for a lower performance peripheral. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7060 are on the APB except the Flash/EE memory, the GPIOs, and the PWM.

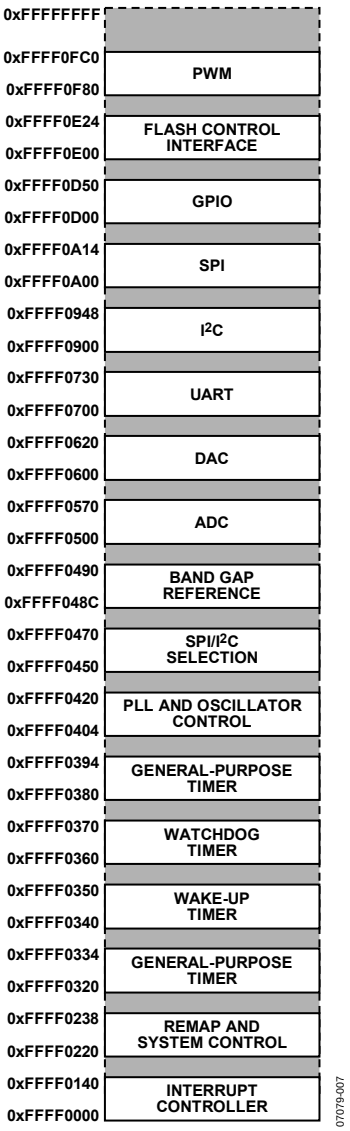


Figure 11. Memory Mapped Registers

COMPLETE MMR LISTING

In the following MMR tables, addresses are listed in hexadecimal code. Access types include R for read, W for write, and R/W for read and write.

Table 16. IRQ Address Base = 0xFFFF0000

Address	Name	Byte	Access Type	Default Value	Description
0x0000	IRQSTA	4	R	0x00000000	Active IRQ source.
0x0004	IRQSIG	4	R		Current state of all IRQ sources (enabled and disabled).
0x0008	IRQEN	4	R/W	0x00000000	Enabled IRQ sources.
0x000C	IRQCLR	4	W	0x00000000	MMR to disable IRQ sources.
0x0010	SWICFG	4	W	0x00000000	Software interrupt configuration MMR.
0x0014	IRQBASE	4	R/W	0x00000000	Base address of all vectors. Points to the start of the 64-byte memory block, which can contain up to 32 pointers to separate subroutine handlers.
0x001C	IRQVEC	4	R	0x00000000	This register contains the subroutine address for the currently active IRQ source.
0x0020	IRQP0	4	R/W	0x00000000	Contains the interrupt priority setting for interrupt Source 1 to Source 7. An interrupt can have a priority setting of 0 to 7. For example: Bits[7:4] contain the priority level for Interrupt 1. Bits[11:8] contain the priority level for Interrupt 2. Bits[31:28] contain the priority level for Interrupt 7.
0x0024	IRQP1	4	R/W	0x00000000	Contains the interrupt priority setting for Interrupt Source 8 to Interrupt Source 15. For example: Bits[7:4] contain the priority level for Interrupt 9. Bits[11:8] contain the priority level for Interrupt 10. Bits[31:28] contain the priority level for Interrupt 15.
0x0028	IRQP2	4	R/W	0x00000000	Contains the interrupt priority setting for Interrupt Source 16 to Interrupt Source 19.
0x0030	IRQCONN	4	R/W	0x00000000	Used to enable IRQ and FIQ interrupt nesting.
0x0034	IRQCONE	4	R/W	0x00000000	Configures the external interrupt sources as rising edge, falling edge, or level triggered.
0x0038	IRQCLRE	4	R/W	0x00000000	Used to clear an edge-level-triggered interrupt source.
0x003C	IRQSTAN	4	R/W	0x00000000	This register indicates the priority level of an interrupt that has just caused an interrupt exception.
0x0100	FIQSTA	4	R	0x00000000	Active FIQ source.
0x0104	FIQSIG	4	R		Current state of all FIQ sources (enabled and disabled).
0x0108	FIQEN	4	R/W	0x00000000	Enabled FIQ sources.
0x010C	FIQCLR	4	W	0x00000000	MMR to disable FIQ sources.
0x011C	FIQVEC	4	R	0x00000000	FIQ interrupt vector.
0x013C	FIQSTAN	4	R/W	0x00000000	Indicates the priority level of an FIQ that has just caused an FIQ exception.

Table 17. System Control Address Base = 0xFFFF0200

Address	Name	Byte	Access Type	Default Value	Description
0x0220	REMAP[1]	1	R/W	0x00	REMAP control register. See the Remap Operation section.
0x0230	RSTSTA	1	R/W	0x01	RSTSTA status MMR. See the Reset section.
0x0234	RSTCLR	1	W	0x00	RSTCLR MMR for clearing the RSTSTA register.

[1]Updated by the kernel.

Table 18. Timer Address Base = 0xFFFF0300

Address	Name	Byte	Access Type	Default Value	Description
0x0320	T0LD	4	R/W	0x00000000	Timer0 load register.
0x0324	T0VAL	4	R	0xFFFFFFFF	Timer0 value register.
0x0328	T0CON	4	R/W	0x01000000	Timer0 control MMR.
0x032C	T0CLRI	1	R/W	N/A	Timer0 interrupt clear register.
0x0330	T0CAP	4	R	0x00000000	Timer0 capture register.
0x0340	T1LD	4	R/W	0x00000000	Timer1 load register.
0x0344	T1VAL	4	R	0xFFFFFFFF	Timer1 value register.
0x0348	T1CON	2	R/W	0x0000	Timer1 control MMR.
0x034C	T1CLRI	1	W	N/A	Timer1 interrupt clear register.
0x0360	T2LD	2	R/W	0x0040	Timer2 load register.
0x0364	T2VAL	2	R	0x0040	Timer2 value register.
0x0368	T2CON	2	R/W	0x0000	Timer2 control MMR.
0x036C	T2CLRI	1	W	N/A	Timer2 interrupt clear register.
0x0380	T3LD	2	R/W	0x0000	Timer3 load register.
0x0384	T3VAL	2	R	0xFFFF	Timer3 value register.
0x0388	T3CON	4	R/W	0x00000000	Timer3 control MMR.
0x038C	T3CLRI	1	W	N/A	Timer3 interrupt clear register.
0x0390	T3CAP	2	R	0x0000	Timer3 capture register.

Table 19. PLL Base Address = 0xFFFF0400

Address	Name	Byte	Access Type	Default Value	Description
0x0404	POWKEY1	2	W	N/A	POWCON0 prewrite key.
0x0408	POWCON0	1	R/W	0x7B	Power control and core speed control register.
0x040C	POWKEY2	2	W	N/A	POWCON0 postwrite key.
0x0410	PLLKEY1	2	W	N/A	PLLCON prewrite key.
0x0414	PLLCON	1	R/W	0x00	PLL clock source selection MMR.
0x0418	PLLKEY2	2	W	N/A	PLLCON postwrite key.
0x0464	GP0KEY1	2	W	0xXXXX	GP0CON1 prewrite key.
0x0468	GP0CON1	1	R/W	0x00	Configures P0.0, P0.1, P0.2, and P0.3 as analog inputs or digital I/Os. Also enables SPI or I^2C mode.
0x046C	GP0KEY2	2	W	0xXXXX	GP0CON1 postwrite key.

Table 20. ADC Address Base = 0xFFFF0500

Address	Name	Byte	Access Type	Default Value	Description
0x0500	ADCSTA	2	R	0x0000	ADC status MMR.
0x0504	ADCMSKI	2	R/W	0x0000	ADC interrupt source enable MMR.
0x0508	ADCMDE	1	R/W	0x03	ADC mode register.
0x050C	ADC0CON	2	R/W	0x8000	Primary ADC control MMR.
0x0510	ADC1CON	2	R/W	0x0000	Auxiliary ADC control MMR.
0x0514	ADCFLT	2	R/W	0x0007	ADC filter control MMR.
0x0518	ADCCFG	1	R/W	0x00	ADC configuration MMR.
0x051C	ADC0DAT	4	R	0x00000000	Primary ADC result MMR.
0x0520	ADC1DAT	4	R	0x00000000	Auxiliary ADC result MMR
0x0524	ADC0OF[1]	2	R/W	0x0000, part specific, factory programmed	Primary ADC offset calibration setting.
0x0528	ADC1OF[1]	2	R/W	0x0000, part specific, factory programmed	Auxiliary ADC offset MMR.
0x052C	ADC0GN[1]	2	R/W	0x5555	Primary ADC offset MMR.
0x0530	ADC1GN[1]	2	R/W	0x5555	Auxiliary ADC offset MMR. See the ADC operation mode configuration bit (ADCLPMCFG[1:0]) in Table 40.
0x0534	ADC0RCR	2	R/W	0x0001	Primary ADC result counter/reload MMR.
0x0538	ADC0RCV	2	R	0x0000	Primary ADC result counter MMR.
0x053C	ADC0TH	2	R/W	0x0000	Primary ADC 16-bit comparator threshold MMR.
0x0540	ADC0THC	2	R/W	0x0001	Primary ADC 16-bit comparator threshold counter limit.
0x0544	ADC0THV	2	R	0x0000	ADC0 8-bit threshold exceeded counter register
0x0548	ADC0ACC	4	R	0x00000000	Primary ADC accumulator.
0x054C	ADC0ATH	4	R/W	0x00000000	Primary ADC 32-bit comparator threshold MMR.
0x0570	IEXCON	1	R/W	0x00	Excitation current sources control register.

[1] Updated by the kernel.

Table 21. DAC Control Address Base = 0xFFFF0600

Address	Name	Byte	Access Type	Default Value	Description
0x0600	DAC0CON	2	R/W	0x0200	DAC control register.
0x0604	DAC0DAT	4	R/W	0x00000000	DAC output data register.

Table 22. UART Base Address = 0xFFFF0700

Address	Name	Byte	Access Type	Default Value	Description
0x0700	COMTX	1	W	N/A	UART transmit register.
0x0700	COMRX	1	R	0x00	UART receive register.
0x0700	COMDIV0	1	R/W	0x00	UART Standard Baud Rate Generator Divisor Value 0.
0x0704	COMIEN0	1	R/W	0x00	UART Interrupt Enable MMR 0.
0x0704	COMDIV1	1	R/W	0x00	UART Standard Baud Rate Generator Divisor Value 1.
0x0708	COMIID0	1	R	0x01	UART Interrupt Identification 0.
0x070C	COMCON0	1	R/W	0x00	UART Control Register 0.
0x0710	COMCON1	1	R/W	0x00	UART Control Register 1.
0x0714	COMSTA0	1	R	0x60	UART Status Register 0.
0x0718	COMSTA1	1	R	0x00	UART Status Register 1.
0X072C	COMDIV2	2	R/W	0x0000	UART fractional divider MMR.

Table 23. I²C Base Address = 0xFFFF0900

Address	Name	Byte	Access Type	Default Value	Description
0x0900	I2CMCON	2	R/W	0x0000	I²C master control register.
0x0904	I2CMSTA	2	R	0x0000	I²C master status register.
0x0908	I2CMRX	1	R	0x00	I²C master receive register.
0x090C	I2CMTX	1	W	0x00	I²C master transmit register.
0x0910	I2CMCNT0	2	R/W	0x0000	I²C master read count register. Write the number of required bytes into this register prior to reading from a slave device.
0x0914	I2CMCNT1	1	R	0x00	I²C master current read count register. This register contains the number of bytes already received during a read from slave sequence.
0x0918	I2CADR0	1	R/W	0x00	Address byte register. Write the required slave address here prior to communications.
0x091C	I2CADR1	1	R/W	0x00	Address byte register. Write the required slave address here prior to communications. Only used in 10-bit mode.
0x0924	I2CDIV	2	R/W	0x1F1F	I²C clock control register. Used to configure the SCLK frequency.
0x0928	I2CSCON	2	R/W	0x0000	I²C slave control register.
0x092C	I2CSSTA	2	R/W	0x0000	I²C slave status register.
0x0930	I2CSRX	1	R	0x00	I²C slave receive register.
0x0934	I2CSTX	1	W	0x00	I²C slave transmit register.
0x0938	I2CALT	1	R/W	0x00	I²C hardware general call recognition register.
0x093C	I2CID0	1	R/W	0x00	I²C Slave ID0 register. Slave bus ID register.
0x0940	I2CID1	1	R/W	0x00	I²C Slave ID1 register. Slave bus ID register.
0x0944	I2CID2	1	R/W	0x00	I²C Slave ID2 register. Slave bus ID register.
0x0948	I2CID3	1	R/W	0x00	I²C Slave ID3 register. Slave bus ID register.
0x094C	I2CFSTA	2	R/W	0x0000	I²C FIFO status register. Used in both master and slave modes.

Table 24. SPI Base Address = 0xFFFF0A00

Address	Name	Byte	Access Type	Default Value	Description
0x0A00	SPISTA	4	R	0x00000000	SPI status MMR.
0x0A04	SPIRX	1	R	0x00	SPI receive MMR.
0x0A08	SPITX	1	W	0xXX	SPI transmit MMR.
0x0A0C	SPIDIV	1	W	0x1B	SPI baud rate select MMR.
0x0A10	SPICON	2	R/W	0x0000	SPI control MMR.

Table 25. GPIO Base Address = 0xFFFF0D00

Address	Name	Byte	Access Type	Default Value	Description
0x0D00	GP0CON	4	RW	0x00000000	GPIO Port 0 control MMR.
0x0D04	GP1CON	4	RW	0x00000000	GPIO Port 1 control MMR.
0x0D08	GP2CON	4	RW	0x00000000	GPIO Port 2 control MMR.
0x0D20	GP0DAT	4	RW	0x000000XX	GPIO Port 0 data control MMR.
0x0D24	GP0SET	4	W	0x000000XX	GPIO Port 0 data set MMR.
0x0D28	GP0CLR	4	W	0x000000XX	GPIO Port 0 data clear MMR.
0x0D2C	GP0PAR	4	R/W	0x00000000	GPIO Port 0 pull-up disable MMR.
0x0D30	GP1DAT	4	RW	0x000000XX	GPIO Port 1 data control MMR.
0x0D34	GP1SET	4	W	0x000000XX	GPIO Port 1 data set MMR.
0x0D38	GP1CLR	4	W	0x000000XX	GPIO Port 1 data clear MMR.
0x0D3C	GP1PAR	4	R/W	0x00000000	GPIO Port 1 pull-up disable MMR.
0x0D40	GP2DAT	4	RW	0x000000XX	GPIO Port 2 data control MMR.
0x0D44	GP2SET	4	W	0x000000XX	GPIO Port 2 data set MMR.
0x0D48	GP2CLR	4	W	0x000000XX	GPIO Port 2 data clear MMR.
0x0D4C	GP2PAR	4	R/W	0x00000000	GPIO Port 2 pull-up disable MMR.

Table 26. Flash/EE Base Address = 0xFFFF0E00

Address	Name	Byte	Access Type	Default Value	Description
0x0E00	FEESTA	2	R	0x20	Flash/EE status MMR.
0x0E04	FEEMOD	2	RW	0x0000	Flash/EE control MMR.
0x0E08	FEECON	1	RW	0x07	Flash/EE control MMR.
0x0E0C	FEEDAT	2	RW	0xXXXX	Flash/EE data MMR.
0x0E10	FEEADR	2	RW	0x0000	Flash/EE address MMR.
0x0E18	FEESIGN	3	R	0xFFFFFF	Flash/EE LFSR MMR.
0x0E1C	FEEPRO	4	RW	0x00000000	Flash/EE protection MMR.
0x0E20	FEEHIDE	4	RW	0xFFFFFFFF	Flash/EE protection MMR.

Table 27. PWM Base Address = 0xFFFF0F80

Address	Name	Byte	Access Type	Default Value	Description
0x0F80	PWMCON	2	R/W	0x0012	PWM control register. See the Pulse-Width Modulator section for full details.
0x0F84	PWM0COM0	2	R/W	0x0000	Compare Register 0 for PWM Output 0 and PWM Output 1.
0x0F88	PWM0COM1	2	R/W	0x0000	Compare Register 1 for PWM Output 0 and PWM Output 1.
0x0F8C	PWM0COM2	2	R/W	0x0000	Compare Register 2 for PWM Output 0 and PWM Output 1.
0x0F90	PWM0LEN	2	R/W	0x0000	Frequency control for PWM Output 0 and PWM Output 1.
0x0F94	PWM1COM0	2	R/W	0x0000	Compare Register 0 for PWM Output 2 and PWM Output 3.
0x0F98	PWM1COM1	2	R/W	0x0000	Compare Register 1 for PWM Output 2 and PWM Output 3.
0x0F9C	PWM1COM2	2	R/W	0x0000	Compare Register 2 for PWM Output 2 and PWM Output 3.
0x0FA0	PWM1LEN	2	R/W	0x0000	Frequency Control for PWM Output 2 and PWM Output 3.
0x0FA4	PWM2COM0	2	R/W	0x0000	Compare Register 0 for PWM Output 4 and PWM Output 5.
0x0FA8	PWM2COM1	2	R/W	0x0000	Compare Register 1 for PWM Output 4 and PWM Output 5.
0x0FAC	PWM2COM2	2	R/W	0x0000	Compare Register 2 for PWM Output 4 and PWM Output 5.
0x0FB0	PWM2LEN	2	R/W	0x0000	Frequency Control for PWM Output 4 and PWM Output 5.
0x0FB8	PWMCLRI	2	W	0x0000	PWM interrupt clear register. Writing any value to this register clears a PWM interrupt source.

RESET

There are four kinds of reset: external reset, power-on-reset, watchdog reset, and software reset. The RSTSTA register indicates the source of the last reset and can be written by user code to initiate a software reset event.

The bits in this register can be cleared to 0 by writing to the RSTCLR MMR at 0xFFFF0234. The bit designations in RSTCLR mirror those of RSTSTA. These registers can be used during a reset exception service routine to identify the source of the reset. The implications of all four kinds of reset events are tabulated in Table 29.

RSTSTA Register

Name: RSTSTA

Address: 0xFFFF0230

Default value: Depends on type of reset

Access: Read and write

Function: This 8-bit register indicates the source of the last reset event and can be written by user code to initiate a software reset.

RSTCLR Register

Name: RSTCLR

Address: 0xFFFF0234

Access: Write only

Function: This 8-bit write only register clears the corresponding bit in RSTSTA.

Table 28. RSTSTA/RSTCLR MMR Bit Designations

Bit	Description
7 to 4	Not used. These bits are not used and always read as 0.
3	External reset. Automatically set to 1 when an external reset occurs. This bit is cleared by setting the corresponding bit in RSTCLR.
2	Software reset. This bit is set to 1 by user code to generate a software reset. This bit is cleared by setting the corresponding bit in RSTCLR.[1]
1	Watchdog timeout. Automatically set to 1 when a watchdog timeout occurs. Cleared by setting the corresponding bit in RSTCLR.
0	Power-on reset. Automatically set when a power-on-reset occurs. Cleared by setting the corresponding bit in RSTCLR.

[1] If the software reset bit in RSTSTA is set, any write to RSTCLR that does not clear this bit generates a software reset.

Table 29. Device Reset Implications

RESET	Reset External Pins to Default State	Kernel Executed	Reset All External MMRs (Excluding RSTSTA)	Peripherals Reset	Watchdog Timer Reset	RAM Valid	RSTSTA (Status After Reset Event)
POR	Yes	Yes	Yes	Yes	Yes	Yes/No	RSTSTA[0] = 1
Watchdog	Yes	Yes	Yes	Yes	No	Yes	RSTSTA[1] = 1
Software	Yes	Yes	Yes	Yes	No	Yes	RSTSTA[2] = 1
External Pin	Yes	Yes	Yes	Yes	No	Yes	RSTSTA[3] = 1

OSCILLATOR, PLL, AND POWER CONTROL

Clocking System

The ADuC7060 integrates a 32.768 kHz ±3% oscillator, a clock divider, and a PLL. The PLL locks onto a multiple of the internal oscillator or an external 32.768 kHz crystal to provide a stable 10.24 MHz clock (UCLK) for the system. To allow power saving, the core can operate at this frequency or at binary submultiples of it. The actual core operating frequency, UCLK/2^{CD}, is refered to as HCLK. The default core clock is the PLL clock divided by 8 (CD = 3) or 1.28 MHz.

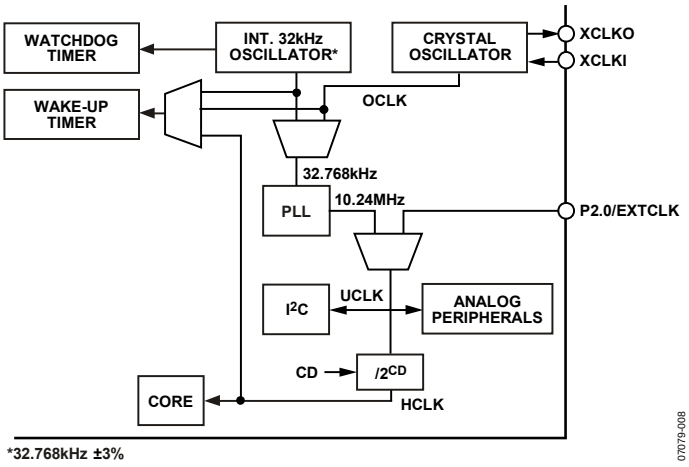


Figure 12. Clocking System

External Crystal Selection

To switch to an external crystal, users must follow this procedure:

1. Enable the Timer1 interrupt and configure it for a timeout period of >120 μs.
2. Follow the write sequence to the PLLCON register, setting the OSEL bits to 1, 0 and clearing the EXTCLK bit.
3. Force the part into nap mode by following the correct write sequence to the POWCON register
4. When the part is interrupted from nap mode by the Timer1 interrupt source, the clock source has switched to the external crystal.

Example source code:

```
T1LD  = 0x80; // 32,768 clock ticks
T1CON = 0xC0; // Periodic mode, enable
              // timer, 32,768 Hz clock/1
IRQEN |= 0x10; // Enable Timer1 interrupt
               // source
PLLKEY1 = 0xAA;  // Switch to external crystal
PLLCON = 0x2;
PLLKEY2 = 0x55;

POWKEY1 = 0x1;   // Enter nap mode
POWCON0 = 0x73;
POWKEY2 = 0xF4;
```

In case of crystal loss, the watchdog timer should be used. During initialization, a test on the RSTSTA can determine if the reset came from the watchdog timer.

External Clock Selection

To switch to an external clock on P2.0, configure P2.0 in Mode 0. The external clock can be up to 20.24 MHz, provided that the tolerance is 1%. The external clock is divided by 2 internally on the part.

Example source code:

```
T1LD  = 0x80;
T1CON = 0xC0;
IRQEN |= 0x10;      // Enable Timer1 interrupt
PLLKEY1 = 0xAA;     // Switch to external clock
PLLCON = 0x4;
PLLKEY2 = 0x55;


POWKEY1 = 0x1;      // Enter NAP mode
POWCON0 = 0x73;
POWKEY2 = 0xF4;
```

The selection of the clock source is in the PLLCON register. By default, the part uses the internal oscillator feeding the PLL.

Power Control System

The core clock frequency is changed by writing to the POWCON0 register. This is a key protected register; therefore, Register POWKEY1 and Register POWKEY2 must be written to immediately before and after configuring the POWCON0 register. The following is a simple example showing how to configure the core clock for 10.24 MHz:

```
POWKEY1 = 0x1;
POWCON0 = 0x78;     //Set core to max CPU
                    //speed of 10.24 MHz
POWKEY2 = 0xF4;
```

A choice of operating modes is available on the ADuC7060. Table 31 describes what part is powered on in the different modes and indicates the power-up time.

Table 32 gives some typical values of the total current consumption (analog + digital supply currents) in the different modes, depending on the clock divider bits. The ADC is turned off. Note that these values also include current consumption of the regulator and other parts on the test board where these values are measured.

Power and Clock Control Registers

Name: POWKEY1

Address: 0xFFFF0404

Default value: 0xXXXX

Access: Write

Function: When writing to POWCON0, the value of 0x01 must be written to this register in the instruction immediately before writing to POWCON0.

Name: POWCON0

Address: 0xFFFF0408

Default value: 0x7B

Access: Read and write

Function: This register controls the clock divide bits controlling the CPU clock (HCLK).

Table 30. POWCON0 MMR Bit Designations

Bit	Name	Description
7	Reserved	This bit must always be set to 0.
6	XPD	XTAL power-down. Cleared by user to power down the external crystal circuitry. Set by user to enable the external crystal circuitry.
5	PLLPD	PLL power-down. Timer peripherals power down if driven from the PLL output clock. Timers driven from an active clock source remain in normal power mode. This bit is cleared to 0 to power down the PLL. The PLL cannot be powered down if either the core or peripherals are enabled; Bit 3, Bit 4, and Bit 5 must be cleared simultaneously. Set by default, and set by hardware on a wake-up event.
4	PPD	Peripherals power-down. The peripherals that are powered down by this bit are as follows: SRAM, Flash/EE memory and GPIO interfaces, and SPI/I²C and UART serial ports. Cleared to power down the peripherals. The peripherals cannot be powered down if the core is enabled; Bit 3 and Bit 4 must be cleared simultaneously. Set by default, and/or by hardware, on a wake-up event. Wake-up timer (Timer1) can remain active.
3	COREPD	Core power-down. If user code powers down the MCU, include a dummy MCU cycle after the power-down command is written to POWCON0. Cleared to power down the ARM core. Set by default and set by hardware on a wake-up event.
2 to 0	CD[2:0]	Core clock depends on CD setting: [000] = 10.24 MHz [001] = 5.12 MHz [010] = 2.56 MHz [011] = 1.28 MHz [default value] [100] = 640 kHz [101] = 320 kHz [110] = 160 kHz [111] = 80 kHz

Table 31. ADuC7060 Power Saving Modes

POWCON0[6:3]	Mode	Core	Peripherals	PLL	XTAL/T2/T3	IRQ0 to IRQ3	Start-Up/Power-On Time
1111	Active	Yes	Yes	Yes	Yes	Yes	130 ms at CD = 0
1110	Pause		Yes	Yes	Yes	Yes	4.8 µs at CD = 0; 660 µs at CD = 7
1100	Nap			Yes	Yes	Yes	4.8 µs at CD = 0; 660 µs at CD = 7
1000	Sleep				Yes	Yes	66 µs at CD = 0; 900 µs at CD = 7
0000	Stop					Yes	66 µs at CD = 0; 900 µs at CD = 7

Table 32. Typical Current Consumption at 25°C in mA [1]

POWCON0[6:3]	Mode	CD = 0	CD = 1	CD = 2	CD = 3	CD = 4	CD = 5	CD = 6	CD = 7
1111	Active[2]	5.22	4.04	2.69	2.01	1.67	1.51	1.42	1.38
1110	Pause[3]	2.6	1.95	1.6	1.49	1.4	1.33	1.31	1.3
1100	Nap[3]	1.33	1.29	1.29	1.29	1.29	1.29	1.29	1.29
1000	Sleep[3]	0.085	0.085	0.085	0.085	0.085	0.085	0.085	0.085
0000	Stop[3]	0.055	0.055	0.055	0.055	0.055	0.055	0.055	0.055

[1] All values listed in Table 32 have been taken with both ADCs turned off.
[2] In active mode, the nTRST pin must be high.
[3] The values for pause, nap, sleep, and stop modes are measured with the nTRST pin low. If nTRST is high in the pause, nap, sleep, and stop modes, add 50 µA to the values in Table 32.

Name: POWKEY2

Address: 0xFFFF040C

Default value: 0xXXXX

Access: Write

Function: When writing to POWCON0, Value 0xF4 must be written to this register in the instruction immediately after writing to POWCON0.

Name: PLLKEY1

Address: 0xFFFF0410

Default value: 0xXXXX

Access: Write

Function: When writing to the PLLCON register, Value 0xAA must be written to this register in the instruction immediately before writing to PLLCON.

Name: PLLCON

Address: 0xFFFF0414

Default value: 0x00

Access: Read and write

Function: This register selects the clock input to the PLL.

Table 33. PLLCON MMR Bit Designations

Bit	Name	Description
7 to 3	Reserved	These bits must always be set to 0.
2	EXTCLK	Set this bit to 1 to select external clock input from P2.0. Clear this bit to disable the external clock.
1 to 0	OSEL	Oscillator selection bits. [00] = internal 32,768 Hz oscillator. [01] = internal 32,768 Hz oscillator. [10] = external crystal. [11] = internal 32,768 Hz oscillator.

Name: PLLKEY2

Address: 0xFFFF0418

Default value: 0xXXXX

Access: Write

Function: When writing to PLLCON, Value 0x55 must be written to this register in the instruction immediately after writing to PLLCON.

ADC CIRCUIT INFORMATION

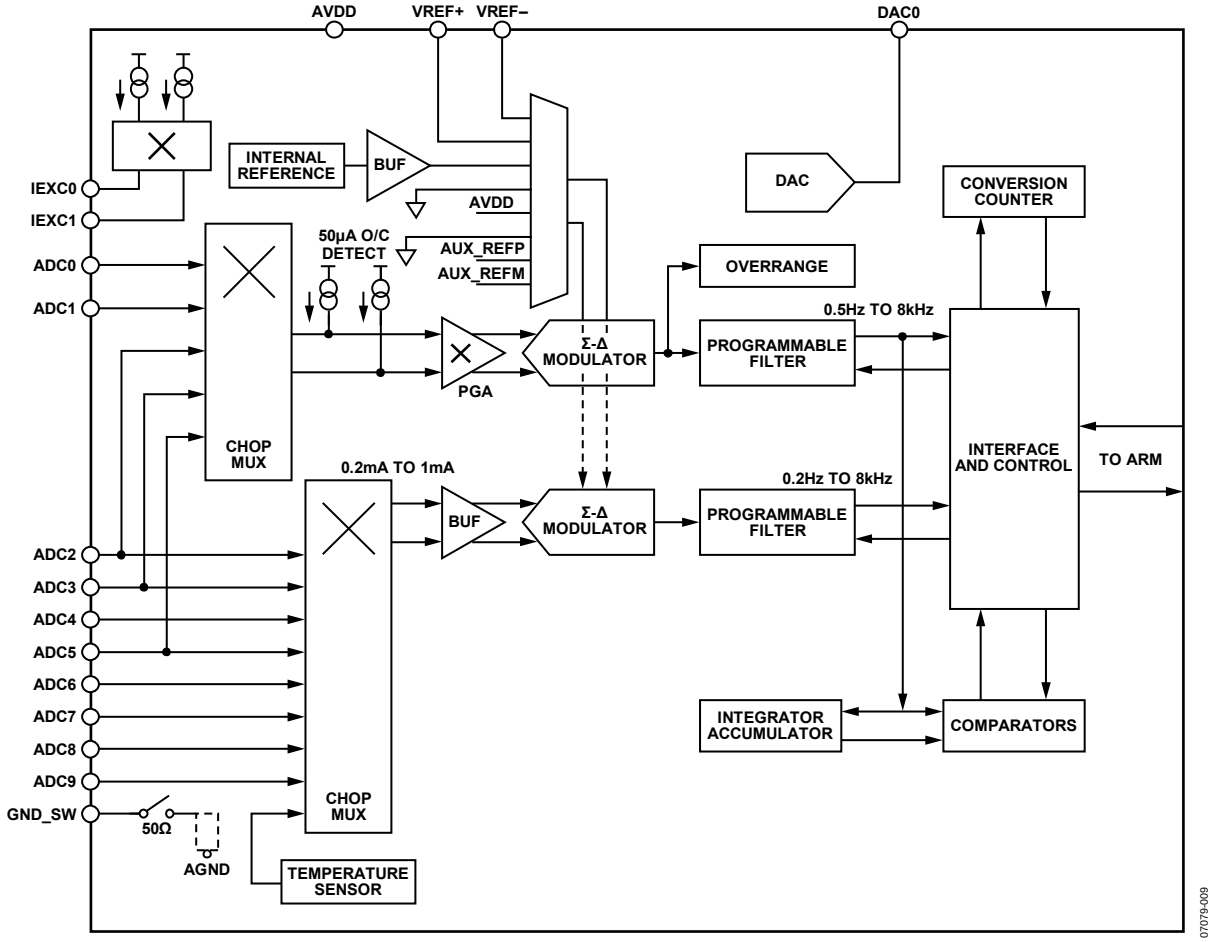


Figure 13. Analog Block Diagram

The ADuC7060 incorporates two independent multichannel Σ-Δ ADCs. The primary ADC is a 24-bit, 5-channel ADC. The auxiliary ADC is a 24-bit Σ-Δ ADC, with up to eight input channels.

The primary ADC input has a mux and a programmable gain amplifier on its input stage. The mux on the primary channel can be configured as two fully differential input channels or as four single-ended input channels.

The auxiliary ADC incorporates a buffer on its input stage. Digital filtering is present on both ADCs, which allows measurement of a wide dynamic range and low frequency signals such as those in pressure sensor, temperature sensor, weigh scale, or strain gage type applications.

The ADuC7060 auxiliary ADC can be configured as four fully differential input channels or as eight single-ended input channels.

Because of internal buffering, the internal channels can convert signals directly from sensors without the need for external signal conditioning.

Table 34. Primary ADC—Typical Output RMS Noise in Normal Mode (μV)

ADC Register Status	Data Update Rate	Input Voltage Noise (mV)									
		±1.2 mV (PGA = 1)	±600 mV (PGA = 2)	±300 mV (PGA = 4)	±150 mV (PGA = 8)	±75 mV (PGA = 16)	±37.5 mV (PGA = 32)	±18.75 mV (PGA = 64)	±9.375 mV (PGA = 128)	±4.68 mV (PGA = 256)	±2.34 mV (PGA = 512)
Chop On	4 Hz	0.62 μV	0.648 μV	0.175 μV	0.109 μV	0.077 μV	0.041 μV	0.032 μV	0.0338 μV	0.032 μV	0.033 μV
Chop Off	50 Hz	1.97 μV	1.89 μV	0.570 μV	0.38 μV	0.27 μV	0.147 μV	0.123 μV	0.12 μV	0.098 μV	0.098 μV
Chop Off	1 kHz	8.54 μV	8.4 μV	2.55 μV	1.6 μV	1.17 μV	0.658 μV	0.53 μV	0.55 μV	0.56 μV	0.52 μV
Chop Off	8 kHz	54.97 μV	55.54 μV	14.30 μV	7.88 μV	4.59 μV	2.5 μV	1.71 μV	1.75 μV	0.915 μV	0.909 μV

Table 35. Primary ADC—Typical Output RMS Effective Number of Bits in Normal Mode (Peak-to-Peak Bits in Parentheses)

ADC Register Status	Data Update Rate	Input Voltage Noise (mV)									
		±1.2 V (PGA = 1)	±600 mV (PGA = 2)	±300 mV (PGA = 4)	±150 mV (PGA = 8)	±75 mV (PGA = 16)	±37.5 mV (PGA = 32)	±18.75 mV (PGA = 64)	±9.375 mV (PGA = 128)	±4.68 mV (PGA = 256)	±2.34 mV (PGA = 512)
Chop On	4 Hz	21.9 (19.1 p-p)	20.8 (18.1 p-p)	21.7 (19.0 p-p)	21.4 (18.7 p-p)	20.9 (18.2 p-p)	20.8 (18.1 p-p)	20.2 (17.4 p-p)	19.1 (16.4 p-p)	18.2 (15.4 p-p)	17.1 (14.4 p-p)
Chop Off	50 Hz	20.2 (17.5 p-p)	19.3 (16.6 p-p)	20.0 (17.3 p-p)	19.6 (16.9 p-p)	19.1 (16.4 p-p)	19.0 (16.2 p-p)	18.2 (15.5 p-p)	17.3 (14.6 p-p)	16.6 (13.8 p-p)	15.5 (12.8 p-p)
Chop Off	1 kHz	18.1 (15.3 p-p)	17.1 (14.4 p-p)	17.8 (15.1 p-p)	17.5 (14.8 p-p)	17.0 (14.2 p-p)	16.8 (14.1 p-p)	16.1 (13.4 p-p)	15.1 (12.3 p-p)	14.0 (11.3 p-p)	13.1 (10.4 p-p)
Chop Off	8 kHz	15.4 (12.7 p-p)	14.4 (11.7 p-p)	15.4 (12.6 p-p)	15.2 (12.5 p-p)	15.0 (12.3 p-p)	14.9 (12.2 p-p)	14.4 (11.7 p-p)	13.4 (10.7 p-p)	13.3 (10.6 p-p)	12.3 (9.6 p-p)

Table 36. Auxilary ADC: Typical Output RMS Noise

ADC Register	Data Update Rate	RMS Value
Chop On	4 Hz	0.633 μV
Chop On	10 Hz	0.810 μV
Chop Off	1 kHz	7.4 μV
Chop Off	8 kHz	54.18 μV

Reference Sources

Both the primary and secondary ADCs have the option of using the internal reference voltage or one of two external differential reference sources. The first external reference is applied to the VREF+/VREF− pins. The second external reference is applied to the ADC4/EXT_REF2IN+ and ADC5/EXT_REF2IN− pins. By default, each ADC uses the internal 1.2 V reference source.

For details on how to configure the external reference source for the primary ADC, see the description of the ADC0REF[1:0] bits in the ADC0 control register, ADC0CON.

For details on how to configure the external reference source for the auxiliary ADC, see the description of the ADC1REF[2:0] bits in the ADC1 control register, ADC1CON.

If an external reference source of greater than 1.35 V is needed for ADC0, the HIGHEXTREF0 bit must be set in ADC0CON.

Similarly, if an external reference source of greater than 1.35 V is used for ADC1, the HIGHEXTREF1 bit must be set in ADC1CON.

Diagnostic Current Sources

To detect a connection failure to an external sensor, the ADuC7060 incorporates a 50 μA constant current source on the selected analog input channels to both the primary and auxiliary ADCs.

The diagnostic current sources for the primary ADC analog inputs are controlled by the ADC0DIAG[1:0] bits in the ADC0CON register.

Similarly, the diagnostic current sources for the auxiliary ADC analog inputs are controlled by the ADC1DIAG[1:0] bits in the ADC0CON register.

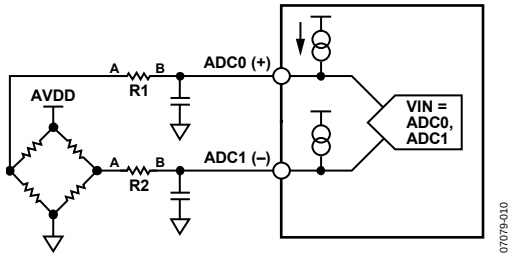


Figure 14. Example Circuit Using Diagnostic Current Sources

Table 37. Example Scenarios for Using Diagnostic Current Sources

Diagnostic Test				
Register Setting	**Description**	**Normal Result**	**Fault Result**	**Detected Measurement for Fault**
ADC0DIAG[1:0] = 0	Convert ADC0/ADC1 as normal with diagnostic currents disabled.	Expected differential result across ADC0/ADC1.	Short circuit.	Primary ADC reading ≈ 0 V regardless of PGA setting.
ADC0DIAG[1:0] = 1	Enable a 50 µA diagnostic current source on ADC0 by setting ADC0DIAG[1:0] = 1. Convert ADC0 and ADC1.	Main ADC changes by ΔV = +50 µA × R1. For example, ~100 mV for R1 = 2 kΩ.	Short circuit between ADC0 and ADC1. Short circuit between R1_a and R1_b.	Primary ADC reading ≈ 0 V regardless of PGA setting.
	Convert ADC0 in single-ended mode with diagnostic currents disabled.	Expected voltage on ADC0.	ADC0 open circuit or R1 open circuit.	Primary ADC reading = +full scale, even on the lowest PGA setting.
ADC0DIAG[1:0] = 3	Enable a 50 µA diagnostic current source on both ADC0 and ADC1 by setting ADC0DIAG[1:0] = 3. Convert ADC0 and ADC1.	Primary ADC changes by ΔV = 50 µA × (R1 − R2); that is, ~10 mV for 10% tolerance.	R1 does not match R2.	Primary ADC reading > 10 mV.

Sinc3 Filter

The number entered into Bits[6:0] of the ADCFLT register sets the decimation factor of the sinc3 filter. See Table 44 and Table 45 for further details on the decimation factor values.

The range of operation of the sinc3 filter (SF) word depends on whether the chop function is enabled. With chopping disabled, the minimum SF word allowed is 3 and the maximum is 127, giving an ADC throughput range of 50 Hz to 2 kHz.

For details on how to calculate the ADC sampling frequency based on the value programmed to the SF[6:0] in the ADCFLT register, refer to Table 44 for more details.

ADC CHOPPING

The ADCs on the ADuC7060 implement a chopping scheme whereby the ADC repeatedly reverses its inputs. Therefore, the decimated digital output values from the sinc3 filter have a positive and negative offset term associated with them. This results in the ADC including a final summing stage that sums and averages each value from the filter with previous filter output values. This new value is then sent to the ADC data MMR. This chopping scheme results in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift and noise rejection are required.

Programmable Gain Amplifier

The primary ADC incorporates an on-chip programmable gain amplifier (PGA). The PGA can be programmed through 10 different settings giving a range of 1 to 512. The gain is controlled by the ADC0PGA[3:0] bits in the ADC0CON MMR.

Excitation Sources

The ADuC7060 contains two matched software configurable current sources. These excitation currents are sourced from AVDD. They are individually configurable to give a current range of 200 µA to 1 mA. The current step sizes are 200 µA. These current sources can be used to excite an external resistive bridge or RTD sensors. The IEXCON MMR controls the excitation current sources. Bit 6 of IEXCON must be set to enable Excitation Current Source 0. Similarly, Bit 7 must be set to enable Excitation Current Source 1. The output current of each current source is controlled by the IOUT[3:0] bits of this register.

It is also possible to configure the excitation current sources to output current to a single output pin, either IEXC0 or IEXC1, by using the IEXC0_DIR and IEXC1_DIR bits of IEXCON. This allows up to 2 mA to output current on a single excitation pin.

ADC Low Power Mode

The ADuC7060 allows the primary and auxiliary ADCs to be placed in low power operating mode. When configured for this mode, the ADC throughput time is reduced, but the power consumption of the primary ADC is reduced by a factor of about 4; the auxiliary ADC power consumption is reduced by a factor of roughly 3. The maximum ADC conversion rate in low power mode is 2 kHz. The operating mode of the ADCs is controlled by the ADCMDE register. This register configures the part for either normal mode (default), low power mode, or low power plus mode. Low power plus mode is the same as low power mode except that the PGA is disabled. To place the ADCs in low power mode, the following steps must be completed:

- ADCMDE[4:3]—Setting these bits enables normal mode, low power mode, or low power plus mode.
- ADCMDE[5]—Setting this bit configures the part for low power mode.
- ADCMDE[7]—Clearing this bit further reduces power consumption by reducing the frequency of the ADC clock.

ADC Comparator and Accumulator

Every primary ADC result can be compared to a preset threshold level (ADC0TH) as configured via ADCCFG[4:3]. An MCU interrupt is generated if the absolute (sign independent) value of the ADC result is greater than the preprogrammed comparator threshold level. An extended function of this comparator function allows user code to configure a threshold counter (ADC0THV) to monitor the number of pimary ADC results that have occurred above or below the preset threshold level. Again, an ADC interrupt is generated when the threshold counter reaches a preset value (ADC0RCR).

Finally, a 32-bit accumulator (ADC0ACC) function can be configured (ADCCFG[6:5]) allowing the primary ADC to add (or subtract) multiple primary ADC sample results. User code can read the accumulated value directly (ADC0ACC) without any further software processing.

TEMPERATURE SENSOR

The ADuC7060 provides a voltage output from an on-chip band gap reference proportional to absolute temperature. This voltage output can also be routed through the front-end auxiliary ADC multiplexer (effectively, an additional ADC channel input), facilitating an internal temperature sensor channel that measures die temperature.

The internal temperature sensor is not designed for use as an absolute ambient temperature calculator. It is intended for use as an approximate indicator of the temperature of the ADuC7060 die.

The typical temperature coefficient is 0.28 mV/°C.

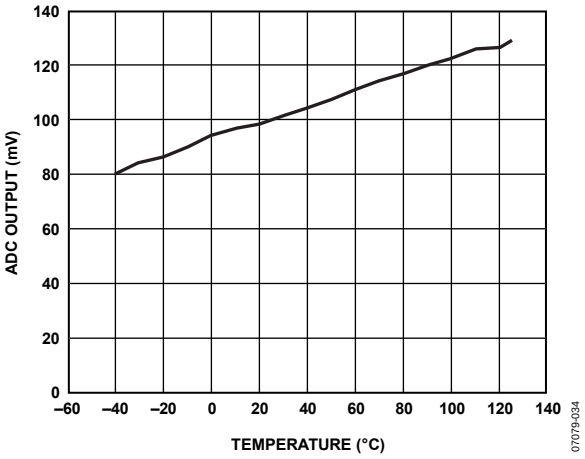


Figure 15. ADC Output vs. Temperature

ADC MMR Interface

The ADCs are controlled and configured through a number of MMRs that are described in detail in the following sections.

In response to an ADC interrupt, user code should interrogate the ADCSTA MMR to determine the source of the interrupt. Each ADC interrupt source can be individually masked via the ADCMSKI MMR described in Table 39.

All primary ADC result ready bits are cleared by a read of the ADC0DAT MMR. If the primary channel ADC is not enabled, all ADC result ready bits are cleared by a read of the ADC1DAT MMR. To ensure that primary ADC and auxiliary ADC conversion data are synchronous, user code should first read the ADC1DAT MMR and then the ADC0DAT MMR. New ADC conversion results are not written to the ADCxDAT MMRs unless the respective ADC result ready bits are first cleared. The only exception to this rule is the data conversion result updates when the ARM core is powered down. In this mode, ADCxDAT registers always contain the most recent ADC conversion result even though the ready bits are not cleared.

ADC Status Register

Name: ADCSTA

Address: 0xFFFF0500

Default value: 0x0000

Access: Read only

Function: This read-only register holds general status information related to the mode of operation or current status of the ADuC7060 ADCs.

Table 38. ADCSTA MMR Bit Designations

Bit	Name	Description
15	ADCCALSTA	ADC calibration status. This bit is set automatically in hardware to indicate that an ADC calibration cycle has been completed. This bit is cleared after ADCMDE is written to.
14		Not used. This bit is reserved for future functionality
13	ADC1CERR	Auxiliary ADC conversion error. This bit is set automatically in hardware to indicate that an auxiliary ADC conversion overrange or underrange has occurred. The conversion result is clamped to negative full scale (underrange error) or positive full scale (overrange error) in this case. This bit is cleared when a valid (in-range) voltage conversion result is written to the ADC1DAT register.
12	ADC0CERR	Primary ADC conversion error. This bit is set automatically in hardware to indicate that a primary ADC conversion overrange or underrange has occurred. The conversion result is clamped to negative full scale (underrange error) or positive full scale (overrange error) in this case. This bit is cleared when a valid (in-range) conversion result is written to the ADC0DAT register.
11 to 7		Not used. These bits are reserved for future functionality and should not be monitored by user code.
6	ADC0ATHEX	ADC0 accumulator comparator threshold exceeded. This bit is set when the ADC0 accumulator value in ADC0ACC exceeds the threshold value programmed in the ADC0 comparator threshold register, ADCOATH. This bit is cleared when the value in ADC0ATH does not exceed the value in ADC0ATH.
5		Not used. This bit is reserved for future functionality and should not be monitored by user code.
4	ADC0THEX	Primary channel ADC comparator threshold. This bit is valid only if the primary channel ADC comparator is enabled via the ADCCFG MMR. This bit is set by hardware if the absolute value of the primary ADC conversion result exceeds the value written in the ADC0TH MMR. If the ADC threshold counter is used (ADC0RCR), this bit is set only when the specified number of primary ADC conversions equals the value in the ADC0THV MMR. Otherwise, this bit is clear.
3	ADC0OVR	Primary channel ADC overrange bit. If the overrange detect function is enabled via the ADCCFG MMR, this bit is set by hardware if the primary ADC input is grossly (>30% approximate) overrange. This bit is updated every 125 µs. After it is set, this bit can be cleared only by software when ADCCFG[2] is cleared to disable the function, or the ADC gain is changed via the ADC0CON MMR.
2		Not used. These bits are reserved for future functionality and should not be monitored by user code.
1	ADC1RDY	Auxiliary ADC result ready bit. If the auxiliary channel ADC is enabled, this bit is set by hardware as soon as a valid conversion result is written in the ADC1DAT MMR. It is also set at the end of a calibration sequence. This bit is cleared by reading ADC1DAT followed by reading ADC0DAT. ADC0DAT must be read to clear this bit, even if the primary ADC is not enabled.
0	ADC0RDY	Primary ADC result ready bit. If the primary channel ADC is enabled, this bit is set by hardware as soon as a valid conversion result is written in the ADC0DAT MMR. It is also set at the end of a calibration sequence. This bit is cleared by reading ADC0DAT.

ADC Interrupt Mask Register

Name: ADCMSKI

Address: 0xFFFF0504

Default value: 0x0000

Access: Read and write

Function: This register allows the ADC interrupt sources to be enabled individually. The bit positions in this register are the same as the lower eight bits in the ADCSTA MMR. If a bit is set by user code to 1, the respective interrupt is enabled. By default, all bits are 0, meaning all ADC interrupt sources are disabled.

Table 39. ADCMSKI MMR Bit Designations

Bit	Name	Description
7		Not used. These bits are reserved for future functionality and should not be monitored by user code.
6	ADC0ATHEX_INTEN	ADC0 accumulator comparator threshold exceeded interrupt enable bit. When set to 1, this bit enables an interrupt when the ADC0ATHEX bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
5		Not used. These bits are reserved for future functionality and should not be monitored by user code.
4	ADC0THEX_INTEN	Primary channel ADC comparator threshold exceeded interrupt enable bit. When set to 1, this bit enables an interrupt when the ADC0THEX bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
3	ADC0OVR_INTEN	When set to 1, this bit enables an interrupt when the ADC0OVR bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
2		Not used. These bits are reserved for future functionality and should not be monitored by user code.
1	ADC1RDY_INTEN	Auxiliary ADC result ready bit. When set to 1, this bit enables an interrupt when the ADC1RDY bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
0	ADC0RDY_INTEN	Primary ADC result ready bit. When set to 1, this bit enables an interrupt when the ADC0RDY bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.

ADC Mode Register

Name: ADCMDE

Address: 0xFFFF0508

Default value: 0x03

Access: Read and write

Function: The ADC mode MMR is an 8-bit register that configures the mode of operation of the ADC subsystem.

Table 40. ADCMDE MMR Bit Designations

Bit	Name	Description
7	ADCCLKSEL	Set this bit to 1 to enable ADCCLK = 4 MHz. This bit should be set for normal ADC operation. Clear this bit to enable ADCCLK = 131 kHz. This bit should be cleared for low power ADC operation.
6		Not used. These bits are reserved for future functionality and should not be monitored by user code.
5	ADCLPMEN	Enable low power mode. This bit has no effect if ADCMDE[4:3] = 00. This bit must be set to 1 in low power mode. Clearing this bit in low power mode results in erratic ADC results. This bit has no effect if the ADC is in normal mode.

Bit	Name	Description
4 to 3	ADCLPMCFG[1:0]	ADC power mode configuration. 0, 0 = ADC normal mode. If enabled, the ADC operates with normal current consumption yielding optimum electrical performance. 0, 1 = ADC low power mode. 1, 0 = ADC normal mode, same as [0, 0]. 1, 1 = ADC low power plus mode (low power mode and PGA off).
2 to 0	ADCMD[2:0]	ADC operation mode configuration. 0, 0, 0 = ADC power-down mode. All ADC circuits and the input amplifier are powered down. 0, 0, 1 = ADC continuous conversion mode. In this mode, any enabled ADC continuously converts at a frequency equal to f_{ADC}. ADCxRDY must be cleared to enable new data to be written to ADC0DAT/ADC1DAT 0, 1, 0 = ADC single conversion mode. In this mode, any enabled ADC performs a single conversion. The ADC enters idle mode when the single shot conversion is complete. A single conversion takes two to three ADC clock cycles depending on the chop mode. 0, 1, 1 = ADC idle mode. In this mode, the ADC is fully powered on but is held in reset. The part enters this mode after calibration. 1, 0, 0 = ADC self-offset calibration. In this mode, an offset calibration is performed on any enabled ADC using an internally generated 0 V. The calibration is carried out at the user-programmed ADC settings; therefore, as with a normal single ADC conversion, it takes two to three ADC conversion cycles before a fully settled calibration result is ready. The calibration result is automatically written to the ADCxOF MMR of the respective ADC. The ADC returns to idle mode, and the calibration and conversion ready status bits are set at the end of an offset calibration cycle. Note: Always use ADC0 for single-ended self-calibration cycles on the primary ADC. Always use ADC0/ADC1 when self-calibrating for a differential input to the primary ADC.
		1, 0, 1 = ADC self-gain calibration. In this mode, a gain calibration against an internal reference voltage is performed on all enabled ADCs. A gain calibration is a two-stage process and takes twice the time of an offset calibration. The calibration result is automatically written to the ADCxGN MMR of the respective ADC. The ADC returns to idle mode and the calibration and conversion ready status bits are set at the end of a gain calibration cycle. An ADC self-gain calibration should only be carried out on the primary channel ADC. Note that self-gain calibration only works when the gain = 1; do not use it when the gain > 1. 1, 1, 0 = ADC system zero-scale calibration. In this mode, a zero-scale calibration is performed on enabled ADC channels against an external zero-scale voltage driven at the ADC input pins. To do this, short the channel externally. 1, 1, 1 = ADC system full-scale calibration. In this mode, a full-scale calibration is performed on enabled ADC channels against an external full-scale voltage driven at the ADC input pins. The ADCxGN register is updated after a full-scale calibration sequence.

Primary ADC Control Register

Name: ADC0CON

Address: 0xFFFF050C

Default value: 0x8000

Access: Read and write

Function: The primary channel ADC control MMR is a 16-bit register. If the primary ADC is reconfigured via ADC0CON, the auxiliary ADC is also reset.

Table 41. ADC0CON MMR Bit Designations

Bit	Name	Description
15	ADC0EN	Primary channel ADC enable. This bit is set to 1 by user code to enable the primary ADC. Clearing this bit to 0 powers down the primary ADC and resets the respective ADC ready bit in the ADCSTA MMR to 0.
14:13	ADC0DIAG[1:0]	Diagnostic current source enable bits. 0, 0 = current sources off. 0, 1 = enables a 50 µA current source on selected positive input (for example, ADC0). 1, 0 = enables a 50 µA current source on selected negative input (for example, ADC1). 1, 1 = enables a 50 µA current source on both selected inputs (for example, ADC0 and ADC1).
12	HIGHEXTREF0	This bit must be set high if the external reference for ADC0 exceeds 1.35 V. Clear this bit when using the internal reference or an external reference of less than 1.35 V.
11	AMP_CM	This bit is set to 1 by user to set the PGA output common-mode voltage to AVDD/2. This bit is cleared to 0 by user code to set the PGA output common-mode voltage to the PGA input common-mode voltage level.
10	ADC0CODE	Primary channel ADC output coding. This bit is set to 1 by user code to configure primary ADC output coding as unipolar. This bit is cleared to 0 by user code to configure primary ADC output coding as twos complement.
9:6	ADC0CH[3:0]	Primary channel ADC input select. [0000] = ADC0/ADC1 (differential mode). [0001] = ADC0/ADC5 (single-ended mode). [0010] = ADC1/ADC5 (single-ended mode). [0011] = VREF+, VREF−. Note: This is the reference selected by the ADC0REF bits. [0100] = Not used. This bit combination is reserved for future functionality and should not be written. [0101] = ADC2/ADC3 (differential mode). [0110] = ADC2/ADC5 (single-ended mode). [0111] = ADC3/ADC5 (single-ended mode). [1000] = internal short to ADC0. [1001] = internal short to ADC1.
5:4	ADC0REF[1:0]	Primary channel ADC reference select. 0, 0 = internal reference selected. In ADC low power mode, the voltage reference selection is controlled by ADCMODE[5]. 0, 1 = external reference inputs (VREF+, VREF−) selected. Set the HIGHEXTREF0 bit if the reference voltage exceeds 1.3 V. 1, 0 = auxiliary external reference inputs (ADC4/EXT_REF2IN+, ADC5/EXT_REF2IN−) selected. Set the HIGHEXTREF0 bit if the reference voltage exceeds 1.3 V. 1, 1 = (AVDD, AGND) divide-by-two selected.
3:0	ADC0PGA[3:0].	Primary channel ADC gain select. Note, nominal primary ADC full-scale input voltage = (VREF/gain). 0, 0, 0, 0 = ADC0 gain of 1. Buffer is active. 0, 0, 0, 1 = ADC0 gain of 2. 0, 0, 1, 0 = ADC0 gain of 4 (default value). Enables the in-amp. 0, 0, 1, 1 = ADC0 gain of 8. 0, 1, 0, 0 = ADC0 gain of 16. 0, 1, 0, 1 = ADC0 gain of 32. 0, 1, 1, 0 = ADC0 gain of 64 (maximum PGIA gain setting). 0, 1, 1, 1 = ADC0 gain of 128 (extra gain implemented digitally). 1, 0, 0, 0 = ADC0 gain of 256. 1, 0, 0, 1 = ADC0 gain of 512. 1, x, x, x = ADC0 gain is undefined.

Auxiliary ADC Control Register

Name: ADC1CON

Address: 0xFFFF0510

Default value: 0x0000

Access: Read and write

Function: The auxiliary ADC control MMR is a 16-bit register.

Table 42. ADC1CON MMR Bit Designations

Bit	Name	Description
15	ADC1EN	Auxiliary channel ADC enable. This bit is set to 1 by user code to enable the auxiliary ADC. Clearing this bit to 0 powers down the auxiliary ADC.
14:13	ADC1DIAG[1:0]	Diagnostic current source enable bits. This is the same current source as that used on ADC0DIAG[1:0]. The ADCs cannot enable the diagnostic current sources at the same time. 0, 0 = current sources off. 0, 1 = enables a 50 µA current source on selected positive input (for example, ADC2). 1, 0 = enables a 50 µ A current source on selected negative input (for example, ADC3). 1, 1 = enables a 50 µ A current source on both selected inputs (for example, ADC2 and ADC3).
12	HIGHEXTREF1	This bit must be set high if the external reference for ADC0 exceeds 1.35 V. Clear this bit when using the internal reference or an external reference of less than 1.35 V.
11	ADC1CODE	Auxiliary channel ADC output coding. This bit is set to 1 by user code to configure auxiliary ADC output coding as unipolar. This bit is cleared to 0 by user code to configure auxiliary ADC output coding as twos complement.
10:7	ADC1CH[3:0]	Auxiliary Channel ADC input select. Note: Single-ended channels are selected with respect to ADC5. Bias ADC5 to a minimum level of 0.1 V. [0000] = ADC2/ADC3 (differential mode). [0001] = ADC4/ADC5 (differential mode). [0010] = ADC6/ADC7 (differential mode). [0011] = ADC8/ADC9 (differential mode). [0100] = ADC2/ADC5 (single-ended mode). [0101] = ADC3/ADC5 (single-ended mode). [0110] = ADC4/ADC5 (single-ended mode). [0111] = ADC6/ADC5 (single-ended mode). [1000] = ADC7/ADC5 (single-ended mode). [1001] = ADC8/ADC5 (single-ended mode). [1010] = ADC9/ADC5 (single-ended mode). [1011] = internal temperature sensor+/internal temperature sensor−. [1100] = VREF+, VREF−. Note: This is the reference selected by the ADC1REF bits. [1101] = DAC_OUT/AGND. [1110] = Undefined. [1111] = Internal short to ADC3.

Bit	Name	Description
6:4	ADC1REF[2:0]	Auxiliary channel ADC reference select. [000] = internal reference selected. In ADC low power mode, the voltage reference selection is controlled by ADCMODE[5]. [001] = external reference inputs (VREF+, VREF−) selected. Set the HIGHEXTREF1 bit if reference voltage exceeds 1.3 V. [010] = auxiliary external reference inputs (ADC4/EXT_REF2IN+, ADC5/EXT_REF2IN−) selected. Set the HIGHEXTREF1 bit if reference voltage exceeds 1.35 V. [011] = (AVDD, AGND) divide-by-two selected. If this configuration is selected, the HIGHEXTREF1 bit is set automatically. [100] = (AVDD, ADC3). ADC3 can be used as the negative input terminal for the reference source. [101] to [111] = reserved.
3:	BUF_BYPASS[1:0]	Buffer bypass. [00] = full buffer on. Both positive and negative buffer inputs active. [01] = negative buffer is bypassed, positive buffer is on. [10] = negative buffer is on, positive buffer is bypassed. [11] = full buffer bypass. Both positive and negative buffer inputs are off.
1:0		Digital gain. Select for auxiliary ADC inputs. [00] = ADC1 gain = 1. [01] = ADC1 gain = 2. [10] = ADC1 gain = 4. [11] = ADC1 gain = 8.

ADC Filter Register

Name: ADCFLT

Address: 0xFFFF0514

Default value: 0x0007

Access: Read and write

Function: The ADC filter MMR is a 16-bit register that controls the speed and resolution of both the on-chip ADCs. Note that, if ADCFLT is modified, the primary and auxiliary ADCs are reset.

Table 43. ADCFLT MMR Bit Designations

Bit	Name	Description
15	CHOPEN	Chop enable. Set by user to enable system chopping of all active ADCs. When this bit is set, the ADC has very low offset errors and drift, but the ADC output rate is reduced by a factor of three if AF = 0 (see sinc3 decimation factor, Bits[6:0] in this table). If AF > 0, then the ADC output update rate is the same with chop on or off. When chop is enabled, the settling time is two output periods.
14	RAVG2	Running average-by-2 enable bit. Set by user to enable a running-average-by-2 function, reducing ADC noise. This function is automatically enabled when chopping is active. It is an optional feature when chopping is inactive, and if enabled (when chopping is inactive), does not reduce the ADC output rate but does increase the settling time by one conversion period. Cleared by user to disable the running average function.
13 to 8	AF[5:0]	Averaging factor (AF). The values written to these bits are used to implement a programmable first-order sinc3 post filter. The averaging factor can further reduce ADC noise at the expense of output rate as described in Bits[6:0] sinc3 decimation factor in this table.

Bit	Name	Description
7	NOTCH2	Sinc3 modify. Set by user to modify the standard sinc3 frequency response to increase the filter stop band rejection by approximately 5 dB. This is achieved by inserting a second notch (NOTCH2) at $f_{NOTCH2} = 1.333 \times f_{NOTCH}$ where f_{NOTCH} is the location of the first notch in the response.
6 to 0	SF[6:0]	Sinc3 decimation factor (SF)[1].The value (SF) written in these bits controls the oversampling (decimation factor) of the sinc3 filter. The output rate from the sinc3 filter is given by $f_{ADC} = (512{,}000/([SF+1] \times 64))$ Hz[2] when the chop bit (Bit 15, chop enable) = 0 and the averaging factor (AF) = 0. This is valid for all SF values ≤ 125. For SF = 126, f_{ADC} is forced to 60 Hz. For SF = 127, f_{ADC} is forced to 50 Hz. For information on calculating the f_{ADC} for SF (other than 126 and 127) and AF values, refer to Table 44.

[1] Due to limitations on the digital filter internal data path, there are some limitations on the combinations of the sinc3 decimation factor (SF) and averaging factor (AF) that can be used to generate a required ADC output rate. This restriction limits the minimum ADC update in normal power mode to 4 Hz or 1 Hz in lower power mode.
[2] In low power mode and low power plus mode, the ADC is driven directly by the low power oscillator (131 kHz) and not 512 kHz. All f_{ADC} calculations should be divided by 4 (approximately).

Table 44. ADC Conversion Rates and Settling Times

Chop Enabled	Averaging Factor	Running Average	f_{ADC} Normal Mode	f_{ADC} Low Power Mode	$t_{SETTLING}$[1]
No	No	No	$\frac{512{,}000}{[SF+1]\times 64}$	$\frac{131{,}072}{[SF+1]\times 64}$	$\frac{3}{f_{ADC}}$
No	No	Yes	$\frac{512{,}000}{[SF+1]\times 64}$	$\frac{131{,}072}{[SF+1]\times 64}$	$\frac{4}{f_{ADC}}$
No	Yes	No	$\frac{512{,}000}{[SF+1]\times 64\times[3+AF]}$	$\frac{131{,}072}{[SF+1]\times 64\times[3+AF]}$	$\frac{1}{f_{ADC}}$
No	Yes	Yes	$\frac{512{,}000}{[SF+1]\times 64\times[3+AF]}$	$\frac{131{,}072}{[SF+1]\times 64\times[3+AF]}$	$\frac{2}{f_{ADC}}$
Yes	N/A	N/A	$\frac{512{,}000}{[SF+1]\times 64\times[3+AF]+3}$	$\frac{131{,}072}{[SF+1]\times 64\times[3+AF]+3}$	$\frac{2}{f_{ADC}}$

[1] An additional time of approximately 60 µs per ADC is required before the first ADC is available.

Table 45. Allowable Combinations of SF and AF

	AF Range		
SF	**0**	**1 to 7**	**8 to 63**
0 to 31	Yes	Yes	Yes
32 to 63	Yes	Yes	No
64 to 127	Yes	No	No

ADC Configuration Register

Name: ADCCFG

Address: 0xFFFF0518

Default value: 0x00

Access: Read and write

Function: The 8-bit ADC configuration MMR controls extended functionality related to the on-chip ADCs.

Table 46. ADCCFG MMR Bit Designations

Bit	Name	Description
7	GNDSW_EN	Analog ground switch enable. This bit is set to 1 by user software to connect the external GND_SW pin to an internal analog ground reference point. This bit can be used to connect and disconnect external circuits and components to ground under program control and thereby minimize dc current consumption when the external circuit or component is not being used. This bit is used in conjunction with ADCCFG[1] to select a 20 kΩ resistor to ground. When this bit is cleared, the analog ground switch is disconnected from the external pin.
6:5	ADC0ACCEN[1:0]	Primary channel (32-bit) accumulator enable. [00] = accumulator disabled and reset to 0. The accumulator must be disabled for a full ADC conversion (ADCSTA[0] set twice) before the accumulator can be re-enabled to ensure that the accumulator is reset. [01] = accumulator active. Positive current values are added to the accumulator total; the accumulator can overflow if allowed to run for >65,535 conversions. Negative current values are subtracted from the accumulator total; the accumulator is clamped to a minimum value of 0. [10] = accumulator active. Same as [01] except there is no clamp. Positive current values are added to the accumulator total; the accumulator can overflow if allowed to run for >65,535 conversions. The absolute values of negative current are subtracted from the accumulator total; the accumulator in this mode continues to accumulate negatively, below 0. [11] = accumulator and comparator active. This causes an ADC0 interrupt if ADCMSKI[6] is set.
4:3	ADC0CMPEN[1:0]	Primary ADC comparator enable bit. [00] = comparator disabled. [01] = comparator active. Interrupt asserted if absolute value of ADC0 conversion result |I| ≥ ADC0TH. [10] = comparator count mode active. Interrupt asserted if absolute value of ADC0 conversion result |I| ≥ ADC0TH for the number of ADC0THC conversions. A conversion value |I| < ADC0TH resets the threshold counter value (ADC0THV) to 0. [11] = comparator count mode active, interrupt asserted if absolute value of ADC0 conversion result |I| ≥ ADC0TH for the number of ADC0THC conversions. A conversion value |I| < ADC0TH decrements the threshold counter value (ADC0THV) toward 0.
2	ADC0OREN	ADC0 overrange enable. Set by user to enable a coarse comparator on the primary channel ADC. If the reading is grossly (>30% approximate) overrange for the active gain setting, then the overrange bit in the ADCSTA MMR is set. The ADC reading must be outside this range for greater than 125 µs for the flag to be set. Do not use this feature in ADC low power mode.
1	GNDSW_RES_EN	Set to 1 to enable a 20 kΩ resistor in series with the ground switch. Clear this bit to disable this resistor.
0	ADCRCEN	ADC result counter enable. Set by user to enable the result count mode. ADC interrupts occur if ADC0RCR = ADC0RCV. Cleared to disable the result counter. ADC interrupts occur after every conversion.

Primary Channel ADC Data Register

Name: ADC0DAT

Address: 0xFFFF051C

Default value: 0x00000000

Access: Read only

Function: This ADC data MMR holds the 24-/16-bit conversion result from the primary ADC. The ADC does not update this MMR if the ADC0 conversion result ready bit (ADCSTA[0]) is set. A read of this MMR by the MCU clears all asserted ready flags (ADCSTA[2:0]).

Table 47. ADC0DAT MMR Bit Designations

Bits	Description
23 to 0	ADC0 24-bit/16-bit conversion result

Auxiliary Channel ADC Data Register

Name: ADC1DAT

Address: 0xFFFF0520

Default value: 0x00000000

Access: Read only

Function: This ADC data MMR holds the 24-bit conversion result from the auxiliary ADC. The ADC does not update this MMR if the ADC0 conversion result ready bit (ADCSTA[1]) is set. A read of this MMR by the MCU clears all asserted ready flags (ADCSTA[2:1]).

Table 48. ADC1DAT MMR Bit Designations

Bits	Description
23 to 0	ADC1 24-bit conversion result

Primary Channel ADC Offset Calibration Register

Name: ADC0OF

Address: 0xFFFF0524

Default value: Part specific, factory programmed

Access: Read and write

Function: This ADC offset MMR holds a 16-bit offset calibration coefficient for the primary ADC. The register is configured at power-on with a factory default value. However, this register automatically overwrites if an offset calibration of the primary ADC is initiated by the user via bits in the ADCMDE MMR. User code can write to this calibration register only if the ADC is in idle mode. An ADC must be enabled and in idle mode before being written to any offset or gain register. The ADC must be in idle mode for at least 23 μs.

Table 49. ADC0OF MMR Bit Designations

Bits	Description
15 to 0	ADC0 16-bit calibration offset value

Auxiliary Channel ADC Offset Calibration Register

Name: ADC1OF

Address: 0xFFFF0528

Default value: Part specific, factory programmed

Access: Read and write

Function: This offset MMR holds a 16-bit offset calibration coefficient for the auxiliary channel. The register is configured at power-on with a factory default value. However, this register is automatically overwritten if an offset calibration of the auxiliary channel is initiated by the user via bits in the ADCMDE MMR. User code can write to this calibration register only if the ADC is in idle mode. An ADC must be enabled and in idle mode before being written to any offset or gain register. The ADC must be in idle mode for at least 23 μs.

Table 50. ADC1OF MMR Bit Designations

Bits	Description
15 to 0	ADC1 16-bit calibration offset value.

Primary Channel ADC Gain Calibration Register

Name: ADC0GN

Address: 0xFFFF052C

Default value: Part specific, factory programmed

Access: Read and write

Function: This gain MMR holds a 16-bit gain calibration coefficient for scaling the primary ADC conversion result. The register is configured at power-on with a factory default value. However, this register is automatically overwritten if a gain calibration of the primary ADC is initiated by the user via bits in the ADCMDE MMR. User code can write to this calibration register only if the ADC is in idle mode. An ADC must be enabled and in idle mode before being written to any offset or gain register. The ADC must be in idle mode for at least 23 μs.

Table 51. ADC0GN MMR Bit Designations

Bits	Description
15 to 0	ADC0 16-bit calibration gain value.

Auxiliary Channel Gain Calibration Register

Name: ADC1GN

Address: 0xFFFF0530

Default value: Part specific, factory programmed

Access: Read and write

Function: This gain MMR holds a 16-bit gain calibration coefficient for scaling an auxiliary channel conversion result. The register is configured at power-on with a factory default value. However, this register is automatically overwritten if a gain calibration of the auxiliary channel is initiated by the user via bits in the ADCMDE MMR. User code can only write to this calibration register if the ADC is in idle mode. An ADC must be enabled and in idle mode before being written to any offset or gain register. The ADC must be in idle mode for at least 23 μs.

Table 52. ADC1GN MMR Bit Designations

Bits	Description
15 to 0	ADC1 16-bit calibration gain value.

Primary Channel ADC Result Counter Limit Register

Name: ADC0RCR

Address: 0xFFFF0534

Default value: 0x0001

Access: Read and write

Function: This 16-bit MMR sets the number of conversions required before an ADC interrupt is generated. By default, this register is set to 0x01. The ADC counter function must be enabled via the ADC result counter enable bit in the ADCCFG MMR.

Table 53. ADC0RCR MMR Bit Designations

Bits	Description
15 to 0	ADC0 result counter limit/reload register.

Primary Channel ADC Result Count Register

Name: ADC0RCV

Address: 0xFFFF0538

Default value: 0x0000

Access: Read only

Function: This 16-bit, read-only MMR holds the current number of primary ADC conversion results. It is used in conjunction with ADC0RCR to mask primary channel ADC interrupts, generating a lower interrupt rate. When ADC0RCV = ADC0RCR, the value in ADC0RCV resets to 0 and recommences counting. It can also be used in conjunction with the accumulator (ADC0ACC) to allow an average calculation to be undertaken. The result counter is enabled via ADCCFG[0]. This MMR is also reset to 0 when the primary ADC is reconfigured, that is, when the ADC0CON or ADCMDE is written.

Table 54. ADC0RCV MMR Bit Designations

Bits	Description
15 to 0	ADC0 result counter register.

Primary Channel ADC Threshold Register

Name: ADC0TH

Address: 0xFFFF053C

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR sets the threshold against which the absolute value of the primary ADC conversion result is compared. In unipolar mode, ADC0TH[15:0] are compared, and in twos complement mode, ADC0TH[14:0] are compared.

Table 55. ADC0TH MMR Bit Designations

Bits	Description
15 to 0	ADC0 16-bit comparator threshold register.

Primary Channel ADC Threshold Count Limit Register

Name: ADC0THC

Address: 0xFFFF0540

Default value: 0x0001

Access: Read and write

Function: This 8-bit MMR determines how many cumulative (values below the threshold decrement or reset the count to 0) primary ADC conversion result readings above ADC0TH must occur before the primary ADC comparator threshold bit is set in the ADCSTA MMR generating an ADC interrupt. The primary ADC comparator threshold bit is asserted as soon as the ADC0THV = ADC0RCR.

Table 56. ADC0THC MMR Bit Designations

Bits	Description
7 to 0	ADC0 8-bit threshold counter limit register.

Primary Channel ADC Threshold Count Register

Name: ADC0THV

Address: 0xFFFF0544

Default value: 0x0000

Access: Read only

Function: This 8-bit MMR is incremented every time the absolute value of a primary ADC conversion result |Result| ≥ ADC0TH. This register is decremented or reset to 0 every time the absolute value of a primary ADC conversion result |Result| < ADC0TH. The configuration of this function is enabled via the primary channel ADC comparator bits in the ADCCFG MMR.

Table 57. ADC0THV MMR Bit Designations

Bits	Description
7 to 0	ADC0 8-bit threshold exceeded counter register.

Primary Channel ADC Accumulator Register

Name: ADC0ACC

Address: 0xFFFF0548

Default value: 0x00000000

Access: Read only

Function: This 32-bit MMR holds the primary ADC accumulator value. The primary ADC ready bit in the ADCSTA MMR should be used to determine when it is safe to read this MMR. The MMR value is reset to 0 by disabling the accumulator in the ADCCFG MMR or reconfiguring the primary channel ADC.

Table 58. ADC0ACC MMR Bit Designations

Bits	Description
31 to 0	ADC0 32-bit threshold exceeded counter register.

Table 59. ADC0ATH MMR Bit Designations

Bits	Description
31 to 0	ADC0 32-bit comparator threshold register of the accumulator.

Primary Channel ADC Comparator Threshold Register

Name: ADC0ATH

Address: 0xFFFF054C

Default value: 0x00000000

Access: Read and write

Function: This 32-bit MMR holds the threshold value for the accumulator comparator of the primary channel. When the accumulator value in ADC0ACC exceeds the value in ADC0ATH, the ADC0ATHEX bit in ADCSTA is set. This causes an interrupt if the corresponding bit in ADCMSKI is also enabled.

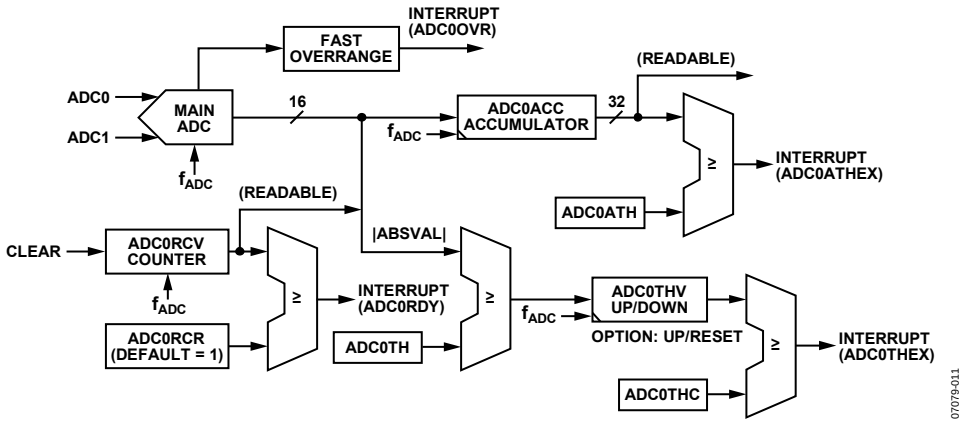


Figure 16. Primary ADC Accumulator/Comparator/Counter Block Diagram

Excitation Current Sources Control Register

Name: IEXCON

Address: 0xFFFF0570

Default value: 0x00

Access: Read and write

Function: This 8-bit MMR controls the two excitation current sources, IEXC0 and IEXC1.

Table 60. IEXCON MMR Bit Designations

Bits	Name	Description
7	IEXC1_EN	Enable bit for IEXC1 current source. Set this bit = 1 to enable Excitation Current Source 1. Clear this bit to disable Excitation Current Source 1.
6	IEXC0_EN	Enable bit for IEXC0 current source. Set this bit = 1 to enable Excitation Current Source 0. Clear this bit to disable Excitation Current Source 0.
5	IEXC1_DIR	Set this bit = 1 to direct Excitation Current Source 1 to the IEXC0 pin. Set this bit = 0 to direct Excitation Current Source 1 to the IEXC1 pin.
4	IEXC0_DIR	Set this bit = 1 to direct Excitation Current Source 0 to the IEXC1 pin. Set this bit = 0 to direct Excitation Current Source 0 to the IEXC0 pin.
3:1	IOUT[3:1]	These bits control the excitation current level for each source. IOUT[3:1] = 000, excitation current = 0 μA + (IOUT[0] × 10 μA). IOUT[3:1] = 001, excitation current = 200 μA + (IOUT[0] × 10 μA). IOUT[3:1] = 010, excitation current = 400 μA+ (IOUT[0] × 10 μA). IOUT[3:1] = 011, excitation current = 600 μA+ (IOUT[0] × 10 μA). IOUT[3:1] = 100, excitation current = 800 μA+ (IOUT[0] × 10 μA). IOUT[3:1] = 101, excitation current = 1 mA + (IOUT[0] × 10 μA). All other values are undefined.
0	IOUT[0]	Set this bit = 1 to enable 10 μA diagnostic current source. Clear this bit = 0 to disable 10 μA diagnostic current source.

EXAMPLE APPLICATION CIRCUITS

Figure 17 shows a simple bridge sensor interface to the ADuC7060, including the RC filters on the analog input channels. Notice that the sense lines from the bridge (connecting to the reference inputs) are wired separately from the excitation lines (going to DVDD/AVDD and ground). This results in a total of six wires going to the bridge. This 6-wire connection scheme is a feature of most off-the-shelf bridge transducers (such as load cells) that helps to minimize errors that would otherwise result from wire impedances.

In Figure 18, AD592 is an external temperature sensor used to measure the thermocouple cold junction, and its output is connected to the auxiliary channel. ADR280 is an external 1.2 V reference part—alternatively, the internal reference can be used. Here, the thermocouple is connected to the primary ADC as a differential input to ADC0/ADC1. Note the resistor between VREF+ and ADC1 to bias the ADC inputs above 100 mV.

Figure 19 shows a simple 4-wire RTD interface circuit. As with the bridge transducer implementation in Figure 17, if a power supply and a serial connection to the outside world are added, then Figure 19 represents a complete system.

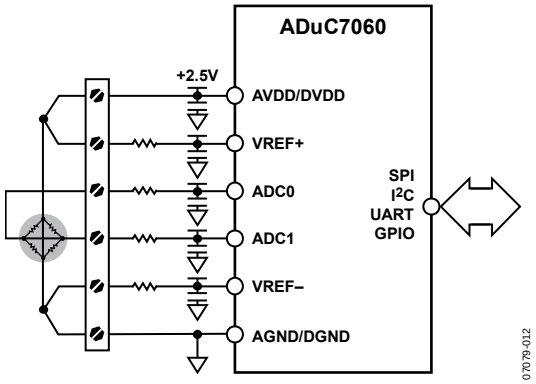


Figure 17. Bridge Interface Circuit

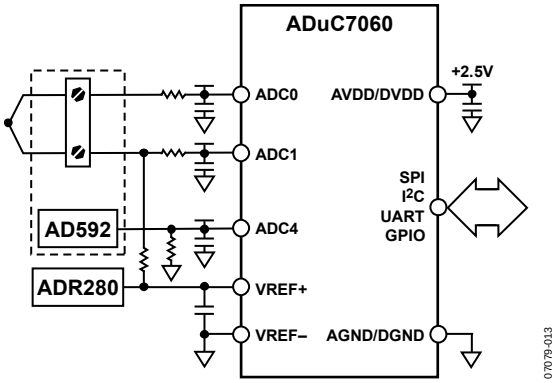


Figure 18. Example of a Thermocouple Interface Circuit

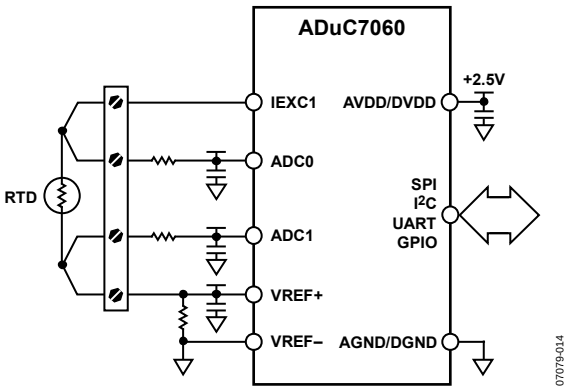


Figure 19. Example of an RTD Interface Circuit

DAC PERIPHERALS

DAC

The ADuC7060 incorporates a 12-bit voltage output DAC on-chip. The DAC has a rail-to-rail voltage output buffer capable of driving 5 kΩ/100 pF.

The DAC has four selectable ranges.

- 0 V to V_{REF} (internal band gap 1.2 V reference)
- VREF– to VREF+
- ADC5/EXT_REF2IN– to ADC4/EXT_REF2IN+
- 0 V to AVDD

The maximum signal range is 0 V to AVDD.

Op Amp Mode

As an option, the DAC can be disabled and its output buffer used as an op amp.

MMR INTERFACE

The DAC is configurable through a control register and a data register.

DAC0CON Register

Name: DAC0CON

Address: 0xFFFF0600

Default value: 0x0200

Access: Read and write

Table 61. DAC0CON MMR Bit Designations

Bit	Value	Name	Description
15:10			Reserved.
9		DACPD	Set to 1 to power down DAC output (DAC output is tristated). Clear this bit to enable the DAC.
8		DACBUFLP	Set to 1 to place the DAC output buffer in low power mode. See the Normal DAC Mode and Op Amp Mode sections for further details on electrical specifications. Clear this bit to enable the DAC buffer.
7		OPAMP	Set to 1 to place the DAC output buffer in op amp mode. Clear this bit to enable the DAC output buffer for normal DAC operation.
6		DACBUFBYPASS	Set to 1 to bypass the output buffer and send the DAC output directly to the output pin. Clear this bit to buffer the DAC output.
5		DACCLK	Set to 1 to update the DAC on the negative edge of HCLK. Set to 0 to update the DAC on the negative edge of Timer1. This mode is ideally suited for waveform generation where the next value in the waveform is written to DAC0DAT at regular intervals of Timer1.
4		$\overline{\text{DACCLR}}$	Set to 1 for normal DAC operation. Set to 0 to clear the DAC output and to set DAC0DAT to 0. Writing to this bit has an immediate effect on the DAC output.
3		DACMODE	Set to 1 to enable DAC in 16-bit interpolation mode. Set to 0 to enable DAC in normal 12-bit mode.
2		Rate	Used with interpolation mode. Set to 1 to configure the interpolation clock as UCLK/16. Set to 0 to configure the interpolation clock as UCLK/32.
1:0	11 10 01 00	DAC range bits	0 V to AVDD range. ADC5/EXT_REF2IN– to ADC4/EXT_REF2IN+. VREF– to VREF+. 0 V to V_{REF} (1.2 V) range. Internal reference source.

DAC0DAT Register

Name: DAC0DAT

Address: 0xFFFF0604

Default value: 0x00000000

Access: Read and write

Function: This 32-bit MMR contains the DAC output value.

Table 62. DAC0DAT MMR Bit Designations

Bit	Description
31:28	Reserved.
27:16	12-bit data for DAC0.
15:12	Extra four bits used in interpolation mode.
11:0	Reserved.

Using the DAC

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier. The functional equivalent is shown in Figure 20.

The reference source for the DAC is user selectable in software. It can be AVDD, VREF±, or ADCx/EXT_REF2IN±.

- In 0-to- AVDD mode, the DAC output transfer function spans from 0 V to the voltage at the AVDD pin.
- In VREF± and ADCx/EXT_REF2IN± modes, the DAC output transfer function spans from negative input voltage to the voltage positive input pin. Note that these voltages must never go below 0 V or above AVDD.
- In 0-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal 1.2 V reference, V_{REF}.

The DAC can be configured in three different user modes: normal mode, DAC interpolation mode, and op amp mode.

Normal DAC Mode

In this mode of operation, the DAC is configured as a 12-bit voltage output DAC. By default, the DAC buffer is enabled, but the output buffer can be disabled. If the DAC output buffer is disabled, the DAC is capable of driving a capacitive load of only 20 pF. The DAC buffer is disabled by setting the DACBUFBYPASS bit in DAC0CON.

The DAC output buffer amplifier features a true, rail-to-rail output stage implementation. This means that when unloaded, each output is capable of swinging to within less than 5 mV of both AVDD and ground. Moreover, the linearity specification of the DAC (when driving a 5 kΩ resistive load to ground) is guaranteed through the full transfer function except Code 0 to Code 100 and, in 0-to- AVDD mode only, Code 3995 to Code 4095. Linearity degradation near ground and AVDD is caused by saturation of the output amplifier, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 20. The dotted line in Figure 20 indicates the ideal transfer function, and the solid line represents what the transfer function may look like with endpoint nonlinearities due to saturation of the output amplifier. Note that Figure 20 represents a transfer function in 0-to-AVDD mode only. In 0-to-V_{REF} or, VREF±, and ADCx/EXT_REF2IN± modes (with V_{REF} < AVDD or ADCx/EXT_REF2IN± < AVDD), the lower nonlinearity is similar. However, the upper portion of the transfer function follows the ideal line right to the end (V_{REF} in this case, not AVDD), showing no signs of endpoint linearity errors.

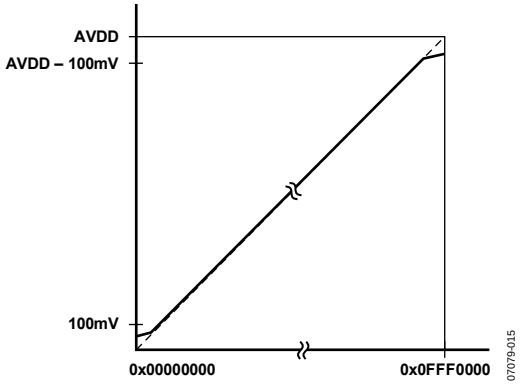


Figure 20. Endpoint Nonlinearities Due to Amplifier Saturation

The endpoint nonlinearities conceptually illustrated in Figure 20 worsen as a function of output loading. Most of the ADuC7060 data sheet specifications in normal mode assume a 5 kΩ resistive load to ground at the DAC output. As the output is forced to source or sink more current, the nonlinear regions at the top or bottom (respectively) of Figure 20 become larger. With larger current demands, this can significantly limit output voltage swing.

DAC Interpolation Mode

In interpolation mode, a higher DAC output resolution of 16 bits is achieved with a longer update rate than normal mode. The update rate is controlled by the interpolation clock rate selected in the DAC0CON register. In this mode, an external RC filter is required to create a constant voltage.

Op Amp Mode

In op amp mode, the DAC output buffer is used as an op amp with the DAC itself disabled.

ADC6 is the positive input to the op amp, ADC7 is the negative input, and ADC8 is the output. In this mode, the DAC should be powered down by setting Bit 9 of DAC0CON.

NONVOLATILE FLASH/EE MEMORY

The ADuC7060 incorporates Flash/EE memory technology on-chip to provide the user with nonvolatile, in-circuit reprogrammable memory space.

Like EEPROM, flash memory can be programmed in-system at a byte level, although it must first be erased. The erase is performed in page blocks. As a result, flash memory is often and, more correctly, referred to as Flash/EE memory.

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. Incorporated in the ADuC7060, Flash/EE memory technology allows the user to update program code space in-circuit, without the need to replace one time programmable (OTP) devices at remote operating nodes.

The ADuC7060 contains a 64 kB array of Flash/EE memory. The lower 62 kB are available to the user and the upper 2 kB contain permanently embedded firmware, allowing in-circuit serial download. These 2 kB of embedded firmware also contain a power-on configuration routine that downloads factory-calibrated coefficients to the various calibrated peripherals (such as ADC, temperature sensor, and band gap references). This 2 kB embedded firmware is hidden from user code.

FLASH/EE MEMORY RELIABILITY

The Flash/EE memory arrays on the parts are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. A single endurance cycle is composed of four independent, sequential events, defined as

- Initial page erase sequence
- Read/verify sequence a single Flash/EE
- Byte program sequence memory
- Second read/verify sequence endurance cycle

In reliability qualification, every half word (16-bit wide) location of the three pages (top, middle, and bottom) in the Flash/EE memory is cycled 10,000 times from 0x0000 to 0xFFFF. The Flash/EE memory endurance qualification is carried out in accordance with JEDEC *Retention Lifetime Specification A117* over the industrial temperature range of −40°C to +125°C. The results allow the specification of a minimum endurance figure over a supply temperature of 10,000 cycles.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the parts are qualified in accordance with the formal *JEDEC Retention Lifetime Specification A117* at a specific junction temperature (T_J = 85°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit, described previously, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its fully specified retention lifetime every time the Flash/EE memory is reprogrammed. Also note that retention lifetime, based on activation energy of 0.6 eV, derates with T_J as shown in Figure 21.

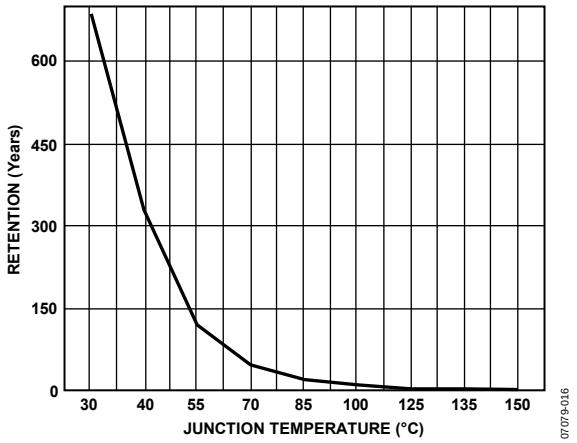


Figure 21. Flash/EE Memory Data Retention

PROGRAMMING

The 62 kB of Flash/EE memory can be programmed in-circuit, using the serial download mode or the provided JTAG mode.

Serial Downloading (In-Circuit Programming)

The ADuC7060 facilitates code download via the standard UART serial port. The parts enter serial download mode after a reset or power cycle if the NTRST/$\overline{\text{BM}}$ pin is pulled low through an external 1 kΩ resistor. When in serial download mode, the user can download code to the full 62 kB of Flash/EE memory while the device is in-circuit in its target application hardware. An executable PC serial download is provided as part of the development system for serial downloading via the UART.

JTAG Access

The JTAG protocol uses the on-chip JTAG interface to facilitate code download and debug.

PROCESSOR REFERENCE PERIPHERALS

INTERRUPT SYSTEM

There are 15 interrupt sources on the ADuC7060 that are controlled by the interrupt controller. All interrupts are generated from the on-chip peripherals, except for the software interrupt (SWI), which is programmable by the user. The ARM7TDMI CPU core recognizes interrupts as one of two types only: a normal interrupt request (IRQ) or a fast interrupt request (FIQ). All the interrupts can be masked separately.

The control and configuration of the interrupt system are managed through a number of interrupt related registers. The bits in each IRQ and FIQ register represent the same interrupt source as described in Table 63.

The ADuC7060 contains a vectored interrupt controller (VIC) that supports nested interrupts up to eight levels. The VIC also allows the programmer to assign priority levels to all interrupt sources. Interrupt nesting needs to be enabled by setting the ENIRQN bit in the IRQCONN register. A number of extra MMRs are used when the full vectored interrupt controller is enabled.

Immediately save IRQSTA/FIQSTA upon entering the interrupt service routine (ISR) to ensure that all valid interrupt sources are serviced.

Table 63. IRQ/FIQ MMRs Bit Designations

Bit	Description	Comments
0	All interrupts OR'ed (FIQ only)	This bit is set if any FIQ is active
1	Software interrupt	User programmable interrupt source
2	Undefined	This bit is not used
3	Timer0	General-Purpose Timer0
4	Timer1 or wake-up timer	General-Purpose Timer1 or wake-up timer
5	Timer2 or watchdog timer	General-Purpose Timer2 or watchdog timer
6	Timer3 or STI timer	General-Purpose Timer3
7	Undefined	This bit is not used
8	Undefined	This bit is not used
9	Undefined	This bit is not used
10	ADC	ADC interrupt source bit
11	UART	UART interrupt source bit
12	SPI	SPI interrupt source bit
13	XIRQ0 (GPIO IRQ0)	External Interrupt 0
14	XIRQ1 (GPIO IRQ1)	External Interrupt 1
15	I^2C master IRQ	I^2C master interrupt source bit
16	I^2C slave IRQ	I^2C slave interrupt source bit
17	PWM	PWM trip interrupt source bit
18	XIRQ2 (GPIO IRQ2)	External Interrupt 2
19	XIRQ3 (GPIO IRQ3)	External Interrupt 3

IRQ

The IRQ is the exception signal to enter the IRQ mode of the processor. It services general-purpose interrupt handling of internal and external events.

All 32 bits are logically OR'ed to create a single IRQ signal to the ARM7TDMI core. The four 32-bit registers dedicated to IRQ follow.

IRQSIG

IRQSIG reflects the status of the different IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, it is cleared. The IRQSIG bits clear when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read only.

IRQSIG Register

Name: IRQSIG

Address: 0xFFFF0004

Default value: Undefined

Access: Read only

IRQEN

IRQEN provides the value of the current enable mask. When a bit is set to 1, the corresponding source request is enabled to create an IRQ exception. When a bit is set to 0, the corresponding source request is disabled or masked which does not create an IRQ exception. The IRQEN register cannot be used to disable an interrupt.

IRQEN Register

Name: IRQEN

Address: 0xFFFF0008

Default value: 0x00000000

Access: Read and write

IRQCLR

IRQCLR is a write-only register that allows the IRQEN register to clear in order to mask an interrupt source. Each bit that is set to 1 clears the corresponding bit in the IRQEN register without affecting the remaining bits. The pair of registers, IRQEN and IRQCLR, allows independent manipulation of the enable mask without requiring an atomic read-modify-write.

IRQCLR Register

Name: IRQCLR

Address: 0xFFFF000C

Default value: 0x00000000

Access: Write only

IRQSTA

IRQSTA is a read-only register that provides the current enabled IRQ source status (effectively a logic AND of the IRQSIG and IRQEN bits). When set to 1, that source generates an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine.

IRQSTA Register

Name: IRQSTA

Address: 0xFFFF0000

Default value: 0x00000000

Access: Read only

FAST INTERRUPT REQUEST (FIQ)

The fast interrupt request (FIQ) is the exception signal to enter the FIQ mode of the processor. It is provided to service data transfer or communication channel tasks with low latency. The FIQ interface is identical to the IRQ interface and provides the second level interrupt (highest priority). Four 32-bit registers are dedicated to FIQ: FIQSIG, FIQEN, FIQCLR, and FIQSTA.

Bit 31 to Bit 1 of FIQSTA are logically OR'ed to create the FIQ signal to the core and to Bit 0 of both the FIQ and IRQ registers (FIQ source).

The logic for FIQEN and FIQCLR does not allow an interrupt source to be enabled in both IRQ and FIQ masks. A bit set to 1 in FIQEN clears, as a side effect, the same bit in IRQEN. Likewise, a bit set to 1 in IRQEN clears, as a side effect, the same bit in FIQEN. An interrupt source can be disabled in both IRQEN and FIQEN masks.

FIQSIG

FIQSIG reflects the status of the different FIQ sources. If a peripheral generates an FIQ signal, the corresponding bit in the FIQSIG is set; otherwise, it is cleared. The FIQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All FIQ sources can be masked in the FIQEN MMR. FIQSIG is read only.

FIQSIG Register

Name: FIQSIG

Address: 0xFFFF0104

Default value: Undefined

Access: Read only

FIQEN

FIQEN provides the value of the current enable mask. When a bit is set to 1, the corresponding source request is enabled to create an FIQ exception. When a bit is set to 0, the corresponding source request is disabled or masked, which does not create an FIQ exception. The FIQEN register cannot be used to disable an interrupt.

FIQEN Register

Name: FIQEN

Address: 0xFFFF0108

Default value: 0x00000000

Access: Read and write

FIQCLR

FIQCLR is a write-only register that allows the FIQEN register to clear in order to mask an interrupt source. Each bit that is set to 1 clears the corresponding bit in the FIQEN register without affecting the remaining bits. The pair of registers, FIQEN and FIQCLR, allows independent manipulation of the enable mask without requiring an atomic read-modify-write.

FIQCLR Register

Name: FIQCLR

Address: 0xFFFF010C

Default value: 0x00000000

Access: Write only

FIQSTA

FIQSTA is a read-only register that provides the current enabled FIQ source status (effectively a logic AND of the FIQSIG and FIQEN bits). When set to 1, that source generates an active FIQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine.

FIQSTA Register

Name: FIQSTA

Address: 0xFFFF0100

Default value: 0x00000000

Access: Read only

PROGRAMMED INTERRUPTS

Because the programmed interrupts are not maskable, they are controlled by another register (SWICFG) that writes into both IRQSTA and IRQSIG registers and/or the FIQSTA and FIQSIG registers at the same time.

SWICFG

The 32-bit register dedicated to software interrupt is SWICFG, described in Table 64. This MMR allows the control of a programmed source interrupt.

SWICFG Register

Name: SWICFG

Address: 0xFFFF0010

Default value: 0x00000000

Access: Write only

Table 64. SWICFG MMR Bit Designations

Bit	Description
31 to 3	Reserved.
2	Programmed interrupt FIQ. Setting/clearing this bit corresponds to setting/clearing Bit 1 of FIQSTA and FIQSIG.
1	Programmed interrupt IRQ. Setting/clearing this bit corresponds to setting/clearing Bit 1 of IRQSTA and IRQSIG.
0	Reserved.

Any interrupt signal must be active for at least the minimum interrupt latency time to be detected by the interrupt controller and to be detected by the user in the IRQSTA/FIQSTA register.

VECTORED INTERRUPT CONTROLLER (VIC)

The ADuC7060 incorporates an enhanced interrupt control system or vectored interrupt controller. The vectored interrupt controller for IRQ interrupt sources is enabled by setting Bit 0 of the IRQCONN register. Similarly, Bit 1 of IRQCONN enables the vectored interrupt controller for the FIQ interrupt sources. The vectored interrupt controller provides the following enhancements to the standard IRQ/FIQ interrupts:

- Vectored interrupts—allows a user to define separate interrupt service routine addresses for every interrupt source. This is achieved by using the IRQBASE and IRQVEC registers.
- IRQ/FIQ interrupts—can be nested up to eight levels depending on the priority settings. An FIQ still has a higher priority than an IRQ. There fore, if the VIC is enabled for both the FIQ and IRQ and prioritization is maximized, then it is possible to have 16 separate interrupt levels.
- Programmable interrupt priorities—using the IRQP0 to IRQP2 registers, an interrupt source can be assigned an interrupt priority level value between 1 and 8.

VIC MMRS

IRQBASE

The vector base register, IRQBASE, is used to point to the start address of memory used to store 32 pointer addresses. These pointer addresses are the addresses of the individual interrupt service routines.

IRQBASE Register

Name: IRQBASE

Address: 0xFFFF0014

Default value: 0x00000000

Access: Read and write

Table 65. IRQBASE MMR Bit Designations

Bit	Type	Initial Value	Description
31:16	Read only	Reserved	Always read as 0
15:0	R/W	0	Vector base address

IRQVEC

The IRQ interrupt vector register, IRQVEC points to a memory address containing a pointer to the interrupt service routine of the currently active IRQ. This register should only be read when an IRQ occurs and IRQ interrupt nesting has been enabled by setting Bit 0 of the IRQCONN register.

IRQVEC Register

Name: IRQVEC

Address: 0xFFFF001C

Default value: 0x00000000

Access: Read only

Table 66. IRQVEC MMR Bit Designations

Bit	Type	Initial Value	Description
31:23	Read only	0	Always read as 0.
22:7	Read only	0	IRQBASE register value.
6:2	Read only	0	Highest priority IRQ source. This is a value between 0 to 19 representing the possible interrupt sources. For example, if the highest currently active IRQ is Timer1, then these bits are [01000].
1:0	Reserved	0	Reserved bits.

Priority Registers

The IRQ interrupt vector register, IRQVEC, points to a memory address containing a pointer to the interrupt service routine of the currently active IRQ. This register should be read only when an IRQ occurs and IRQ interrupt nesting has been enabled by setting Bit 0 of the IRQCONN register.

IRQP0 Register

Name: IRQP0

Address: 0xFFFF0020

Default value: 0x00000000

Access: Read and write

Table 67. IRQP0 MMR Bit Designations

Bit	Name	Description
31:27	Reserved	Reserved bits.
26:24	T3PI	A priority level of 0 to 7 can be set for Timer3.
23	Reserved	Reserved bit.
22:20	T2PI	A priority level of 0 to 7 can be set for Timer2.
19	Reserved	Reserved bit.
18:16	T1PI	A priority level of 0 to 7 can be set for Timer1.
15	Reserved	Reserved bit.
14:12	T0PI	A priority level of 0 to 7 can be set for Timer0.
11:7	Reserved	Reserved bits.
6:4	SWINTP	A priority level of 0 to 7 can be set for the software interrupt source.
3:0	Reserved	Interrupt 0 cannot be prioritized.

IRQP1 Register

Name: IRQP1

Address: 0xFFFF0024

Default value: 0x00000000

Access: Read and write

Table 68. IRQP1 MMR Bit Designations

Bit	Name	Description
31	Reserved	Reserved bit.
30:28	I2CMPI	A priority level of 0 to 7 can be set for I^2C master.
27	Reserved	Reserved bit.
26:24	IRQ1PI	A priority level of 0 to 7 can be set for IRQ1.
23	Reserved	Reserved bit.
22:20	IRQ0PI	A priority level of 0 to 7 can be set for IRQ0.
19	Reserved	Reserved bit.
18:16	SPIMPI	A priority level of 0 to 7 can be set for SPI master.
15	Reserved	Reserved bit.
14:12	UARTPI	A priority level of 0 to 7 can be set for UART.
11	Reserved	Reserved bit.
10:8	ADCPI	A priority level of 0 to 7 can be set for the ADC interrupt source.
7:0	Reserved	Reserved bits.

IRQP2 Register

Name: IRQP2

Address: 0xFFFF0028

Default value: 0x00000000

Access: Read and write

Table 69. IRQP2 MMR Bit Designations

Bit	Name	Description
31:15	Reserved	Reserved bit.
14:12	IRQ3PI	A priority level of 0 to 7 can be set for IRQ3.
11	Reserved	Reserved bit.
10:8	IRQ2PI	A priority level of 0 to 7 can be set for IRQ2.
7	Reserved	Reserved bit.
6:4	SPISPI	A priority level of 0 to 7 can be set for SPI slave.
3	Reserved	Reserved bit.
2:0	I2CSPI	A priority level of 0 to 7 can be set for I^2C slave.

IRQCONN

The IRQCONN register is the IRQ and FIQ control register. It contains two active bits. The first to enable nesting and prioritization of IRQ interrupts the other to enable nesting and prioritization of FIQ interrupts.

If these bits are cleared, then FIQs and IRQs can still be used, but it is not possible to nest IRQs or FIQs. Neither is it possible to set an interrupt source priority level. In this default state, an FIQ does have a higher priority than an IRQ.

IRQCONN Register

Name: IRQCONN

Address: 0xFFFF0030

Default value: 0x00000000

Access: Read and write

Table 70. IRQCONN MMR Bit Designations

Bit	Name	Description
31:2	Reserved	These bits are reserved and should not be written to.
1	ENFIQN	Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.
0	ENIRQN	Setting this bit to 1 enables nesting of IRQ interrupts. Clearing this bit means no nesting or prioritization of IRQs is allowed.

IRQSTAN

If IRQCONN.0 is asserted and IRQVEC is read, then one of these bits is asserted. The bit that asserts depends on the priority of the IRQ. If the IRQ is of Priority 0 then Bit 0 asserts, Priority 1 then Bit 1 asserts, and so forth. When a bit is set in this register, all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is possible to clear only one bit at a time. For example, if this register is set to 0x09, writing 0xFF changes the register to 0x08, and writing 0xFF a second time changes the register to 0x00.

IRQSTAN Register

Name: IRQSTAN

Address: 0xFFFF003C

Default value: 0x00000000

Access: Read and write

Table 71. IRQSTAN MMR Bit Designations

Bit	Name	Description
31:8	Reserved	These bits are reserved and should not be written to.
7:0		Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.

FIQVEC

The FIQ interrupt vector register, FIQVEC, points to a memory address containing a pointer to the interrupt service routine of the currently active FIQ. This register should be read only when an FIQ occurs and FIQ interrupt nesting has been enabled by setting Bit 1 of the IRQCONN register.

FIQVEC Register

Name: FIQVEC

Address: 0xFFFF011C

Default value: 0x00000000

Access: Read only

Table 72. FIQVEC MMR Bit Designations

Bit	Type	Initial Value	Description
31:23	Read only	0	Always read as 0.
22:7	R/W	0	IRQBASE register value.
6:2		0	Highest priority FIQ source. This is a value between 0 to 19 that represents the possible interrupt sources. For example, if the highest currently active FIQ is Timer1, then these bits are [01000].
1:0	Reserved	0	Reserved bits.

FIQSTAN

If IRQCONN.1 is asserted and FIQVEC is read, then one of these bits asserts. The bit that asserts depends on the priority of the FIQ. If the FIQ is of Priority 0 then Bit 0 asserts, Priority 1 then Bit 1 asserts, and so forth.

When a bit is set in this register, all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is possible to clear only one bit as a time. For example, if this register is set to 0x09 then writing 0xFF changes the register to 0x08 and writing 0xFF a second time changes the register to 0x00.

FIQSTAN Register

Name: FIQSTAN

Address: 0xFFFF013C

Default value: 0x00000000

Access: Read and write

Table 73. FIQSTAN MMR Bit Designations

Bit	Name	Description
31:8	Reserved	These bits are reserved and should not be written to.
7:0		Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.

External Interrupts (IRQ0 to IRQ3)

The ADuC7060 provides up to four external interrupt sources. These external interrupts can be individually configured as level or rising/falling edge triggered.

To enable the external interrupt source, first of all, the appropriate bit must be set in the FIQEN or IRQEN register. To select the required edge or level to trigger on, the IRQCONE register must be appropriately configured.

To properly clear an edge based external IRQ interrupt, set the appropriate bit in theIRQCLRE register.

IRQCONE Register

Name: IRQCONE

Address: 0xFFFF0034

Default value: 0x00000000

Access: Read and write

Table 74. IRQCONE MMR Bit Designations

Bit	Value	Name	Description
31:8		Reserved	These bits are reserved and should not be written to.
7:6	11	IRQ3SRC[1:0]	External IRQ3 triggers on falling edge.
	10		External IRQ3 triggers on rising edge.
	01		External IRQ3 triggers on low level.
	00		External IRQ3 triggers on high level.
5:4	11	IRQ2SRC[1:0]	External IRQ2 triggers on falling edge.
	10		External IRQ2 triggers on rising edge.
	01		External IRQ2 triggers on low level.
	00		External IRQ2 triggers on high level.
3:2	11	IRQ1SRC[1:0]	External IRQ1 triggers on falling edge.
	10		External IRQ1 triggers on rising edge.
	01		External IRQ1 triggers on low level.
	00		External IRQ1 triggers on high level.
1:0	11	IRQ0SRC[1:0]	External IRQ0 triggers on falling edge.
	10		External IRQ0 triggers on rising edge.
	01		External IRQ0 triggers on low level.
	00		External IRQ0 triggers on high level.

IRQCLRE Register

Name: IRQCLRE

Address: 0xFFFF0038

Default value: 0x00000000

Access: Read and write

Table 75. IRQCLRE MMR Bit Designations

Bit	Name	Description
31:20	Reserved	These bits are reserved and should not be written to.
19	IRQ3CLRI	A 1 must be written to this bit in the IRQ3 interrupt service routine to clear an edge triggered IRQ3 interrupt.
18	IRQ2CLRI	A 1 must be written to this bit in the IRQ2 interrupt service routine to clear an edge triggered IRQ2 interrupt.
17:15	Reserved	These bits are reserved and should not be written to.
14	IRQ1CLRI	A 1 must be written to this bit in the IRQ1 interrupt service routine to clear an edge triggered IRQ1 interrupt.
13	IRQ0CLRI	A 1 must be written to this bit in the IRQ0 interrupt service routine to clear an edge triggered IRQ0 interrupt.
12:0	Reserved	These bits are reserved and should not be written to.

TIMERS

The ADuC7060 features four general-purpose timer/counters.

- Timer0
- Timer1 or wake-up timer
- Timer2 or watchdog timer
- Timer3

The four timers in their normal mode of operation can be either free running or periodic.

In free running mode, the counter decrements/increments from the maximum or minimum value until zero/full scale and starts again at the maximum or minimum value.

In periodic mode, the counter decrements/increments from the value in the load register (TxLD MMR) until zero/full scale and starts again at the value stored in the load register. Note that the TxLD MMR should be configured before the TxCON MMR.

The value of a counter can be read at any time by accessing its value register (TxVAL). Timers are started by writing in the control register of the corresponding timer (TxCON).

In normal mode, an IRQ is generated each time the value of the counter reaches zero (if counting down) or full scale (if counting up). An IRQ can be cleared by writing any value to the clear register of the particular timer (TxCLRI).

Table 76. Timer Event Capture

Bit	Description
0	Reserved
1	Timer0
2	Timer1 or wake-up timer
3	Timer2 or watchdog timer
4	Timer3
5	Reserved
6	Reserved
7	Reserved
8	ADC
9	UART
10	SPI
11	XIRQ0
12	XIRQ1
13	I^2C master
14	I^2C slave
15	PWM
16	XIRQ2 (GPIO IRQ2)
17	XIRQ3 (GPIO IRQ3)

TIMER0

Timer0 is a 32-bit general-purpose timer, count down or count up, with a programmable prescaler. The prescaler source can be the low power 32.768 kHz oscillator, the core clock, or from one of two external GPIOs. This source can be scaled by a factor of 1, 16, 256, or 32,768. This gives a minimum resolution of 97.66 ns with a prescaler of 1 (ignoring the external GPIOs).

The counter can be formatted as a standard 32-bit value or as hours:minutes:seconds:hundredths.

Timer0 has a capture register (T0CAP) that is triggered by a selected IRQ source initial assertion. When triggered, the current timer value is copied to T0CAP, and the timer continues to run. Use this feature to determine the assertion of an event with increased accuracy. Note that only peripherals that have their IRQ source enabled can be used with the timer capture feature.

The Timer0 interface consists of five MMRS: T0LD, T0VAL, T0CAP, T0CLRI, and T0CON.

- T0LD, T0VAL, and T0CAP are 32-bit registers and hold 32-bit unsigned integers of which T0VAL and T0CAP are read only.
- T0CLRI is an 8-bit register and writing any value to this register clears the Timer0 interrupt.
- T0CON is the configuration MMR, which is described in Table 77.

Timer0 features a postscaler that allows the user to count between 1 and 256 the number of Timer0 timeouts. To activate the post-scaler, the user sets Bit 18 and writes the desired number to count into Bits[24:31] of T0CON. When that number of timeouts is reached, Timer0 can generate an interrupt if T0CON[Bit 18] is set.

Note that, if the part is in a low power mode and Timer0 is clocked from the GPIO or low power oscillator source, Timer0 continues to operate.

Timer0 reloads the value from T0LD when Timer0 overflows.

Timer0 Load Registers

Name: T0LD

Address: 0xFFFF0320

Default value: 0x00000000

Access: Read and write

Function: T0LD is a 32-bit register that holds the 32-bit value that is loaded into the counter.

Timer0 Clear Register

Name: T0CLRI

Address: 0xFFFF032C

Access: Write only

Function: This 8-bit, write-only MMR is written (with any value) by user code to clear the interrupt.

Timer0 Value Register

Name: T0VAL

Address: 0xFFFF0324

Default value: 0xFFFFFFFF

Access: Read only

Function: T0VAL is a 32-bit register that holds the current value of Timer0.

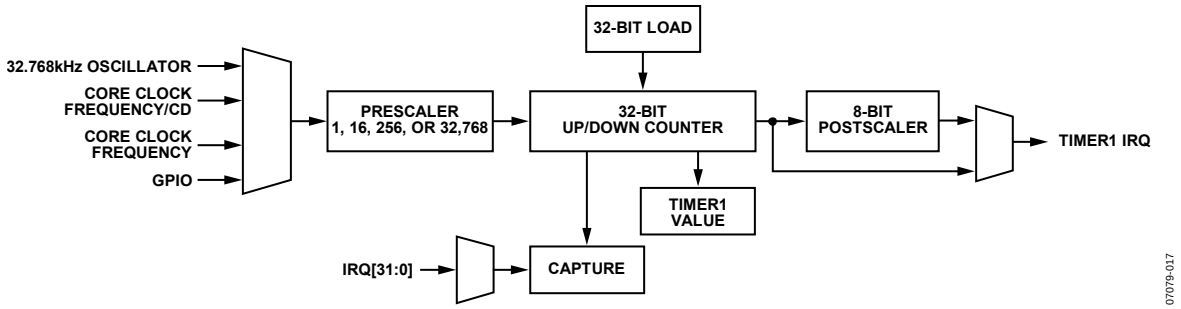


Figure 22. Timer0 Block Diagram

Timer0 Capture Register

Name: T0CAP

Address: 0xFFFF0330

Default value: 0x00000000

Access: Read only

Function: This 32-bit register holds the 32-bit value captured by an enabled IRQ event.

Timer0 Control Register

Name: T0CON

Address: 0xFFFF0328

Default value: 0x01000000

Access: Read and write

Function: This 32-bit MMR configures the mode of operation of Timer0.

Table 77. T0CON MMR Bit Designations

Bit	Name	Description
31 to 24	T0PVAL	8-bit postscaler. By writing to these eight bits, a value is written to the postscaler. Writing 0 is interpreted as a 1. By reading these eight bits, the current value of the counter is read.
23	T0PEN	Timer0 enable postscaler. Set to enable the Timer0 postscaler. If enabled, interrupts are generated after T0CON[31:24] periods as defined by T0LD. Cleared to disable the Timer0 postscaler.
22 to 20		Reserved. These bits are reserved and should be written as 0 by user code.
19	T0PCF	Postscaler compare flag; read only. Set if the number of Timer0 overflows is equal to the number written to the postscaler.
18	T0SRCI	Timer0 interrupt source. Set to select interrupt generation from the postscaler counter. Cleared to select interrupt generation directly from Timer0.
17	T0CAPEN	Event enable bit. Set by user to enable time capture of an event. Cleared by user to disable time capture of an event.
16 to 12	T0CAPSEL	Event select Bits[0:31]. The events are described in Table 76.
11		Reserved bit.
10 to 9	T0CLKSEL	Clock select. 00 = 32.768 kHz. 01 = 10.24 MHz/CD. 10 = 10.24 MHz. 11 = P1.0.
8	T0DIR	Count up. Set by user for Timer0 to count up. Cleared by user for Timer0 to count down (default).
7	T0EN	Timer0 enable bit. Set by user to enable Timer0. Cleared by user to disable Timer0 (default).

Bit	Name	Description
6	T0MOD	Timer0 mode. Set by user to operate in periodic mode. Cleared by user to operate in free running mode (default).
5 to 4	T0FORMAT	Format. 00 = binary (default). 01 = reserved. 10 = hours:minutes:seconds:hundredths (23 hours to 0 hours). 11 = hours:minutes:seconds:hundredths (255 hours to 0 hours).
3 to 0	T0SCALE	Prescaler. 0000 = source clock/1 (default). 0100 = source clock/16. 1000 = source clock/256. 1111 = source clock/32,768. Note that 10XX = undefined.

TIMER1 OR WAKE-UP TIMER

Timer1 is a 32-bit wake-up timer, count down or count up, with a programmable prescaler. The prescaler is clocked directly from one of four clock sources, namely, the core clock (which is the default selection), the low power 32.768 kHz oscillators, external 32.768 kHz watch crystal, or the precision 32.768 kHz oscillator. The selected clock source can be scaled by a factor of 1, 16, 256, or 32,768. The wake-up timer continues to run when the core clock is disabled. This gives a minimum resolution of 97.66 ns when operating at CD zero, the core is operating at 10.24 MHz, and with a prescaler of 1 (ignoring the external GPIOs).

The counter can be formatted as a plain 32-bit value or as hours:minutes:seconds:hundredths.

Timer1 reloads the value from T1LD either when Timer1 overflows or immediately when T1CLRI is written.

The Timer1 interface consists of four MMRS.

- T1LD and T1VAL are 32-bit registers and hold 32-bit unsigned integers. T1VAL is read only.
- T1CLRI is an 8-bit register. Writing any value to this register clears the Timer1 interrupt.
- T1CON is the configuration MMR described in Table 78.

Timer1 Load Registers

Name: T1LD

Address: 0xFFFF0340

Default value: 0x00000000

Access: Read and write

Function: T1LD is a 32-bit register that holds the 32-bit value that is loaded into the counter.

Timer1 Clear Register

Name: T1CLRI

Address: 0xFFFF034C

Access: Write only

Function: This 8-bit, write-only MMR is written (with any value) by user code to clear the interrupt.

Timer1 Value Register

Name: T1VAL

Address: 0xFFFF0344

Default value: 0xFFFFFFFF

Access: Read only

Function: T1VAL is a 32-bit register that holds the current value of Timer1.

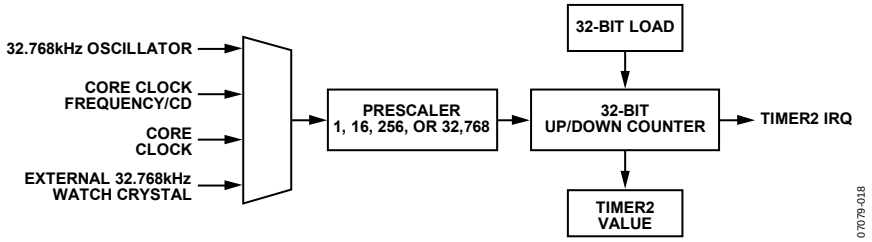


Figure 23. Timer1 Block Diagram

Timer1 Control Register

Name: T1CON

Address: 0xFFFF0348

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR configures the mode of operation of Timer1.

Table 78. T1CON MMR Bit Designations

Bit	Name	Description
15 to 11		Reserved.
10 to 9	T1CLKSEL	Clock source select. 00 = 32.768 kHz oscillator. 01 = 10.24 MHz/CD. 10 = XTAL2. 11 = 10.24 MHz.
8	T1DIR	Count up. Set by user for Timer1 to count up. Cleared by user for Timer1 to count down (default).
7	T1EN	Timer1 enable bit. Set by user to enable Timer1. Cleared by user to disable Timer1 (default).
6	T1MOD	Timer1 mode. Set by user to operate in periodic mode. Cleared by user to operate in free running mode (default).
5 to 4	T1FORMAT	Format. 00 = binary (default). 01 = reserved. 10 = hours:minutes:seconds:hundredths (23 hours to 0 hours). This is only valid with a 32 kHz clock. 11 = hours:minutes:seconds:hundredths (255 hours to 0 hours). This is only valid with a 32 kHz clock.
3 to 0	T1SCALE	Prescaler. 0000 = source clock/1 (default). 0100 = source clock/16. 1000 = source clock/256. This setting should be used in conjunction with Timer1 in the format hours:minutes:seconds:hundredths. See Format 10 and Format 11 listed with Bits[5:4] in this table (Table 78). 1111 = source clock/32,768.

TIMER2 OR WATCHDOG TIMER

Timer2 has two modes of operation, normal mode and watchdog mode. The watchdog timer is used to recover from an illegal software state. When enabled, it requires periodic servicing to prevent it from forcing a reset of the processor.

Timer2 reloads the value from T2LD either when Timer2 overflows or immediately when T2CLRI is written.

Normal Mode

The Timer2 in normal mode is identical to Timer0 in 16-bit mode of operation, except for the clock source. The clock source is the low power, 32.768 kHz oscillator scalable by a factor of 1, 16, or 256.

Watchdog Mode

Watchdog mode is entered by setting T2CON[Bit 5]. Timer2 decrements from the timeout value present in the T2LD register until zero. The maximum timeout is 512 seconds, using a maximum prescaler/256 and full scale in T2LD.

User software should not configure a timeout period of less than 30 ms. This is to avoid any conflict with Flash/EE memory page erase cycles that require 20 ms to complete a single page erase cycle and kernel execution.

If T2VAL reaches 0, a reset or an interrupt occurs, depending on T2CON[Bit 1]. To avoid a reset or an interrupt event, any value must be written to T2CLRI before T2VAL reaches zero. This reloads the counter with T2LD and begins a new timeout period.

When watchdog mode is entered, T2LD and T2CON are write protected. These two registers cannot be modified until a power-on reset event resets the watchdog timer. After any other reset event, the watchdog timer continues to count. To avoid an infinite loop of watchdog resets, configure the watchdog timer in the initial lines of user code. User software should configure a minimum timeout period of 30 ms only.

Timer2 halts automatically during JTAG debug access and only recommences counting after JTAG relinquishes control of the ARM7 core. By default, Timer2 continues to count during power-down. To disable this, set Bit 0 in T2CON. It is recommended to use the default value, that is, that the watchdog timer continues to count during power-down.

Timer2 Interface

The Timer2 interface consists of four MMRs.

- T2CON is the configuration MMR described in (Table 83).
- T2LD and T2VAL are 16-bit registers (Bit 0 to Bit 15) and hold 16-bit unsigned integers. T2VAL is read only.
- T2CLRI is an 8-bit register. Writing any value to this register clears the Timer2 interrupt in normal mode or resets a new timeout period in watchdog mode.

Timer2 Load Register

Name: T2LD

Address: 0xFFFF0360

Default value: 0x0040

Access: Read and write

Function: This 16-bit MMR holds the Timer2 reload value.

Timer2 Value Register

Name: T2VAL

Address: 0xFFFF0364

Default value: 0x0040

Access: Read only

Function: This 16-bit, read-only MMR holds the current Timer2 count value.

Timer2 Clear Register

Name: T2CLRI

Address: 0xFFFF036C

Access: Write only

Function: This 8-bit, write-only MMR is written (with any value) by user code to refresh (reload) Timer2 in watchdog mode to prevent a watchdog timer reset event.

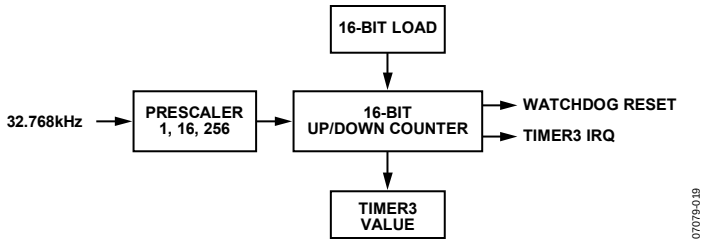


Figure 24. Timer2 Block Diagram

Timer2 Control Register

Name: T2CON

Address: 0xFFFF0368

Default value: 0x0000

Access: Read and write

Function: The 16-bit MMR configures the mode of operation of Timer2, as described in detail in Table 79.

Table 79. T2CON MMR Bit Designations

Bit	Name	Description
15:9		Reserved. These bits are reserved and should be written as 0 by user code.
8	T2DIR	Count up/count down enable. Set by user code to configure Timer2 to count up. Cleared by user code to configure Timer2 to count down.
7	T2EN	Timer2 enable. Set by user code to enable Timer2. Cleared by user code to disable Timer2.
6	T2MOD	Timer2 operating mode. Set by user code to configure Timer2 to operate in periodic mode. Cleared by user to configure Timer2 to operate in free running mode.
5	WDOGMDEN	Watchdog timer mode enable. Set by user code to enable watchdog mode. Cleared by user code to disable watchdog mode.
4		Reserved. This bit is reserved and should be written as 0 by user code.
3:2	T2SCALE	Timer2 clock (32.768 kHz) prescaler. 00 = 32.768 kHz (default). 01 = source clock/16. 10 = source clock/256. 11 = reserved.
1	WDOGENI	Watchdog timer IRQ enable. Set by user code to produce an IRQ instead of a reset when the watchdog reaches 0. Cleared by user code to disable the IRQ option.
0	T2PDOFF	Stop Timer2 when power-down is enabled. Set by user code to stop Timer2 when the peripherals are powered down using Bit 4 in the POWCON0 MMR. Cleared by user code to enable Timer2 when the peripherals are powered down using Bit 4 in the POWCON0 MMR.

TIMER3

Timer3 is a general-purpose, 16-bit, count up/count down timer with a programmable prescaler. Timer3 can be clocked from the core clock or the low power 32.768 kHz oscillator with a prescaler of 1, 16, 256, or 32,768.

Timer3 has a capture register (T3CAP) that can be triggered by a selected IRQ source initial assertion. Once triggered, the current timer value is copied to T3CAP, and the timer continues running. This feature can be used to determine the assertion of an event with increased accuracy.

The Timer3 interface consists of five MMRs.

- T3LD, T3VAL, and T3CAP are 16-bit registers and hold 16-bit unsigned integers. T3VAL and T3CAP are read only.
- T3CLRI is an 8-bit register. Writing any value to this register clears the interrupt.
- T3CON is the configuration MMR described in Table 80.

Timer3 Load Registers

Name: T3LD

Address: 0xFFFF0380

Default value: 0x0000

Access: Read and write

Function: T3LD 16-bit register holds the 16-bit value that is loaded into the counter.

Timer3 Clear Register

Name: T3CLRI

Address: 0xFFFF038C

Access: Write only

Function: This 8-bit, write-only MMR is written (with any value) by user code to clear the interrupt.

Timer3 Value Register

Name: T3VAL

Address: 0xFFFF0384

Default value: 0xFFFF

Access: Read only

Function: T3VAL is a 16-bit register that holds the current value of Timer3.

Time3 Capture Register

Name: T3CAP

Address: 0xFFFF0390

Default value: 0x0000

Access: Read only

Function: This is a 16-bit register that holds the 32-bit value captured by an enabled IRQ event.

Timer3 Control Register

Name: T3CON

Address: 0xFFFF0388

Default value: 0x00000000

Access: Read and write

Function: This 32-bit MMR configures the mode of operation of Timer3.

Table 80. T3CON MMR Bit Designations

Bit	Name	Description
31:18		Reserved.
17	T3CAPEN	Event enable bit. Set by user to enable time capture of an event. Cleared by user to disable time capture of an event.
16:12	T3CAPSEL	Event select range, 0 to 31. The events are described in Table 76.
11		Reserved.
10:9	T3CLKSEL	Clock select. 00 = 32.768 kHz oscillator. 01 = 10.24 MHz/CD. 10 = 10.24 MHz. 11 = reserved.
8	T3DIR	Count up. Set by user for Timer3 to count up. Cleared by user for Timer3 to count down (default).
7	T3EN	Timer3 enable bit. Set by user to enable Timer3. Cleared by user to disable Timer3 (default).
6	T3MOD	Timer3 mode. Set by user to operate in periodic mode. Cleared by user to operate in free running mode (default mode).
5:4		Reserved.
3:0	T3SCALE	Prescaler. 0000 = source clock/1 (default). 0100 = source clock/16. 1000 = source clock/256. 1111 = source clock/32,768.

PULSE-WIDTH MODULATOR

PULSE-WIDTH MODULATOR GENERAL OVERVIEW

The ADuC7060 integrates a 6-channel pulse-width modulator (PWM) interface. The PWM outputs can be configured to drive an H-bridge or can be used as standard PWM outputs. On power-up, the PWM outputs default to H-bridge mode. This ensures that the motor is turned off by default. In standard PWM mode, the outputs are arranged as three pairs of PWM pins. Users have control over the period of each pair of outputs and over the duty cycle of each individual output.

Table 81. PWM MMRs

MMR Name	Description
PWMCON	PWM control.
PWM0COM0	Compare Register 0 for PWM Output 0 and Output 1.
PWM0COM1	Compare Register 1 for PWM Output 0 and PWM Output 1.
PWM0COM2	Compare Register 2 for PWM Output 0 and PWM Output 1.
PWM0LEN	Frequency control for PWM Output 0 and PWM Output 1.
PWM1COM0	Compare Register 0 for PWM Output 2 and PWM Output 3.
PWM1COM1	Compare Register 1 for PWM Output 2 and PWM Output 3.
PWM1COM2	Compare Register 2 for PWM Output 2 and PWM Output 3.
PWM1LEN	Frequency control for PWM Output 2 and PWM Output 3.
PWM2COM0	Compare Register 0 for PWM Output 4 and PWM Output 5.
PWM2COM1	Compare Register 1 for PWM Output 4 and PWM Output 5.
PWM2COM2	Compare Register 2 for PWM Output 4 and PWM Output 5.
PWM2LEN	Frequency control for PWM Output 4 and PWM Output 5.
PWMICLR	PWM interrupt clear.

In all modes, the PWMxCOMx MMRs control the point at which the PWM outputs change state. An example of the first pair of PWM outputs (PWM0 and PWM1) is shown in Figure 25.

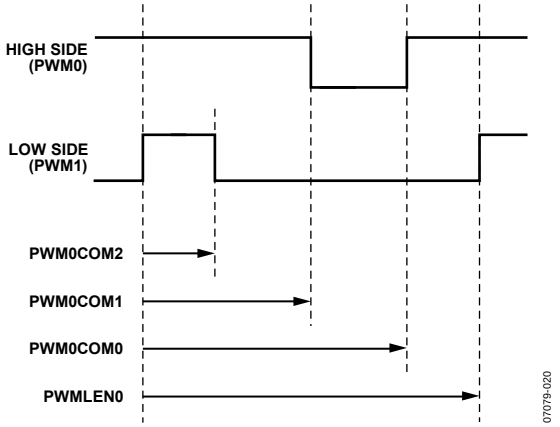


Figure 25. PWM Timing

The PWM clock is selectable via PWMCON with one of the following values: UCLK divided by 2, 4, 8, 16, 32, 64, 128, or 256. The length of a PWM period is defined by PWMxLEN.

The PWM waveforms are set by the count value of the 16-bit timer and the compare registers contents as shown with the PWM0 and PWM1 waveforms in Figure 25.

The low-side waveform, PWM1, goes high when the timer count reaches PWM0LEN, and it goes low when the timer count reaches the value held in PWM0COM2 or when the high-side waveform (PWM0) goes low.

The high-side waveform, PWM0, goes high when the timer count reaches the value held in PWM0COM0, and it goes low when the timer count reaches the value held in PWM0COM1.

Table 82. PWMCON MMR Bit Designations

Bit	Name	Description
14	Sync	Enables PWM synchronization. Set to 1 by user so that all PWM counters are reset on the next clock edge after the detection of a high-to-low transition on the P1.2/SYNC pin. Cleared by user to ignore transitions on the P1.2/SYNC pin.
13	PWM5INV	Set to 1 by user to invert PWM5. Cleared by user to use PWM5 in normal mode.
12	PWM3NV	Set to 1 by user to invert PWM3. Cleared by user to use PWM3 in normal mode.
11	PWM1INV	Set to 1 by user to invert PWM1. Cleared by user to use PWM1 in normal mode.
10	PWMTRIP	Set to 1 by user to enable PWM trip interrupt. When the PWMTRIP input is low, the PWMEN bit is cleared and an interrupt is generated. Cleared by user to disable the PWMTRIP interrupt.
9	ENA	If HOFF = 0 and HMODE = 1. Note that, if not in H-bridge mode, this bit has no effect. Set to 1 by user to enable PWM outputs. Cleared by user to disable PWM outputs. If HOFF = 1 and HMODE = 1, see Table 83.
8:6	PWMCP[2:0]	PWM clock prescaler bits. Sets the UCLK divider. [000] = UCLK/2. [001] = UCLK/4. [010] = UCLK/8. [011] = UCLK/16. [100] = UCLK/32. [101] = UCLK/64. [110] = UCLK/128. [111] = UCLK/256.
5	POINV	Set to 1 by user to invert all PWM outputs. Cleared by user to use PWM outputs as normal.
4	HOFF	High side off. Set to 1 by user to force PWM0 and PWM2 outputs high. This also forces PWM1 and PWM3 low. Cleared by user to use the PWM outputs as normal.
3	LCOMP	Load compare registers. Set to 1 by user to load the internal compare registers with the values in PWMxCOMx on the next transition of the PWM timer from 0x00 to 0x01. Cleared by user to use the values previously stored in the internal compare registers.
2	DIR	Direction control. Set to 1 by user to enable PWM0 and PWM1 as the output signals while PWM2 and PWM3 are held low. Cleared by user to enable PWM2 and PWM3 as the output signals while PWM0 and PWM1 are held low.
1	HMODE	Enables H-bridge mode.[1] Set to 1 by user to enable H-bridge mode and Bit 1 to Bit 5 of PWMCON. Cleared by user to operate the PWMs in standard mode.
0	PWMEN	Set to 1 by user to enable all PWM outputs. Cleared by user to disable all PWM outputs.

[1] In H-bridge mode, HMODE = 1. See Table 83 to determine the PWM outputs.

On power-up, PWMCON defaults to 0x0012 (HOFF = 1 and HMODE = 1). All GPIO pins associated with the PWM are configured in PWM mode by default (see Table 84). Clear the PWM trip interrupt by writing any value to the PWMICLR MMR. Note that when using the PWM trip interrupt, clear the PWM interrupt before exiting the ISR. This prevents generation of multiple interrupts.

Table 83. PWM Output Selection

PWMCOM0 MMR[1]				PWM Outputs[2]			
ENA	**HOFF**	**POINV**	**DIR**	**PWM0**	**PWM1**	**PWMR2**	**PWM3**
0	0	X	X	1	1	1	1
X	1	X	X	1	0	1	0
1	0	0	0	0	0	HS1	LS1
1	0	0	1	HS1	LS1	0	0
1	0	1	0	HS1	LS1	1	1
1	0	1	1	1	1	HS1	LS1

[1] X is don't care.
[2] HS = high side, LS = low side.

Table 84. Compare Register

Name	Address	Default Value	Access
PWM0COM0	0xFFFF0F84	0x0000	R/W
PWM0COM1	0xFFFF0F88	0x0000	R/W
PWM0COM2	0xFFFF0F8C	0x0000	R/W
PWM1COM0	0xFFFF0F94	0x0000	R/W
PWM1COM1	0xFFFF0F98	0x0000	R/W
PWM1COM2	0xFFFF0F9C	0x0000	R/W
PWM2COM0	0xFFFF0FA4	0x0000	R/W
PWM2COM1	0xFFFF0FA8	0x0000	R/W
PWM2COM2	0xFFFF0FAC	0x0000	R/W

PWM0COM0 Compare Register

Name: PWM0COM0

Address: 0xFFFF0F84

Default value: 0x0000

Access: Read and write

Function: PWM0 output pin goes high when the PWM timer reaches the count value stored in this register.

PWM0COM1 Compare Register

Name: PWM0COM1

Address: 0xFFF0F88

Default value: 0x0000

Access: Read and write

Function: PWM0 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM0COM2 Compare Register

Name: PWM0COM2

Address: 0xFFF0F8C

Default value: 0x0000

Access: Read and write

Function: PWM1 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM0LEN Register

Name: PWM0LEN

Address: 0xFFF0F90

Default value: 0x0000

Access: Read and write

Function: PWM1 output pin goes high when the PWM timer reaches the value stored in this register.

PWM1COM0 Compare Register

Name: PWM1COM0

Address: 0xFFF0F94

Default value: 0x0000

Access: Read and write

Function: PWM2 output pin goes high when the PWM timer reaches the count value stored in this register.

PWM1COM1 Compare Register

Name: PWM1COM1

Address: 0xFFF0F98

Default value: 0x0000

Access: Read and write

Function: PWM2 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM1COM2 Compare Register

Name: PWM1COM2

Address: 0xFFF0F9C

Default value: 0x0000

Access: Read and write

Function: PWM3 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM1LEN Register

Name: PWM1LEN

Address: 0xFFF0FA0

Default value: 0x0000

Access: Read and write

Function: PWM3 output pin goes high when the PWM timer reaches the value stored in this register.

PWM2COM0 Compare Register

Name: PWM2COM0

Address: 0xFFF0FA4

Default value: 0x0000

Access: Read and write

Function: PWM4 output pin goes high when the PWM timer reaches the count value stored in this register.

PWM2COM1 Compare Register

Name: PWM2COM1

Address: 0xFFF0FA8

Default value: 0x0000

Access: Read and write

Function: PWM4 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM2COM2 Compare Register

Name: PWM2COM2

Address: 0xFFF0FAC

Default value: 0x0000

Access: Read and write

Function: PWM5 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM1LEN Register

Name: PWM2LEN

Address: 0xFFF0FB0

Default value: 0x0000

Access: Read and write

Function: PWM5 output pin goes high when the PWM timer reaches the value stored in this register.

PWMCLRI Register

Name: PWMCLRI

Address: 0xFFF0FB8

Default value: 0x0000

Access: Write only

Function: Write any value to this register to clear a PWM interrupt source. This register must be written to before exiting a PWM interrupt service routine; otherwise, multiple interrupts occur.

UART SERIAL INTERFACE

The ADuC7060 features a 16,450-compatible UART. The UART is a full-duplex, universal, asynchronous receiver/transmitter. A UART performs serial-to-parallel conversion on data characters received from a peripheral device and parallel-to-serial conversion on data characters received from the ARM7TDMI. The UART features a fractional divider that facilitates high accuracy baud rate generation and a network addressable mode. The UART functionality is available on the P1.0/IRQ1/SIN/T0 and P1.1/SOUT pins of the ADuC7060.

The serial communication adopts an asynchronous protocol that supports various word length, stop bits, and parity generation options selectable in the configuration register.

BAUD RATE GENERATION

The ADuC7060 features two methods of generating the UART baud rate: normal 450 UART baud rate generation and ADuC7060 fractional divider.

Normal 450 UART Baud Rate Generation

The baud rate is a divided version of the core clock using the value in COMDIV0 and COMDIV1 MMRs (16-bit value, DL). The standard baud rate generator formula is

$$Baud\ Rate = \frac{10.24\ \text{MHz}}{16 \times 2 \times DL} \quad (1)$$

Table 85 lists common baud rate values.

Table 85. Baud Rate Using the Standard Baud Rate Generator

Baud Rate	CD	DL	Actual Baud Rate	% Error
9600	0	0x21	9696	1.01%
19,200	0	0x11	18,824	1.96%
115,200	0	0x3	106,667	7.41%
9600	3	0x4	10,000	4.17%
19,200	3	0x2	20,000	4.17%

ADuC7060 Fractional Divider

The fractional divider combined with the normal baud rate generator allows the generation of accurate high speed baud rates.

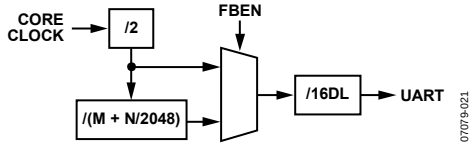


Figure 26. Fractional Divider Baud Rate Generation

Calculation of the baud rate using a fractional divider is as follows:

$$Baud\ Rate = \frac{10.24\ \text{MHz}}{16 \times DL \times 2 \times (M + \frac{N}{2048})} \quad (2)$$

$$M + \frac{N}{2048} = \frac{10.24\ \text{MHz}}{Baud\ Rate \times 16 \times DL \times 2}$$

Table 86 lists common baud rate values.

Table 86. Baud Rate Using the Fractional Baud Rate Generator

Baud Rate	CD	DL	M	N	Actual Baud Rate	% Error
9600	0	0x21	1	21	9598.55	0.015%
19,200	0	0x10	1	85	19,203	0.015%
115,200	0	0x2	1	796	115,218	0.015%

UART REGISTER DEFINITION

The UART interface consists of the following nine registers:

COMTX: 8-bit transmit register
COMRX: 8-bit receive register
COMDIV0: divisor latch (low byte)
COMDIV1: divisor latch (high byte)
COMCON0: line control register
COMSTA0: line status register
COMIEN0: interrupt enable register
COMIID0: interrupt identification register
COMDIV2: 16-bit fractional baud divide register

COMTX, COMRX, and COMDIV0 share the same address location. COMTX and COMRX can be accessed when Bit 7 in the COMCON0 register is cleared. COMDIV0 can be accessed when Bit 7 of COMCON0 is set.

UART Transmit Register

Write to this 8-bit register (COMTX) to transmit data using the UART.

COMTX Register

Name: COMTX

Address: 0xFFFF0700

Access: Write only

UART Receive Register

This 8-bit register (COMRX) is read to receive data transmitted using the UART.

COMRX Register

Name: COMRX

Address: 0xFFFF0700

Default value: 0x00

Access: Read only

UART Divisor Latch Register 0

This 8-bit register (COMDIV0) contains the least significant byte of the divisor latch that controls the baud rate at which the UART operates.

COMDIV0 Register

Name: COMDIV0

Address: 0xFFFF0700

Default value: 0x00

Access: Read and write

UART Divisor Latch Register 1

This 8-bit register contains the most significant byte of the divisor latch that controls the baud rate at which the UART operates.

COMDIV1 Register

Name: COMDIV1

Address: 0xFFFF0704

Default value: 0x00

Access: Read and write

UART Control Register 0

This 8-bit register (COMCON0) controls the operation of the UART in conjunction with COMCON1.

COMCON0 Register

Name: COMCON0

Address: 0xFFFF070C

Default value: 0x00

Access: Read and write

Table 87. COMCON0 MMR Bit Designations

Bit	Name	Description
7	DLAB	Divisor latch access. Set by user to enable access to the COMDIV0 and COMDIV1 registers. Cleared by user to disable access to COMDIV0 and COMDIV1 and enable access to COMRX, COMTX, and COMIEN0.
6	BRK	Set break. Set by user to force transmit to 0. Cleared to operate in normal mode.
5	SP	Stick parity. Set by user to force parity to defined values. 1 if EPS = 1 and PEN = 1. 0 if EPS = 0 and PEN = 1.
4	EPS	Even parity select bit. Set for even parity. Cleared for odd parity.
3	PEN	Parity enable bit. Set by user to transmit and check the parity bit. Cleared by user for no parity transmission or checking.
2	Stop	Stop bit. Set by user to transmit 1.5 stop bits if the word length is 5 bits, or 2 stop bits if the word length is 6 bits, 7 bits, or 8 bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by user to generate one stop bit in the transmitted data.
1:0	WLS	Word length select. 00 = 5 bits. 01 = 6 bits. 10 = 7 bits. 11 = 8 bits.

UART Control Register 1

This 8-bit register controls the operation of the UART in conjunction with COMCON0.

Name: COMCON1

Address: 0xFFFF0710

Default value: 0x00

Access: Read and write

Table 88. COMCON1 MMR Bit Designations

Bit	Name	Description
7:5		Reserved bits. Not used.
4	LOOPBACK	Loopback. Set by user to enable loopback mode. In loopback mode, the transmit pin is forced high.
3:2		Reserved bits. Not used.
1	RTS	Request to send. Set by user to force the RTS output to 0. Cleared by user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by user to force the DTR output to 0. Cleared by user to force the DTR output to 1.

UART Status Register 0

COMSTA0 Register

Name: COMSTA0

Address: 0xFFFF0714

Default value: 0x60

Access: Read only

Function: This 8-bit read-only register reflects the current status on the UART.

Table 89. COMSTA0 MMR Bit Designations

Bit	Name	Description
7		Reserved.
6	TEMT	COMTX and shift register empty status bit. Set automatically if COMTX and the shift register are empty. This bit indicates that the data has been transmitted, that is, no more data is present in the shift register. Cleared automatically when writing to COMTX.
5	THRE	COMTX empty status bit. Set automatically if COMTX is empty. COMTX can be written as soon as this bit is set, the previous data might not have been transmitted yet and can still be present in the shift register. Cleared automatically when writing to COMTX.
4	BI	Break indicator. Set when P1.0/IRQ1/SIN/T0 pin is held low for more than the maximum word length. Cleared automatically.
3	FE	Framing error. Set when the stop bit is invalid. Cleared automatically.
2	PE	Parity error. Set when a parity error occurs. Cleared automatically.
1	OE	Overrun error. Set automatically if data are overwritten before being read. Cleared automatically.
0	DR	Data ready. Set automatically when COMRX is full. Cleared by reading COMRX.

UART Status Register 1

COMSTA1 Register

Name: COMSTA1

Address: 0xFFFF0718

Default value: 0x00

Access: Read only

Function: COMSTA1 is a modem status register.

Table 90. COMSTA1 MMR Bit Descriptions

Bit	Name	Description
7:5		Reserved. Not used.
4	CTS	Clear to send.
3:1		Reserved. Not used.
0	DCTS	Delta CTS. Set automatically if CTS changed state since COMSTA1 was last read. Cleared automatically by reading COMSTA1.

UART Interrupt Enable Register 0

COMIEN0 Register

Name: COMIEN0

Address: 0xFFFF0704

Default value: 0x00

Access: Read and write

Function: The 8-bit register enables and disables the individual UART interrupt sources.

Table 91. COMIEN0 MMR Bit Designations

Bit	Name	Description
7:4		Reserved. Not used.
3	EDSSI	Modem status interrupt enable bit. Set by user to enable generation of an interrupt if any of COMSTA1[3:1] are set. Cleared by user.
2	ELSI	Receive status interrupt enable bit. Set by user to enable generation of an interrupt if any of the COMSTA0[3:1] register bits are set. Cleared by user.
1	ETBEI	Enable transmit buffer empty interrupt. Set by user to enable an interrupt when the buffer is empty during a transmission; that is, when COMSTA[5] is set. Cleared by user.
0	ERBFI	Enable receive buffer full interrupt. Set by user to enable an interrupt when the buffer is full during a reception. Cleared by user.

UART Interrupt Identification Register 0

COMIID0 Register

Name: COMIID0

Address: 0xFFFF0708

Default value: 0x01

Access: Read only

Function: This 8-bit register reflects the source of the UART interrupt.

Table 92. COMIID0 MMR Bit Designations

Status Bits[2:1]	Bit 0	Priority	Definition	Clearing Operation
00	1		No interrupt	
11	0	1	Receive line status interrupt	Read COMSTA0
10	0	2	Receive buffer full interrupt	Read COMRX
01	0	3	Transmit buffer empty interrupt	Write data to COMTX or read COMIID0
00	0	4	Modem status interrupt	Read COMSTA1 register

UART Fractional Divider Register

This 16-bit register (COMDIV2) controls the operation of the fractional divider for the ADuC7060.

COMDIV2 Register

Name: COMDIV2

Address: 0xFFFF072C

Default value: 0x0000

Access: Read and write

Table 93. COMDIV2 MMR Bit Designations

Bit	Name	Description
15	FBEN	Fractional baud rate generator enable bit. Set by user to enable the fractional baud rate generator. Cleared by user to generate the baud rate using the standard 450 UART baud rate generator.
14:13		Reserved.
12:11	FBM[1:0]	M. If FBM = 0, M = 4. See Equation 2 for the calculation of the baud rate using a fractional divider and Table 85 for common baud rate values.
10:0	FBN[10:0]	N. See Equation 2 for the calculation of the baud rate using a fractional divider and Table 85 for common baud rate values.

I²C

The ADuC7060 incorporates an I²C peripheral that can be configured as a fully I²C-compatible I²C bus master device or as a fully I²C bus-compatible slave device. The two pins used for data transfer, SDA and SCL, are configured in a wire-AND'ed format that allows arbitration in a multimaster system. These pins require external pull-up resistors. Typical pull-up values are between 4.7 kΩ and 10 kΩ.

Users program the I²C bus peripheral (addressed in the I²C bus system). This ID can be modified any time a transfer is not in progress. The user can configure the interface to respond to four slave addresses.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the slave device address and the direction of the data transfer (read or write) during the initial address transfer. If the master does not lose arbitration and the slave acknowledges, the data transfer is initiated. This continues until the master issues a stop condition and the bus becomes idle.

The I²C peripheral can be configured only as a master or slave at any given time. The same I²C channel cannot simultaneously support master and slave modes.

The I²C interface on the ADuC7060 includes the following features:

- Support for repeated start conditions. In master mode, the ADuC7060 can be programmed to generate a repeated start. In slave mode, the ADuC7060 recognizes repeated start conditions.
- In master and slave mode, the part recognizes both 7-bit and 10-bit bus addresses.
- In I²C master mode, the ADuC7060 supports continuous reads from a single slave up to 512 bytes in a single transfer sequence.
- Clock stretching is supported in both master and slave modes.
- In slave mode, the ADuC7060 can be programmed to return a no acknowledge (NACK). This allows the validiation of checksum bytes at the end of I²C transfers.
- Bus arbitration in master mode is supported.
- Internal and external loopback modes are supported for I²C hardware testing.
- The transmit and receive circuits in both master and slave mode contain 2-byte FIFOs. Status bits are available to the user to control these FIFOs.

Configuring External Pins for I²C Functionality

The I²C function of the P0.1/SCLK/SCL and P0.3/MOSI/SDA pins of the ADuC7060 device are P0.1 and P0.3. The function of P0.1 is the I²C clock signal and the function of P0.3 is the I²C data signal. To configure P0.1 and P0.3 for I²C mode, Bit 1 and Bit 3 of the GP0CON0 register must be set to 1. Bit 1 of the GP0CON1 register must also be set to 1 to enable I²C mode.

Note that, to write to GP0CON1, the GP0KEY1 register must be set to 0x7 immediately before writing to GP0CON1. Also, the GP0KEY2 register must be set to 0x13 immediately after writing to GP0CON1. The following code example shows this in detail:

```
GP0CON0 = BIT4 + BIT12;    // Select SPI/I²C alternative function for P0.1 and P0.3
GP0KEY1 = 0x7;             // Write to GP0KEY1
GP0CON1 = BIT1;            // Select I²C functionality for P0.1 and P0.3
GP0KEY2 = 0x13;            // Write to GP0KEY2
```

SERIAL CLOCK GENERATION

The I²C master in the system generates the serial clock for a transfer. The master channel can be configured to operate in fast mode (400 kHz) or standard mode (100 kHz).

The bit rate is defined in the I2CDIV MMR as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{(2 + DIVH) + (2 + DIVL)}$$

where:
f_{UCLK} is the clock before the clock divider.
DIVH is the the high period of the clock.
DIVL is the the low period of the clock.

Thus, for 100 kHz operation

DIVH = *DIVL* = 0x33

and for 400 kHz

DIVH = 0x0A, *DIVL* = 0x0F

The I2CDIV register corresponds to DIVH:DIVL.

I²C BUS ADDRESSES

Slave Mode

In slave mode, the I2CID0, I2CID1, I2CID2, and I2CID3 registers contain the device IDs. The device compares the four I2CIDx registers to the address byte received from the bus master. To be correctly addressed, the 7 MSBs of either ID register must be identical to that of the 7 MSBs of the first received address byte. The least significant bit of the ID registers (the transfer direction bit) is ignored in the process of address recognition.

The ADuC7060 also supports 10-bit addressing mode. When Bit 1 of I2CSCON (ADR10EN bit) is set to 1, then one 10-bit address is supported in slave mode and is stored in the I2CID0 and I2CID1 registers. The 10-bit address is derived as follows:

I2CID0[0] is the read/write bit and is not part of the I²C address.

I2CID0[7:1] = Address Bits[6:0].

I2CID1[2:0] = Address Bits[9:7].

I2CID1[7:3] must be set to 11110b

Master Mode

In master mode, the I2CADR0 register is programmed with the I²C address of the device.

In 7-bit address mode, I2CADR0[7:1] are set to the device address. I2CADR0[0] is the read/write bit.

In 10-bit address mode, the 10-bit address is created as follows:

I2CADR0[7:3] must be set to 11110b.

I2CADR0[2:1] = Address Bits[9:8].

I2CADR1[7:0] = Address Bits[7:0].

I2CADR0[0] is the read/write bit.

I²C REGISTERS

The I²C peripheral interface consists overall of 19 MMRs. Ten of these are master related only, seven are slave related only, and two MMRs are common to both master and slave modes.

I²C Master Registers

I²C Master Control, I2CMCON Register

Name: I2CMCON

Address: 0xFFFF0900

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR configures the I²C peripheral in master mode.

Table 94. I2CMCON MMR Bit Designations

Bit	Name	Description
15:9		Reserved. These bits are reserved and should not be written to.
8	I2CMCENI	I^2C transmission complete interrupt enable bit. Set this bit to enable an interrupt on detecting a stop condition on the I^2C bus. Clear this interrupt source.
7	I2CNACKENI	I^2C no acknowledge (NACK) received interrupt enable bit. Set this bit to enable interrupts when the I^2C master receives a no acknowledge. Clear this interrupt source.
6	I2CALENI	I^2C arbitration lost interrupt enable bit. Set this bit to enable interrupts when the I^2C master did not gain control of the I^2C bus. Clear this interrupt source.
5	I2CMTENI	I^2C transmit interrupt enable bit. Set this bit to enable interrupts when the I^2C master has transmitted a byte. Clear this interrupt source.
4	I2CMRENI	I^2C receive interrupt enable bit. Set this bit to enable interrupts when the I^2C master receives data. Cleared by user to disable interrupts when the I^2C master is receiving data.
3	I2CMSEN	I^2C master SCL stretch enable bit. Set this bit to 1 to enable clock stretching. When SCL is low, setting this bit forces the device to hold SCL low until I2CMSEN is cleared. If SCLis high, setting this bit forces the device to hold SCL low after the next falling edge. Clear this bit to disable clock stretching.
2	I2CILEN	I^2C internal loopback enable. Set this bit to enable loopback test mode. In this mode, the SCL and SDA signals are connected internally to their respective input signals. Cleared by user to disable loopback mode.
1	I2CBD	I^2C master backoff disable bit. Set this bit to allow the device to compete for control of the bus even if another device is currently driving a start condition. Clear this bit to back off until the I^2C bus becomes free.
0	I2CMEN	I^2C master enable bit. Set by user to enable I^2C master mode. Cleared to disable the I^2C master mode.

I²C Master Status, I2CMSTA, Register

Name: I2CMSTA

Address: 0xFFFF0904

Default value: 0x0000

Access: Read only

Function: This 16-bit MMR is the ²C status register in master mode.

Table 95. I2CMSTA MMR Bit Designations

Bit	Name	Description
15 to 11		Reserved. These bits are reserved.
10	I2CBBUSY	I²C bus busy status bit. This bit is set to 1 when a start condition is detected on the I²C bus. This bit is cleared when a stop condition is detected on the bus.
9	I2CMRxFO	Master receive FIFO overflow. This bit is set to 1 when a byte is written to the r eceive FIFO when it is already full. This bit is cleared in all other conditions.
8	I2CMTC	I²C transmission complete status bit. This bit is set to 1 when a transmission is complete between the master and the slave with which it was communicating. If the I2CMCENI bit in I2CMCON is set, an interrupt is generated when this bit is set. Clear this interrupt source.
7	I2CMNA	I²C master no acknowledge data bit This bit is set to 1 when a no acknowledge condition is received by the master in response to a data write transfer. If the I2CNACKENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
6	I2CMBUSY	I²C master busy status bit. Set to 1 when the master is busy processing a transaction. Cleared if the master is ready or if another master device has control of the bus.
5	I2CAL	I²C arbitration lost status bit. This bit is set to 1 when the I²C master did not gain control of the I²C bus. If the I2CALENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
4	I2CMNA	I²C master no acknowledge address bit. This bit is set to 1 when a no acknowledge condition is received by the master in response to an address. If the I2CNACKENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit clears in all other conditions.
3	I2CMRXQ	I²C master receive request bit. This bit is set to 1 when data enters the ReceiveFIFO. If the I2CMRENI in I2CMCON is set, an interrupt is generated. This bit is cleared in all other conditions.
2	I2CMTXQ	I²C master transmit request bit. This bit goes high if the transmit FIFO is empty or contains only 1 byte and the master has transmitted an address + write. If the I2CMTENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
1 to 0	I2CMTFSTA	I²C master transmit FIFO status bits. 00 = I²C master transmit FIFO empty. 01 = 1 byte in master transmit FIFO. 10 = 1 byte in master transmit FIFO. 11 = I²C master transmit FIFO full.

I²C Master Receive, I2CMRX, Register

Name: I2CMRX

Address: 0xFFFF0908

Default value: 0x00

Access: Read only

Function: This 8-bit MMR is the I²C master receive register.

I²C Master Transmit, I2CMTX, Register

Name: I2CMTX

Address: 0xFFFF090C

Default value: 0x00

Access: Write only

Function: This 8-bit MMR is the I²C master transmit register.

I²C Master Read Count, I2CMCNT0, Register

Name: I2CMCNT0

Address: 0xFFFF0910

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR holds the required number of bytes when the master begins a read sequence from a slave device.

Table 96. I2CMCNT0 MMR Bit Descriptions

Bit	Name	Description
15:9		Reserved.
8	I2CRECNT	Set this bit if more than 256 bytes are required from the slave. Clear this bit when reading 256 bytes or fewer.
7:0	I2CRCNT	These eight bits hold the number of bytes required during a slave read sequence, minus 1. If only a single byte is required, set these bits to 0.

I²C Master Current Read Count, I2CMCNT1, Register

Name: I2CMCNT1

Address: 0xFFFF0914

Default value: 0x00

Access: Read only

Function: This 8-bit MMR holds the number of bytes received so far during a read sequence with a slave device.

I²C Address 0, I2CADR0, Register

Name: I2CADR0

Address: 0xFFFF0918

Default value: 0x00

Access: Read and write

Function: This 8-bit MMR holds the 7-bit slave address and the read/write bit when the master begins communicating with a slave.

Table 97. I2CADR0 MMR in 7-Bit Address Mode

Bit	Name	Description
7:1	I2CADR	These bits contain the 7-bit address of the required slave device.
0	R/$\overline{W}$	Bit 0 is the read/write bit. When this bit = 1, a read sequence is requested. When this bit = 0, a write sequence is requested.

Table 98. I2CADR0 MMR in 10-Bit Address Mode

Bit	Name	Description
7:3		These bits must be set to [11110b] in 10-bit address mode.
2:1	I2CMADR	These bits contain ADDR[9:8] in 10-bit addressing mode.
0	R/$\overline{W}$	Read/write bit. When this bit = 1, a read sequence is requested. When this bit = 0, a write sequence is requested.

I²C Address 1, I2CADR1, Register

Name: I2CADR1

Address: 0xFFFF091C

Default value: 0x00

Access: Read and write

Function: This 8-bit MMR is used in 10-bit addressing mode only. This register contains the least significant byte of the address.

Table 99. I2CADR1 MMR in 10-Bit Address Mode

Bit	Name	Description
7:0	I2CLADR	These bits contain ADDR[7:0] in 10-bit addressing mode.

I²C Master Clock Control, I2CDIV, Register

Name: I2CDIV

Address: 0xFFFF0924

Default value: 0x1F1F

Access: Read and write

Function: This MMR controls the frequency of the I²C clock generated by the master on to the SCL pin. For further details, see the Serial Clock Generation section.

Table 100. I2CDIV MMR

Bit	Name	Description
15:8	DIVH	These bits control the duration of the high period of SCL.
7:0	DIVL	These bits control the duration of the low period of SCL.

I²C Slave Registers

I²C Slave Control, I2CSCON, Register

Name: I2CSCON

Address: 0xFFFF0928

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR configures the I²C peripheral in slave mode.

Table 101. I2CSCON MMR Bit Designations

Bit	Name	Description
15 to 11		Reserved bits.
10	I2CSTXENI	Slave transmit interrupt enable bit. Set this bit to enable an interrupt after a slave transmits a byte. Clear this interrupt source.
9	I2CSRXENI	Slave receive interrupt enable bit. Set this bit to enable an interrupt after the slave receives data. Clear this interrupt source.
8	I2CSSENI	I^2C stop condition detected interrupt enable bit. Set this bit to enable an interrupt on detecting a stop condition on the I^2C bus. Clear this interrupt source.
7	I2CNACKEN	I^2C no acknowledge enable bit. Set this bit to no acknowledge the next byte in the transmission sequence. Clear this bit to let the hardware control the acknowledge/no acknowledge sequence.
6	I2CSSEN	I^2C slave SCL stretch enable bit. Set this bit to 1 to enable clock stretching. When SCL is low, setting this bit forces the device to hold SCL low until I2CSSEN is cleared. If SCL is high, setting this bit forces the device to hold SCL low after the next falling edge. Clear this bit to disable clock stretching.
5	I2CSETEN	I^2C early transmit interrupt enable bit. Setting this bit enables a transmit request interrupt just after the positive edge of SCL during the read bit transmission. Clear this bit to enable a transmit request interrupt just after the negative edge of SCL during the read bit transmission.
4	I2CGCCLR	I^2C general call status and ID clear bit. Writing a 1 to this bit clears the general call status and ID bits in the I2CSSTA register. Clear this bit at all other times.
3	I2CHGCEN	Hardware general call enable. When this bit and Bit 2 are set, and having received a general call (Address 0x00) and a data byte, the device checks the contents of the I2CALT against the receive register. If the contents match, the device has received a hardware general call. This is used if a device needs urgent attention from a master device without knowing which master it needs to turn to. This is a "to whom it may concern" call. The ADuC7060 watches for these addresses. The device that requires attention embeds its own address into the message. All masters listen, and the one that can handle the device contacts its slave and acts appropriately. The LSB of the I2CALT register should always be written to 1, as per the I^2C January 2000 bus specification.
2	I2CGCEN	General call enable bit. Set this bit to enable the slave device to acknowledge an I^2C general call, Address 0x00 (write). The device then recognizes a data bit. If it receives a 0x06 (reset and write programmable part of the slave address by hardware) as teh data byte, the I^2C interface resets as per the I^2C January 2000 bus specification. This command can be used to reset an entire I^2C system. If it receives a 0x04 (write programmable part of the slave address by hardware) as the data byte, teh general call interrupt status bit sets on any general call. The user must take corrective action by reprogramming the device address.
1	Reserved	Always set this bit = 0.
0	I2CSEN	I^2C slave enable bit. Set by user to enable I^2C slave mode. Clear to disable I^2C slave mode.

I²C Slave Status, I2CSSTA, Register

Name: I2CSSTA

Address: 0xFFFF092C

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR is the I²C status register in slave mode.

Table 102. I2CSSTA MMR Bit Designations

Bit	Name	Description
15		Reserved bit.
14	I2CSTA	This bit is set to 1 if a start condition followed by a matching address is detected, a start byte (0x01) is received, or general calls are enabled and a general call code of 0x00 is received. This bit is cleared on receiving a stop condition
13	I2CREPS	This bit is set to 1 if a repeated start condition is detected. This bit is cleared on receiving a stop condition.
12 to 11	I2CID[1:0]	I²C address matching register. These bits indicate which I2CIDx register matches the received address. [00] = received address matches I2CID0. [01] = received address matches I2CID1. [10] = received address matches I2CID2. [11] = received address matches I2CID3.
10	I2CSS	I²C stop condition after start detected bit. This bit is set to 1 when a stop condition is detected after a previous start and matching address. When the I2CSSENI bit in I2CSCON is set, an interrupt is generated. This bit is cleared by reading this register.
9 to 8	I2CGCID[1:0]	I²C general call ID bits. [00] = no general call received. [01] = general call reset and program address. [10] = general program address. [11] = general call matching alternative ID. Note that these bits are not cleared by a general call reset command. Clear these bits by writing a 1 to the I2CGCCLR bit in I2CSCON.
7	I2CGC	I²C general call status bit. This bit is set to 1 if the slave receives a general call command of any type. If the command received was a reset command, then all registers return to their default states. If the command received was a hardware general call, the receive FIFO holds the second byte of the command, and this can be compared with the I2CALT register. Clear this bit by writing a 1 to the I2CGCCLR bit in I2CSCON.
6	I2CSBUSY	I²C slave busy status bit. Set to 1 when the slave receives a start condition. Cleared by hardware if the received address does not match any of the I2CIDx registers, the slave device receives a stop condition, or a repeated start address does not match any of the I2CIDx registers.
5	I2CSNA	I²C slave no acknowledge data bit. This bit is set to 1 when the slave responds to a bus address with a no acknowledge. This bit is asserted under the following conditions: if a no acknowledge was returned because there was no data in the Tx FIFO or if the I2CNACKEN bit was set in the I2CSCON register. This bit is cleared in all other conditions.
4	I2CSRxFO	Slave receive FIFO overflow. This bit is set to 1 when a byte is written to the receive FIFO when it is already full. This bit is cleared in all other conditions.

Bit	Name	Description
3	I2CSRXQ	I²C slave receive request bit. This bit is set to 1 when the receive FIFO of the slave is not empty. This bit causes an interrupt to occur if the I2CSRXENI bit in I2CSCON is set. The receive FIFO must be read or flushed to clear this bit.
2	I2CSTXQ	I²C slave transmit request bit. This bit is set to 1 when the slave receives a matching address followed by a read. If the I2CSETEN bit in I2CSCON is =0, this bit goes high just after the negative edge of SCL during the read bit transmission. If the I2CSETEN bit in I2CSCON is =1, this bit goes high just after the positive edge of SCL during the read bit transmission. This bit causes an interrupt to occur if the I2CSTXENI bit in I2CSCON is set. This bit is cleared in all other conditions.
1	I2CSTFE	I²C slave FIFO underflow status bit. This bit goes high if the transmit FIFO is empty when a master requests data from the slave. This bit is asserted at the rising edge of SCL during the read bit. This bit is cleared in all other conditions.
0	I2CETSTA	I²C slave early transmit FIFO status bit. If the I2CSETEN bit in I2CSCON is =0, this bit goes high if the slave transmit FIFO is empty. If the I2CSETEN bit in I2CSCON = 1, this bit goes high just after the positive edge of SCL during the write bit transmission. This bit asserts once only for a transfer. This bit is cleared after being read.

I²C Slave Receive, I2CSRX, Register

Name: I2CSRX

Address: 0xFFFF0930

Default value: 0x00

Access: Read only

Function: This 8-bit MMR is the I²C slave receive register.

I²C Slave Transmit, I2CSTX, Register

Name: I2CSTX

Address: 0xFFFF0934

Default value: 0x00

Access: Write only

Function: This 8-bit MMR is the I²C slave transmit register.

I²C Hardware General Call Recognition, I2CALT, Register

Name: I2CALT

Address: 0xFFFF0938

Default value: 0x00

Access: Read and write

Function: This 8-bit MMR is used with hardware general calls when the I2CSCON Bit 3 is set to 1. This register is used in cases where a master is unable to generate an address for a slave and, instead, the slave must generate the address for the master.

I²C Slave Device ID, I2CIDx, Registers

Name: I2CIDx

Addresses: 0xFFFF093C = I2CID0

0xFFFF0940 = I2CID1

0xFFFF0944 = I2CID2

0xFFFF0948 = I2CID3

Default value: 0x00

Access: Read and write

Function: These 8-bit MMRs are programmed with the I²C bus IDs of the slave. See the I²C Bus Addresses section for further details.

I²C Common Registers

I²C FIFO Status, I2CFSTA, Register

Name: I2CFSTA

Address: 0xFFFF094C

Default value: 0x0000

Access: Read and write

Function: These 16-bit MMRs contain the status of the receive/transmit FIFOs in both master and slave modes.

Table 103. I2CFSTA MMR Bit Designations

Bit	Name	Description
15:10		Reserved bits.
9	I2CFMTX	Set this bit to 1 to flush the master transmit FIFO.
8	I2CFSTX	Set this bit to 1 to flush the slave transmit FIFO.
7:6	I2CMRXSTA	I²C master receive FIFO status bits. [00] = FIFO empty. [01] = byte written to FIFO. [10] = 1 byte in FIFO. [11] = FIFO full.
5:4	I2CMTXSTA	I²C master transmit FIFO status bits. [00] = FIFO empty. [01] = byte written to FIFO. [10] = 1 byte in FIFO. [11] = FIFO full.
3:2	I2CSRXSTA	I²C slave receive FIFO status bits. [00] = FIFO empty [01] = byte written to FIFO [10] = 1 byte in FIFO [11] = FIFO full
1:0	I2CSTXSTA	I²C slave transmit FIFO status bits. [00] = FIFO empty. [01] = byte written to FIFO. [10] = 1 byte in FIFO. [11] = FIFO full.

SERIAL PERIPHERAL INTERFACE

The ADuC7060 integrates a complete hardware serial peripheral interface (SPI) on-chip. SPI is an industry standard, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received, that is, full duplex up to a maximum bit rate of 5.12 Mb.

The SPI port can be configured for master or slave operation and typically consists of four pins: MISO, MOSI, SCL, and $\overline{SS}$.

MISO (MASTER IN, SLAVE OUT) PIN

The MISO pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, most significant bit first.

MOSI (MASTER OUT, SLAVE IN) PIN

The MOSI pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, most significant bit first.

SCL (SERIAL CLOCK I/O) PIN

The master serial clock (SCL) synchronizes the data being transmitted and received through the MOSI SCL period. Therefore, a byte is transmitted/received after eight SCL periods. The SCL pin is configured as an output in master mode and as an input in slave mode.

In master mode, polarity and phase of the clock are controlled by the SPICON register, and the bit rate is defined in the SPIDIV register as follows:

$$f_{SERIAL\,CLOCK} = \frac{f_{UCLK}}{2\times(1+SPIDIV)}$$

The maximum speed of the SPI clock is independent on the clock divider bits.

In slave mode, the SPICON register must be configured with the phase and polarity of the expected input clock. The slave accepts data from an external master up to 5.12 Mb.

In both master and slave modes, data transmit on one edge of the SCL signal and sample on the other. Therefore, it is important that the polarity and phase be configured the same for the master and slave devices.

SLAVE SELECT (P0.0/$\overline{SS}$) INPUT PIN

In SPI slave mode, a transfer is initiated by the assertion of $\overline{SS}$ on the P0.0/$\overline{SS}$ pin, which is an active low input signal. The SPI port then transmits and receives 8-bit data until the transfer is concluded by deassertion of $\overline{SS}$. In slave mode, $\overline{SS}$ is always an input.

In SPI master mode, $\overline{SS}$ is an active low output signal. It asserts itself automatically at the beginning of a transfer and deasserts itself upon completion.

CONFIGURING EXTERNAL PINS FOR SPI FUNCTIONALITY

The SPI pins of the ADuC7060 device are represented by the P0[0:3] funtion of the following pins:

- P0.0/$\overline{SS}$ is the slave chip select pin. In slave mode, this pin is an input and must be driven low by the master. In master mode, this pin is an output and goes low at the beginning of a transfer and high at the end of a transfer.
- P0.1/SCLK/SCL is the SCL pin.
- P0.2/MISO is the master in, slave out (MISO) pin.
- P0.3/MOSI/SDA is the master out, slave in (MOSI) pin.

To configure P0.0 to P0.3 for SPI mode, Bit 0 to Bit 3 of the GP0CON0 register must be set to 1. Bit 1 of the GP0CON1 must be set to 1. Note that to write to GP0CON1, the GP0KEY1 register must be set to 0x7 immediately before writing to GP0CON1. Also, the GP0KEY2 register must be set to 0x13 immediately after writing to GP0CON1. The following code example shows this in detail:

```
GP0CON0 = BIT0 + BIT4 + BIT8 + BIT12;   //Select SPI/I²C alternative function for P0[0...3]
GP0KEY1 = 0x7;                          //Write to GP0KEY1
GP0CON1 &=~ BIT1;                       //Select SPI functionality for P0.0 to  P0.3
GP0KEY2 = 0x13;                         //Write to GP0KEY2
```

SPI REGISTERS

The following MMR registers control the SPI interface: SPISTA, SPIRX, SPITX, SPIDIV, and SPICON.

SPI Status Register

SPISTA Register

Name: SPISTA

Address: 0xFFFF0A00

Default value: 0x00000000

Access: Read only

Function: This 32-bit MMR contains the status of the SPI interface in both master and slave modes.

Table 104. SPISTA MMR Bit Designations

Bit	Name	Description
15:12		Reserved bits.
11	SPIREX	SPI receive FIFO excess bytes present. This bit is set when there are more bytes in the receive FIFO than indicated in the SPIRXMDE bits in SPICON. This bit is cleared when the number of bytes in the FIFO is equal to or less than the number in SPIRXMDE.
10:8	SPIRXFSTA[2:0]	SPI receive FIFO status bits. [000] = receive FIFO is empty. [001] = 1 valid byte in the FIFO. [010] = 2 valid byte in the FIFO. [011] = 3 valid byte in the FIFO. [100] = 4 valid byte in the FIFO.
7	SPIFOF	SPI receive FIFO overflow status bit. Set when the receive FIFO was already full when new data was loaded to the FIFO. This bit generates an interrupt except when SPIRFLH is set in SPICON. Cleared when the SPISTA register is read.
6	SPIRXIRQ	SPI receive IRQ status bit. Set when a receive interrupt occurs. This bit is set when SPITMDE in SPICON is cleared and the required number of bytes have been received. Cleared when the SPISTA register is read.
5	SPITXIRQ	SPI transmit IRQ status bit. Set when a transmit interrupt occurs. This bit is set when SPITMDE in SPICON is set and the required number of bytes have been transmitted. Cleared when the SPISTA register is read.
4	SPITXUF	SPI transmit FIFO underflow. This bit is set when a transmit is initiated without any valid data in the transmit FIFO. This bit generates an interrupt except when SPITFLH is set in SPICON. Cleared when the SPISTA register is read.
3:1	SPITXFSTA[2:0]	SPI transmit FIFO status bits. [000] = transmit FIFO is empty. [001] = 1 valid byte in the FIFO. [010] = 2 valid byte in the FIFO. [011] = 3 valid byte in the FIFO. [100] = 4 valid byte in the FIFO.
0	SPIISTA	SPI interrupt status bit. Set to 1 when an SPI based interrupt occurs. Cleared after reading SPISTA.

SPIRX Register

Name: SPIRX

Address: 0xFFFF0A04

Default value: 0x00

Access: Read only

Function: This 8-bit MMR is the SPI receive register.

SPITX Register

Name: SPITX

Address: 0xFFFF0A08

Default value: 0x00

Access: Write only

Function: This 8-bit MMR is the SPI transmit register.

SPIDIV Register

Name: SPIDIV

Address: 0xFFFF0A0C

Default value: 0x1B

Access: Write only

Function: This 8-bit MMR is the SPI baud rate selection register.

SPI Control Register

Name: SPICON

Address: 0xFFFF0A10

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR configures the SPI peripheral in both master and slave modes.

Table 105. SPICON MMR Bit Designations

Bit	Name	Description
15 to 14	SPIMDE	SPI IRQ mode bits. These bits configure when the transmit/receive interrupts occur in a transfer. [00] = transmit interrupt occurs when 1 byte has been transferred. Receive interrupt occurs when one or more bytes have been received into the FIFO. [01] = transmit interrupt occurs when 2 bytes have been transferred. Receive interrupt occurs when one or more bytes have been received into the FIFO. [10] = transmit interrupt occurs when 3 bytes have been transferred. Receive interrupt occurs when three or more bytes have been received into the FIFO. [11] = transmit interrupt occurs when 4 bytes have been transferred. Receive interrupt occurs when the receive FIFO is full or 4 bytes are present.
13	SPITFLH	SPI transmit FIFO flush enable bit. Set this bit to flush the transmit FIFO. This bit does not clear itself and should be toggled if a single flush is required. If this bit is left high, then either the last transmitted value or 0x00 is transmitted, depending on the SPIZEN bit. Any writes to the transmit FIFO are ignored while this bit is set. Clear this bit to disable transmit FIFO flushing.
12	SPIRFLH	SPI receive FIFO flush enable bit. Set this bit to flush the receive FIFO. This bit does not clear itself and should be toggled if a single flush is required. If this bit is set, all incoming data is ignored and no interrupts are generated. If set and SPITMDE = 0, a read of the receive FIFO initiates a transfer. Clear this bit to disable receive FIFO flushing.
11	SPICONT	Continuous transfer enable. Set by user to enable continuous transfer. In master mode, the transfer continues until no valid data is available in the transmit register. $\overline{SS}$ is asserted and remains asserted for the duration of each 8-bit serial transfer until the transmit register is empty. Cleared by user to disable continuous transfer. Each transfer consists of a single 8-bit serial transfer. If valid data exists in the SPITX register, then a new transfer is initiated after a stall period of one serial clock cycle.
10	SPILP	Loopback enable bit. Set by user to connect MISO to MOSI and test software. Cleared by user to be in normal mode.
9	SPIOEN	Slave MISO output enable bit. Set this bit for MISO to operate as normal. Clear this bit to disable the output driver on the MISO pin. The MISO pin is open drain when this bit is cleared.
8	SPIROW	SPIRX overflow overwrite enable. Set by user, the valid data in the receive register is overwritten by the new serial byte received. Cleared by user, the new serial byte received is discarded.
7	SPIZEN	SPI transmit zeros when transmit FIFO is empty. Set this bit to transmit 0x00 when there is no valid data in the transmit FIFO. Clear this bit to transmit the last transmitted value when there is no valid data in the transmit FIFO.
6	SPITMDE	SPI transfer and interrupt mode. Set by user to initiate transfer with a write to the SPITX register. Interrupt only occurs when Transmit is empty. Cleared by user to initiate transfer with a read of the SPIr register. Interrupt occurs only when the receive is full.
5	SPILF	LSB first transfer enable bit. Set by user, the LSB is transmitted first. Cleared by user, the MSB is transmitted first.
4	SPIWOM	SPI wired or mode enable bit. Set to 1 to enable the open-drain data output enable. External pull-ups are required on data out pins. Clear for normal output levels.
3	SPICPO	Serial clock polarity mode bit. Set by user, the serial clock idles high. Cleared by user, the serial clock idles low.

Bit	Name	Description
2	SPICPH	Serial clock phase mode bit. Set by user, the serial clock pulses at the beginning of each serial bit transfer. Cleared by user, the serial clock pulses at the end of each serial bit transfer.
1	SPIMEN	Master mode enable bit. Set by user to enable master mode. Cleared by user to enable slave mode.
0	SPIEN	SPI enable bit. Set by user to enable the SPI. Cleared by user to disable the SPI.

GENERAL-PURPOSE I/O

The ADuC7060 features up to 16 general-purpose bidirectional input/output (GPIO) pins. In general, many of the GPIO pins have multiple functions that are configurable by user code. By default, the GPIO pins are configured in GPIO mode. All GPIO pins have an internal pull-up resistor with a drive capability of 1.6 mA.

All I/O pins are 3.3 V tolerant, meaning the GPIOs support an input voltage of 3.3 V.

When the ADuC7060 enters a power-saving mode, the GPIO pins retain their state.

The GPIO pins are grouped into three port buses.

Table 106 lists all the GPIO pins and their alternative functions. A GPIO pin alternative function can be selected by writing to the correct bits of the GPxCON register.

Table 106. GPIO Multifunction Pin Descriptions

	Configuration via GPxCON		
Port	**Pin Mnemonic**	**00**	**01**
0	P0.0/$\overline{SS}$	GPIO	$\overline{SS}$ (SPI slave select).
	P0.1/SCLK/SCL	GPIO	SCLK/SCL (serial clock/SPI clock).
	P0.2/MISO	GPIO	MISO (SPI—master in/slave out).
	P0.3/MOSI/SDA	GPIO	MOSI (SPI—master out/slave in).
	P0.4/IRQ0/PWM1	GPIO/IRQ0	PWM1 (PWM Input 1).
	P0.5/CTS	GPIO	CTS. UART clear to send pin.
	P0.6/RTS	GPIO	RTS. UART request to send pin.
1	P1.0/IRQ1/SIN/T0	GPIO/IRQ1	SIN (serial input).
	P1.1/SOUT	GPIO	SOUT (serial output).
	P1.2/SYNC	GPIO	PWMsync (PWM sync input pin).
	P1.3/TRIP	GPIO	PWMtrip (PWM trip input pin).
	P1.4/PWM2	GPIO	PWM2 (PWM Input 2).
	P1.5/PWM3	GPIO/IRQ3	PWM3 (PWM Input 3).
	P1.6/PWM4	GPIO	PWM4 (PWM Input 4).
2	P2.0/IRQ2/PWM0/EXTCLK	GPIO/IRQ2/EXTCLK	PWM0 (PWM Input 0).
	P2.1/IRQ3/PWM5	GPIO/IRQ3	PWM5 (PWM Input 5).

GPxCON REGISTERS

GPxCON are the Port x (where x is 0, 1, or 2) control registers, which select the function of each pin of Port x as described in Table 108.

Table 107.GPxCON Registers

Name	Address	Default Value	Access
GP0CON0	0xFFFF0D00	0x00000000	R/W
GP1CON	0xFFFF0D04	0x00000000	R/W
GP2CON	0xFFFF0D08	0x00000000	R/W

Table 108. GPxCON MMR Bit Descriptions

Bit	Description
31:30	Reserved.
29:28	Reserved.
27:26	Reserved.
25:24	Selects the function of the P0.6/RTS and P1.6/PWM pins.
23:22	Reserved.
21:20	Selects the function of the P0.5/CTS and P1.5/PWM3 pins.
19:18	Reserved.
17:16	Selects the function of the P0.4/IRQ0/PWM1 and P1.4/PWM2 pins.
15:14	Reserved.
13:12	Selects the function of the P0.3/MOSI/SDA and P1.3/TRIP pins.
11:10	Reserved.
9:8	Selects the function of the P0.2/MISO and P1.2/SYNC pins.
7:6	Reserved.
5:4	Selects the function of the P0.1/SCLK/SCL, P1.1/SOUT, and P2.1/IRQ3/PWM5 pins.
3:2	Reserved.
1:0	Selects the function of the P0.0/$\overline{SS}$, P1.0/IRQ1/SIN/T0, P2.0/IRQ2/PWM0/EXTCLK pins.

GPxDAT REGISTERS

GPxDAT are Port x configuration and data registers. They configure the direction of the GPIO pins of Port x, set the output value for the pins that are configured as output, and store the input value of the pins that are configured as input.

Table 109. GPxDAT Registers

Name	Address	Default Value	Access
GP0DAT	0xFFFF0D20	0x000000XX	R/W
GP1DAT	0xFFFF0D30	0x000000XX	R/W
GP2DAT	0xFFFF0D40	0x000000XX	R/W

Table 110. GPxDAT MMR Bit Descriptions

Bit	Description
31:24	Direction of the data. Set to 1 by user to configure the GPIO pin as an output. Cleared to 0 by user to configure the GPIO pin as an input.
23:16	Port x data output.
15:8	Reflect the state of Port x pins at reset (read only).
7:0	Port x data input (read only).

GPxSET REGISTERS

GPxSET are data set Port x registers.

Table 111. GPxSET Registers

Name	Address	Default Value	Access
GP0SET	0xFFFF0D24	0x000000XX	W
GP1SET	0xFFFF0D34	0x000000XX	W
GP2SET	0xFFFF0D44	0x000000XX	W

Table 112. GPxSET MMR Bit Descriptions

Bit	Description
31:24	Reserved.
23:16	Data Port x set bit. Set to 1 by user to set bit on Port x; also sets the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data output.
15:0	Reserved.

GPxCLR REGISTERS

GPxCLR are data clear Port x registers.

Table 113. GPxCLR Registers

Name	Address	Default Value	Access
GP0CLR	0xFFFF0D28	0x000000XX	W
GP1CLR	0xFFFF0D38	0x000000XX	W
GP2CLR	0xFFFF0D48	0x000000XX	W

GPxPAR REGISTERS

The GPxPAR registers program the parameters for Port 0, Port 1, and Port 2. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR.

Table 114. GPxPAR Registers

Name	Address	Default Value	Access
GP0PAR	0xFFFF0D2C	0x00000000	R/W
GP1PAR	0xFFFF0D3C	0x00000000	R/W
GP2PAR	0xFFFF0D4C	0x00000000	R/W

Table 115. GPxPAR MMR Bit Descriptions

Bit	Name	Description
31:15		Reserved.
23:16	GPL[7:0]	General I/O port pin functionality lock registers. GPL[7:0] = 0, normal operation. GPL[7:0] = 1, for each GPIO pin, if this bit is set, writing to the corresponding bit in GPxCON or GPxDAT register bit has no effect.
15:8	GPDS[7:0]	Drive strength configuration. This bit is configurable. GPDS[x] = 0, maximum source current is 2 mA. GPDS[x] = 1, maximum source current is 4 mA.
7:0	GPPD[7:0]	Pull-Up Disable Port x[7:0]. GPPD[x] = 0, pull-up resistor is active. GPPD[x] = 1, pull-up resistor is disabled.

GP0CON1 Control Registers

The GP0CON1 write values are as follows: GP0KEY1 = 0x7, GP0CON1 = user value, and GP0KEY2 = 0x13.

Name GP0KEY1

Address: 0xFFFF0464

Default value: 0xXXXX

Access: Write only

Function: When writing to GP0CON1, the value of 0x07 must be written to this register in the instruction immediately before writing to GP0CON1.

Table 116. GPxCLR MMR Bit Descriptions

Bit	Description
31:24	Reserved.
23:16	Data Port x clear bit. Set to 1 by user to clear the bit on Port x; also clears the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data output.
15:0	Reserved.

Table 117. GP0CON1 Write Sequence

Name	Value
GP0KEY1	0x7
GP0CON1	User value
GP0KEY2	0x13

Name: GP0CON1

Address: 0xFFFF0468

Default value: 0x00

Access: Read and write

Function: This register controls the P0.0, P0.1, P0.2 and P0.3 functionality of the multifunction GPIO pins.

Table 118. GP0CON1 MMR Bit Designations

Bit	Name	Description
7:2	Reserved	These bits must always be set to 0.
1	SPII2CSEL	This bit configures the P0.0 to P0.3 functions in I^2C or SPI mode. Note that Bit 0 of GP0CON1 must be set to 0 for this bit to work. To select the P0.0, P0.1,P0.2 and P0.3 functions in SPI mode, clear this bit to 0. To select the P0.0, P0.1,P0.2 and P0.3 functions in I^2C mode, set this bit to 1. This bit is cleared by default.
0	ADCSEL	This bit configures the P0.0 to P0.3 functions as GPIO pins or as ADC input pins. To enable P0.0, P0.1, P0.2 and P0.3 functions as ADC inputs, set this bit to 1. To enable P0.0, P0.1, P0.2, and P0.3 functions as digital I/O, clear this bit to 0. This bit is cleared by default.

Name: GP0KEY2

Address: 0xFFFF046C

Default value: 0xXXXX

Access: Write only

Function: When writing to GP0CON1, the value of 0x13 must be written to this register in the instruction immediately after writing to POWCON0.

HARDWARE DESIGN CONSIDERATIONS

POWER SUPPLIES

The ADuC7060 operational power supply voltage range is 2.375 V to 2.625 V. Separate analog and digital power supply pins (AVDD and DVDD, respectively) allow AVDD to be kept relatively free of noisy digital signals often present on the system DVDD line. In this mode, the part can also operate with split supplies; that is, it can use different voltage levels for each supply. For example, the system can be designed to operate with an DVDD voltage level of 2.6 V whereas the AVDD level can be at 2.5 V or vice versa. A typical split supply configuration is shown in Figure 27.

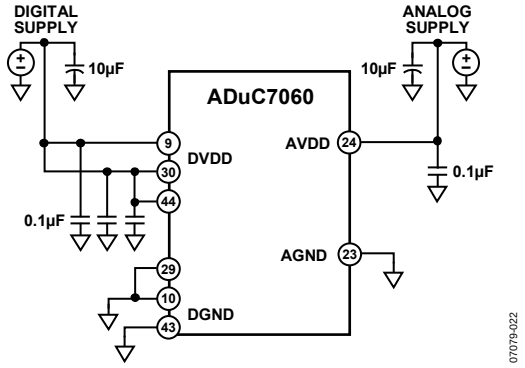


Figure 27. External Dual Supply Connections

As an alternative to providing two separate power supplies, the user can reduce noise on AVDD by placing a small series resistor and/or ferrite bead between AVDD and DVDD, and then decoupling AVDD separately to ground. An example of this configuration is shown in Figure 28. With this configuration, other analog circuitry (such as op amps, voltage reference, and others) can be powered from the AVDD supply line as well.

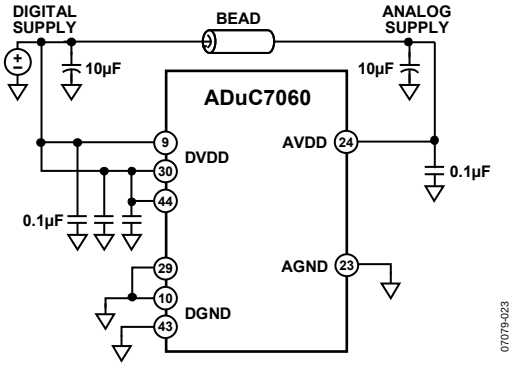


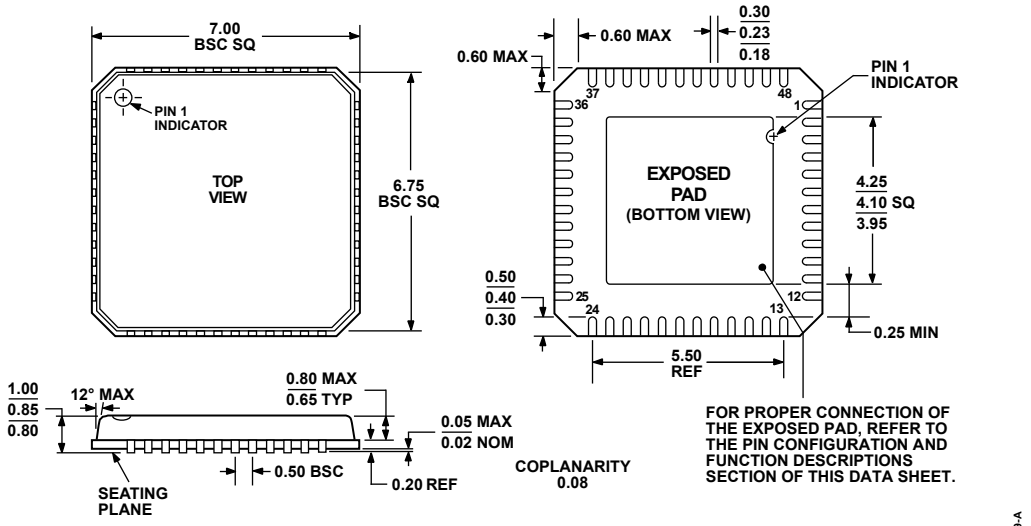
Figure 28. External Single Supply Connections

Notice that in both Figure 27 and Figure 28, a large value (10 µF) reservoir capacitor sits on DVDD, and a separate 10 µF capacitor sits on AVDD. In addition, local small value (0.1 µF) capacitors are located at each AVDD and DVDD pin of the chip. As per standard design practice, be sure to include all of these capacitors and ensure that the smaller capacitors are close to each AVDD pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane.

Note that the analog and digital ground pins on the ADuC7060 must be referenced to the same system ground reference point at all times.

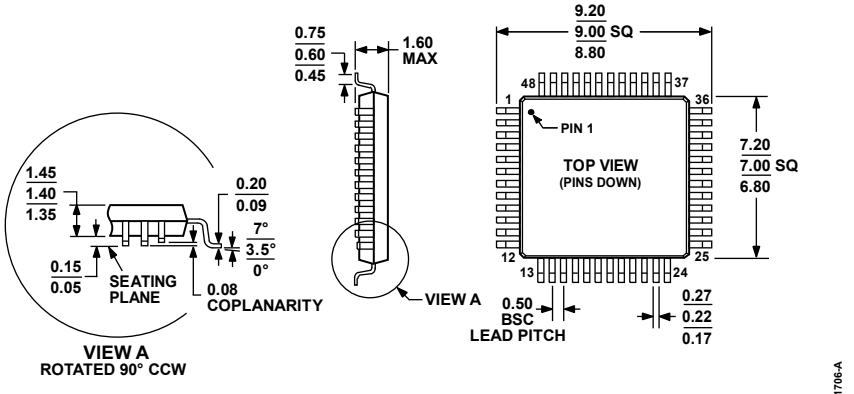
Finally, note that, when the DVDD supply reaches 1.8 V, it must ramp to 2.25 V in less than 128 ms. This is a requirement of the internal power-on reset circuitry.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 29. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-3)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 30. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuC7060BCPZ32[1]	−40°C to +125°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1	
ADuC7060BCPZ32-RL[1]	−40°C to +125°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1	2,500
ADuC7060BSTZ32[1]	−40°C to +125°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48	
ADuC7060BSTZ32-RL[1]	−40°C to +125°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48	2,000
EVAL-ADuC7060QSPZ[1]		ADuC7060 Quick Start Plus Development System		

[1] Z = RoHS Compliant Part.

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