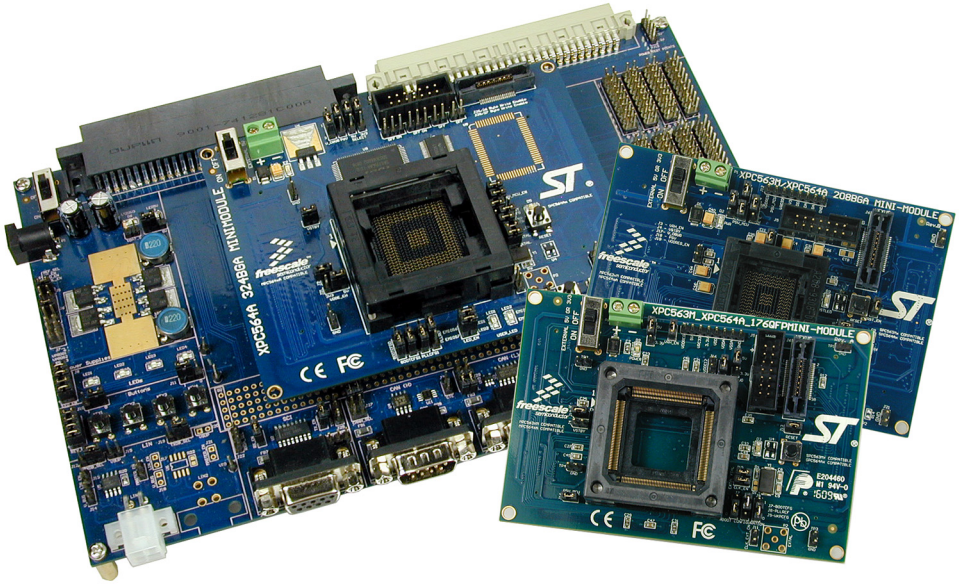
xPC564A EVB User Manual



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XPC564AEVBUM

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1 OVERVIEW

The xPC564A EVB is an evaluation system supporting Freescale MPC564xA microprocessors. The complete system consists of an xPC56XXMB Motherboard and an xPC564AADPT Mini-Module which plugs into the motherboard. Different Mini-Modules are available for evaluating devices with different footprints in the MPC564xA family of microprocessors. The evaluation system allows full access to the CPU, all of the CPU's I/O signals, and the motherboard peripherals (such as CAN, SCI, LIN). The Mini-Module may be used as a stand-alone unit, which allows access to the CPU, but no access to the I/O pins or any motherboard peripherals.

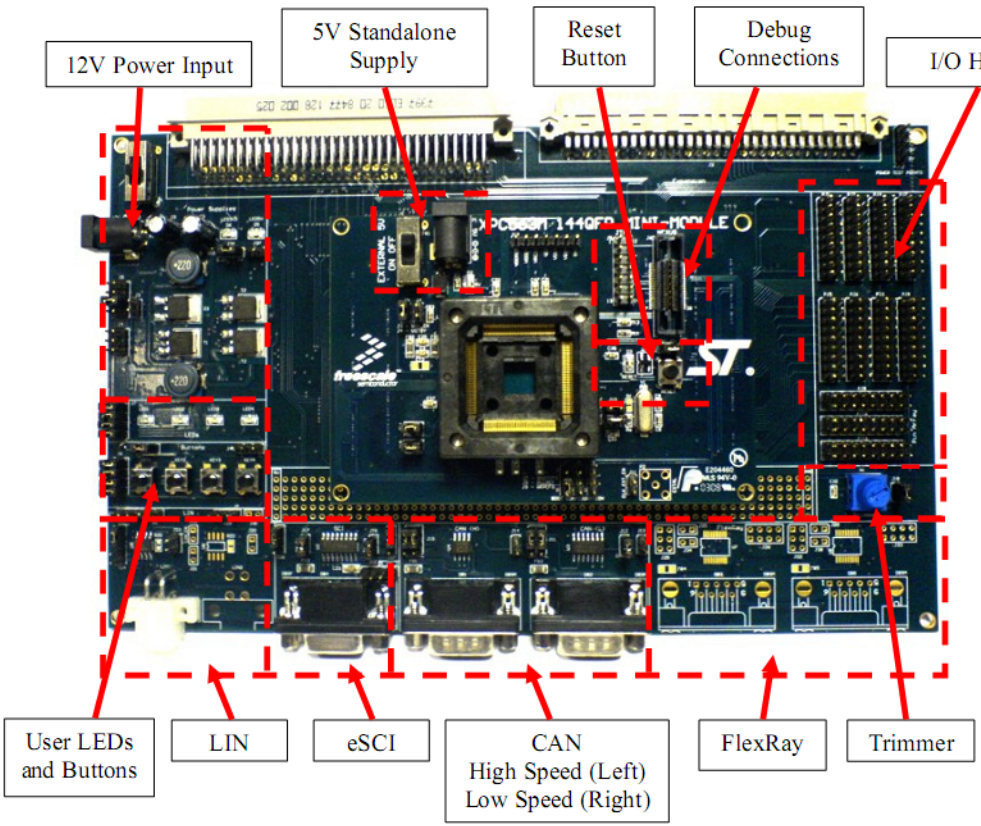


Figure 1-1: Overview of the xPC564A EVB

1.1 Package Contents

An xPC564A Evaluation Kit includes the following items:

- One xPC56XXMB Motherboard
- One xPC564AADPT176S or xPC564AADPT208S or xPC564AADPT324S Mini-Module
- One xPC56XX Resources CD-ROM
- One P&E USB-ML-PPCNEXUS Hardware Interface Cable
- One USB A-to-B Cable
- Freescale Warranty Card

An xPC564A Adapter Package includes the following items:

- One xPC564AADPT176S or xPC564AADPT208S or xPC564AADPT324S Mini-Module
- One xPC56XX Resources CD-ROM
- Freescale Warranty Card

1.2 Supported Devices

The xPC564AADPT176S Mini-Module supports the following devices:

- MPC564xA (176 LQFP package)

The xPC564AADPT208S Mini-Module supports the following devices:

- MPC564xA (208 BGA package)

The xPC564AADPT324S Mini-Module supports the following devices:

- MPC564xA (324 BGA package)

1.3 Recommended Materials

- Freescale MPC5646A reference manual and datasheet
- xPC56XXMB schematic
- xPC564AADPT176S schematic
- xPC564AADPT208S schematic
- xPC564AADPT324S schematic

1.4 Handling Precautions

Please take care to handle the package contents in a manner such as to prevent electrostatic discharge.

2 HARDWARE FEATURES

The xPC564A EVB is an evaluation system for Freescale's MPC564xA microprocessors. A 38-pin Mictor Nexus port and/or a 14-pin JTAG port are provided on the Mini-Module to allow usage of an external PowerPC Nexus interface such as P&E USB-ML-PPCNEXUS cable and Cyclone MAX automated programmer.

2.1 xPC56XXMB Board Features

- ON/OFF Power Switch w/ LED indicators
- A 12VDC power supply input barrel connector
- Onboard STMicroelectronics L9758 regulator provides three different power voltages simultaneously: 5V, 3.3V, and 1.2V
- Onboard peripherals can be configured to operate at 5V or 3.3V logic levels
- Two CAN channels with jumper enables
  - One CAN channel with High-Speed transceiver and DB9 male connector
  - One CAN channel with Low-Speed Fault Tolerant and High-Speed transceiver (selectable with jumpers) and DB9 male connector
- Two LIN channels with jumper enables
  - One channel with transceiver and pin header connector populated
  - One channel with footprints only
- One SCI channel with jumper enables
  - Transceiver with DB9 female connector
- Two FlexRay channels with jumper enables

- One channel with transceiver and DB9 male connector
- One channel with footprint only

- Four user push buttons with jumper enables and polarity selection
- Four user LED's with jumper enables
- One potentiometer for analog voltage input
- Pin array for accessing all I/O signals
- Expansion connectors for accessing all I/O signals
- Development zone with 0.1" spacing and SOIC footprint prototyping
- Specifications:
  - Board Size 5.5" x 9.0"
  - 12VDC Center Positive power supply with 2.5/5.5mm barrel connector

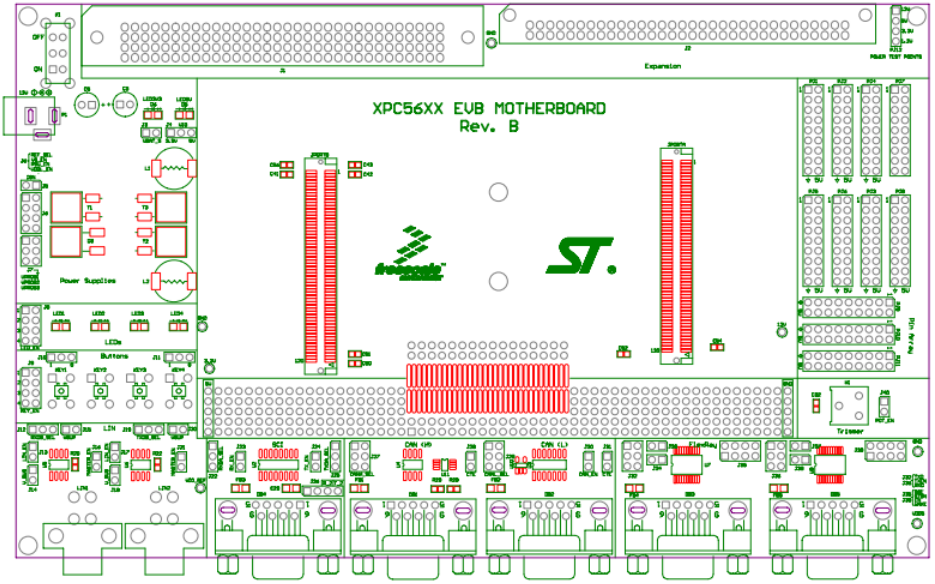


Figure 2-1: xPC56XXMB Top Component Placement

2.2 xPC564AADPT Mini-Module Board Features

- Can be used as a stand-alone board by providing external 5V power supply input
- ON/OFF Power Switch w/ LED indicator
- Reset button with filter and LED indicator
- xPC564AADPT176S has socket for MPC564xA in 176LQFP footprint
- xPC564AADPT208S has socket for MPC564xA in 208BGA footprint
- xPC564AADPT324S has socket for MPC564xA in 324BGA footprint
- Debug ports: 38-pin Mictor Nexus port and/or 14-pin JTAG port
- Direct clock input through SMA connector (footprint only)
- Jumpers for boot configuration

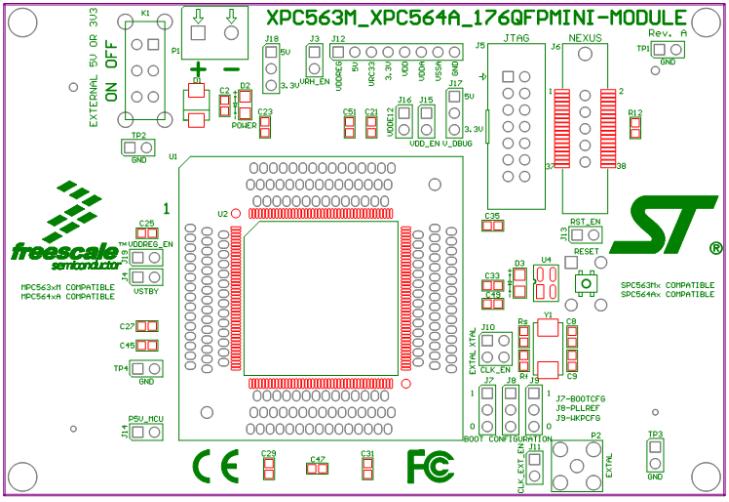


Figure 2-2: xPC564AADPT176S Top Component Placement

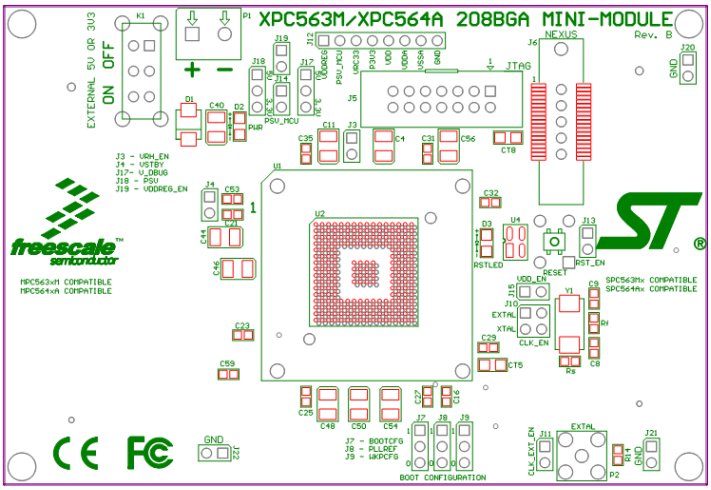


Figure 2-3: xPC564AADPT208S Top Component Placement

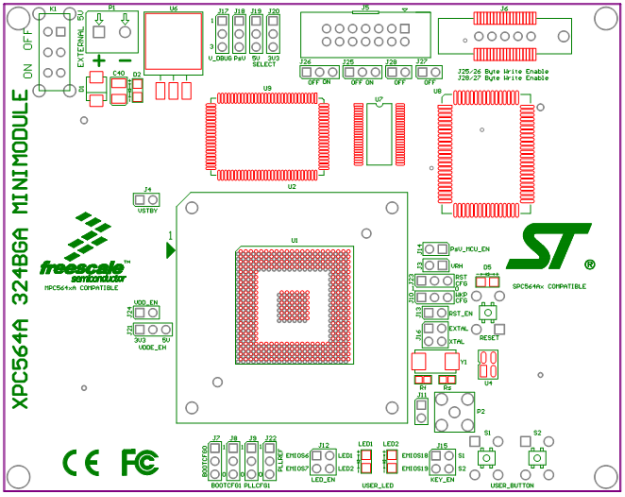


Figure 2-4: xPC564AADPT324S Top Component Placement

2.3 Pin Numbering for Jumpers

Jumpers for both the xPC56XXMB motherboard and the xPC564A Mini-Modules have a rounded corner to indicate the position of pin 1. See

examples below for the numbering convention used in this manual for jumper settings.

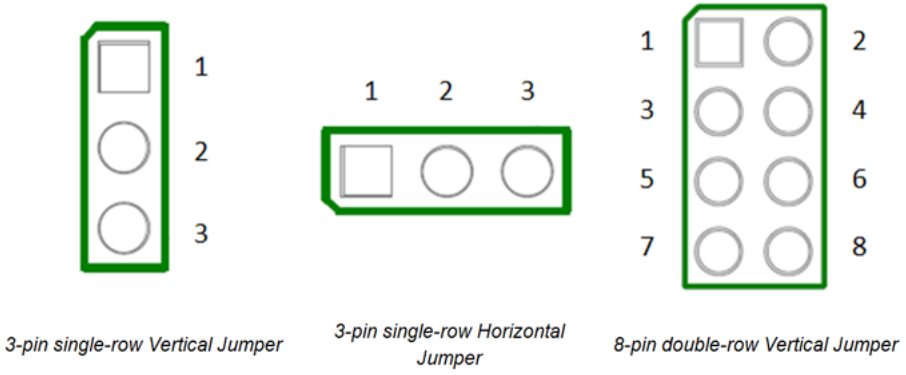


Figure 2-5: Pin Numbering

3 xPC56XXMB HARDWARE & JUMPER SETTINGS

Please note that this section of the manual is written for revision B of the xPC56XXMB motherboard. Revision B motherboards are indicated by the "Rev. B" silkscreen text in the center of the motherboard.

Revision A motherboards have different jumper numbers. These differences can be found in the table below:

Revision A	Revision B	Jumper Description
J3	J6, pins 1+2	VSA Tracking Regulator Configuration
J4	J7	VPROG Regulators Control
J5 (pins 1+2)	J5	IGN Control
J5 (pins 3+4, 5+6, 7+8)	J6, pins 3+4, 5+6, 7+8	Regulators Enable & Standby
J36	J4	VIO Peripherals Logic Level

J37	J3	VBat low voltage detection
J7	J8	LEDs Enable
J8	J9	Buttons Enable
J9	J10	Buttons Driving Configuration
J40	J11	Buttons Idle Configuration
J22	J13	LIN1 enable
J24	J14	LIN1 VBUS configuration
J6	J15	LIN1 VSUP configuration
J23	J16	LIN1 master selection
J28	J22	LIN1/SCI RxD selection
J27	J25	LIN1/SCI TxD selection
J19	J17	LIN2 enable
J21	J18	LIN2 VBUS configuration
J31	J20	LIN2 VSUP configuration
J20	J21	LIN2 master selection
J30	J12	LIN2/SCI RxD selection
J29	J19	LIN2/SCI TxD selection
J17	J23	SCI RxD Enable
J16	J24	SCI TxD Enable
J27	J25	LIN1/SCI TxD selection

J28	J22	LIN1/SCI RxD selection
J14	J28	CAN (H) Transmit Enable
J15	J27	CAN (H) TxD/RxD Enable
J13	J31	CAN (L) CTE
J12	J30	CAN (L) Enable
J11	J29	CAN (L) TxD/RxD Enable
J25	J32	FlexRay Bus Driver 1 Enable
J26	J35	FlexRay Bus Driver 1 Configuration
J34	J34	FlexRay 1 Terminal Resistor Connection
J35	J33	FlexRay 1 Terminal Resistor Connection
J32	J36	FlexRay Bus Driver 2 Enable
J33	J39	FlexRay Bus Driver 2 Configuration
J38	J38	FlexRay 2 Terminal Resistor Connection
J39	J37	FlexRay 2 Terminal Resistor Connection
J18	J40	POT Enable

3.1 Power Supplies

The xPC56XXMB obtains its power from the 12VDC Center Positive input barrel connector. The following jumpers are used to configure the power supply output:

J3 – VBat low voltage detection

Jumper Setting	Effect
On	Low battery detection is enabled
Off (default)	Low battery detection is disabled

J4 – VIO Peripherals Logic Level

Jumper Setting	Effect
1+2	Onboard peripherals are configured for 3.3V logic
2+3 (default)	Onboard peripherals are configured for 5V logic

J5 – IGN Control

Jumper Setting	Effect
On (default)	The power regulator is always on
Off	If 5+6 is also OFF on J6, the power regulator is in standby

J6 – Regulators Enable & Standby

Jumper Setting	Position	Effect

1+2	On	The ST L9758 tracking regulator VSA tracks the input voltage at its TRACK_REF pin.
	Off (default)	The ST L9758 tracking regulator VSA tracks 5V
3+4	On	VSB, VSC, and VSD tracking regulators are disabled
	Off (default)	VSB, VSC, and VSD tracking regulators are enabled
5+6	On (default)	The power regulator is always on
	Off	The power regulator is in standby if jumpers 1+2 are also in the “off” position
7+8	On	VDLL and VCORE regulators are disabled
	Off (default)	VDLL and VCORE regulators are enabled

J7 – VPROG Regulators Control

Jumper Setting	Position	Effect
1+2	On	VKAM regulator output is programmed to 1V
	Off (default)	VKAM regulator output is programmed to 1.5V
3+4	On	VSTBY regulator output is programmed to 2.6V
	Off (default)	VSTBY regulator output is programmed to 3.3V

5+6	On	VDLL regulator output is programmed to 2.6V
	Off (default)	VDLL regulator output is programmed to 3.3V

J37 – VBat low voltage detection

Jumper Setting	Effect
On	Low battery detection is enabled
Off (default)	Low battery detection is disabled

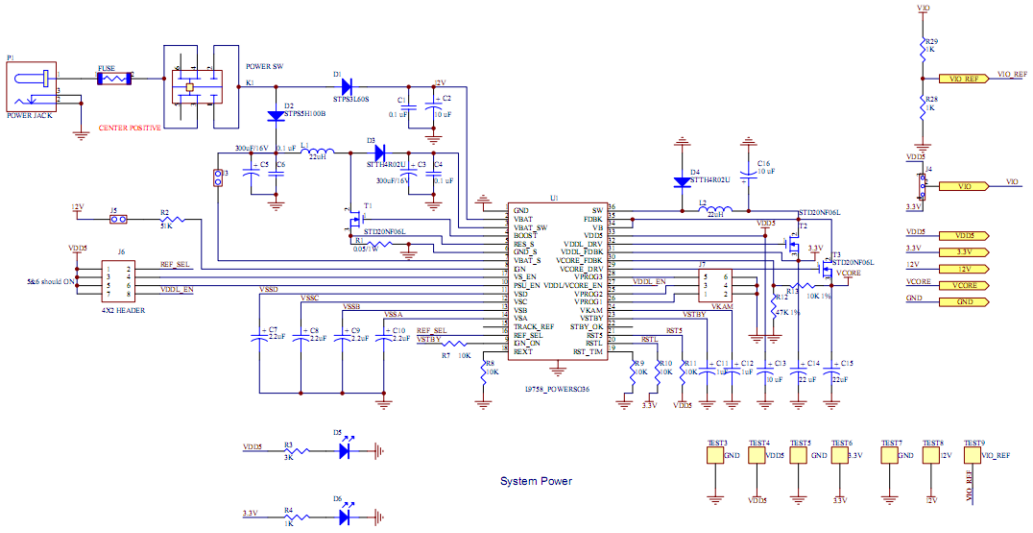


Figure 3-1: Power Supply circuitry schematic

3.2 LEDs

There are four user LEDs available on the xPC56XXMB. All LEDs are active low.

J8 – LEDs Enable

Controls whether the LEDs on the xPC56XXMB motherboard are connected to I/O pins of the processor. The jumpers can be removed and wires can be used to connect each LED to any processor I/O pin, if desired.

Jumper Setting	Effect
1+2 (default on)	LED1 connected to eMIOS9
3+4 (default on)	LED2 connected to eMIOS10
5+6 (default on)	LED3 connected to eMIOS11
7+8 (default on)	LED4 connected to eMIOS12

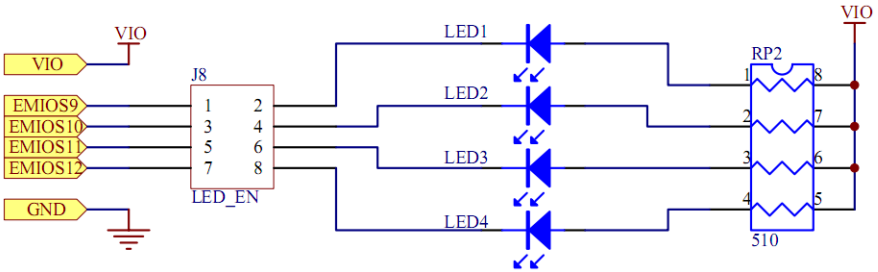


Figure 3-2: LEDs circuitry schematic

3.3 Buttons

There are four user buttons available on the xPC56XXMB.

J9 – Buttons Enable

Controls whether the buttons on the xPC56XXMB motherboard are connected to I/O pins of the processor. The jumpers can be removed and wires can be used to connect each button to any processor I/O pin, if desired.

Jumper Setting	Effect
1+2 (default on)	KEY1 connected to eMIOS0
3+4 (default on)	KEY2 connected to eMIOS2
5+6 (default on)	KEY3 connected to eMIOS4
7+8 (default on)	KEY4 connected to eMIOS8

J10 – Buttons Driving Configuration

Selects whether the buttons drive logic high or drive logic low when pressed.

Jumper Setting	Effect
1+2	When pressed, buttons will send logic high to the connected I/O pin
2+3 (default)	When pressed, buttons will send logic low to the connected I/O pin

J11 – Buttons Idle Configuration

Selects whether the I/O pins are pulled logic high or pulled logic low. This controls the default logic level of the I/O pins when the buttons are not pressed.

Jumper Setting	Effect
1+2 (default)	I/O pins connected to the buttons are pulled up to logic high
2+3	I/O pins connected to the buttons are pulled down to logic low

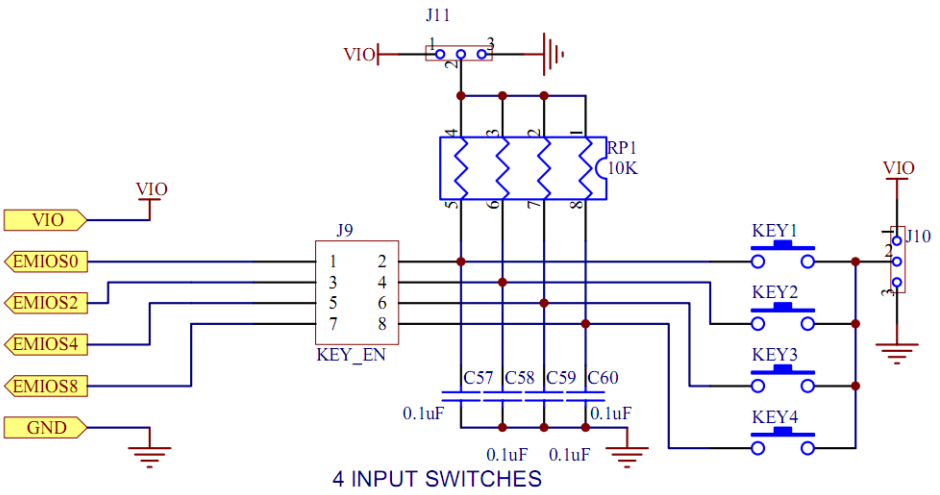


Figure 3-3: Buttons circuitry schematic

3.4 LIN

There are footprints for two LIN connections on the xPC56XXMB. By default,

one LIN circuit is assembled (LIN1) and the other circuit is left unpopulated (LIN2).

J13 – LIN1 enable

Jumper Setting	Effect
On	Enables the LIN1 transceiver
Off (default)	Disables the LIN1 transceiver

J14 – LIN1 VBUS configuration

Jumper Setting	Effect
On	LIN1 VBUS is connected to 12V
Off (default)	LIN1 VBUS is not connected to 12V

J15 – LIN1 VSUP configuration

Jumper Setting	Effect
On	LIN1 VSUP is connected to 12V
Off (default)	LIN1 VSUP is not connected to 12V

J16 – LIN1 master selection

Jumper Setting	Effect
On	LIN1 is configured as a master node
Off (default)	LIN1 is configured as a slave node

J22 – LIN1/SCI RxD selection

Controls whether the RxD pin on LIN1 or SCI is connected to the default I/O pin on the MPC564xA processor.

Jumper Setting	Effect
1+2	The LIN1 RxD pin is connected to the “RXDA” pin on the MPC564xA processor. This should be set if enabling LIN1.
2+3	The SCI RxD pin is connected to the “RXDA” pin on the MPC564xA processor.

J25 – LIN1/SCI TxD selection

Controls whether the TxD pin on LIN1 or SCI is connected to the default I/O pin on the MPC564xA processor.

Jumper Setting	Effect
1+2	The LIN1 TxD pin is connected to the “TXDA” pin on the MPC564xA processor. This should be set if enabling LIN1.

2+3	The SCI TxD pin is connected to the “TXDA” pin on the MPC564xA processor.

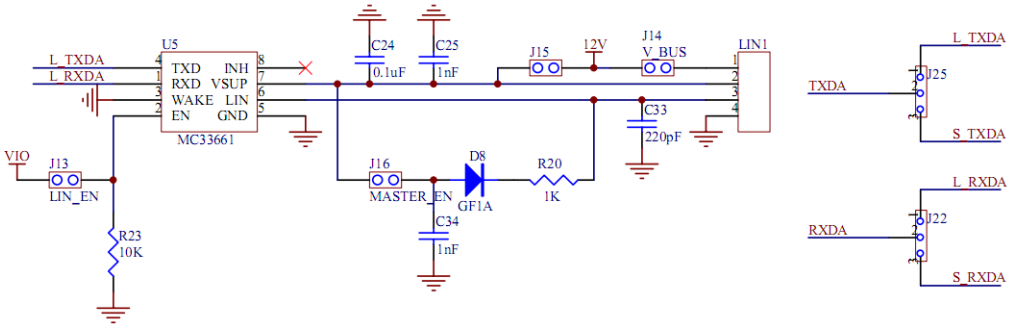


Figure 3-4: LIN1 Schematic

J17 – LIN2 enable

Jumper Setting	Effect
On	Enables the LIN2 transceiver
Off (default)	Disables the LIN2 transceiver

J18 – LIN2 VBUS configuration

Jumper Setting	Effect
On	LIN2 VBUS is connected to 12V
Off (default)	LIN2 VBUS is not connected to 12V

J20 – LIN2 VSUP configuration

Jumper Setting	Effect
On	LIN2 VSUP is connected to 12V
Off (default)	LIN2 VSUP is not connected to 12V

J21 – LIN2 master selection

Jumper Setting	Effect
On	LIN2 is configured as a master node
Off (default)	LIN2 is configured as a slave node

J12 – LIN2/SCI RxD selection

Controls whether the RxD pin on LIN2 or SCI is connected to the default I/O pin on the MPC564xA processor.

Jumper Setting	Effect
1+2	The LIN2 RxD pin is connected to the “RXDB” pin on the MPC564xA processor. This should be set if enabling LIN2.
2+3 (default)	The SCI RxD pin is connected to the “RXDB” pin on the MPC564xA processor.

J19 – LIN2/SCI TxD selection

Controls whether the TxD pin on LIN2 or SCI is connected to the default I/O pin on the MPC564xA processor.

Jumper Setting	Effect
1+2	The LIN2 TxD pin is connected to the “TXDB” pin on the MPC564xA processor. This should be set if enabling LIN2.
2+3 (default)	The SCI TxD pin is connected to the “TXDB” pin on the MPC564xA processor.

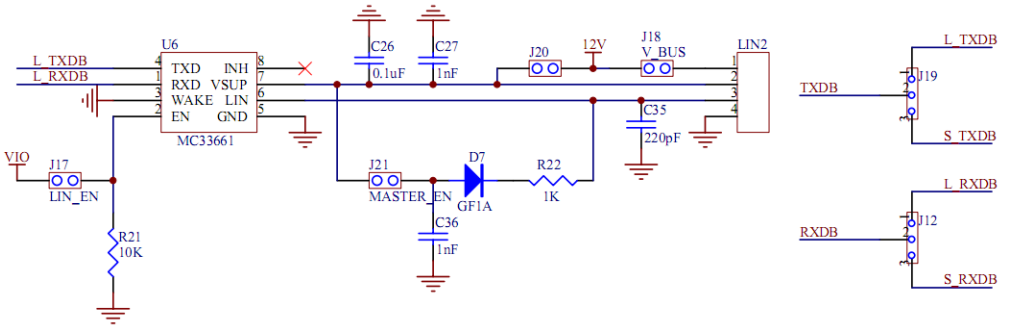


Figure 3-5: LIN2 schematic (Not populated by default)

3.5 SCI

One SCI interface is available on the xPC56XXMB.

J23 – SCI RxD Enable

Jumper Setting	Effect
On (default)	Enables SCI receive
Off	Disables SCI receive

J24 – SCI TxD Enable

Jumper Setting	Effect
On (default)	Enables SCI transmit
Off	Disables SCI transmit

J25 – LIN1/SCI TxD selection

Controls whether the TxD pin on LIN1 or SCI is connected to the default I/O pin on the MPC564xA processor.

Jumper Setting	Effect
1+2	The LIN1 TxD pin is connected to the “TXDA” pin on the MPC564xA processor.
2+3	The SCI TxD pin is connected to the “TXDA” pin on the MPC564xA processor. This should be set if enabling SCI.

J22 – LIN1/SCI RxD selection

Controls whether the RxD pin on LIN1 or SCI is connected to the default I/O pin on the MPC564xA processor.

Jumper Setting	Effect
1+2	The LIN1 RxD pin is connected to the “RXDA” pin on the MPC564xA processor.
2+3	The SCI RxD pin is connected to the “RXDA” pin on the MPC564xA processor. This should be set if enabling SCI.

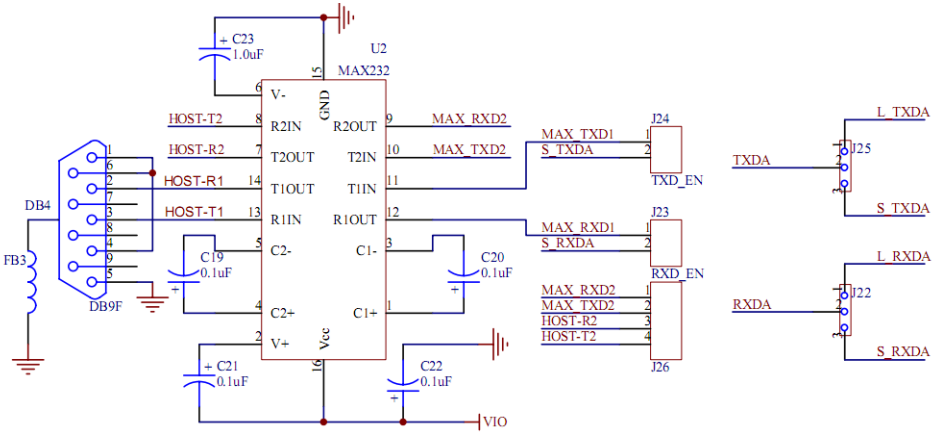


Figure 3-6: SCI schematic

3.6 CAN

Two CAN interfaces are implemented on the xPC56XXMB: a high-speed CAN interface and a low-speed CAN interface.

J28– CAN (H) Transmit Enable

Jumper Setting	Effect
On	Enables CAN transmission
Off (default)	Disables CAN transmission

J27 – CAN (H) TxD/RxD Enable

Controls which I/O pins on the MPC564xA processor are connected to the TxD and RxD pins on CAN (H). If CAN (H) is not used, it is recommended that all jumpers are removed.

Jumper Setting	Effect
1+3 (default)	The RxD pin of the CAN (H) interface is connected to the “CNRXA” pin of the MPC564xA processor.
3+5	The RxD pin of the CAN (H) interface is connected to the “CNRXC” pin of the MPC564xA processor.
2+4 (default)	The TxD pin of the CAN (H) interface is connected to the “CNTXA” pin of the MPC564xA processor.
4+6	The TxD pin of the CAN (H) interface is connected to the “CNTXC” pin of the MPC564xA processor.

J30 – CAN (L) Enable

Jumper Setting	Effect

On (default)	Enables CAN (L) transceiver
Off	Disables CAN (L) transceiver

J31 – CAN (L) CTE

Jumper Setting	Effect
On	Enables CAN transmission
Off (default)	Disables CAN transmission

J29 – CAN (L) TxD/RxD Enable

Controls which I/O pins on the MPC564xA processor are connected to the TxD and RxD pins on CAN (L). If CAN (L) is not used, it is recommended that all jumpers are removed.

Jumper Setting	Effect
1+3	The RxD pin of the CAN (L) interface is connected to the “CNRXA” pin of the MPC564xA processor.
3+5 (default)	The RxD pin of the CAN (L) interface is connected to the “CNRXC” pin of the MPC564xA processor.
2+4	The TxD pin of the CAN (L) interface is connected to the “CNTXA” pin of the MPC564xA processor.
4+6 (default)	The TxD pin of the CAN (L) interface is connected to the “CNTXC” pin of the MPC564xA processor.

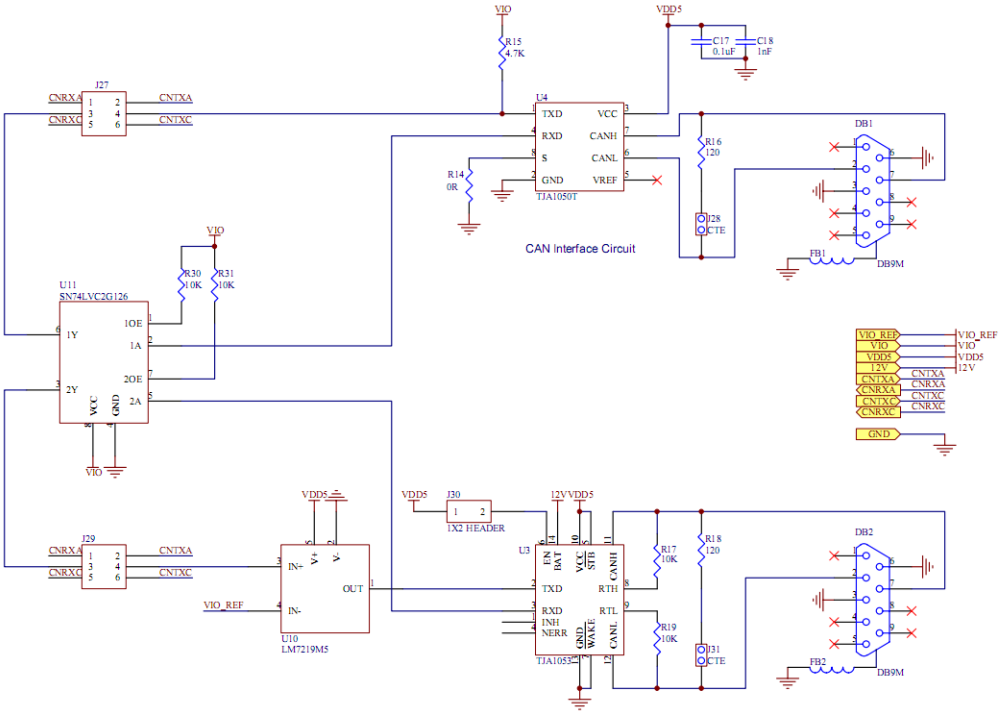


Figure 3-7: CAN schematic

3.7 FlexRay

The xPC56XXMB has footprints for two FlexRay interfaces. However, only one circuit is assembled by default. The FlexRay circuit comprises of two DB9 connectors. DB3 contains signals for both FlexRay channels and is compatible with major FlexRay tools. DB5 contains channel B signal, thereby also allowing 2 separate FlexRay connectors for channel A and channel B operation.

J32 – FlexRay Bus Driver 1 Enable

Controls whether the TxD, TxEN, RxD pins on FlexRay channel A is

connected to the default I/O pin on the MPC564xA processor.

Jumper Setting	Effect
1+2	The TxD pin of the FlexRay Channel A interface is connected to the “FR_A_TX” pin of the MPC564xA processor.
3+4	The TxEN pin of the FlexRay Channel A interface is connected to the “FR_A_TX_EN” pin of the MPC564xA processor.
5+6	The RxD pin of the FlexRay Channel A interface is connected to the “FR_A_RX” pin of the MPC564xA processor.

J35 – FlexRay Bus Driver 1 Configuration

Controls configuration pins on the FlexRay Bus Driver.

Jumper Setting	Effect
1+2	The BGE pin on the FlexRay Bus Driver is pulled up to 5V
3+4	The STBN pin on the FlexRay Bus Driver is pulled up to 5V
5+6 (default on)	The EN pin on the FlexRay Bus Driver is pulled up to 5V
7+8 (default on)	The WAKE pin on the FlexRay Bus Driver is pulled down to GND

J33 & J34 FlexRay 1 Terminal Resistor Connection

Jumper Setting	Effect
On	Terminal resistors connected
Off (default)	Terminal resistors not connected

J36 – FlexRay Bus Driver 2 Enable

Controls whether the TxD, TxEN, RxD pins on FlexRay channel B is connected to the default I/O pin on the MPC564xA processor.

Jumper Setting	Effect
1+2	The TxD pin of the FlexRay Channel A interface is connected to the “FR_B_TX” pin of the MPC564xA processor.
3+4	The TxEN pin of the FlexRay Channel A interface is connected to the “FR_B_TX_EN” pin of the MPC564xA processor.
5+6	The RxD pin of the FlexRay Channel A interface is connected to the “FR_B_RX” pin of the MPC564xA processor.

J39 – FlexRay Bus Driver 2 Configuration

Controls configuration pins on the FlexRay Bus Driver.

Jumper Setting	Effect

1+2	The BGE pin on the FlexRay Bus Driver is pulled up to 5V
3+4	The STBN pin on the FlexRay Bus Driver is pulled up to 5V
5+6	The EN pin on the FlexRay Bus Driver is pulled up to 5V
7+8	The WAKE pin on the FlexRay Bus Driver is pulled down to GND

J37 & J38 – FlexRay 2 Terminal Resistor Connection

Jumper Setting	Effect
On	Terminal resistors connected
Off (default)	Terminal resistors not connected

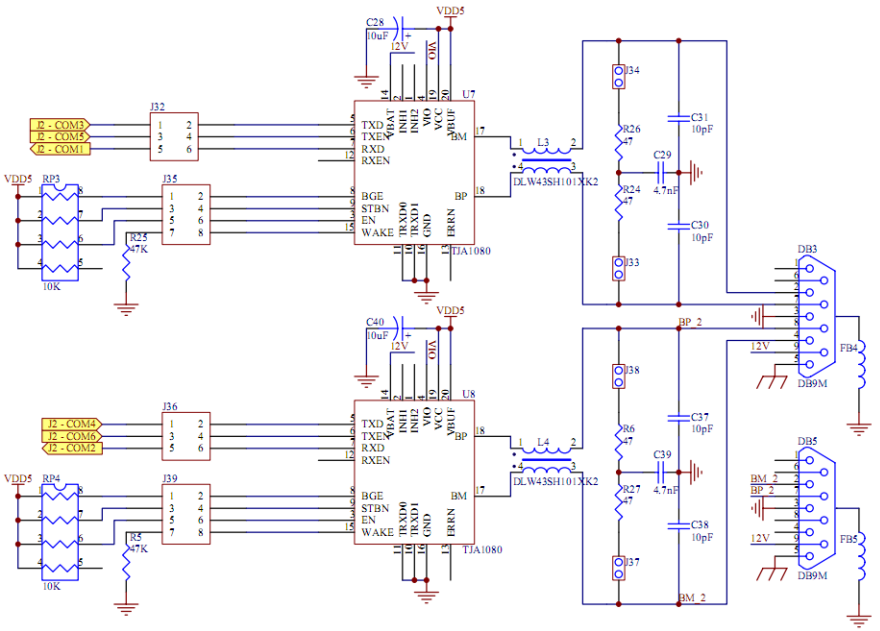


Figure 3-8: FlexRay Schematic

3.8 Potentiometer

A potentiometer is available on the xPC56XXMB to allow an analog voltage input.

J40 – POT Enable

Jumper Setting	Effect
On (default)	The potentiometer wiper terminal is connected to the “AN17” pin on the MPC564xA processor.
Off	The potentiometer wiper terminal is left disconnected.

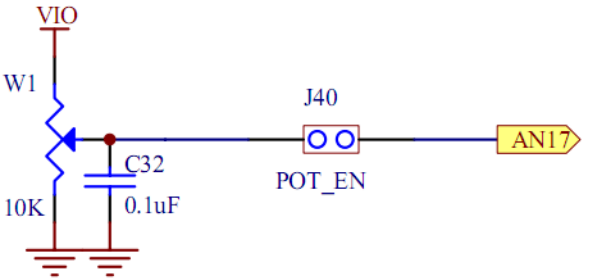
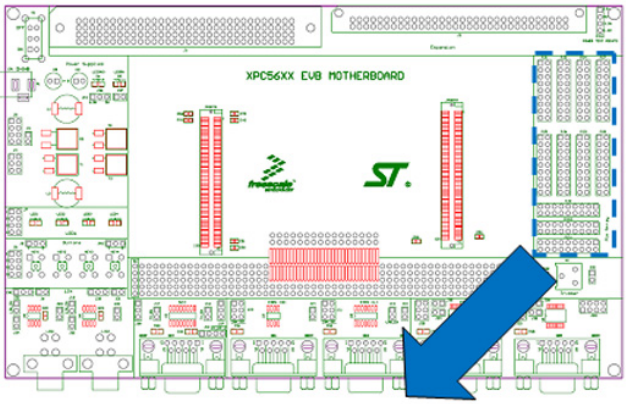


Figure 3-9: Potentiometer schematic

3.9 Pin Mapping

The following is the xPC564A EVB pin assignment for the Pin Array headers:



PJ1

RESET	RSTOUT
CNRXA	CNRXC
CNTXA	CNTXC
SINB	SOUTB
SCKB	PCSB0
PCSB1	PCSB2
RXDA	TXDA
RXDB	TXDB
GND	5V

PJ2

BOOTCFG0	PLLCFG1
BOOTCFG1	PLLREF
WKPCFG	RSTCFG
PCSB3	PCSB4
PCSB5	X
ADDR18	ADDR21
ADDR16	ADDR19
ADDR17	ADDR20
GND	5V

PJ4 - Nexus

MCKO	EVTO
MSEO0	EVTI
MSEO1	TDO
MDO0	TDI
MDO1	TCKOUT
MDO2	TMS
MDO3	JCOMP
GPIO206	GPIO207
GND	5V

PJ7 - AN[0:16]

AN0	AN1
AN2	AN3
AN4	AN5
AN6	AN7
AN9	AN11
AN12	AN13
AN14	AN15
AN16	X
VRH	VRL

PJ5 - AN[17:35]

AN17	AN18
AN21	AN22
AN23	AN24
AN25	AN26
AN27	AN28
AN30	AN31
AN32	AN33
AN34	AN35
GND	5V

PJ6

AN38	AN39
AN8	AN10
AN19	AN20
AN29	AN36
AN37	X
X	X
X	X
ENGLCK	CLKOUT
GND	5V

PJ3

MDO5	MDO6
MDO7	MDO8
MDO9	MDO10
MDO11	TCRCLKA
EMIOS5	EMIOS16
EMIOS17	EMIOS18
EMIOS19	EMIOS20
EMIOS21	EMIOS22
GND	5V

PJ8 - eMIOS

EMIOS0	EMIOS2
EMIOS4	EMIOS8
EMIOS9	EMIOS10
EMIOS11	EMIOS12
EMIOS14	EMIOS23
EMIOS1	EMIOS13
EMIOS15	EMIOS3
EMIOS6	EMIOS7
GND	5V

PJ9 - eTPUA[0:15]

GND	ETPUA14	ETPUA12	ETPUA10	ETPUA8	ETPUA6	ETPUA4	ETPUA2	ETPUA0
5V	ETPUA15	ETPUA13	ETPUA11	ETPUA9	ETPUA7	ETPUA5	ETPUA3	ETPUA1

PJ10 - eTPUA[16:31]

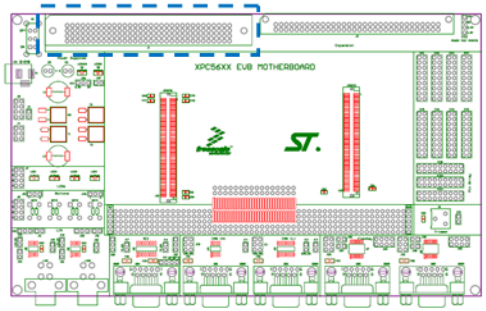
GND	ETPUA30	ETPUA28	ETPUA26	ETPUA24	ETPUA22	ETPUA20	ETPUA18	ETPUA16
5V	ETPUA31	ETPUA29	ETPUA27	ETPUA25	ETPUA23	ETPUA21	ETPUA19	ETPUA17

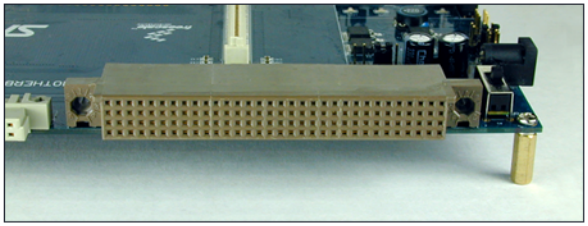
PJ11

GND	GPIO203	RXDC	SCKA	SINA	PCSA4	PCSA1	PCSA3	CNRXB
5V	GPIO204	TXDC	X	SOUTA	PCSA5	PCSA0	PCSA2	CNTXB

Figure 3-10: Pin Mapping

3.10 Expansion Port Pin Mapping – DIN41612 (4x32)



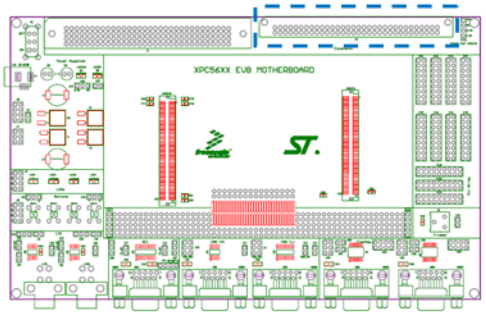


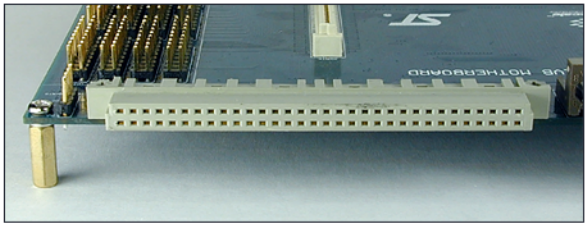
D32	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
C32	C31	C30	C29	C28	C27	C26	C25	C24	C23	C22	C21	C20	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1
B32	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
A32	A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1

A1	GND	B1	GND	C1	GND	D1	5V
A2	CNRXA	B2	CNRXC	C2	CNTXA	D2	CNTXC
A3	RXDA	B3	TXDA	C3	RXDB	D3	TXDB
A4	ADDR18	B4	ADDR21	C4	ADDR16	D4	PCSB2
A5	ADDR19	B5	ADDR17	C5	ADDR20	D5	PCSB1
A6	SINB	B6	SOUTB	C6	SCKB	D6	PCSB0
A7	PCSB3	B7	PCSB4	C7	PCSB5	D7	X
A8	BOOTCFG0	B8	PLLCFG1	C8	GND	D8	12V
A9	RESET_MB	B9	RESETOUT	C9	VRH	D9	VRL
A10	BOOTCFG1	B10	PLLREF	C10	RXDC	D10	TXDC
A11	WKPCFG	B11	RSTCFG	C11	GPIO203	D11	GPIO204
A12	MDO5	B12	MDO6	C12	EMIOS5	D12	EMIOS16
A13	MDO7	B13	MDO8	C13	EMIOS17	D13	EMIOS18
A14	MDO9	B14	MDO10	C14	EMIOS19	D14	EMIOS20
A15	MDO11	B15	TCRCLKA	C15	EMIOS21	D15	EMIOS22
A16	ETPUA0	B16	ETPUA1	C16	ETPUA16	D16	ETPUA17
A17	ETPUA2	B17	ETPUA3	C17	ETPUA18	D17	ETPUA19
A18	ETPUA4	B18	ETPUA5	C18	ETPUA20	D18	ETPUA21
A19	ETPUA6	B19	ETPUA7	C19	ETPUA22	D19	ETPUA23
A20	ETPUA8	B20	ETPUA9	C20	ETPUA24	D20	ETPUA25
A21	ETPUA10	B21	ETPUA11	C21	ETPUA26	D21	ETPUA27
A22	ETPUA12	B22	ETPUA13	C22	ETPUA28	D22	ETPUA29
A23	ETPUA14	B23	ETPUA15	C23	ETPUA30	D23	ETPUA31
A24	AN0	B24	AN1	C24	EMIOS0	D24	EMIOS2
A25	AN2	B25	AN3	C25	EMIOS4	D25	EMIOS8
A26	AN4	B26	AN5	C26	EMIOS9	D26	EMIOS10
A27	AN6	B27	AN7	C27	EMIOS11	D27	EMIOS12
A28	AN9	B28	AN11	C28	EMIOS14	D28	EMIOS23
A29	AN12	B29	AN13	C29	EMIOS1	D29	EMIOS15
A30	AN14	B30	AN15	C30	EMIOS13	D30	EMIOS3
A31	AN16	B31	AN17	C31	EMIOS6	D31	EMIOS7
A32	GND	B32	3.3V	C32	GND	D32	5V

Figure 3-11: Expansion Port Pin Mapping – DIN41612 (4x32)

3.11 Expansion Port Pin Mapping – DIN41612 (2x32)





B32	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
A32	A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1

A1	GND	B1	5V
A2	AN0	B2	AN1
A3	AN2	B3	AN3
A4	AN4	B4	AN5
A5	AN6	B5	AN7
A6	AN9	B6	AN11
A7	AN12	B7	AN13
A8	AN14	B8	AN15
A9	AN16	B9	X
A10	AN17	B10	AN18
A11	AN21	B11	AN22
A12	AN24	B12	AN23
A13	AN25	B13	AN26
A14	AN27	B14	AN28
A15	AN30	B15	AN31
A16	AN32	B16	AN33
A17	AN34	B17	AN35
A18	AN38	B18	AN39
A19	AN8	B19	AN10
A20	AN19	B20	AN20
A21	AN29	B21	AN36
A22	AN37	B22	X
A23	X	B23	X
A24	X	B24	X
A25	ENGLCK	B25	CLKOUT
A26	CNRXB	B26	CNTXB
A27	PCSA3	B27	PCSA2
A28	PCSA1	B28	PCSA0
A29	PCSA4	B29	PCSA5
A30	SINA	B30	SOUTA
A31	SCKA	B31	X
A32	GND	B32	3.3V

Expansion Port Pin Mapping – DIN41612 (2x32)

4 xPC564AADPT324S HARDWARE & JUMPER SETTINGS

4.1 Boot Configuration

The following jumpers affect the operation of the processor as it initially comes out of the reset state:

J7 – BOOTCFG0 Configuration

Controls the status of the BOOTCFG0 pin

Jumper Setting	Effect
1+2	The BOOTCFG0 pin on the processor is pulled up
2+3 (default)	The BOOTCFG0 pin on the processor is pulled down

J8 – BOOTCFG1 Configuration

Controls whether the processor boots from internal FLASH or from a serial interface (CAN, SCI)

Jumper Setting	Effect
1+2	The MPC564xA processor uses serial boot mode
2+3 (default)	The MPC564xA processor uses internal boot mode

J9 – PLLCFG1 Configuration

Controls the status of the PLLCFG1 pin

Jumper Setting	Effect

1+2	The PLLCFG1 pin on the processor is pulled up
2+3 (default)	The PLLCFG1 pin on the processor is pulled down

J10 – WKPCFG Configuration

Controls whether specified eTPU and eMIOS pins on the processor are configured with weak pull-up or a weak pull-down when the processor comes out of reset

Jumper Setting	Effect
1+2	Pins are configured as weak pull-up
2+3 (default)	Pins are configured as weak pull-down

J22 – PLLREF Configuration

Controls the clock source the processor uses: a crystal source or an external source

Jumper Setting	Effect
1+2 (default)	The MPC564xA processor uses a crystal clock source
2+3	The MPC564xA processor uses an external clock source

J23 – RSTCFG Configuration

Controls the status of the RSTCFG pin

Jumper Setting	Effect
1+2 (default)	The RSTCFG pin on the processor is pulled up
2+3	The RSTCFG pin on the processor is pulled down

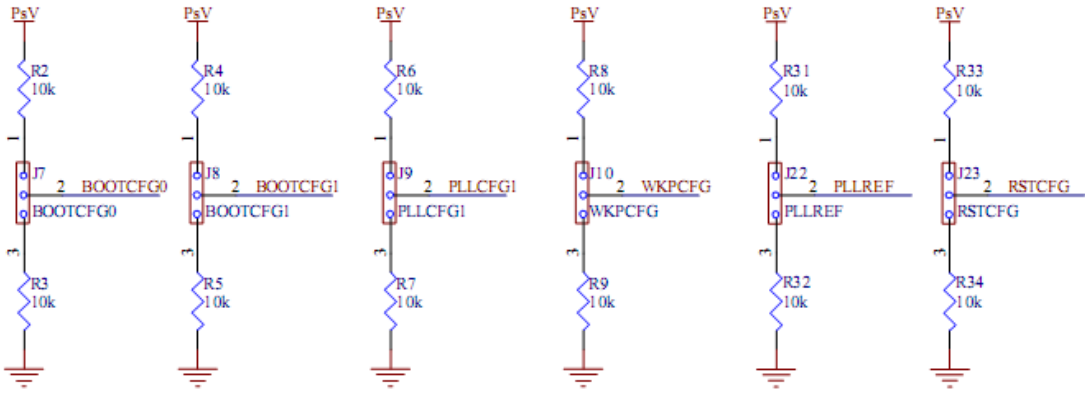


Figure 4-1: Boot Configuration Jumpers

4.2 Power Configuration

When the xPC564A Mini-Module is plugged into the xPC56XXMB motherboard, power is supplied directly by the motherboard. In this setup, the external power supply input available on the Mini-Module should NOT be used.

When the xPC564A Mini-Module is used as a stand-alone board, an external 5V power supply must be used.

The following jumpers affect the power supply pins of the MPC564xA processor:

J3 – VRH enable

Controls whether power is provided to the Voltage Reference High (VRH) input pin used by the eQADC module on the MPC564xA processor.

Jumper Setting	Effect
On (default)	The VRH pin is connected to 5V power
Off	The VRH pin is left disconnected

J4 – VSTBY Configuration

Jumper Setting	Effect
On (default)	The MPC564xA “VSTBY” pin is pulled down to GND
Off	The MPC564xA “VSTBY” pin is only connected to a 100nF bypass capacitor. External 1V supply should be applied to this pin.

J14 – I/O Supply Input Enable

Controls whether power is provided to the “I/O Supply Input” pins on the MPC564xA processor.

Jumper Setting	Effect
On (default)	MPC564xA I/O Supply Input pins are connected to 3.3V or 5V (determined by J18)
Off	MPC564xA I/O Supply Input pins are unpowered

J17 – Debug Ports Power Configuration

Controls whether the power pins on the debug ports (VDDE7 on the 14-pin JTAG port and VREF on the 28-pin Mictor port) are connected to 3.3V or 5V.

Jumper Setting	Effect
1+2	The power pins on the debug ports are connected to 5V
2+3 (default)	The power pins on the debug ports are connected to 3.3V

J18 – Processor I/O Voltage Configuration

Sets the voltage level applied to the I/O Supply Input pins of the MPC564xA processor.

Jumper Setting	Effect
1+2 (default)	The “I/O Supply Input” pins of the MPC564xA processor are powered by 5V
2+3	The “I/O Supply Input” pins of the MPC564xA processor are powered by 3.3V

J19 – 3.3V Voltage Source

Controls whether the voltage source for 3.3V on the MPC564xA processor is provided by the motherboard or by the 5V external source on the Mini-Module via a voltage regulator.

Jumper Setting	Effect

1+2 (default)	3.3V is provided to the MPC564xA processor by the motherboard
2+3	3.3V is provided to the MPC564xA processor by the 5V external source on the xPC564A Mini-Module

J20 – 5V Voltage Source

Controls whether the voltage source for 5V on the MPC564xA processor is provided by the motherboard or by the 5V external source on the Mini-Module.

Jumper Setting	Effect
1+2 (default)	5V is provided to the MPC564xA processor by the motherboard
2+3	5V is provided to the MPC564xA processor by the 5V external source on the xPC564A Mini-Module

J21 – VDDEH Voltage Selector

Controls whether the voltage provided to the VDDEH pins on the MPC564xA processor is 3.3V or 5V.

Jumper Setting	Effect
1+2 (default)	3.3V is provided to the VDDEH pins
2+3	5V is provided to the VDDEH pins

J24 – Internal VDD enable

Controls whether power is provided to the “Internal Logic Supply Input” pins on the MPC564xA processor.

Jumper Setting	Effect
On (default)	MPC564xA Internal Logic Supply Input pins are connected to 1.2V
Off	MPC564xA Internal Logic Supply Input pins are unpowered

4.3 System Clock Configuration

The xPC564A Mini-Modules support the usage of crystal clock sources as well as external clock sources.

J16 – Crystal clock source enable

Both of the jumpers below need to be installed to enable the crystal clock source.

Jumper Setting	Effect
1+2 (default)	The MPC564xA “EXTAL” signal is connected to the crystal clock source on the xPC564A Mini-Module
3+4 (default)	The MPC564xA “XTAL” signal is connected to the crystal clock source on the xPC564A Mini-Module

J11 – External clock source enable

The xPC564A Mini-Module contains a footprint for an SMA connector, which can be used to provide an external clock source to the system.

Jumper Setting	Effect
On	The MPC564xA “EXTAL” signal is connected to the SMA connector on the xPC564A Mini-Module
Off (default)	The SMA connector on the xPC564A Mini-Module is disconnected from the processor

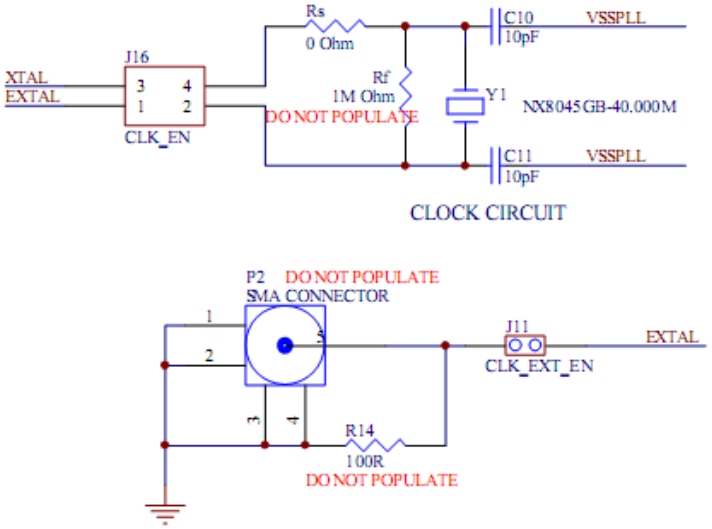


Figure 4-2: System Clock schematic

4.4 General Configuration

J13 – Reset Enable

A RESET push button on the xPC564A Mini-Module can be used to reset the

processor.

Jumper Setting	Effect
On (default)	The RESET button on the xPC564A Mini-Module is enabled
Off	The RESET button on the xPC564A Mini-Module is disabled

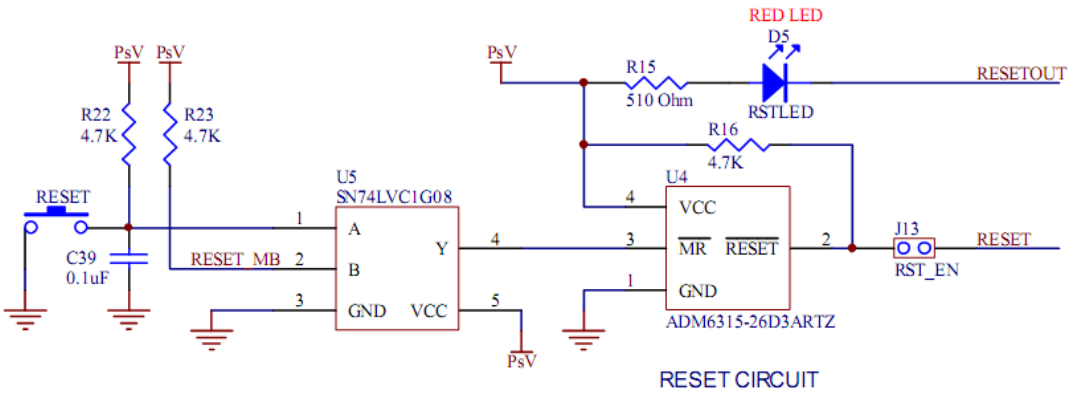


Figure 4-3: Reset circuitry schematic

4.5 LEDs

There are two user LEDs available on the xPC564A Mini-Module. All LEDs are active low.

J12 – LEDs Enable

Controls whether the LEDs on the xPC564A Mini-Module are connected to I/O pins of the processor. The jumpers can be removed and wires can be used

to connect each LED to any processor I/O pin, if desired.

Jumper Setting	Effect
1+2 (default on)	LED1 connected to eMIOS16 on the MPC564xA processor
3+4 (default on)	LED2 connected to eMIOS17 on the MPC564xA processor

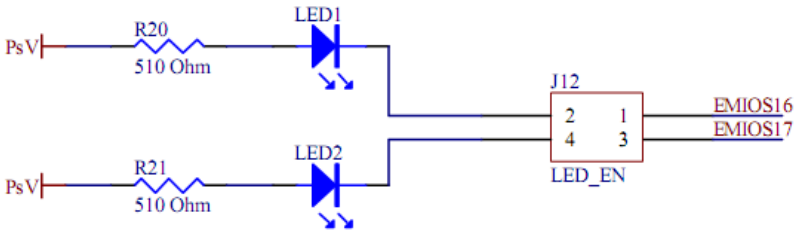


Figure 4-4: LEDs circuitry schematic

4.6 Buttons

There are two user buttons available on the xPC564A Mini-Module.

J15 – Buttons Enable

Controls whether the buttons on the xPC564A Mini-Module are connected to I/O pins of the MPC564xA processor. The jumpers can be removed and wires can be used to connect each button to any processor I/O pin, if desired.

Jumper Setting	Effect
1+2 (default on)	S1 connected to eMIOS18 on the MPC564xA processor

3+4 (default on)	S2 connected to eMIOS19 on the MPC564xA processor

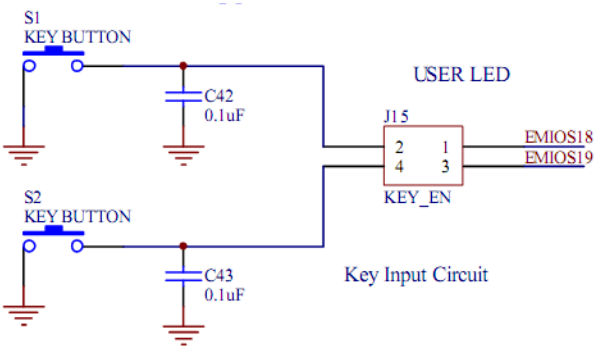


Figure 4-5: Buttons circuitry schematic

4.7 External SRAM configuration

There is an external SRAM module (U9) on the xPC564xA Mini-Module which is able to be configured for byte-write.

J25 – Byte-Write A Enable

Controls whether Byte-Write A Enable is connected to ADDR13 of the MPC564xA processor or ground.

Jumper Setting	Effect
1+2	Byte-Write A Enable is connected to ADDR13 of the MPC564xA processor.
2+3	Byte-Write A Enable is connected to Ground.

J26 – Byte-Write B Enable

Controls whether Byte-Write B Enable is connected to ADDR14 of the MPC564xA processor or ground.

Jumper Setting	Effect
1+2	Byte-Write B Enable is connected to ADDR14 of the MPC564xA processor
2+3	Byte-Write B Enable is connected to ground.

J27 – ADDR13

Controls whether ADDR13 of the MPC564xA processor is connected to the external SRAM module (U9).

Jumper Setting	Effect
On	ADDR13 is connected to external SRAM
Off	ADDR13 is not connected to the external SRAM.

J28 – ADDR14 enable

Controls whether ADDR14 of the processor is connected to the external SRAM module (U9).

Jumper Setting	Effect
On	ADDR14 is connected to the external SRAM
Off	ADDR14 is not connected to the external SRAM

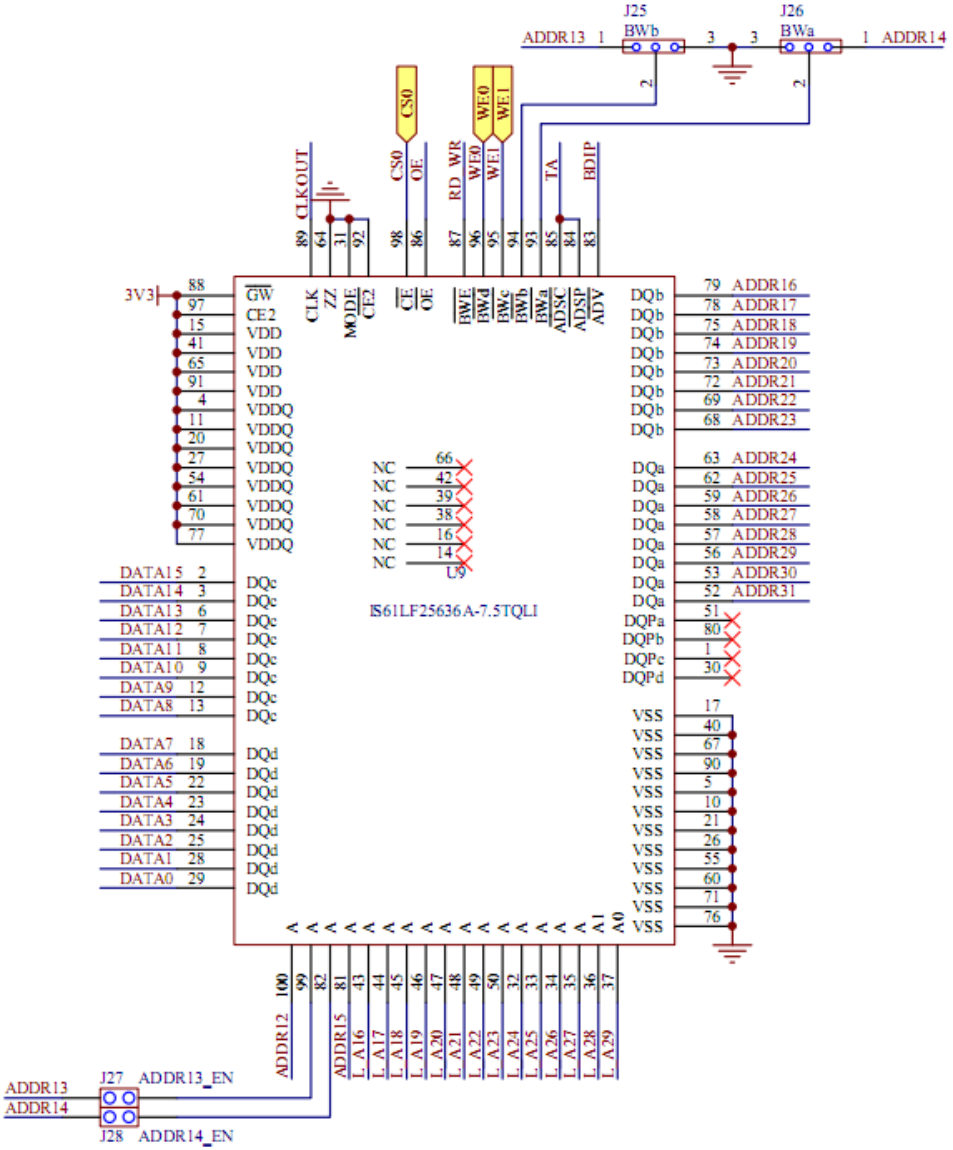


Figure 4-6: External SRAM schematic

5 xPC564AADPT208S / xPC564AADPT176S HARDWARE & JUMPER SETTINGS

5.1 Boot Configuration

The following jumpers affect the operation of the processor as it initially comes out of the reset state:

J7 – BOOTCFG Configuration

Controls whether the processor boots from internal FLASH or from a serial interface (CAN, SCI)

Jumper Setting	Effect
1+2	The MPC564xA processor uses serial boot mode
2+3 (default)	The MPC564xA processor uses internal boot mode

J8 – PLLREF Configuration

Controls the clock source the processor uses: a crystal source or an external source

Jumper Setting	Effect
1+2 (default)	The MPC564xA processor uses a crystal clock source
2+3	The MPC564xA processor uses an external clock source

J9 – WKPCFG Configuration

Controls whether specified eTPU and eMIOS pins on the processor are configured as a weak pull-up or a weak pull-down when the processor comes

out of reset

Jumper Setting	Effect
1+2	Pins are configured as weak pull-up
2+3 (default)	Pins are configured as weak pull-down

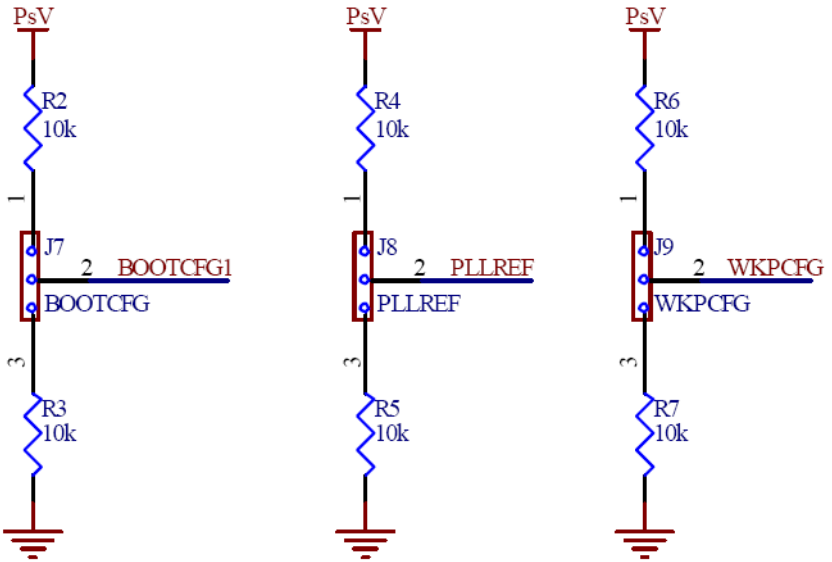


Figure 5-1: Boot Configuration Jumpers

5.2 Power Configuration

When the xPC564A Mini-Module is plugged into the xPC56XXMB motherboard, power is supplied directly by the motherboard. In this setup, the external power supply input available on the Mini-Module should NOT be used.

When the xPC564A Mini-Module is used as a stand-alone board, an external 5V power supply must be used.

The following jumpers affect the power supply pins of the MPC564xA processor:

J3 – VRH enable

Controls whether power is provided to the Voltage Reference High (VRH) input pin used by the eQADC module on the MPC564xA processor.

Jumper Setting	Effect
On (default)	The VRH pin is connected to 5V or 3.3V power (determined by J18)
Off	The VRH pin is left disconnected

J4 – VSTBY Configuration

Jumper Setting	Effect
On (default)	The MPC564xA “VSTBY” pin is pulled down to GND
Off	The MPC564xA “VSTBY” pin is only connected to a 100nF bypass capacitor. External 1V supply should be provided to this pin.

J14 – I/O Supply Input Enable

Controls whether power is provided to the “I/O Supply Input” pins on the MPC564xA processor.

Jumper Setting	Effect

On (default)	MPC564xA I/O Supply Input pins are connected to 3.3V or 5V (determined by J18)
Off	MPC564xA I/O Supply Input pins are unpowered

J15 – Internal VDD enable

Controls whether power is provided to the “Internal Logic Supply Input” pins on the MPC564xA processor.

Jumper Setting	Effect
On (default)	MPC564xA Internal Logic Supply Input pins are connected to 1.2V
Off	MPC564xA Internal Logic Supply Input pins are unpowered

J16 – VDDE12 Voltage Configuration (xPC564AADPT176S only)

Controls whether power is provided to the “VDDE12” pins on the MPC564xA processor.

Jumper Setting	Effect
On	MPC564xA VDDE12 pins are connected to 3.3V
Off (default)	MPC564xA VDDE12 pins are only connected to bypass capacitors

J17 – Debug Ports Power Configuration

Controls whether the power pins on the debug ports (VDDE7 on the 14-pin JTAG port and VREF on the 28-pin Mictor port) are connected to 3.3V or 5V.

Jumper Setting	Effect
1+2	The power pins on the debug ports are connected to 5V
2+3 (default)	The power pins on the debug ports are connected to 3.3V

J18 – Processor I/O Voltage Configuration

Sets the voltage level applied to the I/O Supply Input pins of the MPC564xA processor.

Jumper Setting	Effect
1+2 (default)	The “I/O Supply Input” pins of the MPC564xA processor are powered by 5V
2+3	The “I/O Supply Input” pins of the MPC564xA processor are powered by 3.3V

J19 – Voltage Regulator Configuration

Controls whether power is provided to the voltage regulator and LVI block. .

Jumper Setting	Effect
On (default)	The regulator on the MPC564xA processor is powered

Off	The regulator on the MPC564xA processor is unpowered, external regulation and low-voltage control must be supplied.

CT1 – VRL enable

Controls whether ground is provided to the Voltage Reference Low (VRL) input pin used by the eQADC module on the MPC564xA processor.

Jumper Setting	Effect
Connected (default)	The VRL pin is connected to ground
Disconnected	The VRL pin is left disconnected

CT2 – VRC33 Configuration

Controls whether the VRC33 pin of the MPC564xA processor is connected to 3.3V.

Jumper Setting	Effect
Connected	The VRC33 pin is connected to 3.3V (not recommended by the MPC564xA reference manual)
Disconnected (default)	The VRC33 pin is connected only to a bypass capacitor

CT3 – VDDE7 3.3V Configuration (xPC564AADPT208S only)

This cut trace, along with CT5, determines whether the VDDE7 pins are

powered by external 3.3V or by the 3.3V VRC33 voltage regulator output from the MPC564xA processor.

When the Mini-Module is attached to the xPC56XXMB motherboard, the 3.3V external power is directly derived from the motherboard itself. When the Mini-Module is operated as a stand-alone unit, the 3.3V power is derived from the voltage supply that is powering the Mini-Module. Note that if the Mini-Module is powered by 5V instead of 3.3V, the 3.3V will be unavailable to power VDDE7. Jumper J18 should be set correctly to prevent damage.

Jumper Setting	Effect
Connected (default)	VDDE7 is powered by external 3.3V
Disconnected	VDDE7 is not powered by external 3.3V

CT4 – VDDREG 5V Configuration (xPC564AADPT176S only)

This cut trace determines whether the VDDREG pin is powered by 5V from the xPC56XXMB motherboard, or dictated by jumpers J18 and J19

Jumper Setting	Effect
Connected (default)	VDDREG is powered by 5V from the xPC56XXMB motherboard
Disconnected	VDDREG is not powered by 5V from the xPC56XXMB motherboard and its power is instead dictated by J18 and J19

CT5 – VDDE7 5V Configuration (xPC564AADPT208S only)

This cut trace, along with CT3, determine whether the VDDE7 pins are powered by external 3.3V or by the 3.3V VRC33 voltage regulator output from

the MPC564xA processor.

Jumper Setting	Effect
Connected	VDDE7 is powered by the VRC33 output from the MPC564xA processor
Disconnected (default)	VDDE7 is not powered by the VRC33 output from the MPC564xA processor

CT6 – 1.2V Power Generation

Controls whether the 1.2 power supply is generated from the NPN transistor or supplied directly from the xPC56XXMB motherboard.

Jumper Setting	Effect
Connected	1.2V power is provided directly by the xPC56XXMB motherboard
Disconnected (default)	1.2V power is generated by the NPN transistor circuit on the xPC564A Mini-Module

CT8 – Mictor VEN_IO2 Configuration

Controls whether the VEN_IO2 pin on the 38-pin Mictor port is connected to the BOOTCFG1 pin on the MPC564xA processor.

Jumper Setting	Effect
Connected	The VEN_IO2 pin is connected to BOOTCFG1

Disconnected (default)	The VEN_IO2 pin is left disconnected

5.3 System Clock Configuration

The xPC564A Mini-Modules support the usage of crystal clock sources as well as external clock sources.

J10 – Crystal clock source enable

Both of the jumpers below need to be installed to enable the crystal clock source.

Jumper Setting	Effect
1+2 (default)	The MPC564xA “EXTAL” signal is connected to the crystal clock source on the xPC564A Mini-Module
3+4 (default)	The MPC564xA “XTAL” signal is connected to the crystal clock source on the xPC564A Mini-Module

J11 – External clock source enable

The xPC564A Mini-Module contains a footprint for an SMA connector, which can be used to provide an external clock source to the system.

Jumper Setting	Effect
On	The MPC564xA “EXTAL” signal is connected to the SMA connector on the xPC564A Mini-Module
Off (default)	The SMA connector on the xPC564A Mini-Module is disconnected from the processor

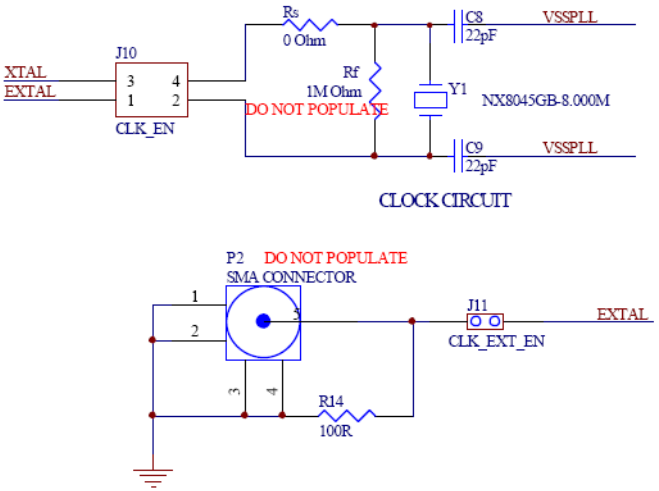


Figure 5-2: System Clock Schematic

5.4 General Configuration

J13 – Reset Enable

A RESET push button on the xPC564A Mini-Module can be used to reset the processor.

Jumper Setting	Effect
On (default)	The RESET button on the xPC564A Mini-Module is enabled
Off	The RESET button on the xPC564A Mini-Module is disabled

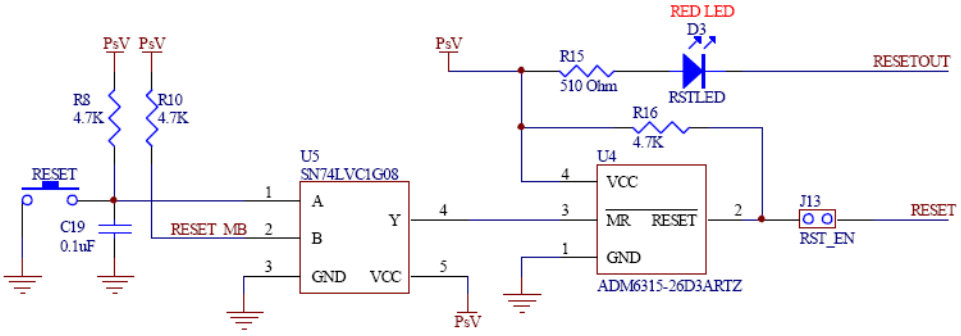


Figure 5-3: Reset circuitry schematic

6 DEBUGGING/PROGRAMMING xPC564A EVB

P&E provides hardware and software tools for debugging and programming the xPC564A EVB system.

P&E's USB-ML-PPCNEXUS and Cyclone MAX offer two effective hardware solutions, depending on your needs. The USB-ML-PPCNEXUS is a development tool that will enable you to debug your code and program it onto your target. The Cyclone MAX is a more versatile and robust development tool with advanced features and production programming capabilities, as well as Ethernet support.

More information is available below to assist you in choosing the appropriate development tool for your needs.

6.1 Hardware Solutions At A Glance

The USB-ML-PPCNEXUS offers an affordable and compact solution for your development needs, and allows debugging and programming to be accomplished simply and efficiently. Those doing rapid development will find the USB-ML-PPCNEXUS easy to use and fully capable of fast-paced debugging and programming.

The Cyclone MAX is a more complete solution designed for both development and production. The Cyclone MAX features multiple communications interfaces (including USB, Ethernet, and Serial), stand-alone programming functionality, high speed data transfer, a status LCD, and many other advanced capabilities.

Below is an overview of the features and intended use of the USB-ML-PPCNEXUS and Cyclone MAX.

6.1.1 USB-ML-PPCNEXUS Key Features

- Programming and debugging capabilities
- Compact and lightweight
- Communication via USB 2.0
- Supported by P&E software and Freescale's CodeWarrior

6.1.2 Cyclone MAX Key Features

- Advanced programming and debugging capabilities, including:

- PC-Controlled and User-Controlled Stand-Alone Operation
- Interactive Programming via Host PC
- In-Circuit Debugging, Programming, and Testing

- Compatible with Freescale's ColdFireV2/3/4, PowerPC 5xx/8xx/55xx/56xx, and ARM7 microcontroller families
- Communication via USB, Serial, and Ethernet Ports
- Multiple image storage
- LCD screen menu interface
- Supported by P&E software and Freescale's CodeWarrior

6.2 Working With P&E's USB-ML-PPCNEXUS

Figure 6-1: P&E's USB-ML-PPCNEXUS

6.2.1 Product Features & Implementation

P&E's USB-ML-PPCNEXUS Interface (USB-ML-PPCNEXUS) connects your target to your PC and allows the PC access to the debug mode on Freescale's PowerPC 5xx/8xx/55xx/56xx microcontrollers. It connects between a USB port on a Windows 2000/XP/2003/Vista machine and a standard 14-pin JTAG/Nexus connector on the target.

By using the USB-ML-PPCNEXUS Interface, the user can take advantage of the background debug mode to halt normal processor execution and use a PC to control the processor. The user can then directly control the target's execution, read/write registers and memory values, debug code on the processor, and program internal or external FLASH memory devices. The USB-ML-PPCNEXUS enables you to debug, program, and test your code on your board.

6.2.2 Software

The USB-ML-PPCNEXUS Interface works with Codewarrior as well as P&E's in-circuit debugger and flash programmer to allow debug and flash programming of the target processor. P&E's USB-ML-PPCNEXUS Development Packages come with the USB-ML-PPCNEXUS Interface, as well as flash programming software, in-circuit debugging software, Windows IDE, and register file editor.

6.3 Working With P&E's Cyclone MAX

Figure 6-2: P&E's Cyclone MAX

6.3.1 Product Features & Implementation

P&E's Cyclone MAX is an extremely flexible tool designed for debugging, testing, and in-circuit flash programming of Freescale's ColdFireV2/3/4, PowerPC 5xx/8xx/55xx/56xx, and ARM7 microcontrollers. The Cyclone MAX connects your target to the PC via USB, Ethernet, or Serial Port and enables you to debug your code, program, and test it on your board. After development is complete the Cyclone MAX can be used as a production tool on your manufacturing floor.

For production, the Cyclone MAX may be operated interactively via Windows-based programming applications as well as under batch or .dll commands from a PC. Once loaded with data by a PC it can be disconnected and operated manually in a stand-alone mode via the LCD menu and control buttons. The Cyclone MAX has over 3Mbytes of non-volatile memory, which allows the on-board storage of multiple programming images. When connected to a PC for programming or loading it can communicate via the ethernet, USB, or serial interfaces.

6.3.2 Software

The Cyclone MAX comes with intuitive configuration software and interactive programming software, as well as easy to use automated control software. The Cyclone MAX also functions as a full-featured debug interface, and is supported by Freescale's CodeWarrior as well as development software from P&E.

P&E's Cyclone MAX is also available bundled with additional software as part of various Development Packages. In addition to the Cyclone MAX, these Development Packages include in-circuit debugging software, flash programming software, a Windows IDE, and register file editor.

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