Rev 1.1

TECHNICAL DESCRIPTION

Fastrax UP500 GPS Receiver

This document describes the electrical connectivity and main functionality of the Fastrax UP500 hardware.

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Fastrax Ltd.

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CHANGE LOG

Rev.	Notes	Date
0.1	First Draft	2008-04-21
0.2	2nd Draft	2008-05-02
0.3	Specification updated based on measured performance. Mechanics drawing added.	2008-07-30
0.4	Operating modes clarified.	2008-09-26
0.5	PCB mounting description added.	2008-10-02
0.6	Table 2 updated	2008-10-17
1.0	Release version	2008-10-27
1.1	Default firmware configuration changed. SBAS enabled.	2008-12-02

CONTENTS

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COMPLEMENTARY READING

The following Fastrax reference documents are complementary reading for this document.

Ref. #	File name	Document name
I		
II		
III		
IV		

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1. GENERAL DESCRIPTION

The Fastrax UP500 is a GPS receiver module with embedded antenna and tiny form factor 22.0 x 22.0mm x 8mm. The Fastrax UP500 receiver provides very fast TTFF together with weak signal acquisition and tracking capability to meet even the most stringent urban canyon performance expectations. The Fastrax UP500 module supports enhanced navigation accuracy by utilizing WAAS/EGNOS corrections.

The Fastrax UP500 module provides complete signal processing from internal antenna to serial data output in NMEA messages. The module requires a power supply VDD and a backup supply BU voltage for non-volatile RTC & RAM blocks. There is a variant of the module available with on-board backup battery, which will eliminate the need for external backup voltage source. PPS signal output is available for accurate timing applications.

The Fastrax UP500 module interfaces to the customer's application via one serial port, which uses CMOS voltage levels. If RS232 signal levels are required, there is a variant of Fastrax UP500 available with on-board CMOS-to-RS232 level converter. PPS output is available from the module with CMOS levels.

1.1 Default firmware configuration

Fastrax UP500 default firmware configuration:

1. Port 0: NMEA 9600 baud

2. NMEA output: GGA, RMC, GSV, GSA (all 1 sec interval)

3. DGPS/SBAS: Enabled (Module supports WAAS/EGNOS)

4. Datum: WGS84

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2. SPECIFICATIONS

2.1 General

Table 1   General Specifications

Receiver	GPS L1 C/A-code, SPS
Channels	32 channels
Update rate	1 Hz default (fix rate configurable up to 5Hz)
Acquisition Sensitivity (Cold start)	-146dBm (1)
Re-acquisition Sensitivity	-155dBm (1)
Navigation Sensitivity	-159dBm (1)
Tracking Sensitivity	-159dBm (1)
Supply voltage, VDD	+3.0V…+5.5V
Back up supply voltage, BU	+1.5V…+5.5V
Power consumption, VDD	90 mW typical @ 3.0V
Power consumption, BU	10 uW typical @ 3.0V (during battery backup state). Current at BU pin may peak up to 100uA in full operating state.
Operating temperature range	-40ºC…+85ºC (2)
Serial port protocol	Port 0: NMEA
Serial data format	8 bits, no parity, 1 stop bit
Serial data speed (default)	NMEA: 9600 baud
I/O signal levels	CMOS compatible: low state: 0.0…0.4V; high state: 0.7…3.3V. (3)
I/O sink/source capability	+/- 2 mA max.
PPS output	+/- 1us accuracy

Note (1): measured by conducted measurement from GPS simulator.

Note (2): All performance metrics are not guaranteed below -30°C.

Note (3): Fastrax UP500R UART signals are RS232 compatible.

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2.2 Absolute maximum ratings

Table 2   Absolute maximum ratings

Item	Min	Max	unit
Operating temperature	-40	+85	ºC
Storage temperature	-40	+85	ºC
Power dissipation	-	500	mW
Supply voltage, VDD	-0.3	+6.0	V
Supply voltage, VDD_B	-0.3	+6.0	V
Input voltage on any input connection	-0.3	+3.6	V
RF input level	-	+15	dBm

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3. OPERATION

3.1 Operating modes

After power up the receiver boots from the internal flash memory for normal operation. Modes of operation:

- Tracking/navigating mode

- Low power tracking/navigating mode

- Backup mode

3.1.1 Tracking/Navigating mode

In tracking/navigating mode the Fastrax UP500 receiver module will search for additional satellites and collects almanac data. Once the receiver has collected almanac data (this takes about 12 minutes from Cold Start), it will enter Low Power Tracking mode. The VDD power consumption in table 1 is measured in Low Power Tracking/Navigating mode.

3.1.2 Low Power Tracking/Navigating mode

In Low power tracking/navigating mode the receiver continues normal navigation but does not collect further Almanacs data. Therefore the current consumption is reduced to level of <90mW (<100mW for UP500R with default UART baud rate).

3.1.3 Backup mode

When the operating voltage VDD is removed from the Fastrax UP500, the module enters Backup mode. In this mode, the module is keeping time by the RTC oscillator. Also, satellite ephemeris data is stored in battery backup RAM in order to get fast TTFF when VDD is connected again. Any user configuration settings are also valid as long as the backup supply BU is active. When the BU is powered off, the configuration is reset to factory configuration on next power up.

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4. CONNECTIVITY

4.1 Connection assignments

The I/O connections are available on the 6-pin, 2.54mm pitch pin-header pads.

Table 3 Connections

Contact	Signal name	I/O	Alternative signal name	Signal description
1	RXD	I	-	UART Port 0 async. input. Internal pull high resistor 75kΩ.
2	TXD	O	-	UART Port 0 async. output.
3	GND	-	-	Ground
4	VDD	I	-	Main power supply
5	BU	I	-	Backup supply
6	PPS	O	-	Pulse per second output.
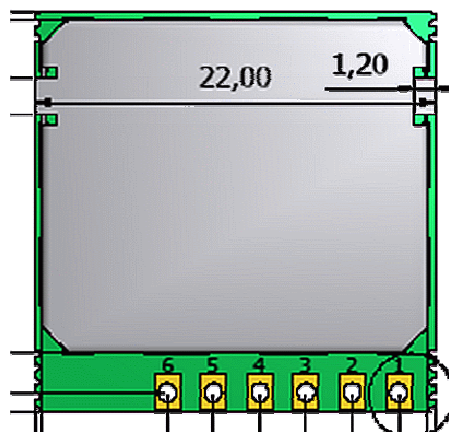
Figure 1. Pin numbering in the Fastrax UP500 module.

4.2 Power supply

The Fastrax UP500 module requires two separate power supplies: BU for non-volatile back up block and the VDD for digital parts and I/O. VDD can be switched off when navigation is not needed but if

possible keep the back up supply BU active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF.

Back up supply BU draws typically <4uA current in back up state. During navigation (while VDD is active) BU current may peak up to 100uA, while staying at <20uA average level.

On-board backup battery is available as an assembly option (UP500B). In this case the Backup supply can be left open and the module handles the backup state power supply automatically. The backup battery is charged when VDD supply is connected.

Main power supply VDD current varies according to the processor load and satellite acquisition. Typically VDD peak current is up to 60mA during Search mode. In Low Power Tracking mode the VDD current is typically below 30 mA for the Fastrax UP500 and UP500B modules, and below 33 mA for Fastrax UP500R module with default baud rate of 9600 baud.

4.3 Reset

Reset can be initiated by switching off VDD supply for >150 ms.

4.4 UART

The device supports UART communication via Port 0 of the GPS IC. With the standard firmware the Port 0 is configured by default to NMEA protocol (9600 baud).

I/O levels form the serial ports are CMOS compatible (see table 1). On-board RS232 level converter is available with the Fastrax UP500R module.

4.5 Mechanical dimensions and contact numbering

Module size is 22.0mm (width) x 22.0mm (length) x 8mm (thickness). General tolerance is ±0.3mm. Detailed mechanical drawing is presented in figure 2.
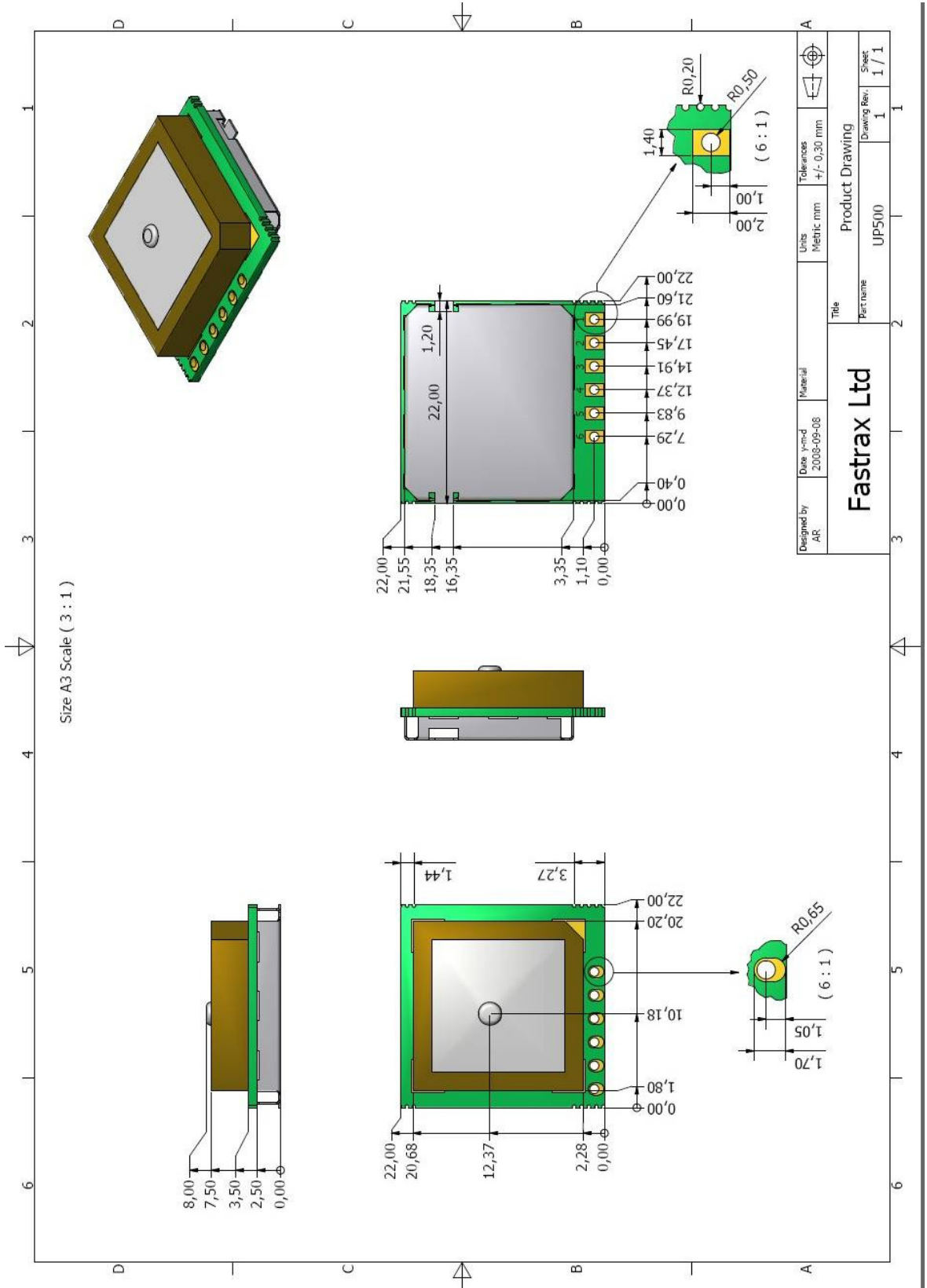
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Figure 2. Mechanics drawing of the Fastrax UP500 module.

5. MODULE OPTIONS

Fastrax UP500 module is available in three different HW-configurations. This makes it possible for a customer to select optimal solution for different applications depending on required functionality and/or price target.

The following table will summarize the differences in the Fastrax UP500 module options.

Table 1 Fastrax UP500 HW options.

UP500 option	On-board backup battery	On-board RS232 driver	Notes
UP500	NO	NO	Standard module, lowest price. CMOS level UART.
UP500B	YES	NO	On-board backup battery, simplifies host power management. CMOS level UART.
UP500R	YES	YES	Easy connectivity to PC or other RS232 level UART systems.

Fastrax UP500 is available as a standard module with standard lead time. Please contact Fastrax for lead time and availability on the Fastrax UP500B and Fastrax UP500R.

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6. PCB MOUNTING

The Fastrax UP500 can be mounted on a customer PCB ("motherboard" in the instructions below) by using standard 2.54mm pitch 1x6 pin header (for example Samtec TLW-106-06-G-S). Two dummy pads are used to solder the module metal shield on the motherboard. Reference pad layout is shown in figure 3.
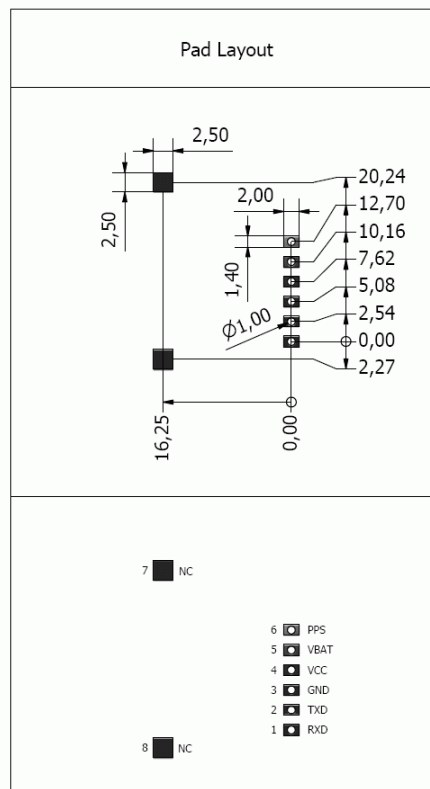

Figure 3. Pad layout of mounting side for UP500 module.

There are some rules that needs to be followed in order to maintain good performance for the on-board patch antenna of the UP500:

- Solder the pin header to the module in such way that the pins are as short as possible on the antenna side of the UP500 module (see figure 4).

- Place any active circuitry (processors, memory busses, switching regulators, etc.) on the motherboard as far away as possible from the UP500 module.

- Design a solid VDD source for the UP500 module (VDD voltage ripple should be <50mV).

- If UP500B is used and there is no need for the PPS signal, a 4-pin header (for example Samtec TLW-104-06-G-S) can be used to contact pins #1 through #4. However, the 6-pin header is recommended since it is mechanically more robust. In this case pins #5 and #6 may be left floating on the motherboard.

Samtec TLW-106-06-G-S
or similar Pinheader.
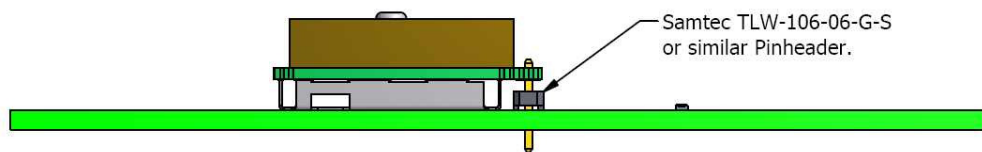
Figure 4. Side view of the pin header assembly for the UP500 module.

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